Hardware Design Flow

電機 26 級 陳亮宇

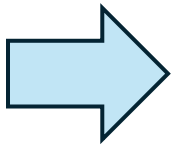
Outline

1. 系統規格
2. 系統架構
3. 選 IC
4. 設計範例
5. 畫電路圖 (Schematic)
6. 畫 Layout

第一步：定義系統規格

- 以螢光舞為例，我們的系統規格包括：
  - 需要幾個可以獨立控制的燈？
  - 總共需要多少電流？
  - 電池需要撐多久？

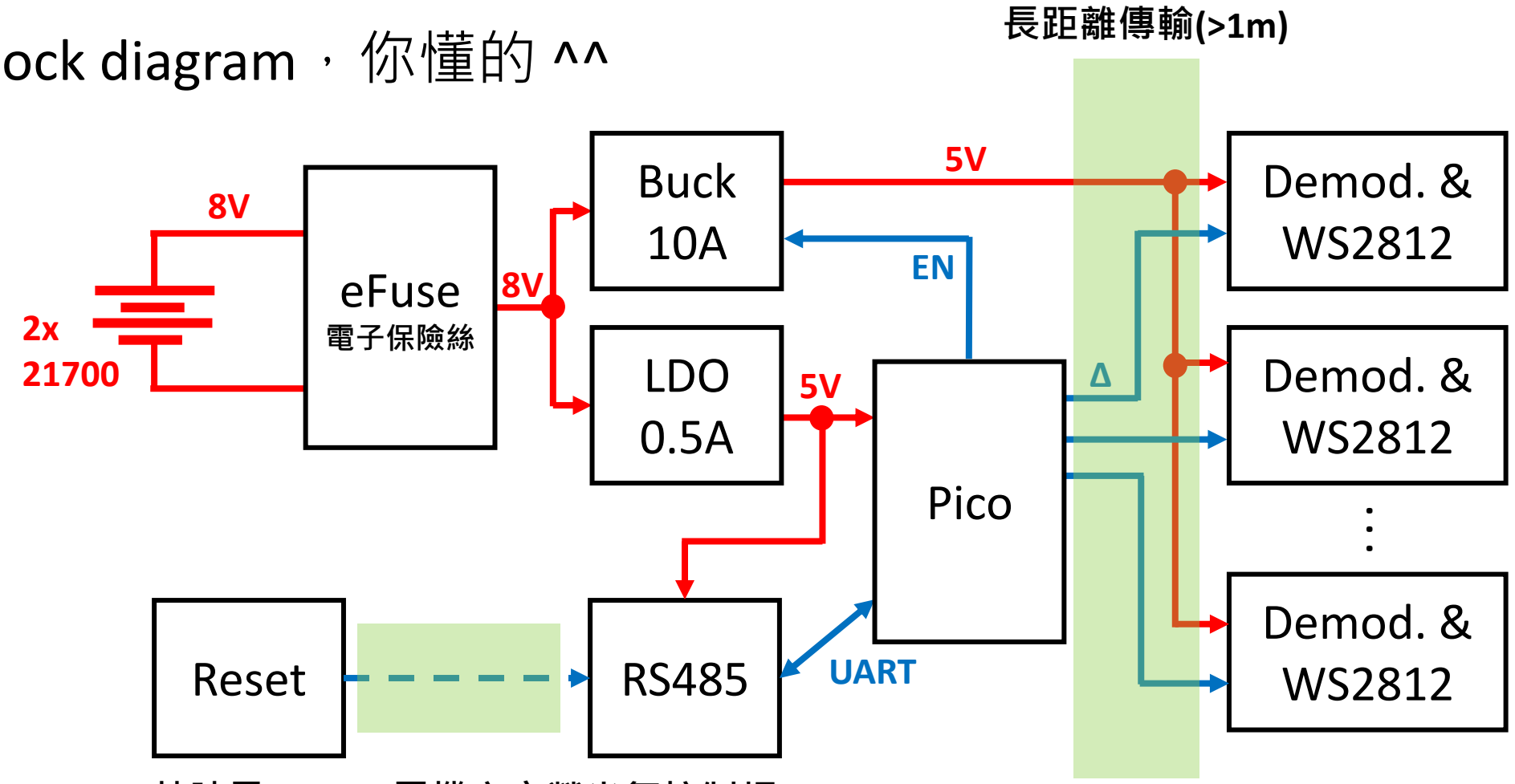
用一系列的問題
去定義好系統要達到的目標



後續設計會根據規格
決定要用什麼架構
或什麼等級的 IC

第二步：建立系統架構

- Block diagram，你懂的 ^^



林映君，2026 電機之夜螢光舞控制板

第三步：選擇適合的 IC

通常是從一個
block的規格下手

例如：
Buck converter
Input 8V
Output 5V
Current 10 A

TPS56A37 ACTIVE

4.5V to 28V input, 10A synchronous buck converter

Product notifications

Order now

DATA SHEET TPS56A37 4.5V to 28V Input, 10A, Synchronous Buck Converter datasheet PDF | HTML

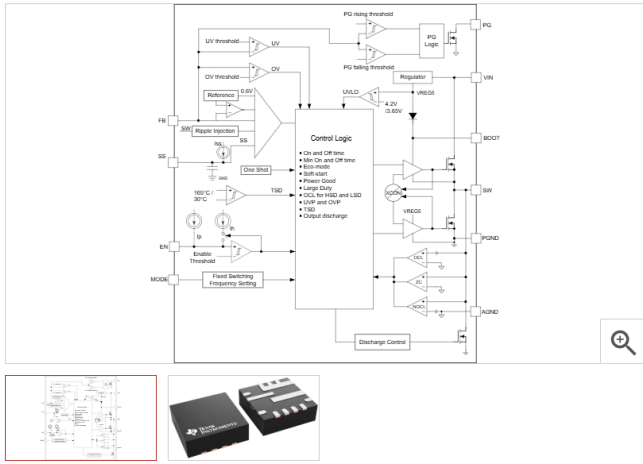
Datasheet

Product details | Technical documentation | Design & development | Ordering & quality | Support & training

Product details

Parameters | Package | Pins | Size | Features | Description

Rating	Catalog
Topology	Buck
Iout (max) (A)	10
Vin (max) (V)	28
Vin (min) (V)	4.5
Vout (max) (V)	13
Vout (min) (V)	0.6
Features	Adjustable soft start, Enable, Forced PWM, Light-load efficiency, Overcurrent protection, Synchronous rectification

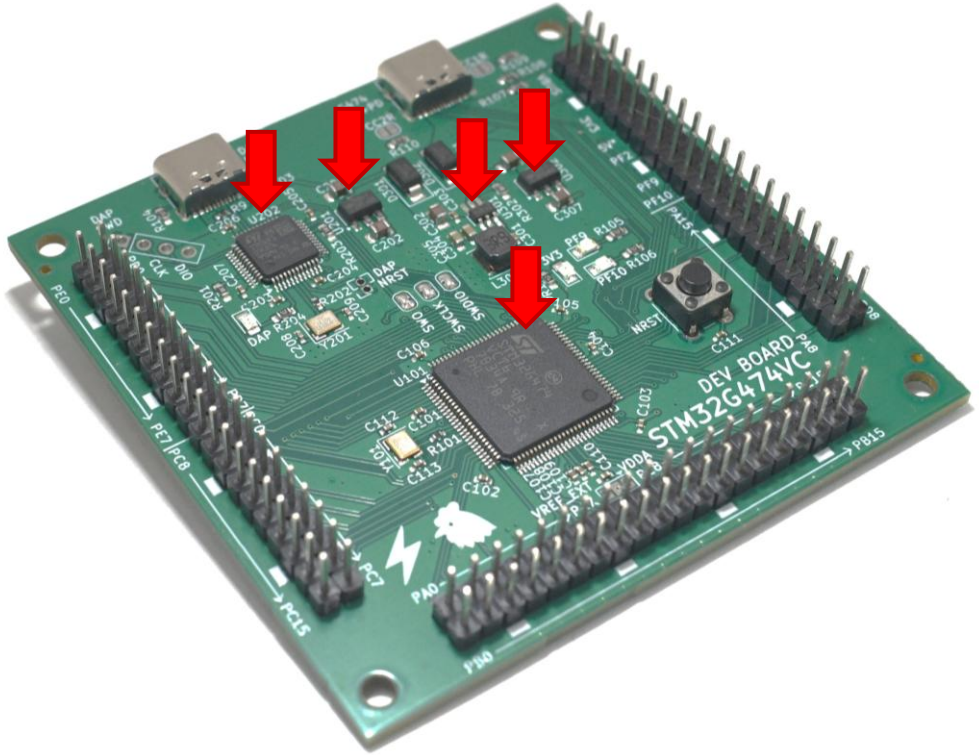


什麼是 IC？

Integrated Circuit

整合的　　電路

- 把很多電路整合到一顆晶片上面
- 可以是簡單幾個邏輯閘，到上億個電晶體的 GPU



如何讀 Datasheet ?

- Specification
  - 看是否符合需求
- Pin configuration
  - 看 IC 的腳長在哪裡 (下一頁)
- Typical application
  - 範例電路，抄

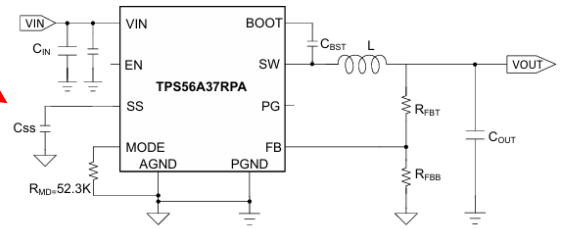
TPS56A37 4.5V to 28V Input, 10A, Synchronous Buck Converter

1 Features

- 4.5V to 28V input voltage range
- 0.6V to 13V output voltage range
- Supports 10A continuous output current
- Integrated 19.4mΩ and 8.5mΩ MOSFETs
- 0.6V ±1% reference voltage at 25°C
- 45uA low quiescent current
- D-CAP3™ control mode for fast transient response
- Eco-mode (auto-skip mode) for high light-load efficiency
- Fixed 500kHz switching frequency
- Cycle by cycle over current limit
- Adjustable soft-start time with default 1.8ms
- Built-in output discharge function
- Power-good indicator to monitor output voltage
- Supports up to 98% duty operation
- Non-latched protections for UV, OV, OT, and UVLO
- –40°C to +150°C operating junction temperature
- Small 10-pin 3.0mm × 3.0mm HotRod™ QFN package
- Pin-to-pin compatible with 6A TPS56637 and 8A TPS56837

2 Applications

- Industrial PC, EPOS, factory automation and control
- Multifunction printers, video conference system
- Monitors, TV, speakers, PC and notebooks, portable electronics
- General purposes for 12V,19V, 24V power-bus supply



Simplified Schematic

3 Description

The TPS56A37 is a high-efficiency, easy-to-use, synchronous buck converter with a wide input voltage range of 4.5V to 28V. The device supports up to 10A continuous output current at output voltages between 0.6V and 13V.

The TPS56A37 uses D-CAP3 control mode to provide fast transient response, good line and load regulation, no requirement for external compensation, and supports low equivalent series resistance (ESR) output capacitors like MLCC.

The TPS56A37 operates at Eco-mode to attain high efficiency at light load with fixed 500kHz switching frequency. The TPS56A37 has adjustable soft-start time by connecting the SS capacitor and with default 1.8ms with the SS pin floating.

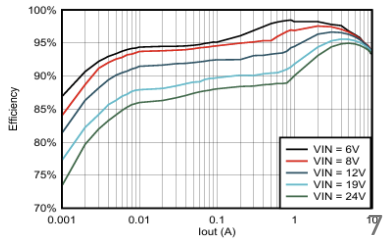
The TPS56A37 provides complete non-latched OV (overvoltage), UV (undervoltage), OC (overcurrent), OT (overtemperature), and UVLO (undervoltage lockout) protections combined with power-good indicator and output discharge function features.

The TPS56A37 is available in a 10-pin, 3.0mm × 3.0mm HotRod QFN package, and the junction temperature is specified from –40°C to 150°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS56A37	RPA (VQFN-HR, 10)	3.00mm × 3.00mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency, Vout = 5V, Fsw = 500kHz

如何讀 Datasheet ?

Pin Configuration

- IC 有哪幾隻腳、長在哪裡
- 每隻腳各自的功能、接法
- 畫電路圖的時候常用到

4 Pin Configuration and Functions

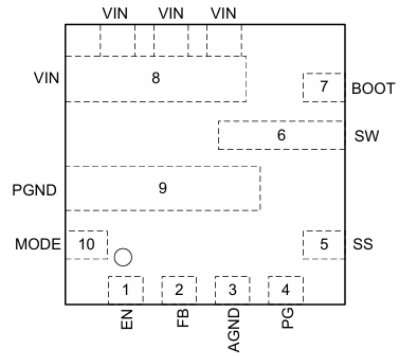


Figure 4-1. RPA Package, 10-Pin VQFN-HR (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input control. Driving EN high or leaving this pin floating enables the converter. A resistor divider between this pin, VIN and AGND can be used to implement an external UVLO.
FB	2	I	Output feedback. Connect FB to the output voltage with a feedback resistor divider.
AGND	3	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
PG	4	O	Open drain power-good indicator, this pin is asserted low if output voltage is out of PG threshold due to overvoltage, undervoltage, thermal shutdown, EN shutdown, or during soft start.
SS	5	O	Soft-start time selection pin. Connecting an external capacitor to AGND to set the soft-start time and if no external capacitor is connected, the soft-start time is 1.8ms by default.
SW	6	O	Switching node terminal. Connect the output inductor to this pin with wide and short tracks.
BOOT	7	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1µF bootstrap capacitor between BOOT and SW.
VIN	8	P	Input voltage supply pin. Drain terminal of high-side MOSFET. Connect the input decoupling capacitors between VIN and PGND.
PGND	9	G	Power GND terminal. Source terminal of low-side MOSFET.
MODE	10	I	Connect this pin with a 52.3K resistor to AGND.

(1) I = Input, P = Power, G = Ground, O = Output.

如何讀 Datasheet ?

Detailed Description

- 深入解釋 IC 的功能
- 設計電路的時候可能要讀懂
- 通常內容比較複雜

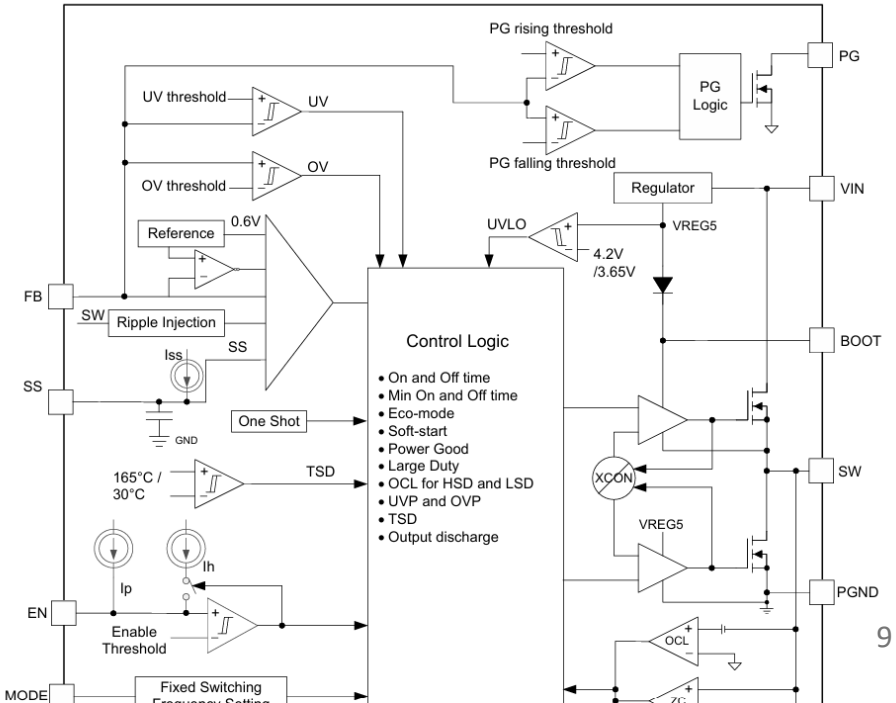
6 Detailed Description

6.1 Overview

The TPS56A37 is an 10A synchronous buck converter operating from 4.5V to 28V input voltage (Vin). The device output voltage ranges from 0.6V to 13V (Vout) and supports 10A continuous output current with fixed 500kHz switching frequency. The proprietary D-CAP3 control mode enables low external component count, ease of design, optimization of the power design for power, size and efficiency. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. Eco-mode allows the TPS56A37 to maintain high efficiency at light load. The TPS56A37 is able to adapt both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The EN pin has an internal pullup current that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. Soft-start time can be set by connecting a capacitor to the SS pin. Leaving the SS pin floating is set to default 1.8ms soft-start time. The TPS56A37 has the PG pin to indicate output status and has a built-in discharge function by using an integrated MOSFET with 200Ω $R_{DS(on)}$. The device is protected from output short, undervoltage, overvoltage, and overtemperature conditions.

6.2 Functional Block Diagram



如何讀 Datasheet ?

Application

- 應用上的範例
- 可以直接抄範例電路來用

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic of Figure 7-1 shows a typical application for TPS56A37. This design converts an input voltage range of 5.5V to 28V down to 5V with a maximum output current of 10A.

7.2 Typical Application

The application schematic in Figure 7-1 shows the TPS58637 5.5V to 28V input, 5V output converter design meeting the requirements for 10A output. This circuit is available as the evaluation module (EVM). The following sections provide the design procedure.

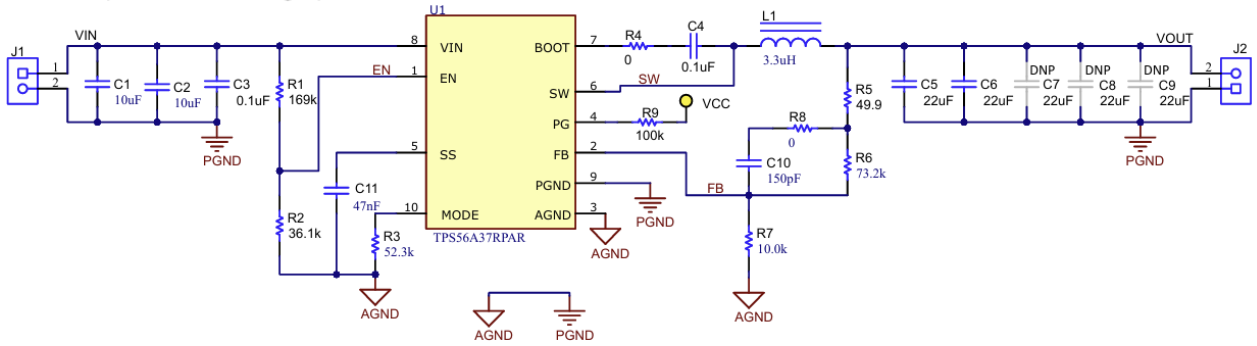


Figure 7-1. TPS56A37 5V, 10A Reference Design

7.2.1 Design Requirements

Table 7-1 shows the design parameters for this application.

Table 7-1. Design Parameters

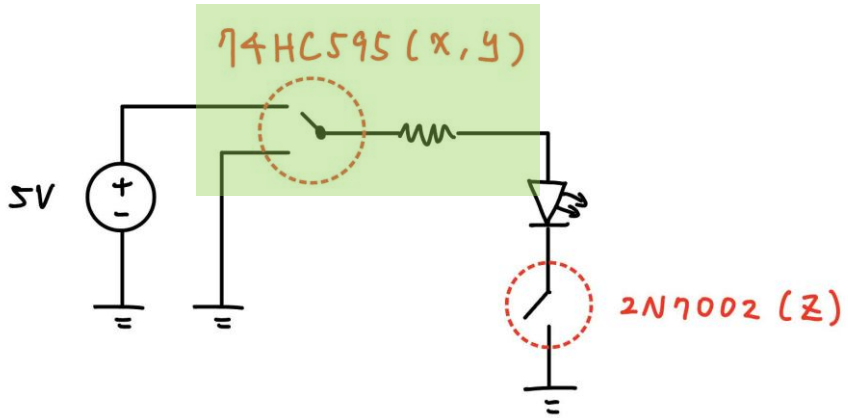
PARAMETER	EXAMPLE VALUE
Input voltage range	24V nominal, 5.5V to 28V
Output voltage	5V
Transient response, 10A load step	ΔV_{OUT} = ±5%
Output ripple voltage	< 50mV at CCM
Output current rating	10A
Operating frequency	500kHz

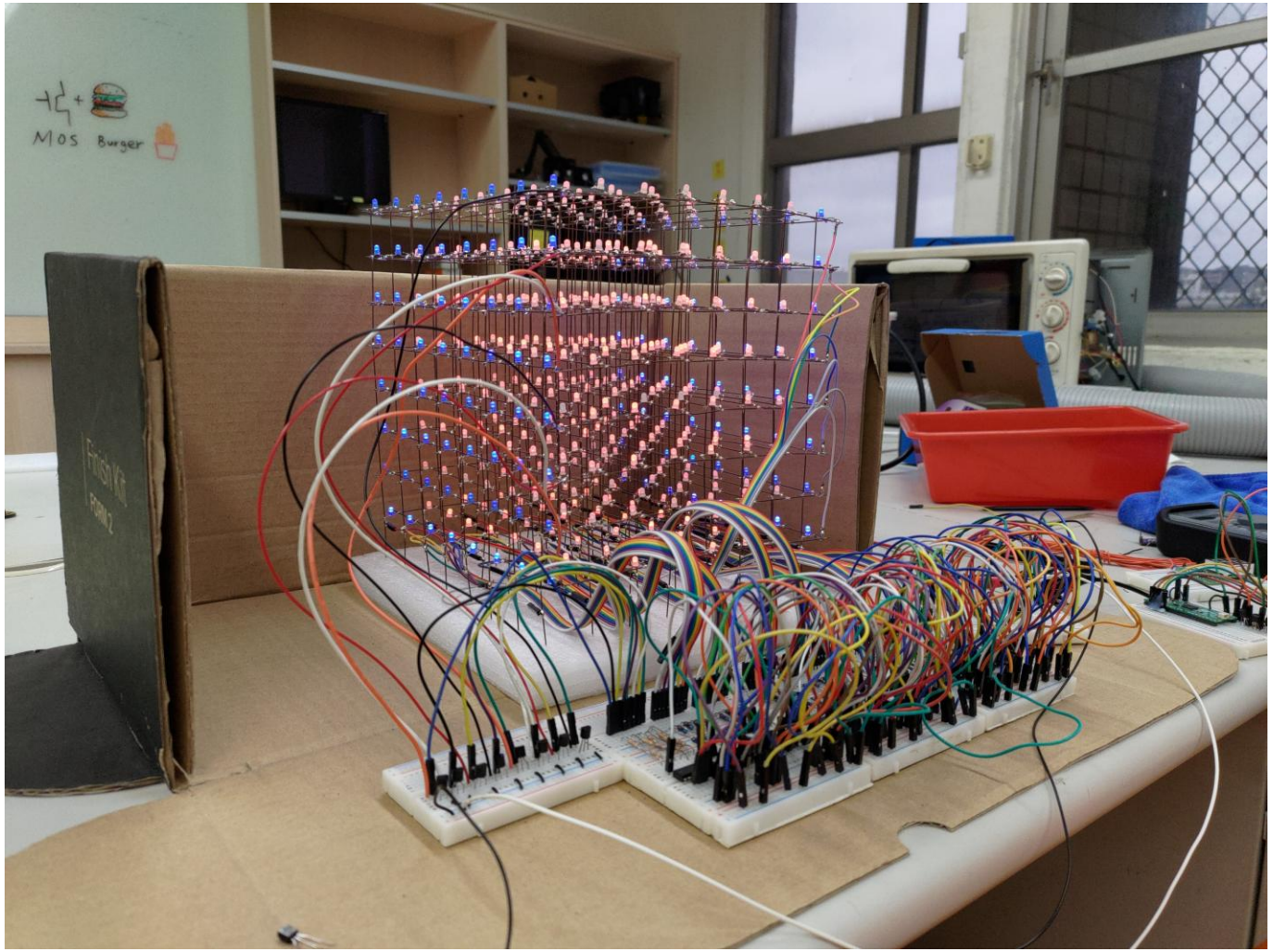
Design Example:
74HC595 Shift Register LED Driver

目標

幫 8x8x8 LED 方塊
做一個更好的驅動電路

我們今天要做控制 x, y 方向的電路



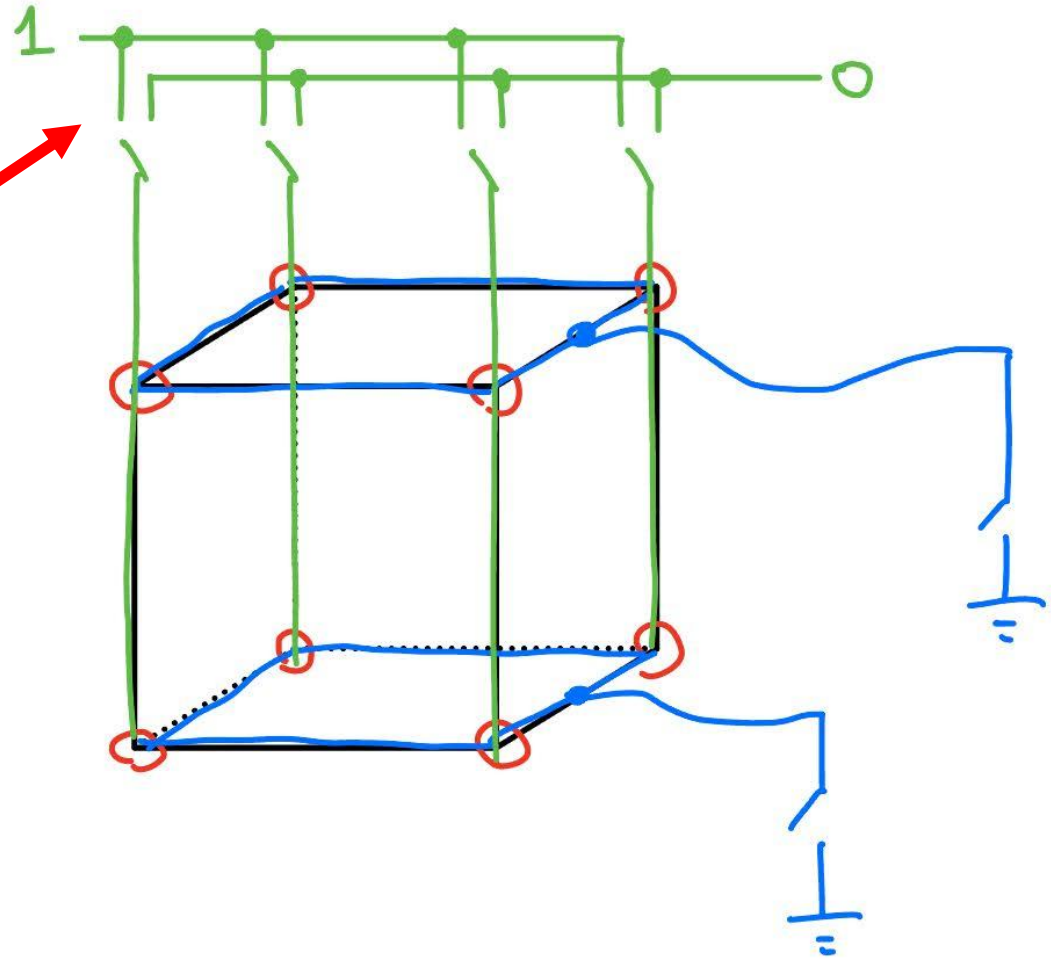


LED 的控制方法

我們今天做的電路會控制 x, y 方向是否給電

另一個電路控制 z 方向是否導通

搭配控制的程式就可以獨立操控每一顆 LED

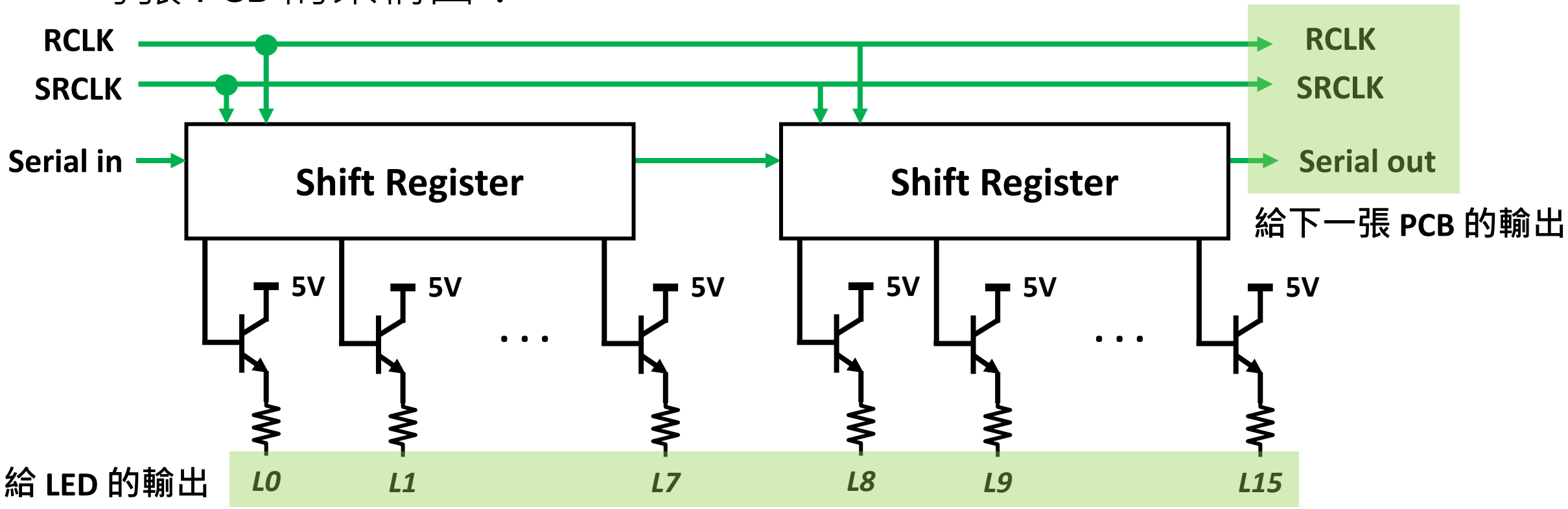


第一步：定義系統規格

- 我們的系統規格包括：
  - x,y 方向總共有幾條需要獨立控制的線？ 8 x 8 = 64條
  - 每條線最高需要多少電流？10mA x 8顆 LED = 80mA

第二步：建立系統架構

- 因為 PCB 一次最少要做 5 張，所以我們把 64 條線分配給 4 張 PCB。
- 每張 PCB 的架構圖：



第三步：選擇適合的 IC

74XX / CD4XXX -> 邏輯電路 IC

TEXAS INSTRUMENTS

SN54HC595, SN74HC595

SCLS041J – DECEMBER 1982 – REVISED OCTOBER 2021

SNx4HC595 8-Bit Shift Registers With 3-State Output Registers

1 Features

- 8-bit serial-in, parallel-out shift
- Wide operating voltage range of 2 V to 6 V
- High-current 3-state outputs can drive up to 15 LSTTL loads
- Low power consumption: 80-μA (maximum) I_{CC}
- t_{pd} = 13 ns (typical)
- ±6-mA output drive at 5 V
- Low input current: 1 μA (maximum)
- Shift register has direct clear
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Network switches
- Power infrastructure
- LED displays
- Servers

3 Description

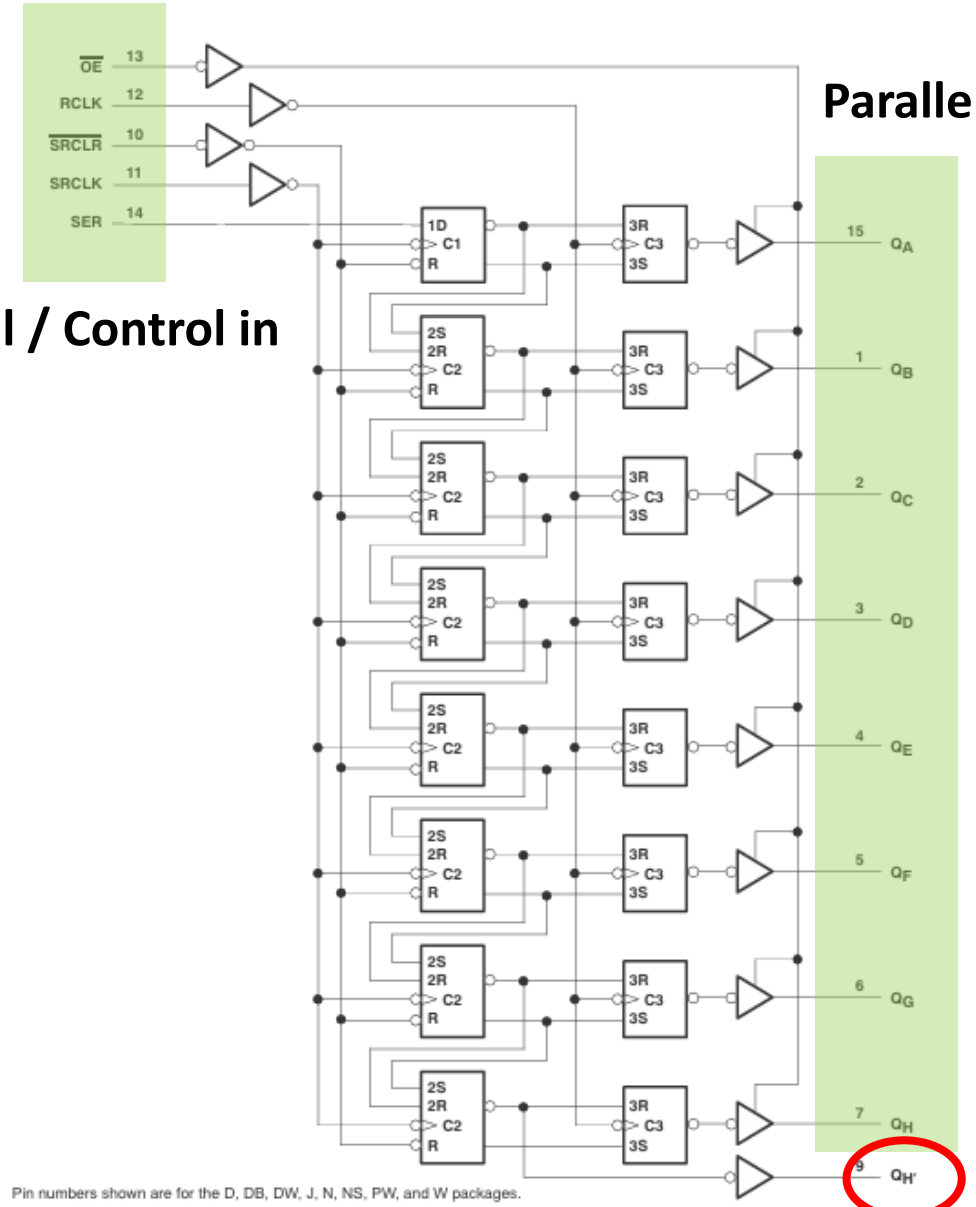
The SNx4HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN54HC595FK	LCCC (20)	8.89 mm × 8.89 mm
SN54HC595J	CDIP (16)	21.34 mm × 6.92 mm
SN74HC595N	PDIP (16)	19.31 mm × 6.35 mm
SN74HC595D	SOIC (16)	9.90 mm × 3.90 mm
SN74HC595DW	SOIC (16)	10.30 mm × 7.50 mm
SN74HC595DB	SSOP (16)	6.20 mm × 5.30 mm
SN74HC595PW	TSSOP (16)	5.00 mm × 4.40 mm

Parallel out

Serial / Control in



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

Functional Block Diagram

Serial out

Key Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

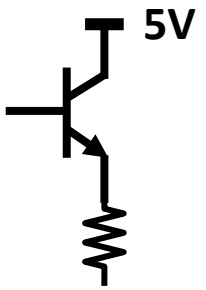
			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current [2]	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

ok，我們用 5V

不 ok，我們要額外設計電路

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

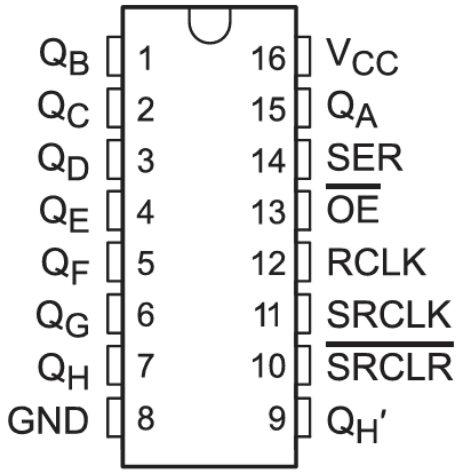
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



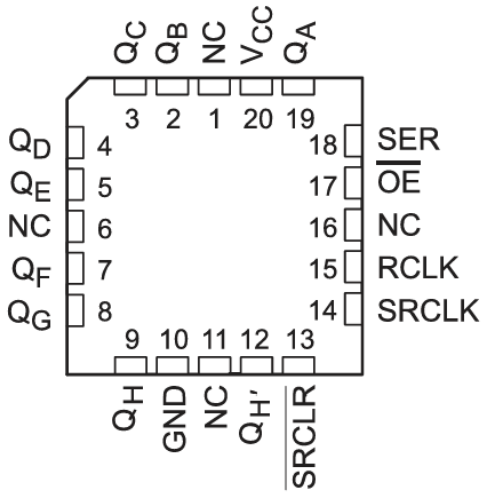
用 NPN 電晶體接
Emitter Follower 增強電流
詳情請見電子學一

Pin Configuration

5 Pin Configuration and Functions



D, N, NS, J, DB, or PW Package
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View

有時候同一款 IC 會有不同封裝，
我們今天用的是 SOIC-16 封裝

Detailed Description

邏輯 IC 的話會給 Truth Table 或 Timing Diagram

回去讀 Datasheet P11-12，
下禮拜問大家 Input 訊號要怎麼給

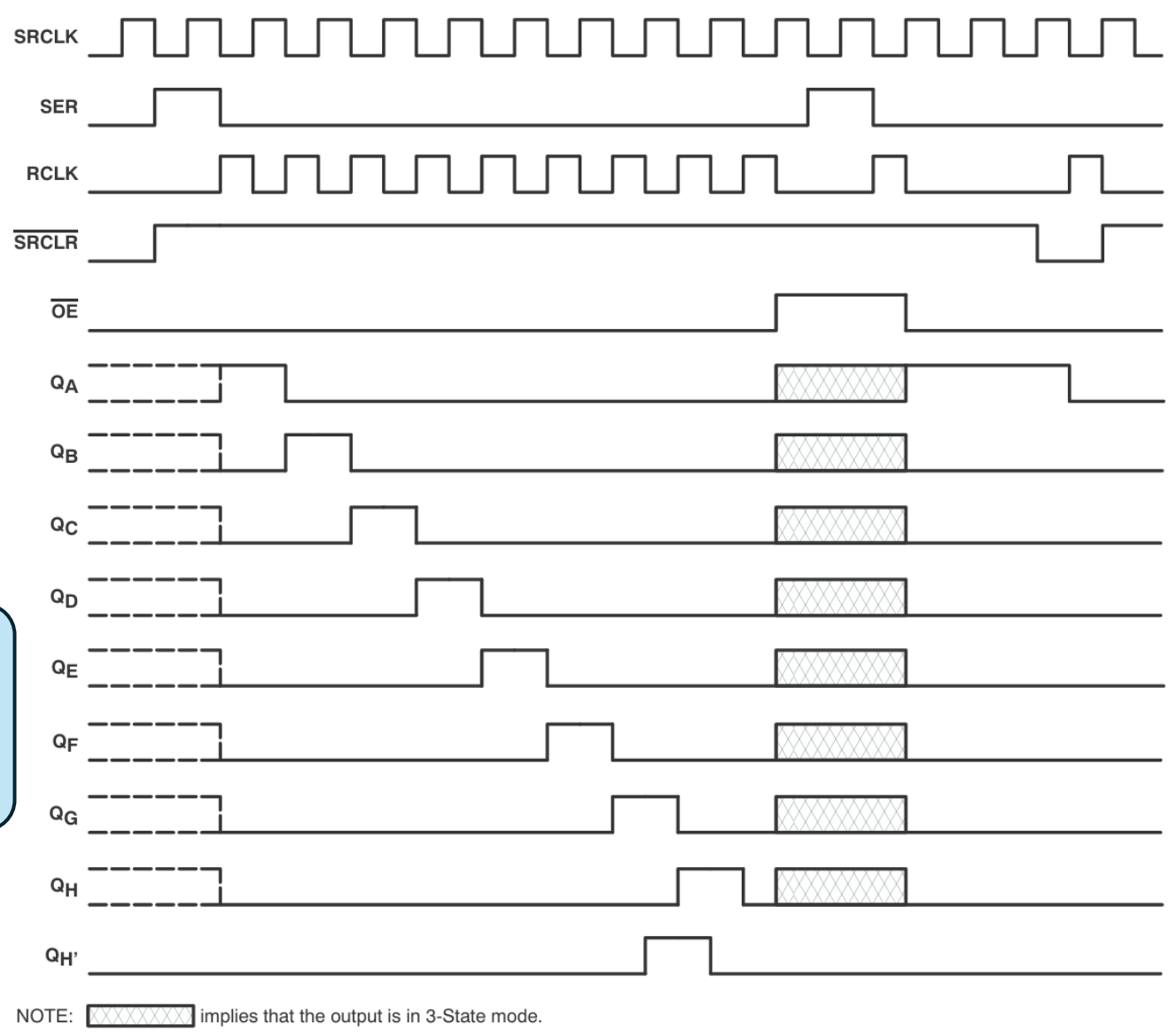
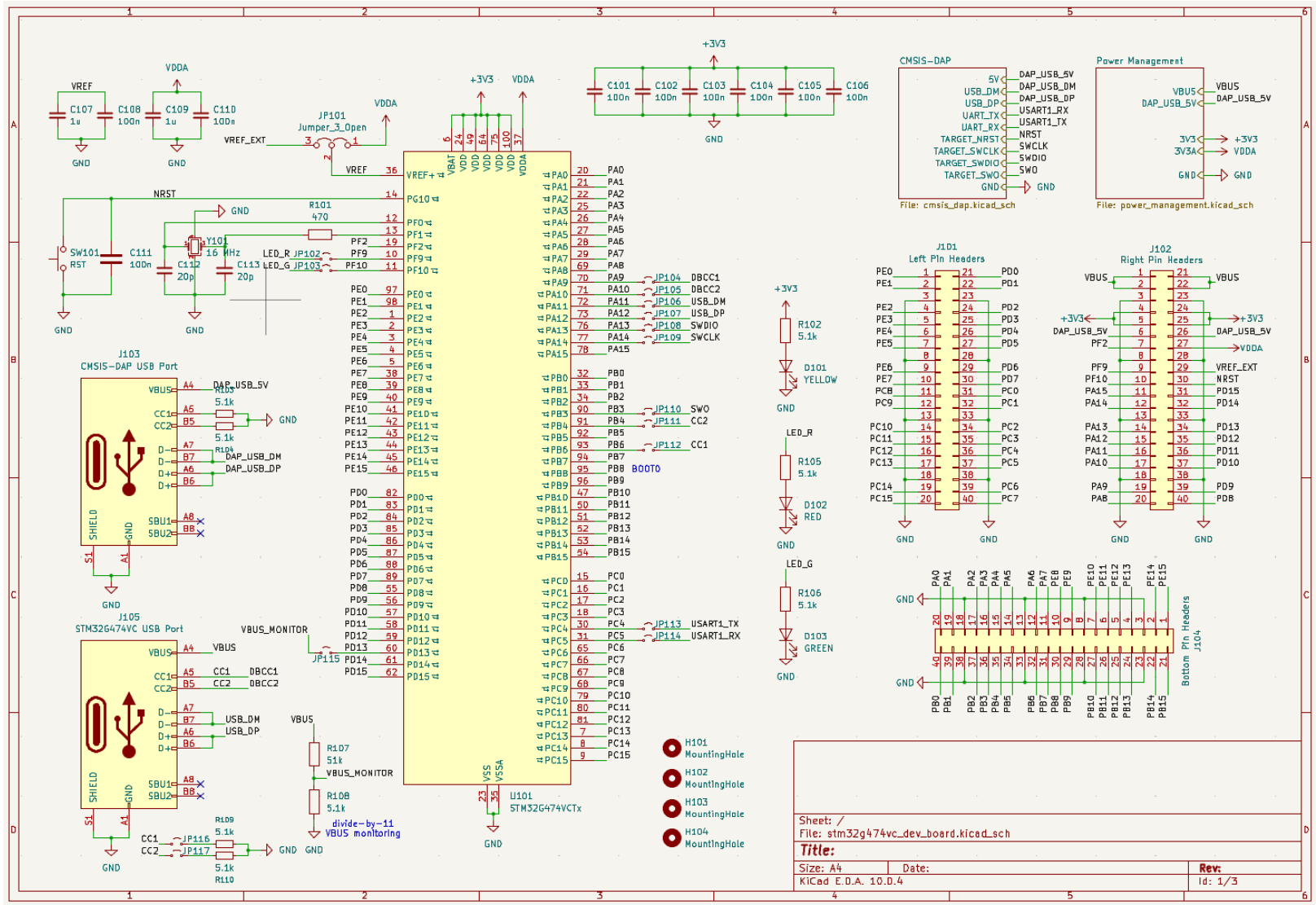


Figure 6-1. Timing Diagram

第四步：畫電路圖 Schematic

「想像中」IC 該怎麼接起來

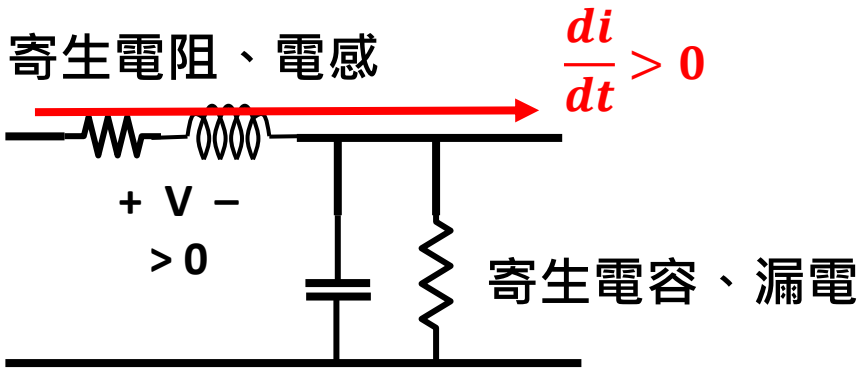
- 盡量高電位在上、GND在下
- 相關的電路畫近一點
- 可以用 label 把線取代掉

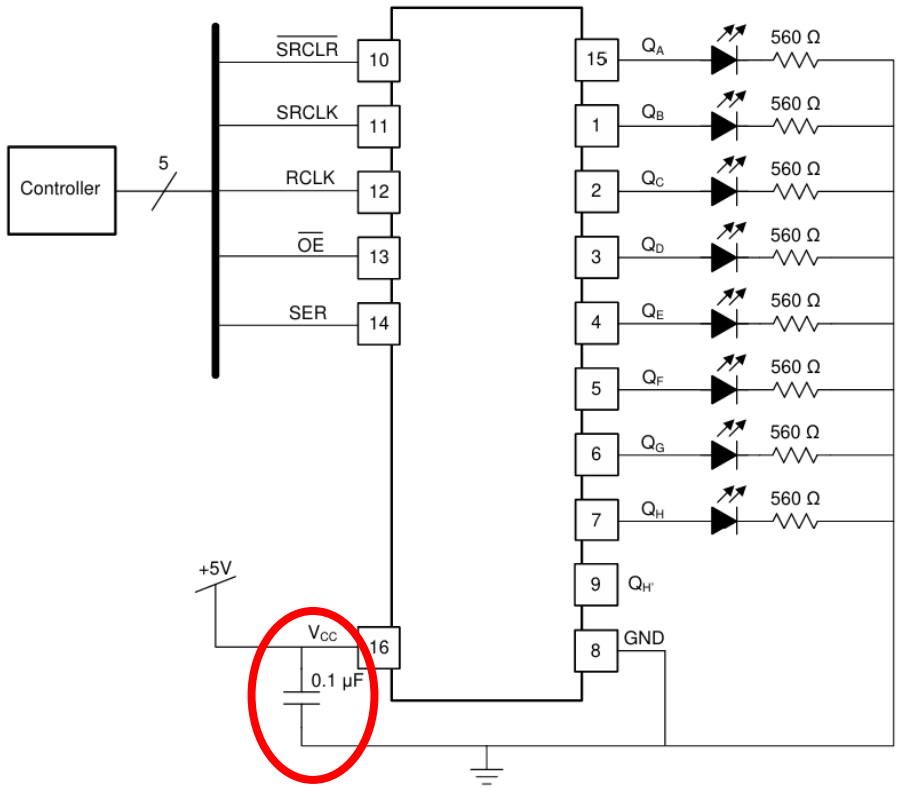


去耦電容 Decoupling Capacitor

實際上的導線不是完美的短路

在 IC 供電的腳位旁邊放電容，
提供 IC 瞬間需要的電流



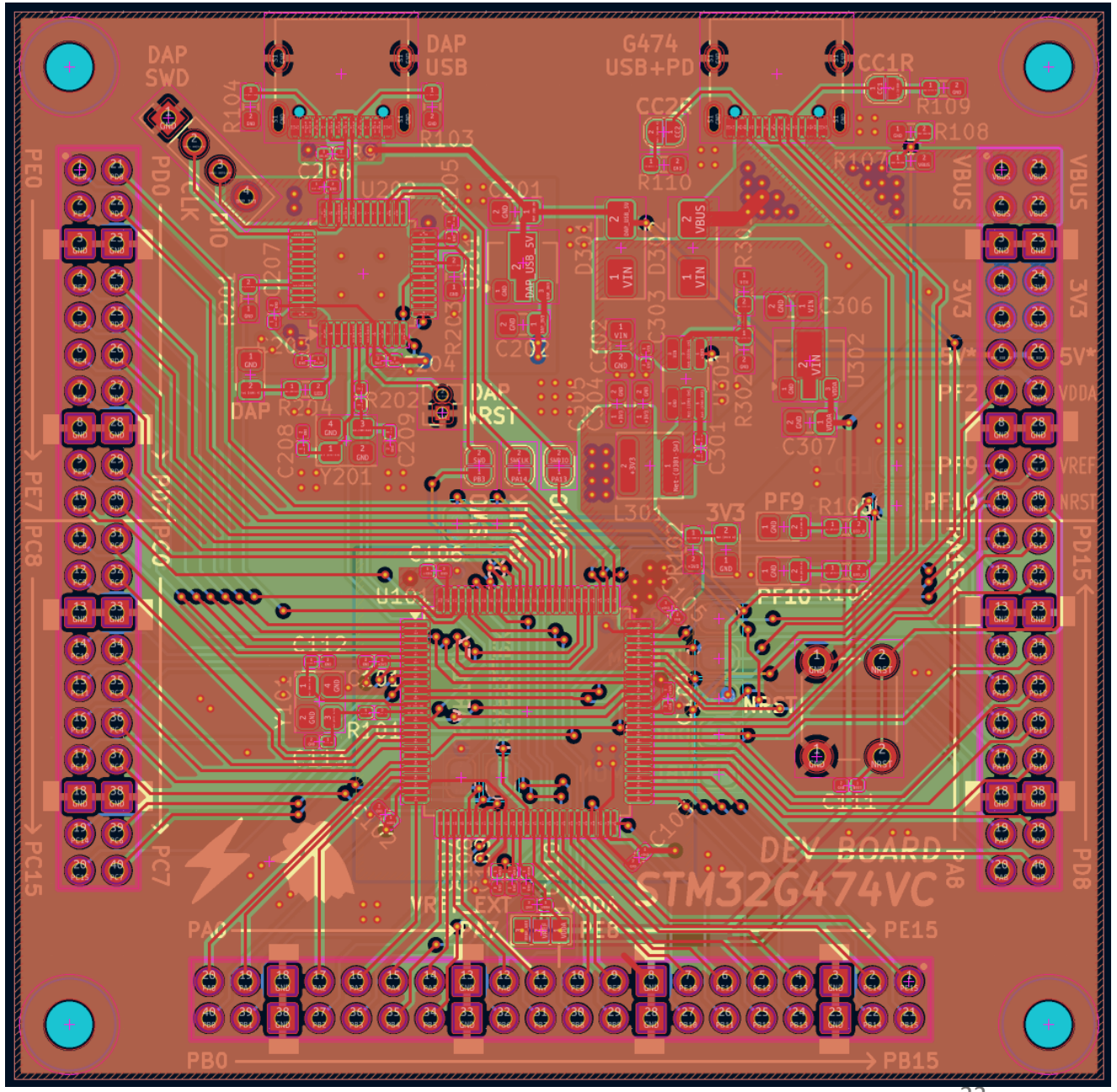


這概念類似蹲久突然站起來會頭暈一樣，
放一顆電容來讓 IC 不要暈倒。

第五步：畫 Layout

「物理上」怎麼接起來

- 相關的電路畫近一點
- 不可以用 label 把線取代掉
- 去耦電容要擺在 IC 旁邊越近越好
- 盡量不要讓線在兩面銅之間鑽來鑽去
- 記得考慮測試的時候會想要看什麼訊號
- 水很深 Orz

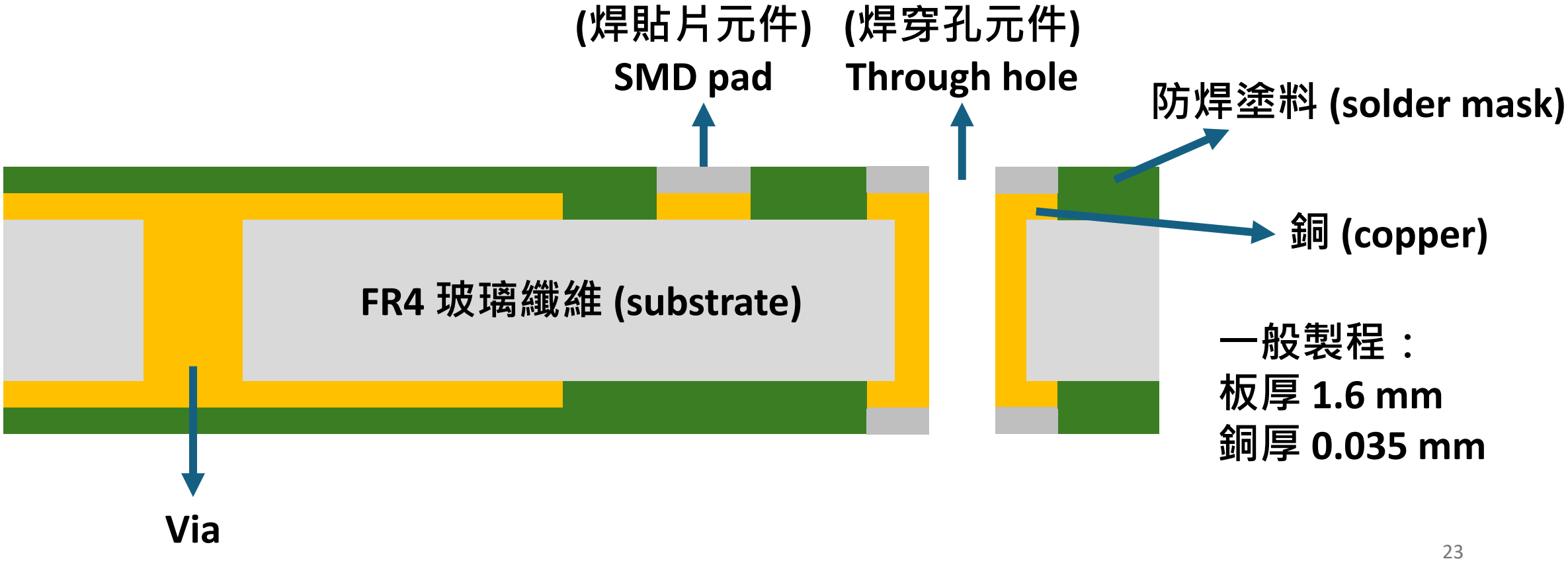


PCB 常見名詞

我們畫 PCB 基本上就是在
控制哪裡有銅哪裡沒有銅

兩層板 (2-layer board):

你願意付錢的話可以搞十幾層



一般製程：
板厚 1.6 mm
銅厚 0.035 mm

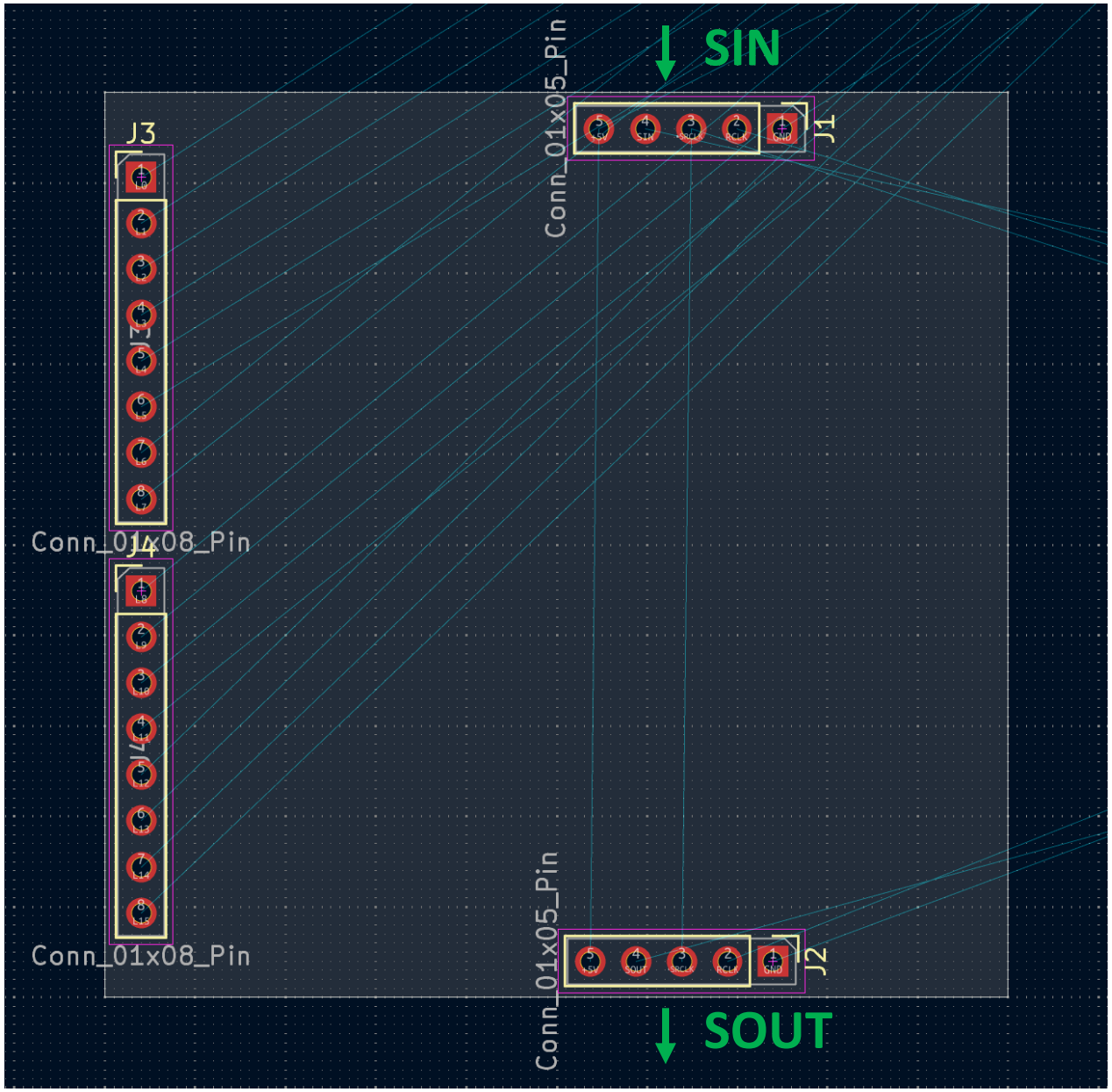
PCB 常見名詞

- Pad: 用來焊接元件的地方
- Via: 用來將兩層銅打洞連接的地方
- Net: 接在一起的同一條線
- Clearance: 兩塊不同 net 的銅之間的距離
- SMD: Surface Mount Device 貼片型元件
- THT: Through Hole Technology 穿孔型元件
- Trace: 銅線
- Plane / Zone: 銅片

Layout 限制

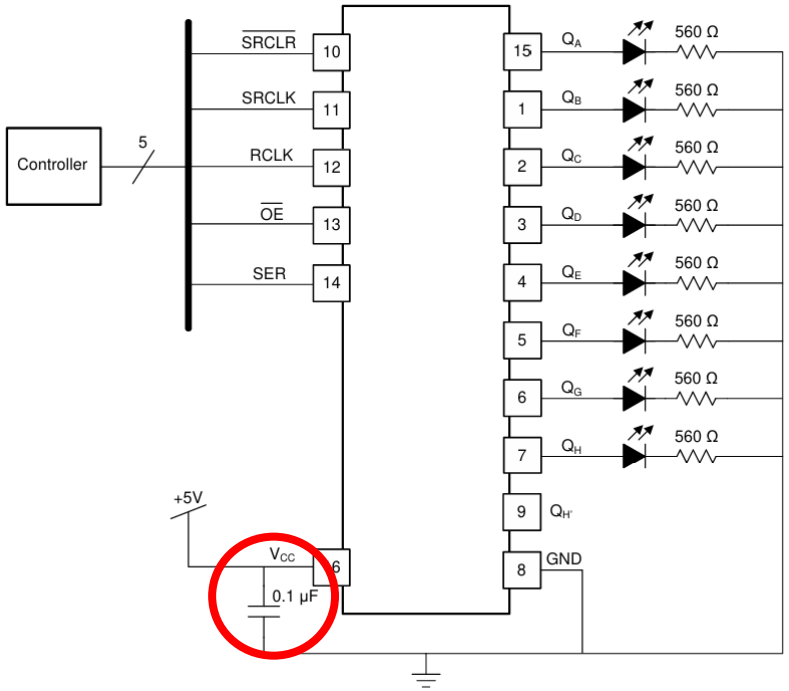
依照系統物理尺寸位置去限制 PCB 上對外連接的位置

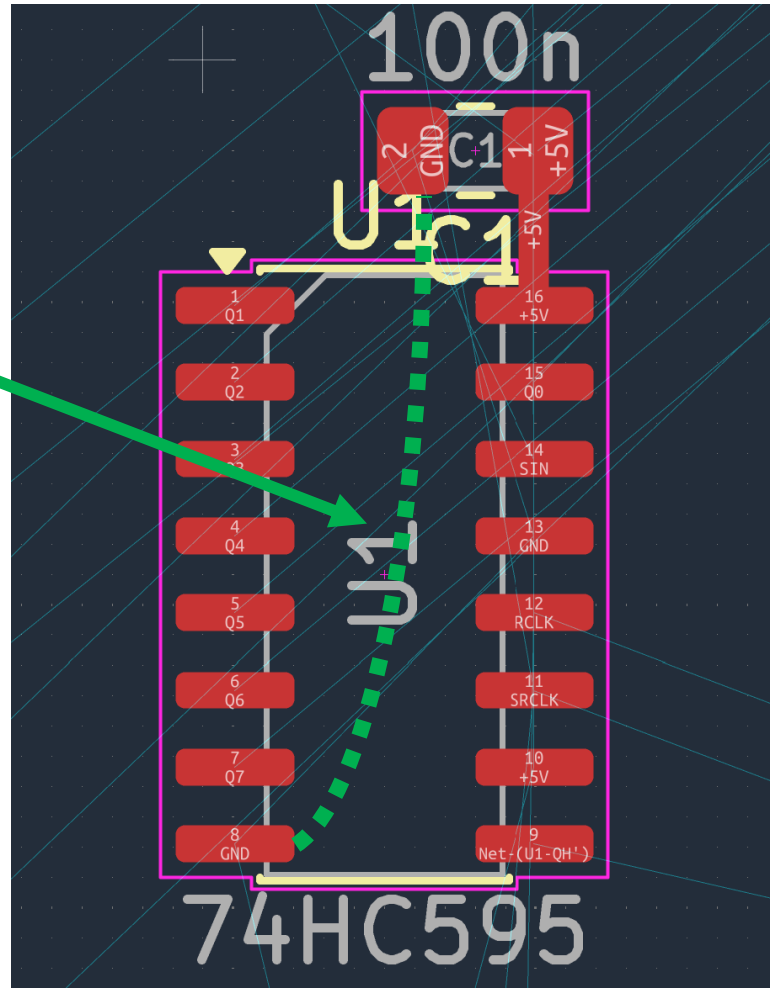
- PCB 尺寸 50x50 (mm)
- PCB 左上角座標 (100, 100)
- 01x08 排針位置 (102, 104.68) 和 (102, 127.54)
- 01x05 排針 x 座標和方向須相同



去耦電容 Decoupling Capacitor

- 去耦電容需要離 IC 的供電腳位越近越好
- GND 的部分最後我們會鋪整塊的銅，
  可以先不用接，但要留一條直接的路

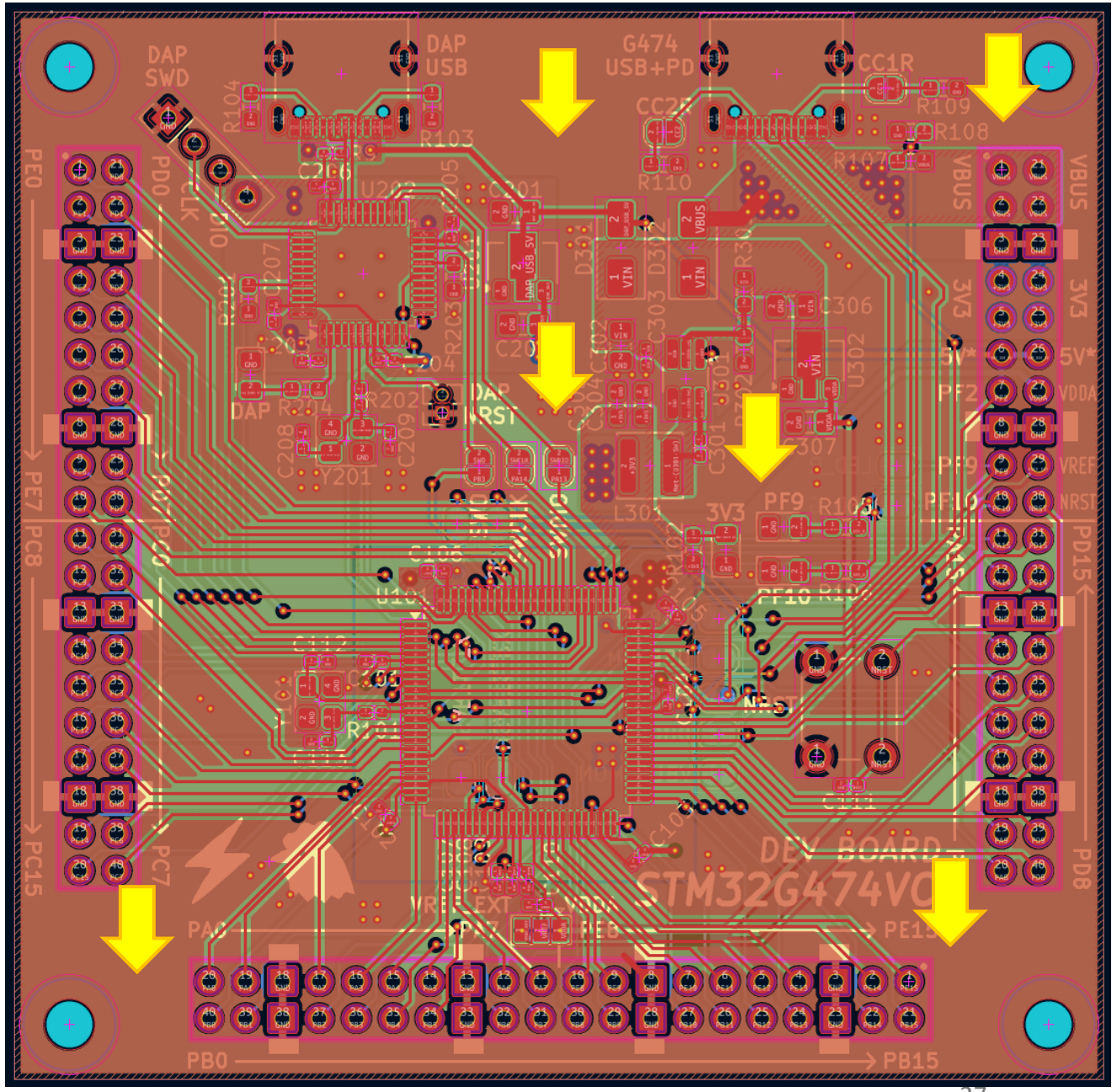




Ground plane

GND 是所有訊號的參考電位

我們會舖一整面的銅連到 GND，讓到處都離參考電位很近

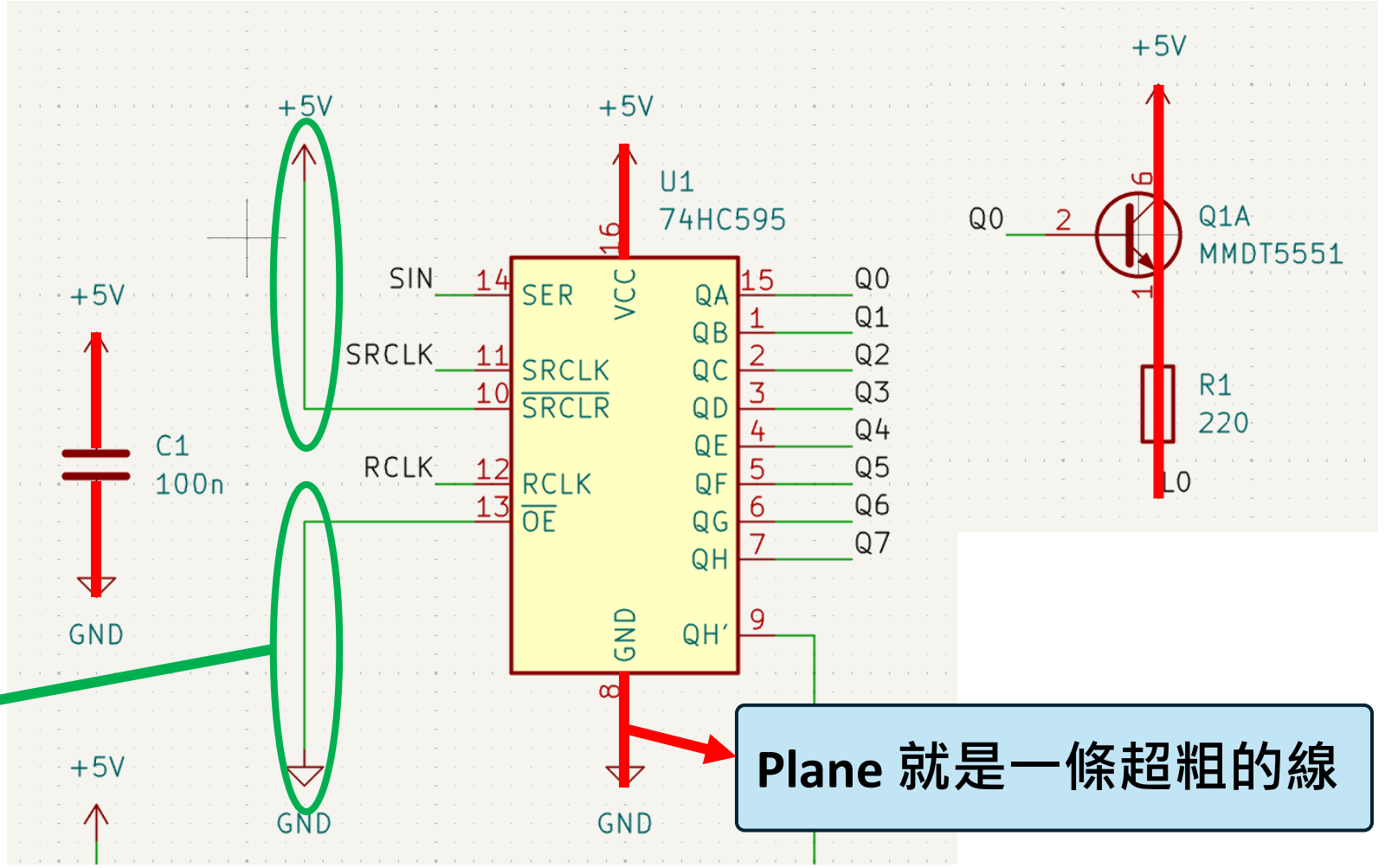


如何找大電流路徑？

大電流路徑要用粗線

- 供電路徑
- LED 驅動路徑

(因為我們一次推 8 顆)



雖然他們也是連到 5V / GND，但是他們只是控制訊號，不會有大電流

Plane 就是一條超粗的線