EE21 106061125 吳俊毅

(a)

(1)

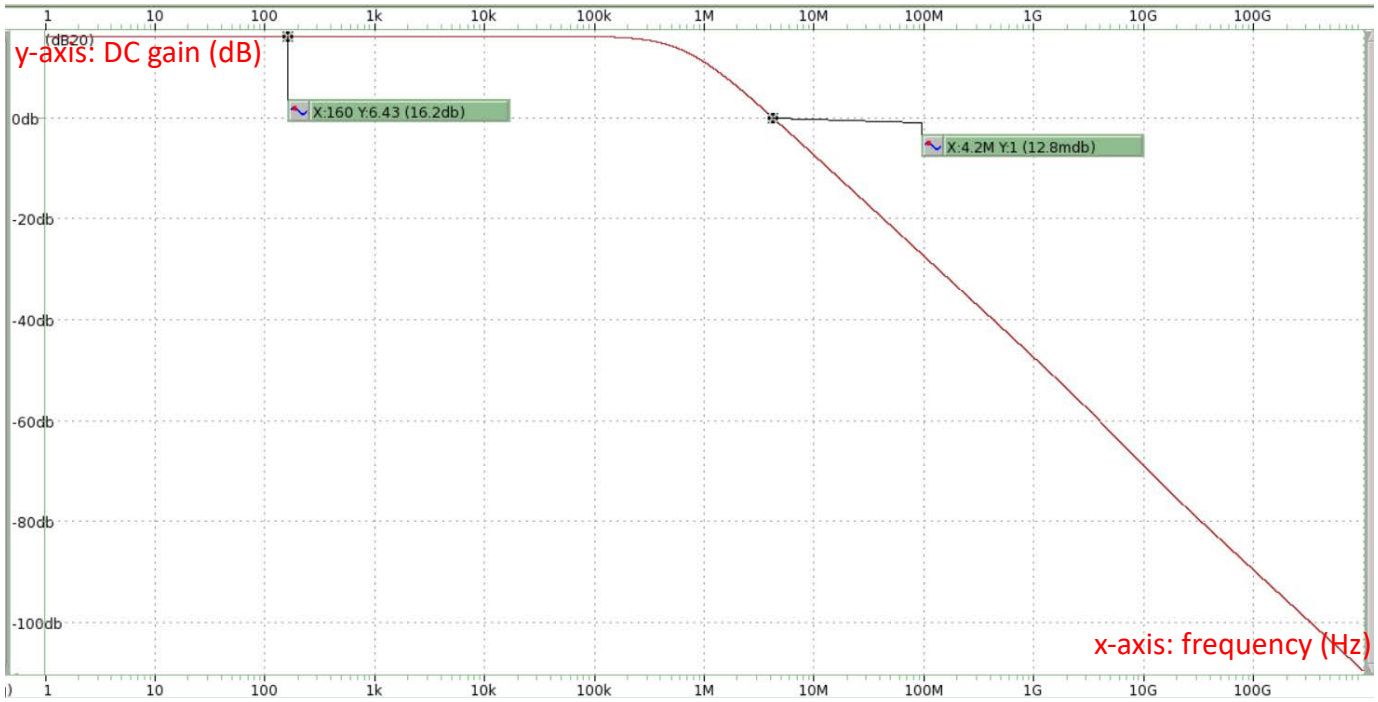


Fig. 1 Differential mode response

From fig. 1, DC gain has reached 16.2dB (>16dB). And the unity gain frequency is about 4.2MHz (>4MHz)

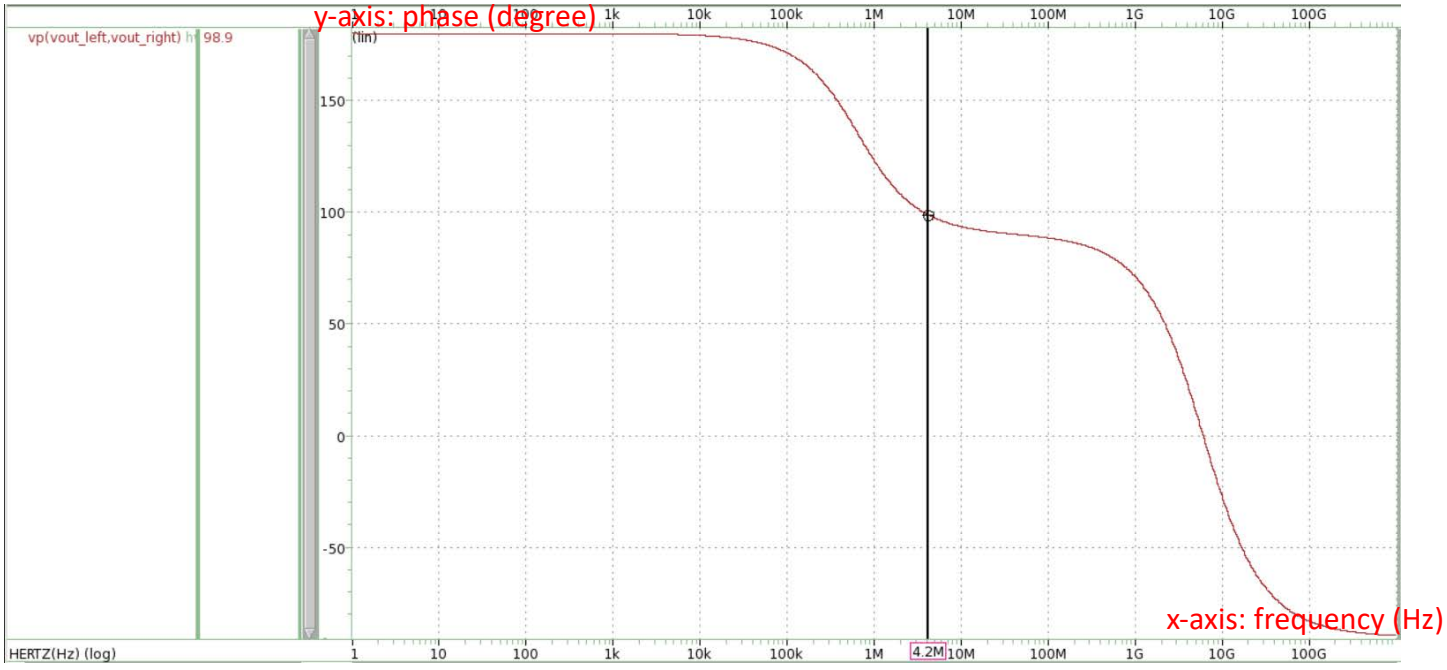


Fig. 2 Phase change over different frequency

From fig. 2, the phase margin is 98.9°+180°=278.9° (>45°)

(2)

**** mosfets

subckt					
element	0:mp_left	0:mp_right	0:mn_left	0:mn_right	0:mx
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-1.9313u	-1.9313u	1.9313u	1.9313u	3.8626u
ibs	8.810e-22	8.810e-22	-89.0805a	-89.0805a	-1.298e-21
ibd	65.4011a	65.4011a	-142.6756a	-142.6756a	-48.9807a
vgs	-1.1929	-1.1929	520.9292m	520.9292m	510.0000m
vds	-1.1929	-1.1929	228.0715m	228.0715m	379.0708m
vbs	0.	0.	-379.0708m	-379.0708m	0.
vth	-492.9590m	-492.9590m	519.6956m	519.6956m	501.4588m
vdsat	-679.5355m	-679.5355m	72.5098m	72.5098m	93.3777m
vod	-699.8986m	-699.8986m	1.2336m	1.2336m	8.5412m
beta	8.0503u	8.0503u	1.4935m	1.4935m	1.6088m
gam eff	557.0845m	557.0845m	517.1285m	517.1285m	507.4462m
gm	5.2609u	5.2609u	40.3121u	40.3121u	66.1390u
gds	40.7593n	40.7593n	966.4096n	966.4096n	3.2910u
gmb	1.6682u	1.6682u	6.0713u	6.0713u	8.9308u
cdtot	398.7292a	398.7292a	3.2091f	3.2091f	1.2477f
cgtot	3.0763f	3.0763f	5.8696f	5.8696f	1.2103f
cstot	3.7934f	3.7934f	6.6350f	6.6350f	1.8721f
cbtot	1.7392f	1.7392f	6.2406f	6.2406f	2.2445f
cgs	2.6901f	2.6901f	3.9775f	3.9775f	735.4284a
cgd	92.6108a	92.6108a	859.0921a	859.0921a	298.3134a

Fig. 3 small signal parameters of each mosfet

(3)

****
****** pole/zero analysis

input = 0:v1 output = v(vout_left,vout)

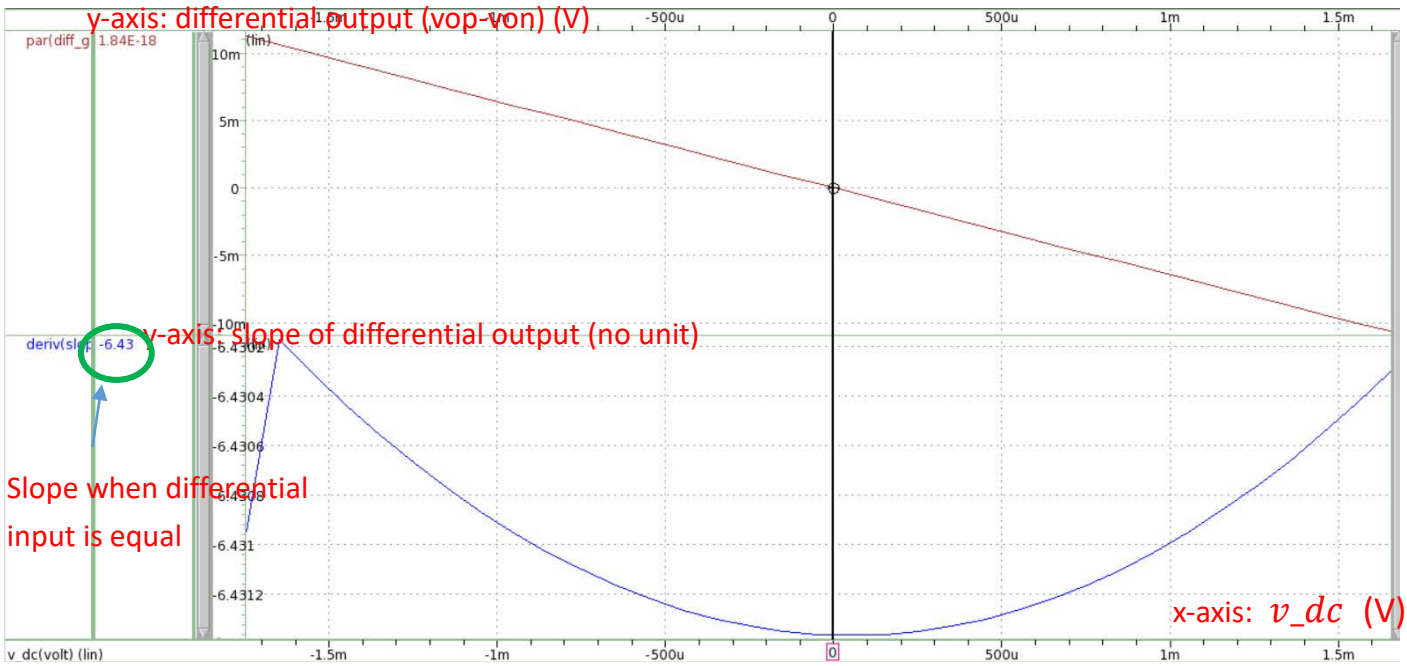
poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-3.54033x	0.	-563.460k	0.
-4.16002x	0.	-662.088k	0.
-7.09541g	0.	-1.12927g	0.
-34.0790g	0.	-5.42384g	0.
-49.5080g	0.	-7.87945g	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-3.56039x	0.	-566.654k	0.
-5.48470g	0.	-872.917x	0.
27.8907g	0.	4.43894g	0.
-41.3711g	0.	-6.58442g	0.

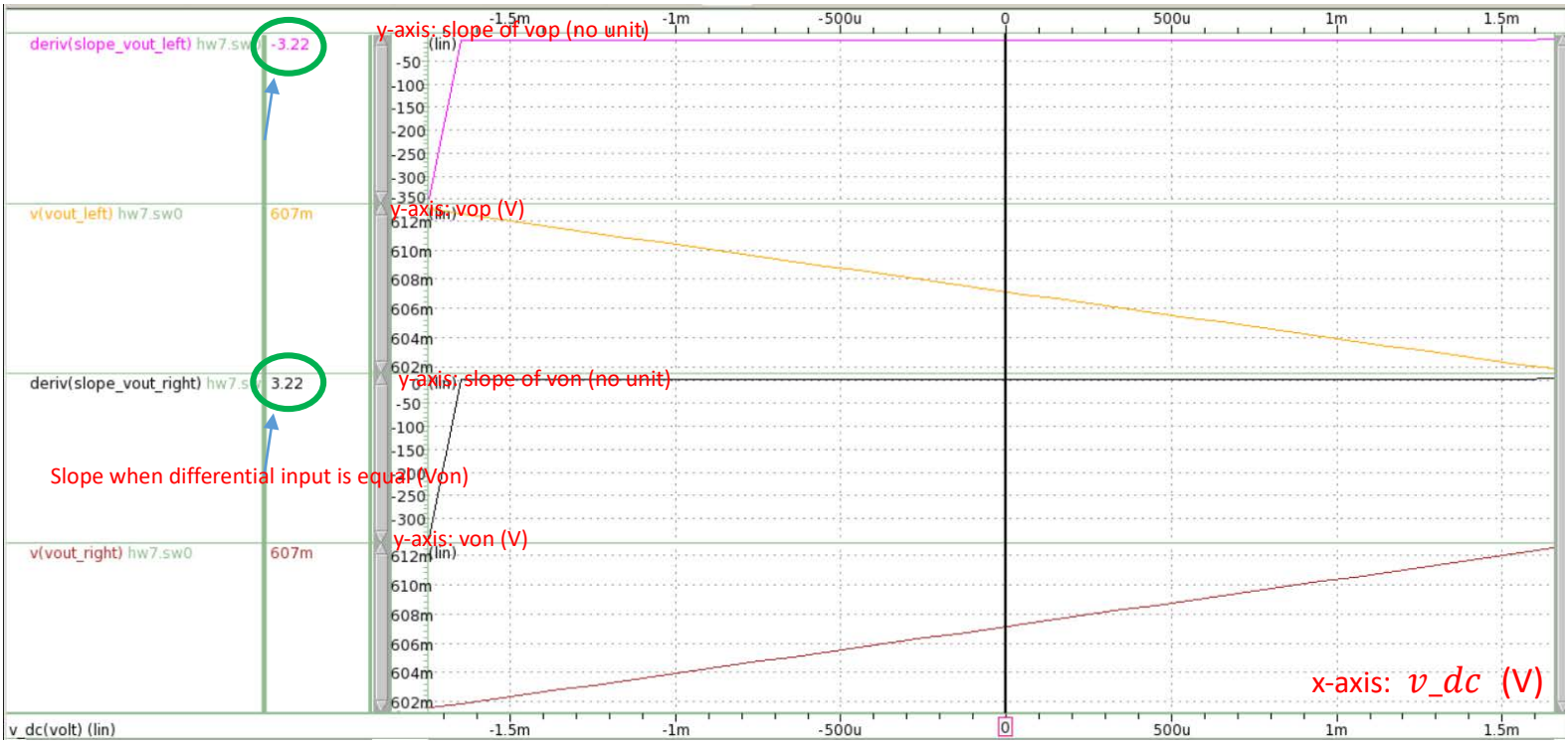
***** constant factor = 26.1548x
******

Fig. 4 pole/zero analysis result

(b)

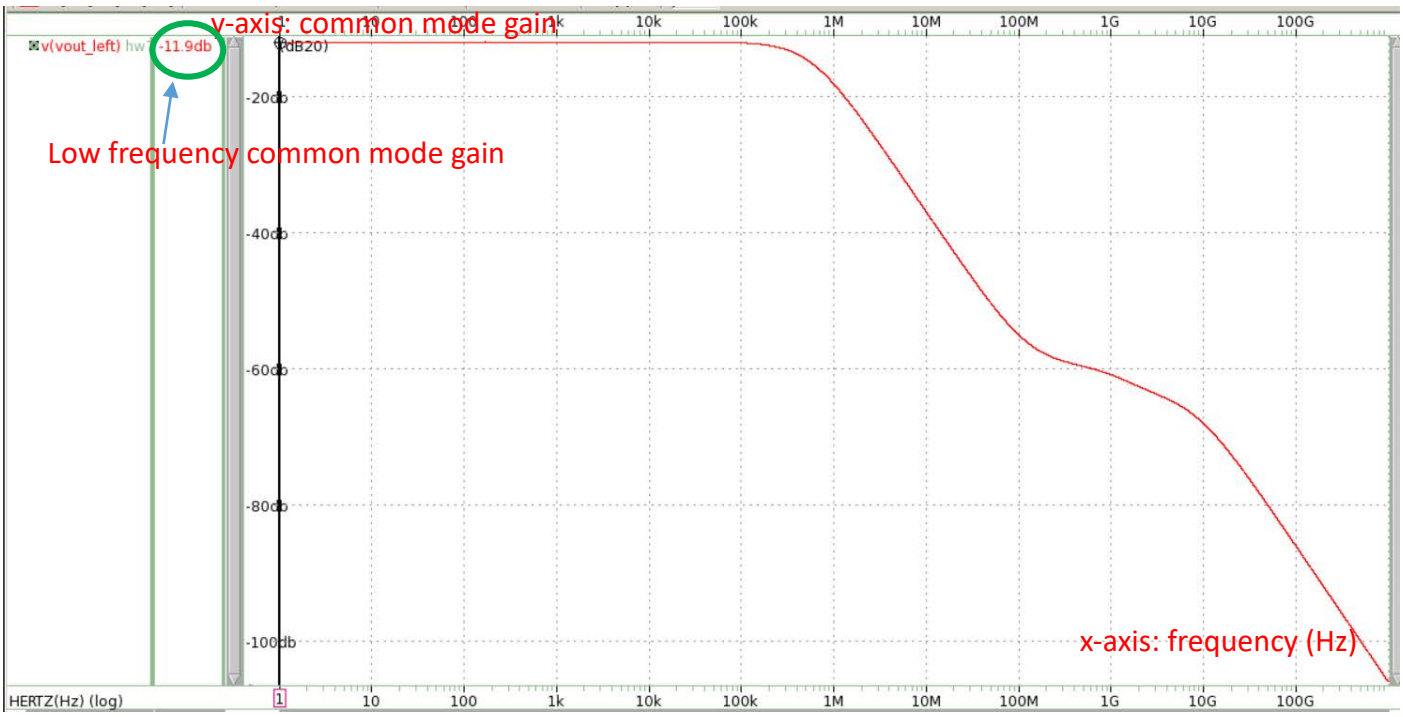


As NMOS (left/right) overdrive voltage is 1.2336m, Thus, maximum of $|V_{in\_left} - V_{in\_right}|$ is $\sqrt{2} \times 0.0012336 = 0.001747$, which is the maximum x-axis value. v_dc is parameter in hspice ($=\frac{V_{in\_left} - V_{in\_right}}{2}$). According to this figure, the slope is -6.43. $20 \times \log|-6.43| = 16.16dB$. The gain is like AC response!



As left-ended output (vop) DC gain is 3.22 (V/V) and right-ended output (von) gain is -3.22 (V/V). So, it implies differential gain is 3.22-(-3.22) = 6.44(V/V) ~16.17dB. It's like AC response

(c)



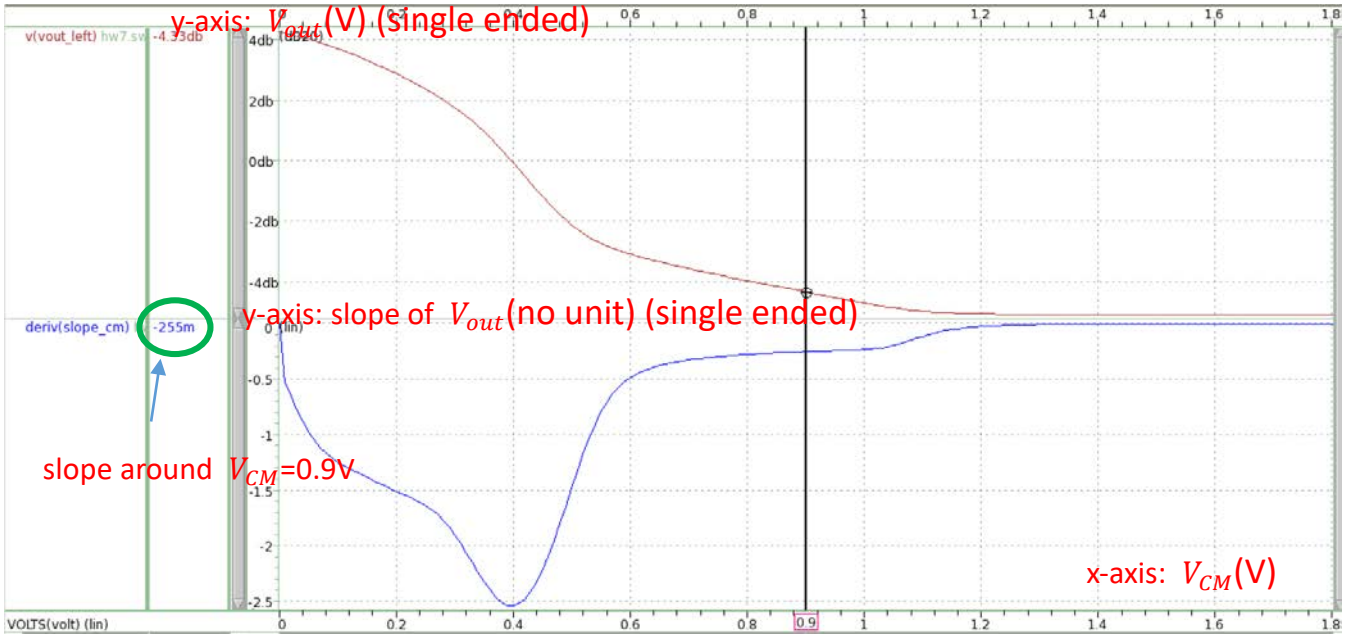
Hand calculation:

$$\frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{\frac{1}{g_{mp}}//r_{op}}{2r_o(NMOS\_tail)+g_m{}^{-1}(NMOS\_left)} = \frac{\frac{1}{5.2609u}//\frac{1}{4.0759n}}{\frac{2}{3.29u}+\frac{1}{40.3121u}}$$ = -0.298 ~-10.5dB

The simulation result is -11.9dB. Error rate is $\frac{-10.5-(-11.9)}{-11.9} = -11.7\%$

This error rate is acceptable. Error may come from imprecise value of tail current source's finite impedance.

(d)



The slope around V_{CM} = 0.9V is -0.255~-11.8dB, which is the so-called common mode gain. It's really close to AC response!

(e)

1MHz

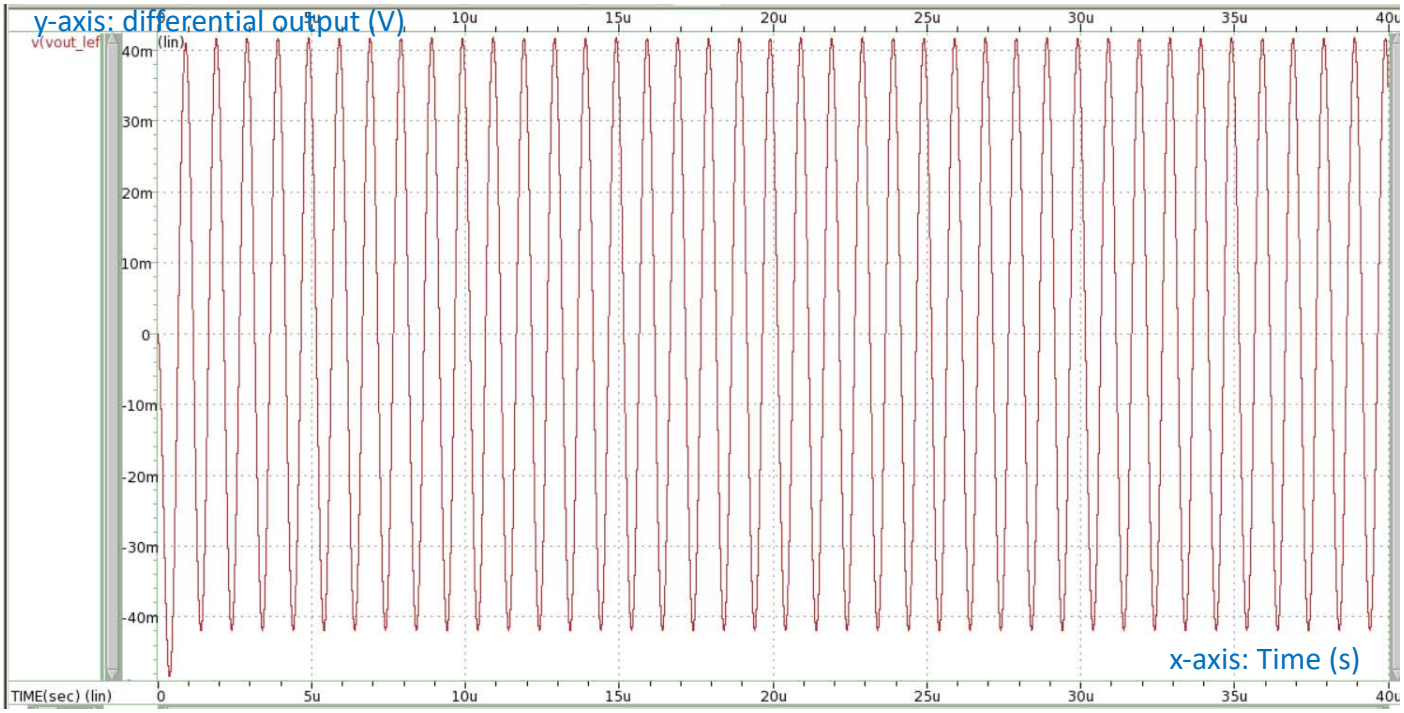


Fig. differential output waveform when input amplitude = 11.8mV at 1MHz

```
harmonic  frequency   fourier     normalized  phase       normalized
no        (hz)        component   component   (deg)       phase (deg)
1            1.0000x   41.7786m     1.0000     33.4860      0.
2            2.0000x   39.5208u   945.9584u   -32.1477    -65.6337
3            3.0000x   13.0155u   311.5360u    19.3671    -14.1189
4            4.0000x   79.4330n     1.9013u   114.0490     80.5630
5            5.0000x   26.1842n   626.7371n  -172.5416   -206.0276
6            6.0000x    5.2204n   124.9544n   170.0762    136.5902
7            7.0000x   16.7827n   401.7063n  -140.7566   -174.2426
8            8.0000x  220.1891p     5.2704n   135.5153    102.0294
9            9.0000x    6.1929n   148.2309n  -108.5433   -142.0293

total harmonic distortion =   0.099594  percent

         ***** job concluded
******
```

By the definition of linear range in this homework, my linear range is 11.8mV!

10MHz

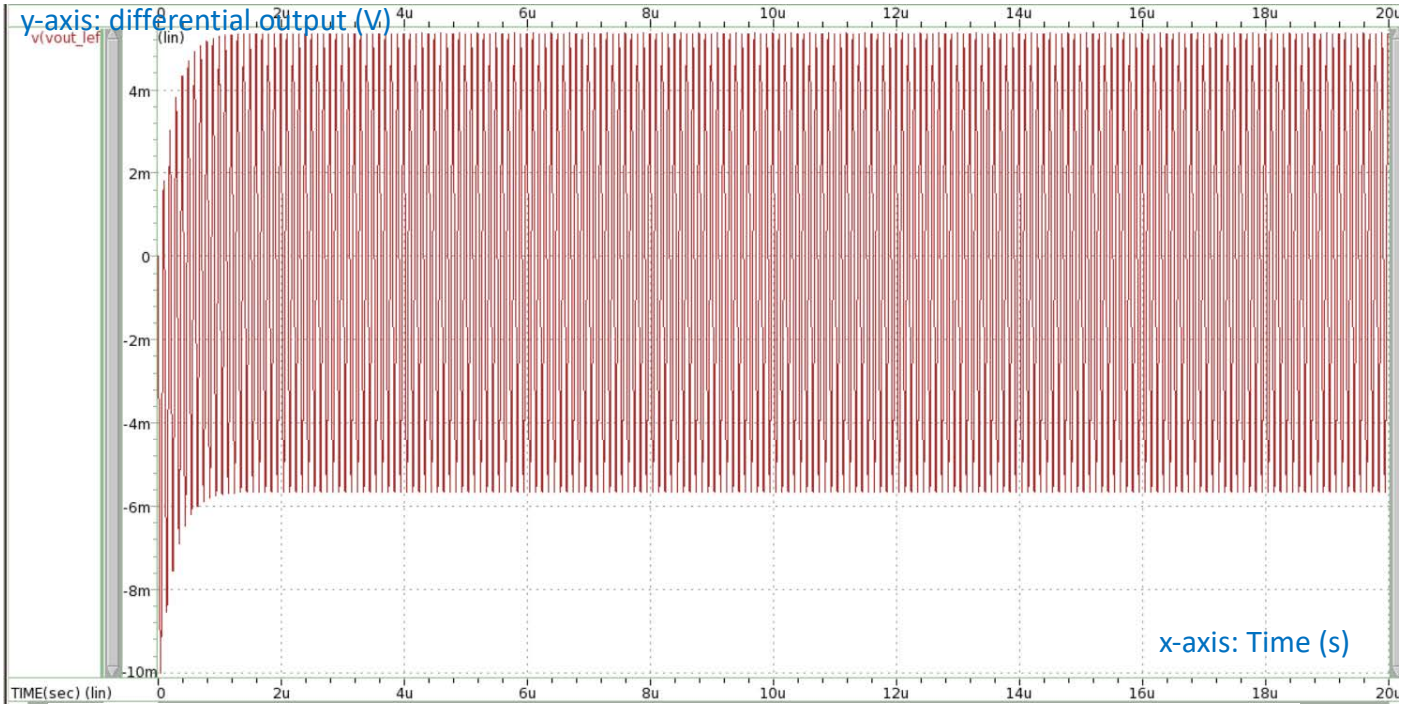


Fig. differential output waveform when input amplitude = 13mV at 10MHz

```
harmonic  frequency   fourier     normalized  phase       normalized
no        (hz)        component   component   (deg)       phase (deg)
1           10.0000x    5.5034m     1.0000      3.6004      0.
2           20.0000x    5.0155u   911.3437u   -78.7811    -82.3815
3           30.0000x    2.2421u   407.3919u   518.0410m    -3.0823
4           40.0000x   35.1457n     6.3861u  -102.7652   -106.3656
5           50.0000x   27.3400n     4.9678u   -69.3563    -72.9567
6           60.0000x    5.9443n     1.0801u  -115.0244   -118.6248
7           70.0000x   11.4661n     2.0834u   -41.5349    -45.1353
8           80.0000x   12.6325n     2.2954u   115.2464    111.6460
9           90.0000x   13.5269n     2.4579u  -149.2673   -152.8676

total harmonic distortion =   0.0998297  percent

          ***** job concluded
******
```

Hand calculation:

By definition, -60dB distortion, input amplitude < $0.2V_{od\_mn\_left}$. According fig. 3 $V_{od\_mn\_left}$ is 1.23mV. $0.2\times 1.23mV$ = 0.246mV. So the linear range is supposed to be lower than 0.246mV. In my case it's 11.8mV.

Error rate is so large! The formula of linear range is based on input amplitude << $V_{od\_mn\_left}$. In my design $V_{od\_mn\_left}$ (1.23mV) << sinwave input amplitude (11.8mV). I think that's why the error rate is that large.

(f)

Since fully differential pair can be analyzed through its half circuit, which is a common source amplifier with active load.

Small signal gain:

Small signal gain = $g_{mn} \times (R_d // r_{on})$, g_{mn} is g_m of NMOS input pair, R_d is effective resistance looking from drain of diode connected PMOS. r_{on} is r_o of NMOS inout pair. Therfore, $R_d = \frac{1}{g_{mp}} // r_{op}$, usually r_{op} >> $\frac{1}{g_{mp}}$ (To satisfy this condition, I increased length of PMOS a little bit as $r_{op} \propto \frac{1}{\lambda I}, \frac{1}{\lambda} \propto Length.$) Similarly, r_{on} >> $\frac{1}{g_{mp}}$ (To satisfy this condition, I increased length of NMOS a little bit). Now gain = $\frac{g_{mn}}{g_{mp}}$ (as $\frac{1}{g_{mp}} // r_{op}$~$\frac{1}{g_{mp}}$, $\frac{1}{g_{mp}} // r_{on}$ ~ $\frac{1}{g_{mp}}$) ~ $\frac{V_{odp}}{V_{odn}}$. But overdrive voltage of PMOS is almost fixed (output common mode voltage is supposed to falls in the range of 0.6V~0.9V). So what I can do is to decrease overdrive voltage of NMOS pair. $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{odn})^2$[ignore CLM]. And I don't want to current to change (NMOS may leave saturation region), when increasing width of NMOS, V_{odn} is supposed to decrease until the gain meet the requirement of problem sets.

Unity gain bandwidth:

I think unity gain bandwidth is related to -3dB bandwidth. (i.e. the larger -3dB bandwidth is, the larger unity gain bandwidth is) -3dB bandwidth = $\frac{1}{R_d \times C_L}$ where R_d is effective resistance looking from drain of diode connected PMOS, which is about $\frac{1}{g_{mp}}$ (analyzed above) and C_L is a fixed value given by problem sets (1.5pF). So, -3dB bandwidth is equal to $\frac{2I}{|V_{odp}| \times C_L}$ $V_{odp} = |V_{out\_left} - VDD| - |V_{th}|$, VDD is fixed, V_{th} is almost fixed. So, output common mode should be be as close to 0.9V as possible (the requirement is 0.6V ~ 0.9V). And at the same time, I also try to increase width of tail NMOS to increase current until unity gain bandwidth larger than 4MHz (as FOM = $\frac{unity\ gain\ bandwidth \times linear\ range}{tail\ current}$)

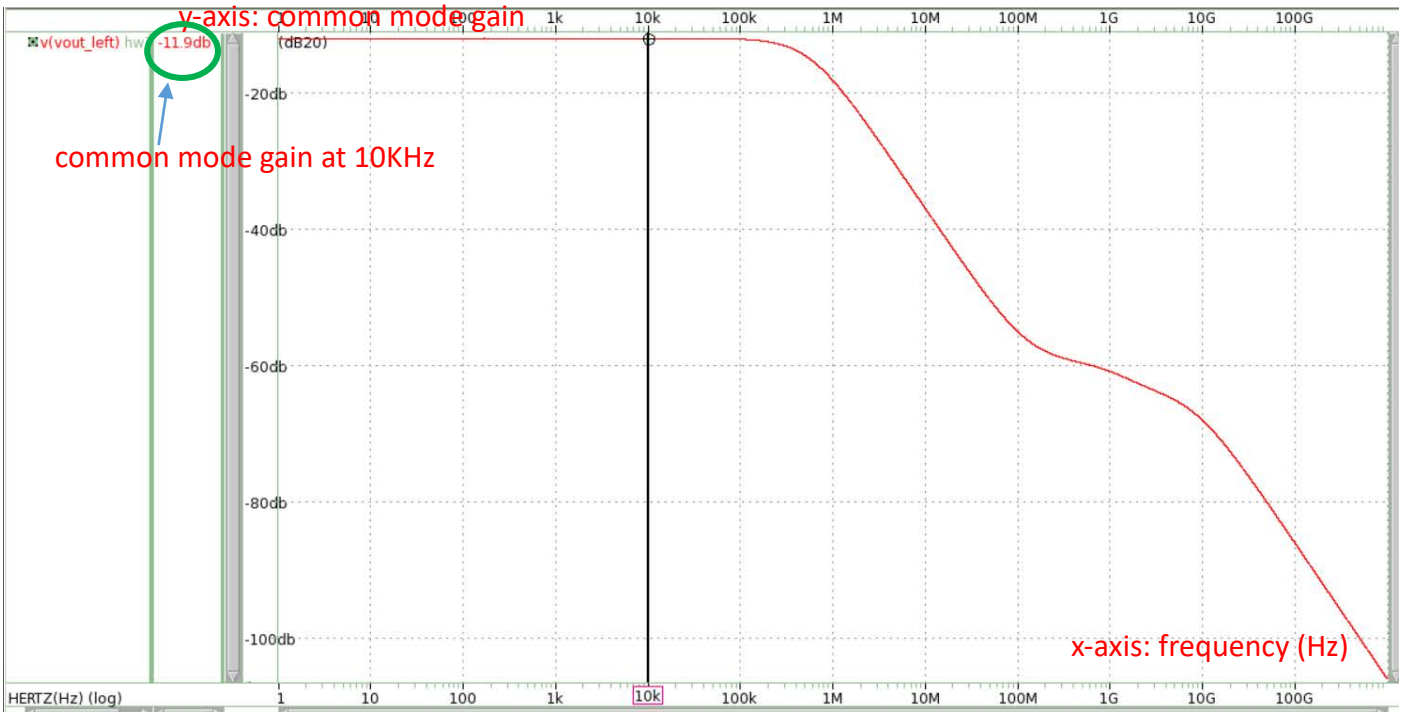
Linear range:

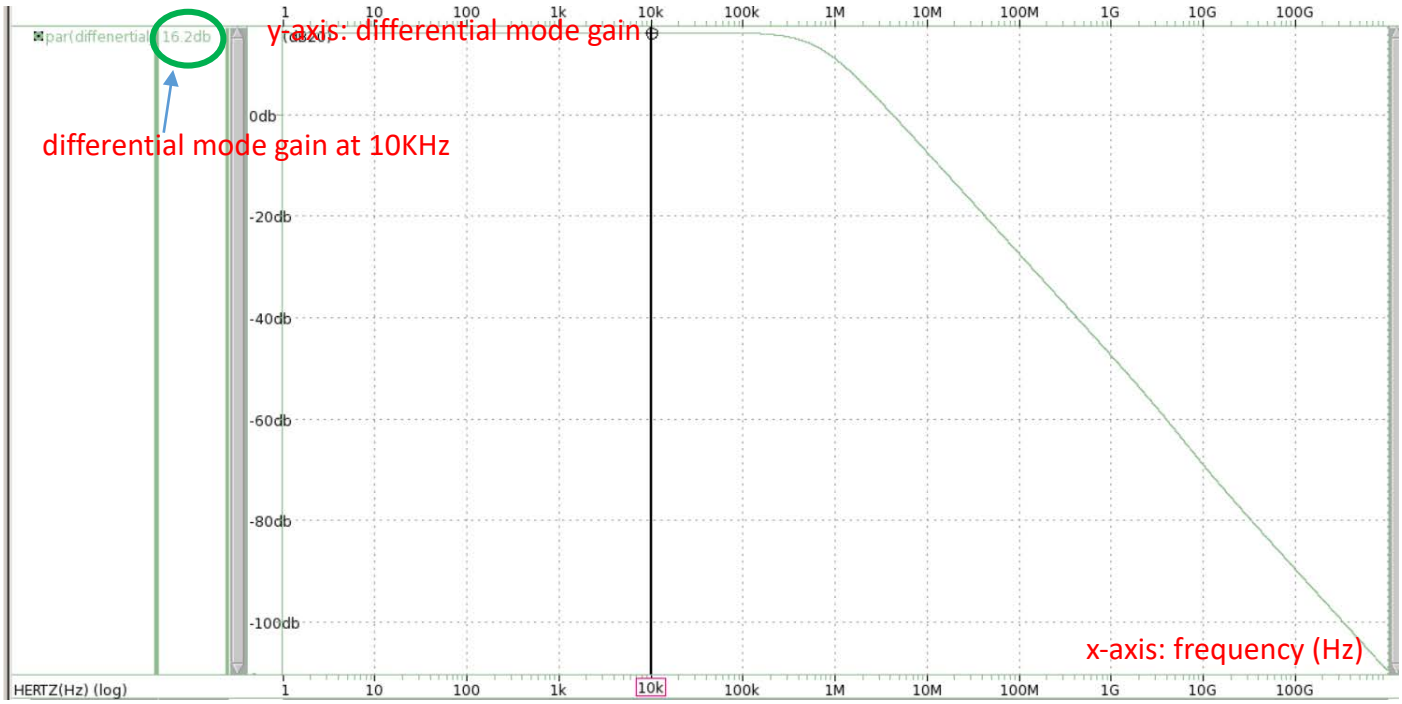
Linear range is equal to 0.2× $(overdrive\ voltage\ of\ NMOS\ pair)$. $V_{odn} = V_{CM} - V_s - V_{thn}$. V_{CM} Has been given by problem sets (0.9V). V_{thn} is almost fixed. Therefore, to increasae V_{odn}, what I can do is reduce V_s. So, I stregthen tail NMOS by increasing its width and set its length to miuimum value in 'cic018.l'. (not too much or the tail current will exceed 4uA).

Tail current:

Tail current = $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{od\_nmos\_tail}\right)^2$ [ignore CLM]. So I set VBS 0.51V, so that the current will not exceed 4uA easily. Also, all mosfets need to stay in saturation region, VBS can not be too high. In general the optimal VBS is the smaller, the better to make all mosfets stay in saturation and have small tail current. And as tail current should provide enough current from differential pair, its width is a little larger.

CMRR @ 10KHz:





CMRR=16.2dB-(11.9dB) = 28.1dB

Hspice code

```
.prot
.lib 'cic018.l'TT
.unprot
.option
+post
+Accuracy=1
+captab
+DELMAX=1e-10
.param v_DC=0
.param VBS = 0.51
.param MN_width=2.3u
.param MN_length=0.5u
.param MP_width=0.25u
```

```
.param MP_length=2u
*mos
MP_left Vout_left Vout_left VDD VDD p_18 w = MP_width l = MP_length m = 1
MP_right Vout_right Vout_right VDD VDD p_18 w = MP_width l = MP_length m = 1
MN_left Vout_left Vg_left Vx gnd n_18 w = MN_width l = MN_length m = 1
MN_right Vout_right Vg_right Vx gnd n_18 w = MN_width l = MN_length m = 1
MX Vx VBS gnd gnd n_18 w = 0.8u l = 0.18u m = 1
*resistor
RS_left Vi+ Vg_left 5k
RS_right Vi- Vg_right 5k
*voltage source
v1 Vi+ VCM DC =0.5*v_DC AC = 0.5 0
v2 Vi- VCM DC = -0.5*v_DC AC = 0.5 180
v3 VCM gnd 0.9
v4 VBS gnd VBS
v5 VDD gnd 1.8
*capacitor
CL_left Vout_left gnd 1.5p
CL_right Vout_right gnd 1.5p

*(c) change both v1 and v2 to AC = 1 0 and check vout_left



*find phase margin
.AC DEC 10k 1 1T
.probe AC
+diffenertial_gain = par('V(Vout_left)-V(Vout_right)')
.meas AC unity_frequency when vdb(vout_left, vout_right)=0
.meas AC phase find vp(vout_left,vout_right) at=unity_frequency
.meas AC phase_margin param='180+phase'



.pz V(Vout_left, Vout_left) v1

.DC v_DC -1.747m 1.747m 0.1m
.probe DC diff_gain = par('V(Vout_left)-V(Vout_right)')
.probe DC slope_diff = deriv(diff_gain)
.probe DC slope_vout_left = deriv('V(vout_left)')
.probe DC slope_vout_right = deriv('V(vout_right)')

*d
```

```
.alter
.DC v3 0 1.8 0.01
.probe DC slope_cm = deriv('V(vout_left)')
.alter
v1 Vi+ VCM    sin(0 11.8m 1x 0n)
v2 Vi- VCM
.tran    2u 40u
.four 1x V(Vout_left, Vout_right)
.alter
v1 Vi+ VCM    sin(0 13m 10x 0n)
v2 Vi- VCM
.tran 1u 20u
four 10x V(Vout_left, Vout_right)

.op
.END
```