NTHUEE

EE3235 Analog IC Analysis & Design - I 2019. Fall.

HW7

Due date : 2020. 01. 03 (Fri.) 23:59pm (upload to iLMS System)

First release : 2019. 12. 18

This homework is for you to design a differential outputs one-stage op amp. The results should include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

Please note:

1. Please hand in your report using LMS.
2. Please note, **no delay allowed!!!**
3. **Please generate your report with *pdf* format (AIC_HW{X}_StudentID.pdf). At first page please add your student ID and name. Try to make the information "readable".** (Note: Don't use black color in background for your screen capture figures).
4. Please **hand in the spice code file (AIC_HW{X}_StudentID. sp)** with your report for each work. Do not include output file.
5. Please fill the results into HW7.xls. **(without this file, -20pt)**
6. Do not zip your whole package.

Please attach your spice code at the end of report.

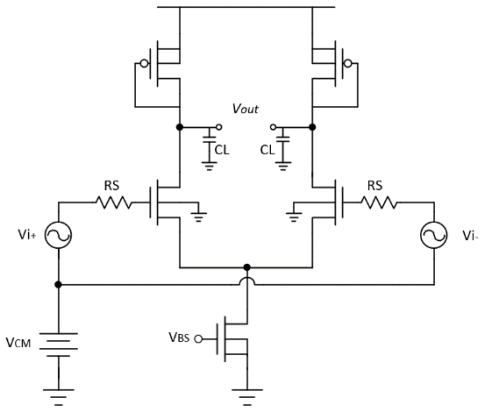


Fig. (1). differential outputs one-stage op amp

In this op amp circuit, please use V_{DD}=1.8V. The source impedance Rs is assumed 5Kohm, the loading capacitance is assumed 1.5pF, tail current is assumed smaller than 4uA and the common mode voltage V_{CM} is assumed 0.9V. The output common mode voltage is also 0.9V.

Please design the device size of input pair NMOS, diode connected PMOS loads, tail current source NMOS and the bias voltage V_{BS}, to make the small differential signal voltage gain (vout/vi) be larger than 16 dB, unity-gain frequency (Hz) be larger than 4MHz, and the phase margin be

larger than 45°.

(※ NMOS tail current source must stay in saturation region).

Simulations

(a) Open-loop differential mode AC response

(1). Please run .AC with differential input signals and plot the AC magnitude and phase response of differential mode gain. Mark the DC gain (dB), unity-gain frequency (Hz) and phase margin (degree) in the figure.

(2). Please print out the small signal parameters (from .op) of active devices from list file.

(3). Please print the poles/zeros from .pz command.

(b) Open-loop differential mode DC sweep

Please run .DC with differential input signals and plot the single-ended (vop and von separated) and differential (vop-von) outputs. Mark the slope to make sure the gain is like AC response.

(c) Open-loop common mode AC response

Please plot the magnitude response of common mode gain. Mark the DC gain (dB) and check it with your hand calculation.

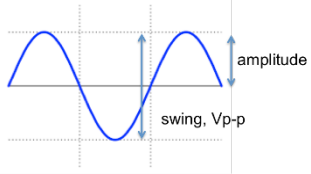
(d) Open-loop common mode DC sweep

Please plot the outputs for inputs with common mode signals. Mark the operation point. And also mark the slope at this point to make sure the gain is like AC response.

(e) Linear range

Please input differential sinusoidal waveform to estimate the harmonic distortion. Please plot the maximum output differential voltage waveforms that achieve -60dB THD (.four) at 1MHz and 10MHz respectively. The single-ended input amplitude value at 1MHz is defined as the linear range in this homework. Compare it with the hand calculation.

(Try to set DELMAX < 1e-9 in .option
for better accuracy in THD simulation)



(f) Here we use "bandwidth (MHz) x linear range (mV) / power (μA)" as the figure of merit (FoM). Please use your design equations to explain how to maximize FOM.

Design Items	Specifications	My work
Technology	CIC pseudo 0.18um technology	
Supply voltage	1.8V	
Input common mode	0.9V	
Tail current	< 4uA, as smaller as possible [#1]	
Loading	1.5 pF	
Source Impedance	5k ohm	
Simulations		
Gain	> 16 dB, as large as possible	
Unity-GBW	> 4MHz, as large as possible [#2]	
P.M.	> 45°	
C.M.R.R @ 10kHz	Open for design (dB)	
Linear range	Single-ended input amplitude (mV) [#3]	
FOM	(#2) x (#3) / (#1)	