NTHUEE

EE3235 Analog IC Analysis & Design - I 2019. Fall.

HW5

Due date : 2019. 12. 06 (Fri.) 23:59pm (upload to iLMS System)

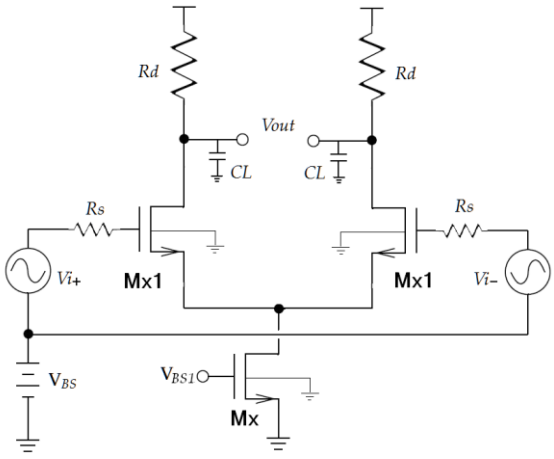
First release : 2019. 11. 21

HW5 –Differential Pair

This homework is for you to design a **differential pair** stage. The results should include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.
Please note:

1. Please hand in your report using LMS.
2. Please note, **no delay allowed!!!**
3. **Please generate your report with *pdf* format (AIC_HW{X}_StudentID.pdf). At first page please add your student ID and name. Try to make the information "readable".** (Note: Don't use black color in background for your screen capture figures).
4. Please **hand in the spice code file (AIC_HW{X}_StudentID. sp)** with your report for each work. Do not include output file.
5. Please fill the results into HW5.xls. **(without this file, -20pt)**
6. Do not zip your whole package.

Please attached your spice code for each working item in your report, in addition to separate .sp file.



In this differential pair circuit, please use V_{DD}=1.8V. The source impedance Rs is assumed 5Kohm and the loading capacitance is assumed 1.5pF.

(a) Please design the device size of Mx, Mx1, load resistance Rd, and the bias voltage VBS and VBS1 by your own. Make sure the small differential signal voltage gain (vout/vi) should be larger than 9 (V/V).
※Mx is a current source. It must stay in saturation region.

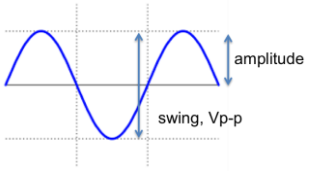
(b) Please print out the small signal parameters (from .op) of active devices from list file.

(c) Please run .DC then plot the **common mode input – common mode output** transfer function. Please select your common mode bias voltage V_{BS}, and print out its common-mode gain. Compare it with the hand calculation.

(d) Please run .DC then plot the **differential input – differential output** transfer function. Print out its differential-mode gain, and compare it with the hand calculation.

(e) Please simulate and plot the frequency response of differential signal (use .pz to simulate and mark the poles/zeros on this curve). Compare with the hand calculations.

(f) Please input differential sinusoidal waveform to estimate the harmonic distortion. Please plot the maximum output differential voltage waveforms that achieve -60dB THD (.four) at 10KHz,100KHz,1MHz and 10MHz respectively. The single-ended input amplitude value at 1MHz is defined as the linear range in this homework. Compare it with the hand calculation.
(Try to set DELMAX < 1e-9 in .option for better accuracy in THD simulation)



(g) Here we use "bandwidth (MHz) x linear range (mV) / power (μA)" as the figure of merit (FoM). Please try to make this FoM large. Please use your design equations to explain how to achieve max FOM.

Working Item	Specification	Simulation	Calculation
Vdd	1.8-V		
Tail current (Im_x)	Open for design (μA) [#1],as small as possible	76.021u	
Differential-mode gain	9 (V/V)	9.0167	
Input common mode	Open for design (V_{BS}, V)	0.7	
Common-mode gain	Open for design (V/V)	0.55	
Input size	Open for design (W/L)		
Differential gm	Open for design (mA/V)	0.311	
Load R	Open for design (Ohm)	30K	
Bandwidth	Open for design (MHz) [#2]		
Linear range	Single-ended input amplitude (mV) [#3]		
FoM	(#2) x (#3) / (#1)		