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Working Item	Simulation result
Vdd	1.5-V
Reference I_o	0.1mA
Reference size (W/L_{bottom}, $W/L_{cascode}$)	1.5u/0.18u (bottom), 5u/0.18u (cascode) (x1, x2, x4, x8)
Output load R_{out}	0.5 Kohm
DAC unit size (W/L_{bottom}, $W/L_{cascode}$)	1.5u/0.18u (bottom), 5u/0.18u (cascode), 2u/0.18u (switch) (x1, x2, x4, x8)
Output voltage range (0.75)	0.744V

DNL Error (%) [|(this level – previous level)|- ideal step] / ideal step (0.75V/15)

I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
-0.4	-0.4	-0.4	-0.6	-0.4	-0.6	-0.6	-0.6	-0.6	-0.8	-0.8	-1	-1.4	-1.8	-2.2

INL Error (%) (this level – ideal level)/ ideal step (0.75V/15)

I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
0.4	0.8	1.2	1.8	2.2	2.8	3.4	4	4.6	5.4	6.2	7.2	8.6	10.4	12.6

(b)

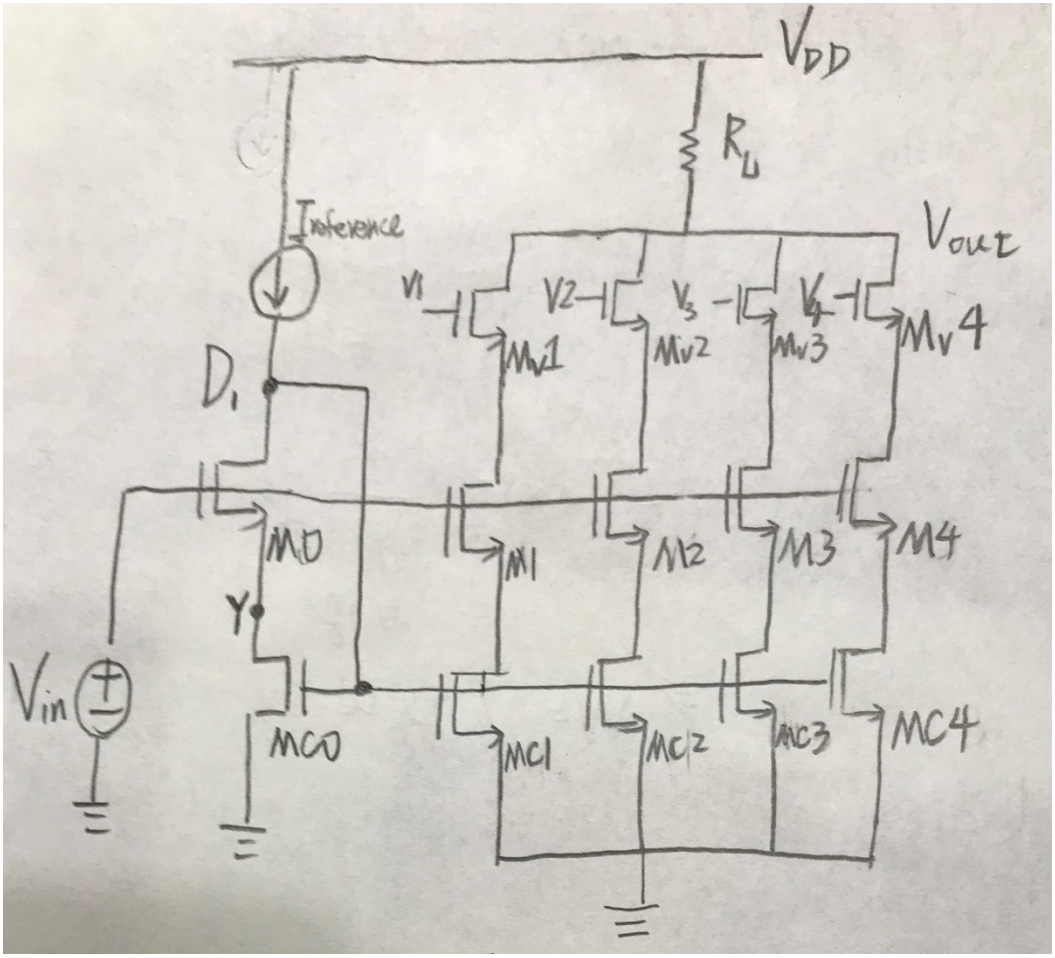

Fig. 2 The whole figure of the designed circuit

V1 =S_1 in problem sets

V2 =S_2 in problem sets

V3 =S_3 in problem sets

V4 =S_4 in problem sets

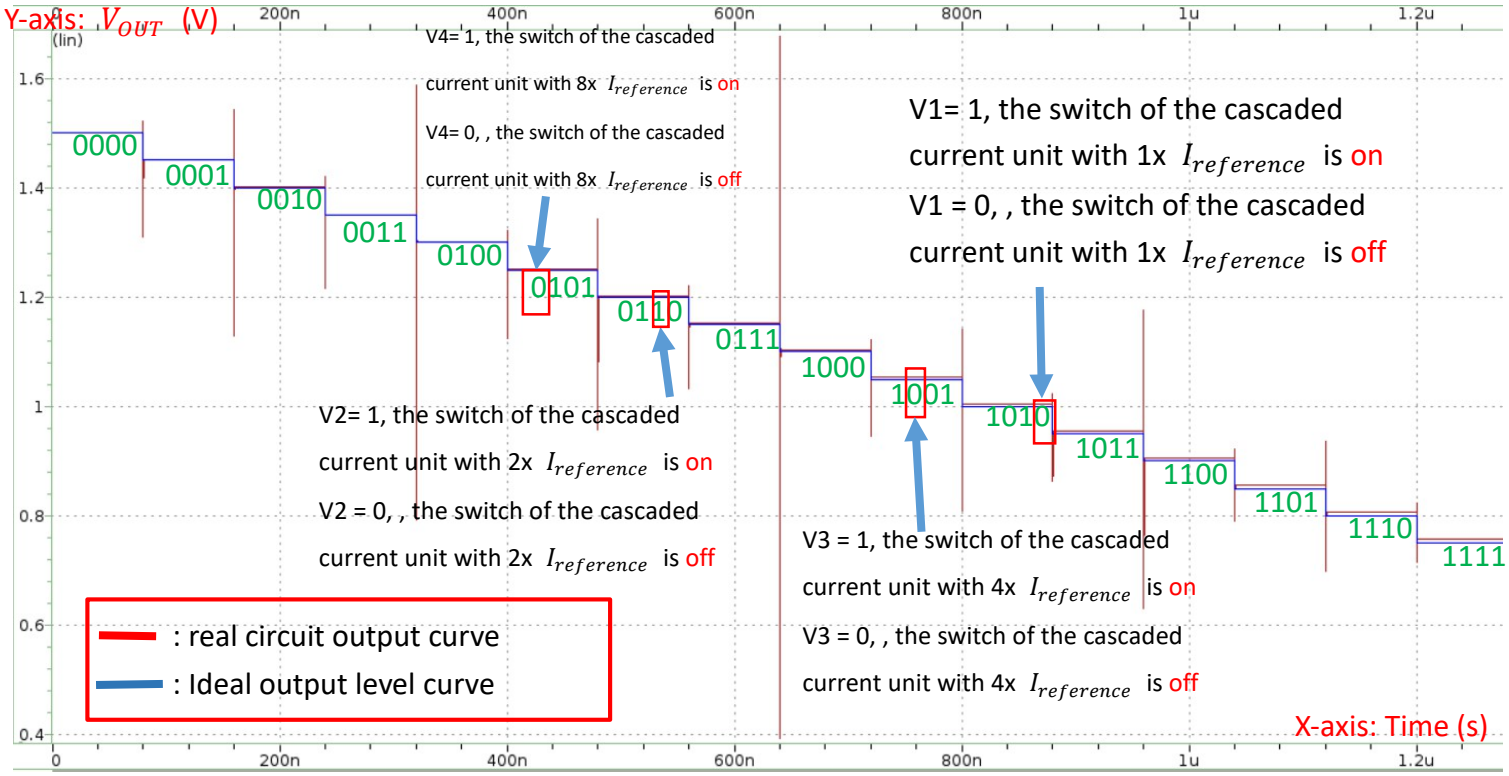

Fig. 1 Real circuit output V.S. Ideal output level

Discussion:

Basically, real circuit output is consistent with ideal output level. The biggest difference happened in transition place (ex: from code 0000 -> code 0001). The real circuit output would oscillate a lot in transition place. There are some reasons for this.

1) Since the switch (S_X) is a pulse function and rise time/fall time are too short, causing big jump of V_{out}. For example parasitic capacitor C_{gd}, if the switch (gate on the transistor) voltage increases suddenly, drain voltage (V_{out}) will also increase suddenly

due to coupling effect. Take fig. 2 for example, if V1 or V2 or V3 or V3 increase/decrease suddenly, V_{out} will be also increase/decrease due to coupling effect.

2) And the parasitic capacitance ∝ (transistors' Area (W × L)). Therefore, V_{out} of big size transistors tends to oscillate a lot more than smaller size transistor.

(c)

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
i_0=   1.5000
i_1=   1.4502
i_2=   1.4004
i_3=   1.3506
i_4=   1.3009
i_5=   1.2511
i_6=   1.2014
i_7=   1.1517
i_8=   1.1020
i_9=   1.0523
i_10=   1.0027
i_11= 953.0992m
i_12= 903.5988m
i_13= 854.2579m
i_14= 805.1568m
i_15= 756.3867m
```

Fig. 3 My value of V_{out} at each level. i_0 means code = 0000, i_1 means code = 0001, i_2 means code = 0010… so on and so forth.

Each level	Ideal level
i_0	1.5
i_1	1.45
i_2	1.4
i_3	1.35
i_4	1.3
i_5	1.25
i_6	1.2
i_7	1.15
i_8	1.1
i_9	1.05
i_10	1
i_11	0.95
i_12	0.9
i_13	0.85
i_14	0.8
i_15	0.75

Fig. 4 Ideal value of V_{out} at each level. i_0 means code = 0000, i_1 means code = 0001, i_2 means code = 0010… so on and so forth.

With this information and the formula provided by problem sets, I can calculate INL and DNL error as the following figure.

DNL Error (%)	[|(this level – previous level)|- ideal step] / ideal step (0.75V/15)													
I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
-0.4	-0.4	-0.4	-0.6	-0.4	-0.6	-0.6	-0.6	-0.6	-0.8	-0.8	-1	-1.4	-1.8	-2.2
INL Error (%)	(this level – ideal level)/ ideal step (0.75V/15)													
I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
0.4	0.8	1.2	1.8	2.2	2.8	3.4	4	4.6	5.4	6.2	7.2	8.6	10.4	12.6

Take DNL and INL error of I_1 for example,

DNL error = $\frac{|1.4502-1.5|-0.05}{0.05}$= -0.4%

INL error = $\frac{1.4502-1.45}{0.05}$ = 0.4%

Similar calculation for other levels!

(d)

$I_{reference}$ (in fig. 2):

According to fig. 2, if switch V1 is on (V1=VDD), it has 1x $I_{reference}$ current flowing through this path (Mv1 -> M1 -> MC1). If switch V2 is on (V2=VDD), it has 2x $I_{reference}$ current flowing through this path (Mv2 -> M2 -> MC2). If switch V3 is on (V3=VDD), it has 4x $I_{reference}$ current flowing through this path (Mv3 -> M3 -> MC3) and if switch V4 is on (V4=VDD), it has 8x $I_{reference}$ current flowing through this path (Mv4 -> M4 -> MC4). Therefore, when V1, V2, V3 and V4 are on at the same time (i.e. code = 1111) The output is supposed to be 0.75V with 15x $I_{reference}$(1+2+4+8 = 15) in total flowing through R_L. So $15 \times I_{reference} = \frac{VDD-V_{out}}{R_L} \Longrightarrow I_{reference} = \frac{1.5V-0.75V}{15\times 0.5K\Omega} = 0.1mA$

Device sizes and V_{in} (in fig. 2):

First of all, I looked at path $I_{reference}$ -> M0 (cascade) -> MC0 (bottom) in fig. 2. Assume M0, MC0 are in saturation region. So $0.5 \times \mu_n \times C_{ox} \times (\frac{W}{L})_{cascode} \times (V_{in} - V_Y - V_{th(M0)})^2 \times [1 + \lambda_{M0}(V_{D1} - V_Y)]$ = 0.1mA = $0.5 \times \mu_n \times C_{ox} \times (V_{D1} - V_{th(MC0)})^2 \times (\frac{W}{L})_{bottom} \times [1 + \lambda_{MC0}(V_Y)]$. V_{th} ~ 0.5V in 180nm technology. So I assume V_{th} is 0.5V for both M0 and MC0. And assume V_{D1} is 0.75 ($0.5 \times VDD$) since usually $V_{GS(MC0)}$ = $0.5 \times VDD$ can let mosfet stay in saturation region. And V_Y ($V_{DS(MC0)}$) has to larger than ($V_{GS(MC0)}$ - $V_{th} = 0.25V$), so I assume V_Y=0.3V. And for M0 to stay in saturation region, $V_{DS(M0)} = V_{D1} - V_Y = 0.75V - 0.3V = 0.45V$ has to

larger than $(V_{GS(M0)} - V_{th}) = V_{in} - V_Y - V_{th} = V_{in} - 0.3 - 0.5$, So I set V_{in} $0.95V$. (These are very rough assumptions, but it's reasonable enough to help me analyze the circuit) Finally, $\mu_n \times C_{ox}$ is $usually$ $around$ $300u$.

For MC0 and M0, I set length = 0.18u first, which is very short so that I need to take channel length modulation into consideration. But for the convenience, I will consider it later after calculation. Also I chose the smallest length in 'cic018.l' is because the calculated width wouldn't be too large, which leads to large parasitic capacitor.

(reference mosfet (in fig. 2): MC0 size)

So, 0.1mA = $0.5 \times \mu_n \times C_{ox} \times (V_{D1} - V_{th(MC0)})^2 \times (\frac{W}{L})_{bottom} \Longrightarrow W = 0.1mA \div 0.5 \div 300 \div 0.25^2 \times 0.18 = 1.92u$. But as I mention before, I need to take CLM into consideration ($I_D = 0.5 \times \mu_n \times C_{ox} \times (V_{D1} - V_{th(MC0)})^2 \times (\frac{W}{L})_{bottom} \times [1 + \lambda_{MC0}(V_Y)]$). So, width would be less than 1.92u. So I decrease the width from 1.92u to the point where MC0 is in saturation region (which is 1.5u in my design).

(reference mosfet in (fig. 2): M0 size)

$0.1mA = 0.5 \times \mu_n \times C_{ox} \times (\frac{W}{L})_{cascode} \times (V_{in} - V_Y - V_{th(M0)})^2 \Longrightarrow W = 0.1mA \div 0.5 \div 300 \times 0.18 \div 0.15^2 =$ 5.33u. Again, I need to consider CLM. Thus, width is supposed to less than 5.33u. So I decrease the width from 5.33u to the point where M0 is in saturation region (which is 5u in my design)

(Other MOS except switching mosfets)

As reference mosfets (M0, MC0) use **current mirror** to connect to other mosfets,

their width and length (W, L) should be exactly the same as the reference MOS (M0, MC0). But, multiple size ratio is different from each other. So other mosfets will also all stay in saturation region since multiple size ratio means how many mosfets with the same size in parallel together (their $V_{GS}, V_{DS}, V_{th}\ \ are\ \ exactly\ \ the\ \ same$)

Plus, by the request of problem sets (**use the multiple device size ratio**), I set m = 1 for mosfets on the path (Mv1 -> M1 -> MC1) to produce 1x reference current, m = 2 for mosfets on the path (Mv2 -> M2 -> MC2) to produce 2x reference current, m = 4 for mosfets on the path (Mv3 -> M3 -> MC3) to produce 4x reference current and m = 8 for mosfets on the path (Mv4 -> M4 -> MC4) to produce 8x reference current.

(Switching mosfets (in fig. 2): Mv1, Mv2, Mv3, Mv4)

First of all, I set V1, V2, V3 and V4 (switching voltage) equal to 1.5V to see if the other mosfets on the same path (ex: M1, MC1, Mv1 are the on the same path) will stay in saturation when the switch is on.

Because switching mosfets drains are all at V_{out}, which is changing against time, it's a little hard to calculate their sizes. Also, these mosfets serve as switches so that they don't necessarily need to stay in saturation region. So I set their 0.18u first, and increase their width from 0.25u (smallest in 'cic018.l') to the point where they are in linear region and other mosfets on the same path are still in saturation region, which can be viewed as the switches are on because current can flow through mosfets.

Input pattern ($V1, V2, V3$ *and* $V4$ in fig. 2):

Figure of input pattern:

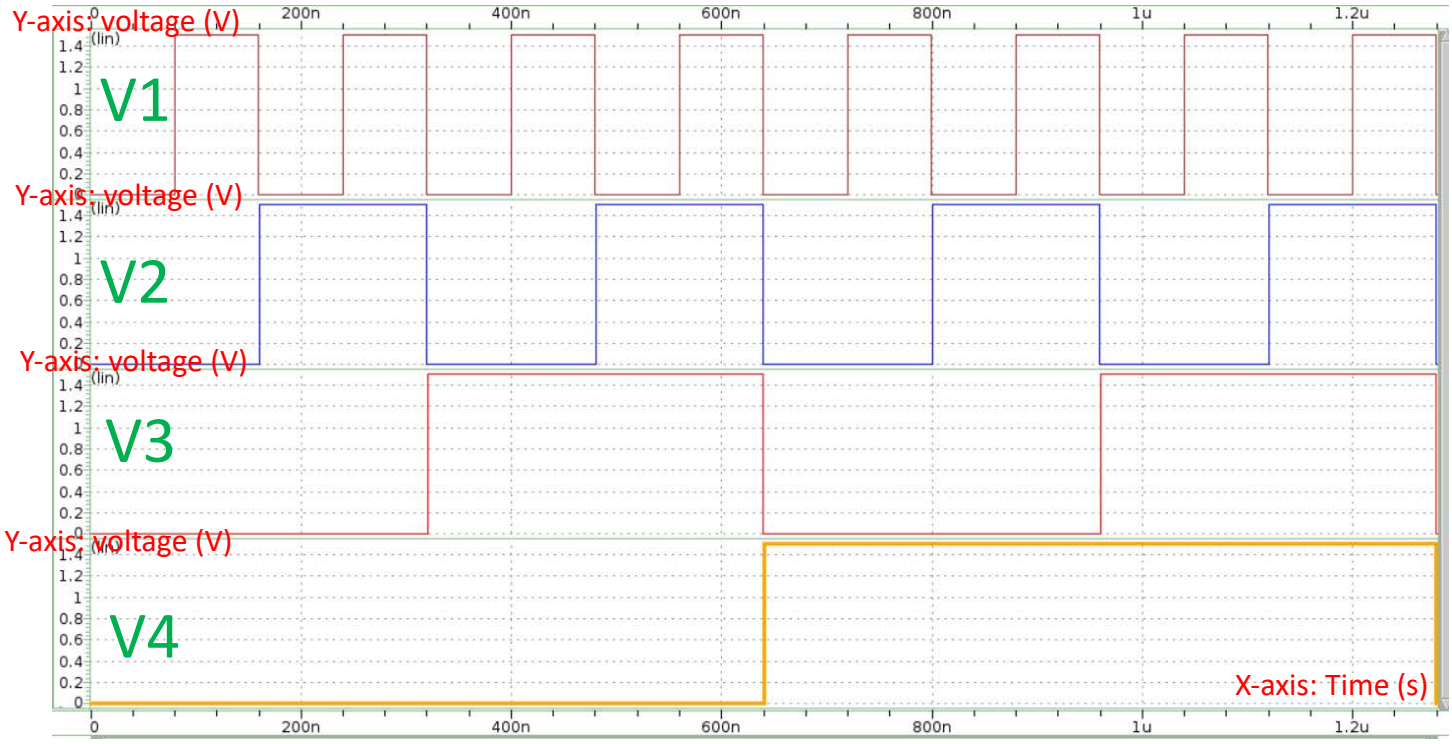

Fig. 5 Input pattern of switch (V1, V2, V3, V4 in fig. 2)

code	Current through R_L
0000	0 $I_{reference}$
0001	1x $I_{reference}$
0010	2x $I_{reference}$
0011	3x $I_{reference}$
0100	4x $I_{reference}$
0101	5x $I_{reference}$
0110	6x $I_{reference}$
0111	7x $I_{reference}$
1000	8x $I_{reference}$
1001	9x $I_{reference}$
1010	10x $I_{reference}$
1011	11x $I_{reference}$
1100	12x $I_{reference}$
1101	13x $I_{reference}$
1110	14x $I_{reference}$
1111	15x $I_{reference}$

From fig. 1, I make a table on the left. And I set each code will last 80ns, thus, 1280ns (from code 0000 to code 1111) in total. And according to this table,

Period of V1 = $1280 \div 8$ = 160ns (8 times from 0 -> 1)

Period of V2 = $1280 \div 4$ = 320ns (4 times from 0 -> 1)

Period of V3 = $1280 \div 2$ = 640ns (twice from 0 -> 1)

Period of V4 = $1280 \div 1$ = 1280ns (once from 0 -> 1)

So, that's the reason I set my input pattern like fig. 5.

The error between the real and ideal outputs:

DNL error means the error between my real circuit step and the ideal step (0.75/15 = 0.05V). According to the results I calculated in part (c), the error in each kind of code is pretty small, which means V_{out} can drop 0.05V precisely during each step. I think the small error comes from the assumption for the convenience of analysis (ex: assume $V_Y = 0.3V \ in \ fig. \ 2$). Also, DNL is all negative because DAC unit is not able to provide enough current (i.e. less than 1x, 2x, 4x, 8x $I_{reference}$) due to the fact that switch is only in linear region when is on. So V_{out} is higher than expected. This problem is especially serious when DAC unit need to produce 8x $I_{reference}$ (path Mv4 -> M4 -> Mc4 in fig. 2) so that the error gets larger when more and more current flows through R_L.

INL error means the error between each real circuit level and each ideal level (like fig. 4). According to the results I calculated in part (c), the error gets larger and larger when more current flow through R_L. The error may also come from the initial assumption I made for analysis. And the error is larger when more current flow through R_L also means the paths (Mv3 -> M3 -> MC3(m = 4) , Mv4 -> M4 -> MC4 (m = 8) in fig. 2) produce current less than 4x, 8x $I_{reference}$ (Since switch mosfets (Mv3, Mv4) are only in linear region, which are too weak to produce large current), which causes V_{out} higher than ideal level. That's why INL errors are all positive.

Hspice code:

```
.prot
.lib'cic018.l'TT
.unprot
.option
+ post
+ ACCURATE=1


*current sources
I1 VDD D1 0.1m

*resistor
Rl VDD Vout 0.5k

*voltage sources

VD VDD GND    1.5
VG Vin GND 0.95

v1 V1 GND PULSE(0 1.5 80n 1p 1p 79.9n 160n)
v2 V2 GND PULSE(0 1.5 160n 1p 1p 159.9n 320n)
v3 V3 GND PULSE(0 1.5 320n 1p 1p 319.9n 640n)
V4 V4 GND PULSE(0 1.5 640n 1p 1p 639.9n 1280n)


*check if saturation when the switch is on
*v1 V1 GND 1.5
*v2 V2 GND 1.5
```

```
*v3 V3 GND 1.5
*v4 V4 GND 1.5

*Mos reference
M0 D1 Vin S0 GND n_18 w = 5u l = 0.18u m = 1
MC0    S0 D1 GND GND n_18 w = 1.5u l = 0.18u m = 1

*Mos 1x
Mv1    Vout V1 one GND n_18 w = 2u l = 0.18u m = 1
M1      one    Vin s1 GND n_18 w = 5u l = 0.18u m = 1
MC1    s1 D1 GND GND n_18 w = 1.5u l = 0.18u m = 1

*Mos 2x
Mv2    Vout V2 two GND n_18 w = 2u l = 0.18u m = 2
M2      two    Vin s2 GND n_18 w = 5u l = 0.18u m = 2
MC2    s2 D1 GND GND n_18 w = 1.5u l = 0.18u m = 2

*Mos 4x
Mv3    Vout V3 four GND n_18 w = 2u l = 0.18u m = 4
M3      four    Vin s4 GND n_18 w = 5u l = 0.18u m = 4
MC3    s4 D1 GND GND n_18 w = 1.5u l = 0.18u m = 4

*Mos 8x
Mv4    Vout V4 eight GND n_18 w = 2u l = 0.18u m = 8
M4      eight    Vin s8 GND n_18 w = 5u l = 0.18u m = 8
MC4    s8 D1 GND GND n_18 w = 1.5u l = 0.18u m = 8

.TRAN 1n 1280n
.meas TRAN I_0 find V(Vout) AT = 40n
.meas TRAN I_1 find V(Vout) AT = 120n
.meas TRAN I_2 find V(Vout) AT = 200n
.meas TRAN I_3 find V(Vout) AT = 280n
.meas TRAN I_4 find V(Vout) AT = 360n
.meas TRAN I_5 find V(Vout) AT = 440n
.meas TRAN I_6 find V(Vout) AT = 520n
.meas TRAN I_7 find V(Vout) AT = 600n
.meas TRAN I_8 find V(Vout) AT = 680n
.meas TRAN I_9 find V(Vout) AT = 760n
.meas TRAN I_10 find V(Vout) AT = 840n
.meas TRAN I_11 find V(Vout) AT = 920n
.meas TRAN I_12 find V(Vout) AT = 1000n
.meas TRAN I_13 find V(Vout) AT = 1080n
```

```
.meas TRAN I_14 find V(Vout) AT = 1160n
.meas TRAN I_15 find V(Vout) AT = 1240n
.op

.end
```