NTHUEE

EE3235 Analog IC Analysis & Design - I 2019. Fall.

HW4

Due date : 2019. 11. 22 (Fri) 23:59pm (upload to iLMS System)

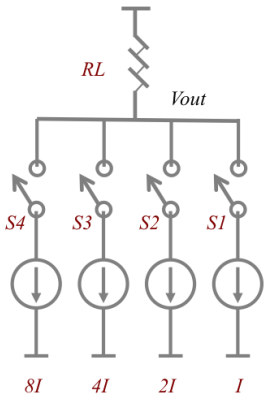
First release : 2019. 11. 07

HW4 –Current DAC with Mirrors

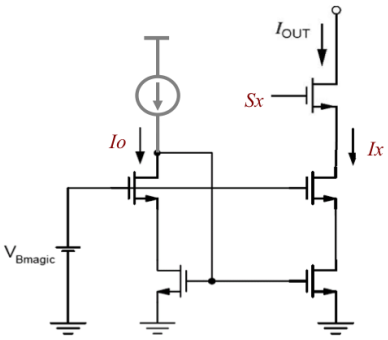
In this homework is for you to design a current-steering digital-to-analog converter (CS-DAC) with binary-scaled current sources. The problem sets include HSPICE simulations compared with the ideal curve. The SPICE model is cic018.l.
Please note:

1. Please hand in your report using LMS.
2. Please note, **no delay allowed!!!**
3. **Please generate your report with *pdf* format (AIC_HW{X}_StudentID.pdf). At first page please add your student ID and name. Try to make the information "readable".** (Note: Don't use black color in background for your screen capture figures).
4. Please **hand in the spice code file (AIC_HW{X}_StudentID. sp)** with your report for each work. Do not include output file.
5. Please fill the results into **the table in the last page. (without this table, -20pt)**
6. Do not zip your whole package.

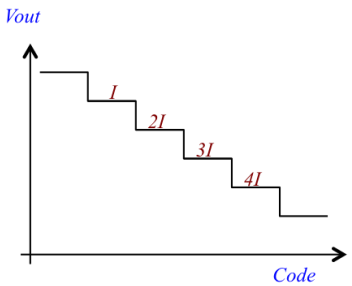
Please attached your spice code for each working item in your report, in addition to separate .sp file.



(Ideal 4-b CS-DAC)



(Cascaded current unit)



(Ideal DAC output)

In this differential pair circuit, please use V_{DD}=1.5V. The load impedance R_L is assumed 0.5Kohm and the output full swing range is 0.75V.

(a) Please design your cascaded current unit to generate all the current level. (please use the multiple device size ratio, ie, x1, x2, x4, x8).

(b) Please plot the ideal DAC output level and compare to your real circuit output.

(c) Please calculate the DNL and INL error of each code.

(d) Discuss your selection on circuit bias and device size, and the error between the ideal and the real outputs.

Working Item								Simulation result						
Vdd								1.5-V						
Reference I_o								0.1mA						
Reference size (W/L_{bottom}, $W/L_{cascode}$)								1.5u/0.18u (bottom), 5u/0.18u (cascode) (x1, x2, x4, x8)						
Output load R_{out}								0.5 Kohm						
DAC unit size (W/L_{bottom}, $W/L_{cascode}$)								1.5u/0.18u (bottom), 5u/0.18u (cascode), 2u/0.18u (switch) (x1, x2, x4, x8)						
Output voltage range (0.75)								0.744V						
DNL Error (%) [|(this level – previous level)|- ideal step] / ideal step (0.75V/15)														
I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
-0.4	-0.4	-0.4	-0.6	-0.4	-0.6	-0.6	-0.6	-0.6	-0.8	-0.8	-1	-1.4	-1.8	-2.2
INL Error (%) (this level – ideal level)/ ideal step (0.75V/15)														
I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
0.4	0.8	1.2	1.8	2.2	2.8	3.4	4	4.6	5.4	6.2	7.2	8.6	10.4	12.6