Problem 1 (Common source)

(a) My FOM is 31.5. The detail is in 'HW3.xlsx'.

(b)

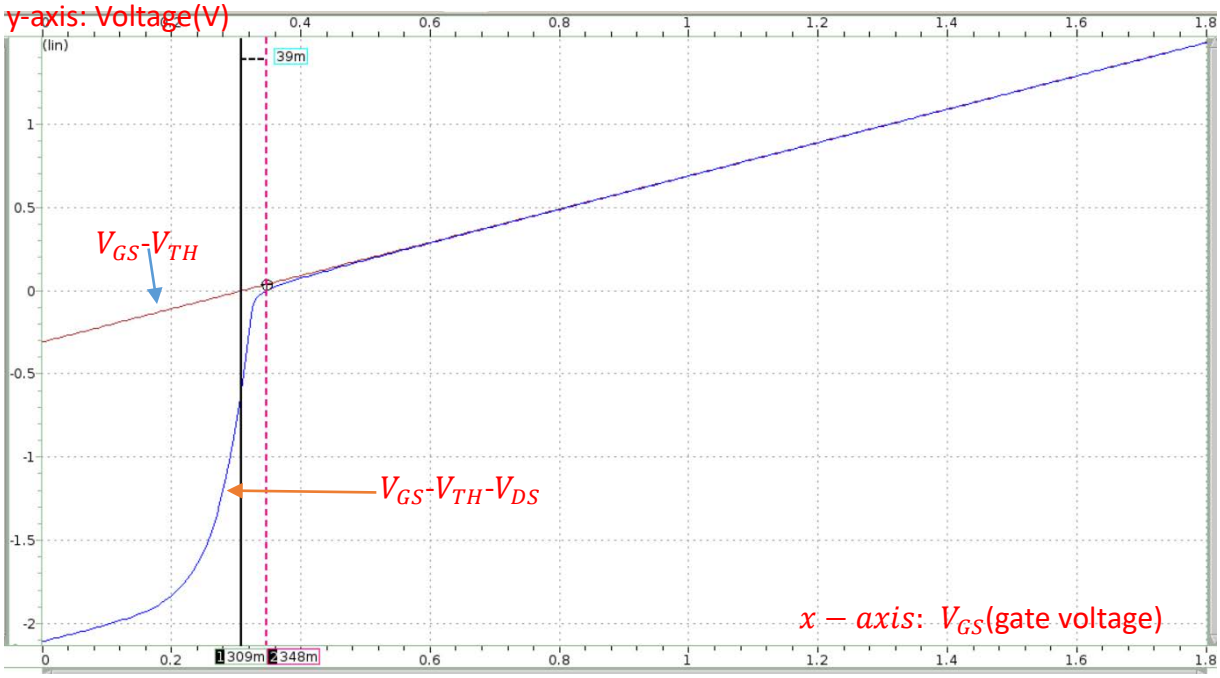
```
**** mosfets


subckt
element  0:mn
model    0:n_18.1
region     Saturati
 id       325.2592n
 ibs     -4.876e-23
 ibd     -863.8011a
 vgs      320.0000m
 vds      255.0162m
 vbs        0.
 vth      309.6876m
 vdsat     60.9219m
 vod       10.3124m
 beta     283.2849u
 gam eff  507.4459m
 gm         6.9777u
 gds       10.9633n
 gmb        1.4596u
 cdtot     86.7694f
 cgtot     10.4766p
 cstot      9.1920p
 cbtot      4.1588p
 cgs        8.0602p
 cgd       24.2426f
```

(c)

$$Hand\ \ calculate\ \ gain = \ \ g_m \times (R_L // r_o) \ \ = 6.978u \times \frac{4.75M \times \frac{1}{10.96n}}{4.75M + \frac{1}{10.96n}} = 31.51$$

And my simulation result is 31.5. Error rate is $\frac{31.51-31.5}{31.5} = \ \ 0.032\%$. So basically, hand calculation result is highly consistent with the hspice simulation results.

(d)



Saturation region for NMOS are:

1. V_{GS} > V_{TH} (0.309V)
2. V_{DS} > V_{GS} - V_{TH} (by the figure above, it happened when0.309 < V_{GS} < 0.348V)

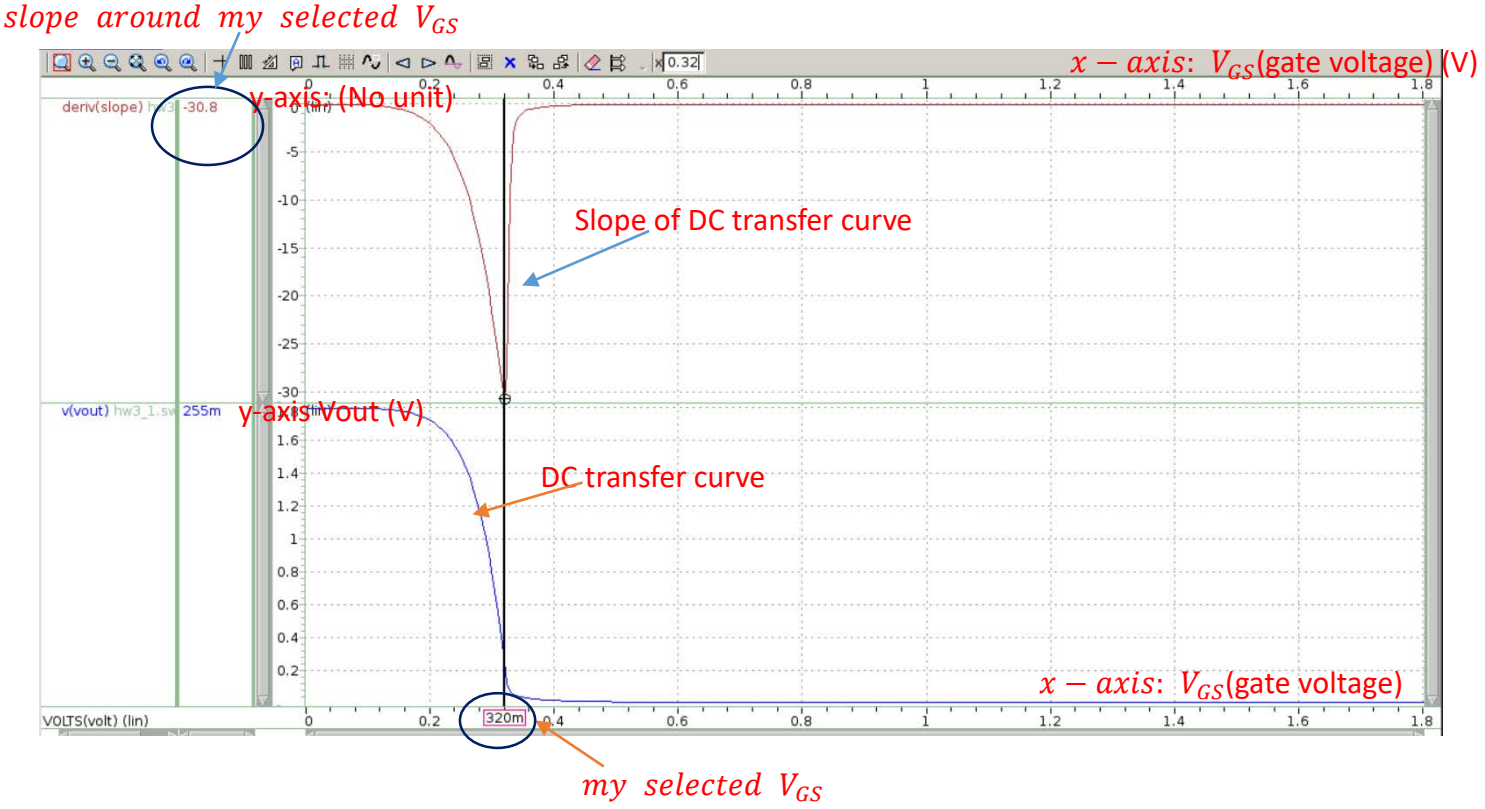
Linear region for NMOS is

1. V_{GS} > V_{TH} (0.309V)
2. V_{DS} < V_{GS} - V_{TH} (by the figure above, it happened when V_{GS} > 0.348V)

Cutoff region for NMOS is

1. V_{GS} < V_{TH} (0.309V)

With these information, I draw DC transfer curve below!



So, according to my figure above the DC transfer curve around my selected my V_{GS} is -30.8, which means “voltage gain”. It’s pretty close my AC analysis results. (low frequency gain is 31.5)

(e)

First, I try to calculate $gain = \ g_m \times (R_L // r_o)$ and simplify it.

$$g_m \times (R_L // r_o) = \frac{2 \times I_D}{V_{od}} \times \frac{R_L \times \frac{1}{\lambda I_D}}{R_L + \frac{1}{\lambda I_D}} = \frac{\frac{2 \times R_D}{\lambda}}{V_{od} \times (R_L + \frac{1}{\lambda I_D})} = \frac{\frac{2}{\lambda}}{V_{od} \times (1 + \frac{1}{\lambda I_D R_D})} = \frac{2}{V_{od} \times (\lambda + \frac{1}{I_D R_D})}$$

And, $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$.

The followings are my observations of how to get larger small voltage gain.

1. I tried to minimize 'overdrive voltage' (V_{od}) and set V_{GS} to a lower value (around 0.32V) because I found it's more effective to get higher gain when setting lower V_{GS}.
2. I tried to minimize λ, $\lambda \ \propto \ \frac{1}{L}$. So I increase L (length) to reduce λ, causing I_D to decrease and therefore $\frac{1}{I_D R_D}$ to increase . Thus, at the same time, I also need to increase R_D to make sure $\frac{1}{I_D R_D}$ is not increasing that much (Theoretically, I can also increase width to maintain I_D, but I found it doesn't work that well. Therefore, I just adjust R_D only). And finally, I only need to find a suitable R_D which is not too high to make MOS leave saturation region.
3. I needed to consider every kind of effect related to MOSFETs (ex: Channel Length Modulation in this problem, body effect, etc.), which sometimes could significantly influence the simulation results. So, I take CLM into consideration at the beginning of my analysis.

Problem 2 (Common drain)

(a) My maximum small signal gain is 0.857. And, the detail is in 'HW3.xlsx'.

(b)

**** small-signal transfer characteristics

	input resistance at v2	output resistance at v(vout)	v(vout)/v2
0.	1.000e+20	2.5117x	2.6674m
50.0000m	1.000e+20	2.4715x	15.6513m
100.0000m	1.000e+20	2.2854x	76.0276m
150.0000m	1.000e+20	1.8090x	231.4919m
200.0000m	1.000e+20	1.2690x	408.9578m
250.0000m	1.000e+20	900.4005k	531.4728m
300.0000m	1.000e+20	675.9409k	607.3268m
350.0000m	1.000e+20	534.2758k	656.2645m
400.0000m	1.000e+20	439.3181k	689.9564m
450.0000m	1.000e+20	372.1203k	714.5426m
500.0000m	1.000e+20	322.4153k	733.3547m
550.0000m	1.000e+20	284.3196k	748.3045m
600.0000m	1.000e+20	254.2628k	760.5539m
650.0000m	1.000e+20	230.0004k	770.8349m
700.0000m	1.000e+20	210.0212k	779.6417m
750.0000m	1.000e+20	193.2972k	787.3114m
800.0000m	1.000e+20	179.1018k	794.0835m
850.0000m	1.000e+20	166.9073k	800.1327m
900.0000m	1.000e+20	156.3223k	805.5894m
950.0000m	1.000e+20	147.0503k	810.5531m
1.0000	1.000e+20	138.8630k	815.1008m
1.0500	1.000e+20	131.5818k	819.2935m
1.1000	1.000e+20	125.0650k	823.1800m
1.1500	1.000e+20	119.1989k	826.7998m
1.2000	1.000e+20	113.8911k	830.1854m
1.2500	1.000e+20	109.0660k	833.3636m
1.3000	1.000e+20	104.6608k	836.3570m
1.3500	1.000e+20	100.6233k	839.1848m
1.4000	1.000e+20	96.9094k	841.8630m
1.4500	1.000e+20	93.4819k	844.4057m
1.5000	1.000e+20	90.3091k	846.8248m
1.5500	1.000e+20	87.3636k	849.1306m
1.6000	1.000e+20	84.6220k	851.3322m
1.6500	1.000e+20	82.0639k	853.4372m
1.7000	1.000e+20	79.6716k	855.4523m
1.7500	1.000e+20	77.4295k	857.3829m
1.8000	1.000e+20	75.3240k	859.2331m

圖 1. (.TF analysis)Small signal transfer characteristics.

By the region I use red rectangular to highlight,

$Z_i = \ 10^{20}\Omega(Infinity)$
$Z_o = 77.4295K\Omega$

Gain = 0.857 V/V

(c)

Hand calculation:

Output impedance: (hspice simulation result is 77.4295KΩ)

$$Zo = \frac{1}{g_m} // r_o // R_L = (\frac{1}{11.07\times10^{-6}}\Omega) // (\frac{1}{12.808\times10^{-9}}\Omega) //$$

$(2520K\Omega)$ = 89.468KΩ

Error rate = $\frac{89.868K\Omega - 77.4295K\Omega}{77.4295K\Omega}$ = 13.08%

But, if considering Body effect,

$$Zo' = \frac{1}{g_m + g_{mb}} // r_o // R_L = (\frac{1}{11.07\times10^{-6} + 1.4323\times10^{-6}}\Omega) //$$

$(\frac{1}{12.808\times10^{-9}}\Omega) // (2520K\Omega)$= 77.484 KΩ

Error rate = $\frac{77.484K\Omega - 77.4295K\Omega}{77.4295K\Omega}$ = 0.0008%.

Gain: (hspice simulation result is 0.857)

$$\text{gain} = \frac{r_o || R_L}{\frac{1}{g_m} + r_o || R_L} = \frac{(\frac{1}{12.808\times10^{-9}}\Omega) // (2520K\Omega)}{(\frac{1}{11.07\times10^{-6}}\Omega) + (\frac{1}{12.808\times10^{-9}}\Omega) //\ (2520K\Omega)} = 0.964.$$

Error rate = $\frac{0.964 - 0.857}{0.857}$ = 12.4%

But if considering Body effect, $\text{gain} = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_o || R_L}}$ =

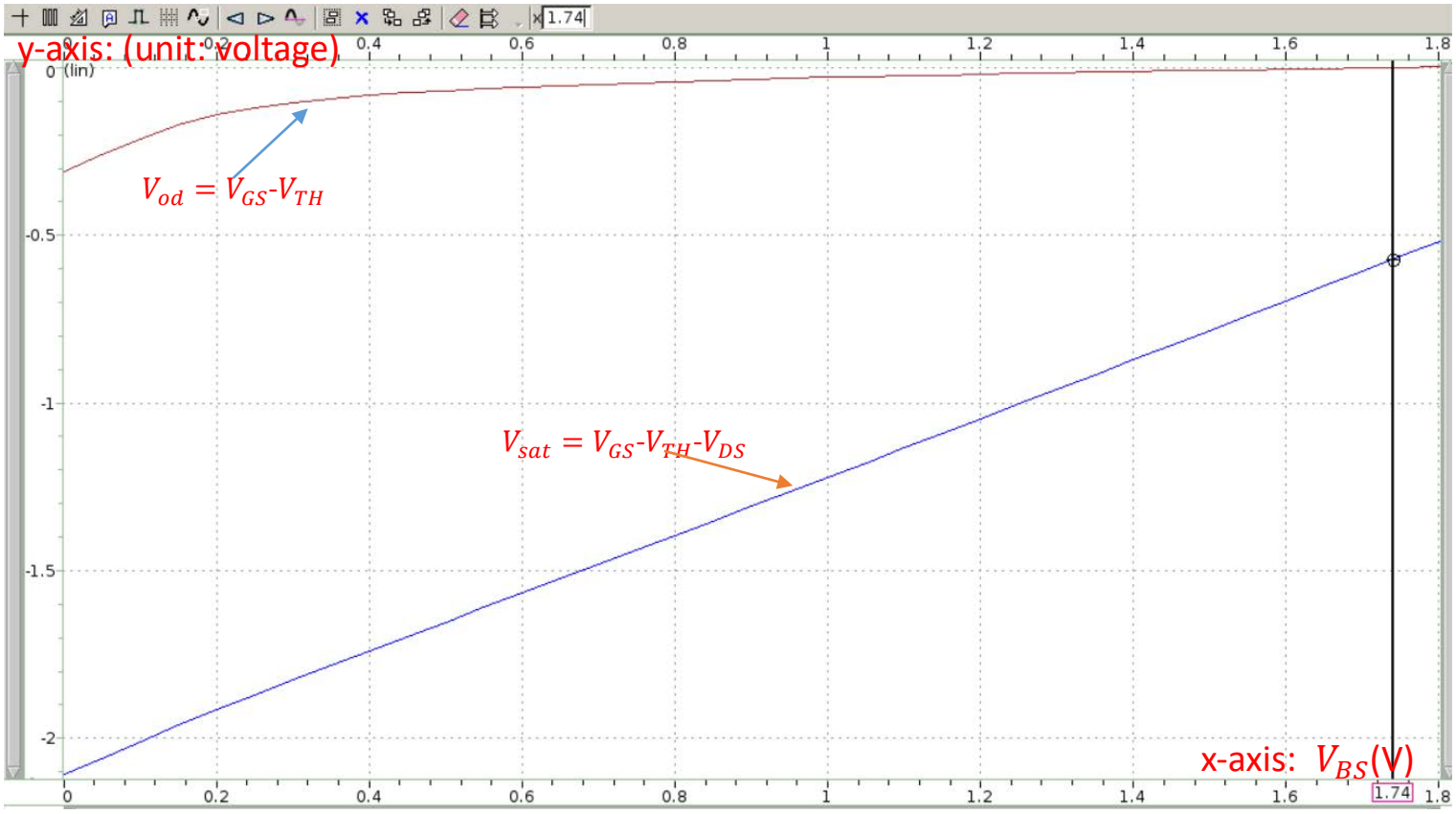
$$\frac{11.07\times10^{-6}}{(11.07\times10^{-6}) + 1.432\times10^{-6}\Omega + \frac{1}{(\frac{1}{12.808\times10^{-9}}) // (2520\times10^{3})}} = 0.858$$

Error rate is almost 0.

Operation point of MOS in problem 2

```
**** mosfets


subckt
element  0:mn
model    0:n_18.1
region     Saturati
 id       490.4719n
 ibs       -7.0629f
 ibd      -10.2859f
 vgs      514.0125m
 vds      564.0125m
 vbs       -1.2360
 vth      512.4405m
 vdsat     62.8401m
 vod        1.5720m
 beta     487.2968u
 gam eff  534.6447m
 gm        11.0731u
 gds       12.8078n
 gmb        1.4323u
 cdtot     94.3167f
 cgtot     15.1075p
 cstot     12.8710p
 cbtot      4.7941p
 cgs       11.9065p
 cgd       22.7206f
```

(d)



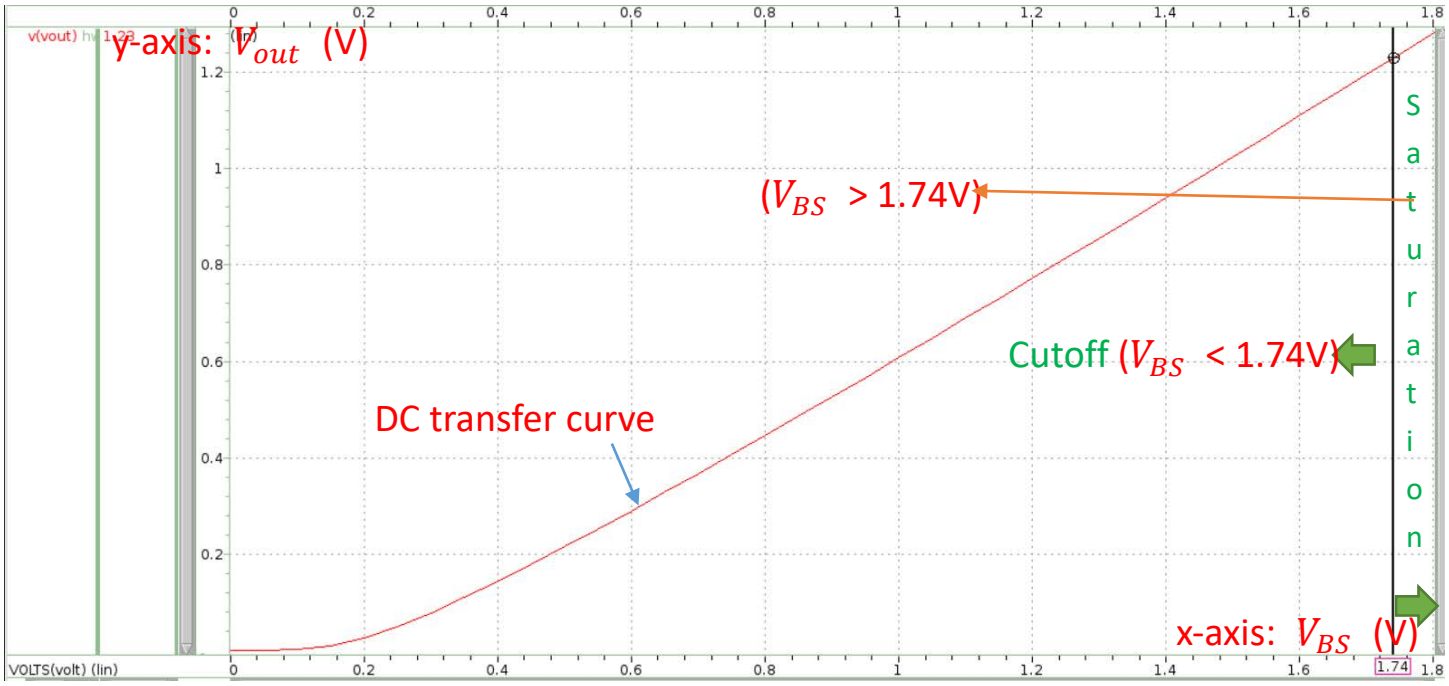
Saturation region for NMOS are:

1. $V_{GS} > V_{TH}$
2. $V_{DS} > V_{GS} - V_{TH}$ (by the figure above, it happened when V_{BS} > 1.74V)

By figure above, $V_{sat}(= V_{GS}$-V_{TH}-V_{DS}) is always under 0, no linear region at all.

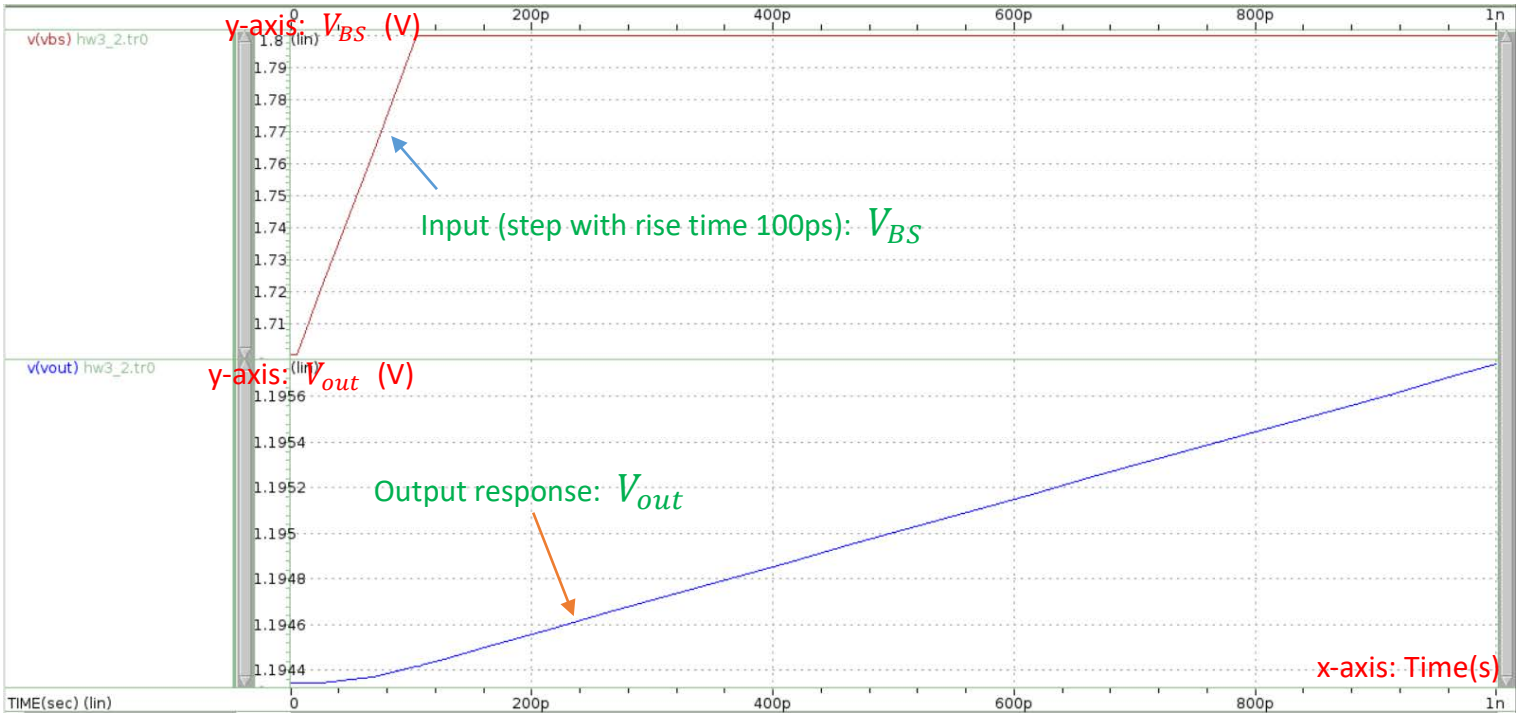
Cutoff region for NMOS is

1. $V_{GS} < V_{TH}$ (by the figure above, it happened when V_{BS} < 1.74V)



Since gate voltage (V_{BS}) increases, I_D also increases and $V_{out} = I_D \times R_D$, V_{out} will increase along with V_{BS} (gate voltage).

(e)



Discussion:

Since my chosen V_{BS} is 1.75V, my V_{BS} will increase from 1.7V(1.75-0.05) to 1.8V(1.75+0.05).

During 100ps input rise time, $V_{out} = I_D \times R_D$, when V_{BS} (= gate voltage) increases, I_D also increases. After that, input is not change at all, V_{out} is still getting larger. I think it's because loading capacitance C_L at V_{out}. With C_L, output can not respond to the input change very quickly, which leads to delay. Therefore, although V_{BS} is fixed after rising time, V_{out} is still getting larger. After enough time V_{out} will be fixed at a fixed value.

Discussion of how to get max small signal voltage gain:

$$\text{Gain} = \frac{r_o||R_d}{\frac{1}{g_m}+r_o||R_d} = \frac{1}{\frac{1}{g_m\times(r_o||R_d)}+1},\ g_m \times (r_o||R_d) = \frac{2\times I_D}{V_{od}} \times \frac{R_L\times\frac{1}{\lambda I_D}}{R_L+\frac{1}{\lambda I_D}} = \frac{\frac{2\times R_D}{\lambda}}{V_{od}\times(R_L+\frac{1}{\lambda I_D})} = \frac{\frac{2}{\lambda}}{V_{od}\times(1+\frac{1}{\lambda I_D R_D})} = \frac{2}{V_{od}\times(\lambda+\frac{1}{I_D R_D})},\ V_S = I_D R_D.$$

I need to maximize $\frac{2}{V_{od}\times(\lambda+\frac{1}{I_D R_D})}$ to let small signal gain get close to 1. The following are my strategies to maximize gain.

1. Set V_{BS} at very high value because it's highly effective to get higher voltage by my observation.
2. Then I want to minimize λ, so I set length to maximum value in 'cic018.l'.
3. I want to decrease V_{od}, so I increase V_S $(= I_D R_D)$, by increasing both $I_D(increase\ \ width)$ and R_D until the MOS is about to leave the saturation.

4. Finally, I get my small signal voltage gain.

Hspice code

```
***Problem 1 (common source)***

.prot
.lib 'cic018.l' TT
.unprot
.option
+post
+accuracy = 1
*MOS
MN Vout Vg gnd gnd n_18 w = 47u l = 49u m = 1
*Resistors
Rs Vgs Vg 10k
RL VDD Vout 4750k
*capacitor
CL Vout gnd 1p
*voltage sources
```

```
v1 VDD 0 1.8

v2 Vgs 0 DC 0.32 AC 1

*DC analysis

.DC v2 0 1.8 0.005

.probe DC

+Vov = par('V(Vg)-Vth(MN)')

+Vsat = par('V(Vg)-Vth(MN)-V(Vout)')

+slope = deriv('V(Vout)')

*AC analysis

.AC DEC 10k 1 1T

.probe AC

+gain = 'V(Vout)' $since AC of Vgs = 1

.op

.END

***Problem 2 (common drain)***



.prot

.lib 'cic018.l' TT

.unprot

.option

+post
```

```
+accuracy = 1
*MOS
MN VDD Vg Vout gnd n_18 w = 80u l = 49.99u m = 1
*resistor
Rs Vbs Vg 10k
Rd Vout gnd 2520k
*capacitor
CL Vout gnd 1p
*voltage sources
v1 VDD 0 1.8
v2 Vbs 0 DC 1.75 AC 1
$VSTEP Vbs 0 PWL 0p 1.7 100p 1.8 1n 1.8 R 0 $input step function with 100ps
rise time
*.tran analysis
.tran 0.1p 1n
*DC analysis
.DC v2 0 1.8 0.05
.probe DC
+Vov = par('V(Vg)-V(Vout)-Vth(MN)')
+Vsat = par('V(Vg)-V(Vout)-Vth(MN)-V(VDD)+V(Vout)')
*AC analysis
.AC DEC 10k 1 1T
```

```
.probe AC

+gain = 'V(Vout)'

*TF analysis

.TF V(Vout) v2

.op

.END
```