NTHUEE

EE 3235 Analog IC Analysis & Design - I 2019. Fall.

HW3

Due date : 2019. 11. 08 (Friday) 23:59pm (upload to iLMS System)

First release : 2019. 10. 25

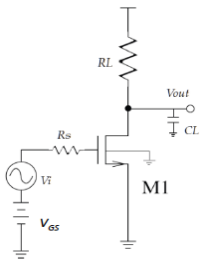
HW3 – Common source and Common Drain (DC)

This homework is for you to design a **common source** stage and a **common drain** stage. The results should include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.
Please note:

1. Please hand in your report using LMS.
2. Please note, **no delay allowed!!!**
3. **Please generate your report with *pdf* format (AIC_HW{X}_StudentID.pdf). At first page please add your student ID and name. Try to make the information "readable".**
(Note: Don't use black color in background for your screen capture figures).
4. Please **hand in the spice code file (AIC_HW{X}_StudentID. sp)** with your report for each work. Do not include output file.
5. Please fill the results into HW3.xls. **(without this file, -20pt)**
6. Do not zip your whole package.

Please attach your spice code at the end of report.

1. Common Source



Please follow the rules as before.
In the common source, please use V_{DD}=1.8V. The source impedance Rs is assumed 10Kohm and the loading capacitance C_L is 1.0pF.

(maximize the FoM)

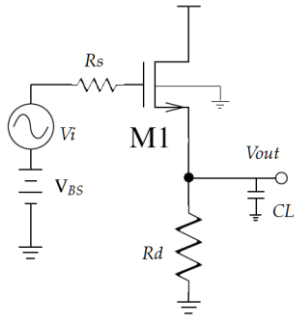
(a) We will use the "maximal small-signal voltage gain" as the figure of merit (FOM). Please try your best.

(determine the operation point)

(b) Please use .op command to print out its small signal parameters.
(c) Please hand-calculate the gain value using SPICE parameters from (b).
(d) Please sweep the gate DC voltage to draw its DC transfer curve. Please observe and mark the input-output linear transfer range around the selected V_{GS}.
(e) Please discuss your observations for best FOM.

For FoM (max small-signal voltage gain (V/V))	
M_1 Device Size (W/L)	
M_1 Bias Current (μA)	
M_1 Overdrive Voltage (mV)	
Load R (ohm)	
Small-Signal Voltage Gain (V/V)	
FoM (max small-signal voltage gain (V/V))	

2. Common Drain



In the common source circuits, please use V_{DD}=1.8V. The source impedance R_s is assumed 10 Kohm and the loading capacitance C_L is assumed 1 pF.

(maximize the FoM)

(a) Please design the device size of M1, load resistance R_d, and the bias voltage V_{BS}, to make the small signal voltage gain (vout/vi) largest.

   i. *(note: gate voltage should not be higher than V_{DD}).*

(b) Please use .tf to get gain, Z_i and Z_o.

(c) Please calculate the gain and Z_o of (b).

(d) Under this operation point, please sweep the DC of *Vi*, to draw its DC transfer curve.

(e) Please give a step (V_{BS}-50mV to V_{BS}+50mV with 100ps rise time) at input and plot its output waveform.

Please discuss your strategy to get the max small signal gain.

For FoM (max small-signal voltage gain (V/V))	
Device size (W/L)	
Bias current (mA)	
gm1 (mA/V)	
Rd (ohm)	
V_{BS} (V)	
FoM (max small-signal voltage gain (V/V))	