

Problem 1 (FOM₁)

(a)、(b)小題已寫在 HW2.xlsx 裡，圖 1 為 simulation results. FOM1 為 0.217

(C)

**** mosfets

```

subckt
element 0:m1
model 0:n_18.1
region Saturati
id 6.1784u
ibs -1.048e-21
ibd -298.5559a
vgs 451.5000m
vds 554.6994m
vbs 0.
vth 449.1399m
vdsat 71.4434m
vod 2.3601m
beta 4.5681m
gam_eff 507.4460m
gm 128.1826u
gds 2.0262u
gmb 24.8738u
cdtot 9.0578f
cgtot 16.6239f
cstot 19.7697f
cbtot 19.0138f
cgs 11.0421f
cgd 2.4695f

```

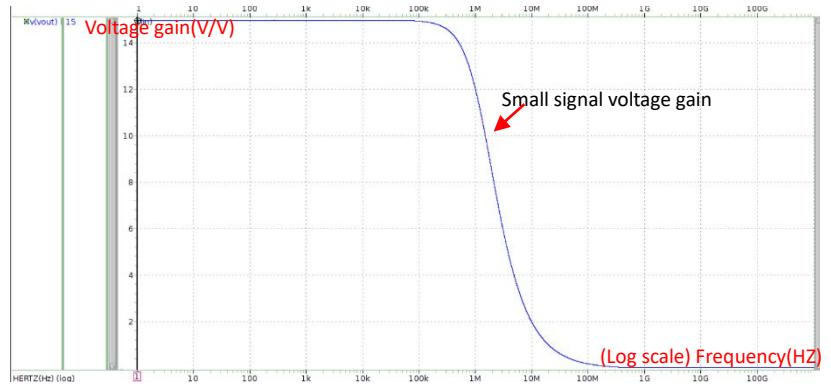


圖 1 frequency response of FMO1.

(d) In Common source, $A_v = -gm * (RL//ro) = -128.183 \times 10^{-6} \times$

$$\frac{153000 * 493534.696}{153000 + 493534.696} = 14.971. \text{ The simulation result is } 15.$$

Therefore, Error rate = $\frac{14.971 - 15}{15} = 0.19\%$

(e)

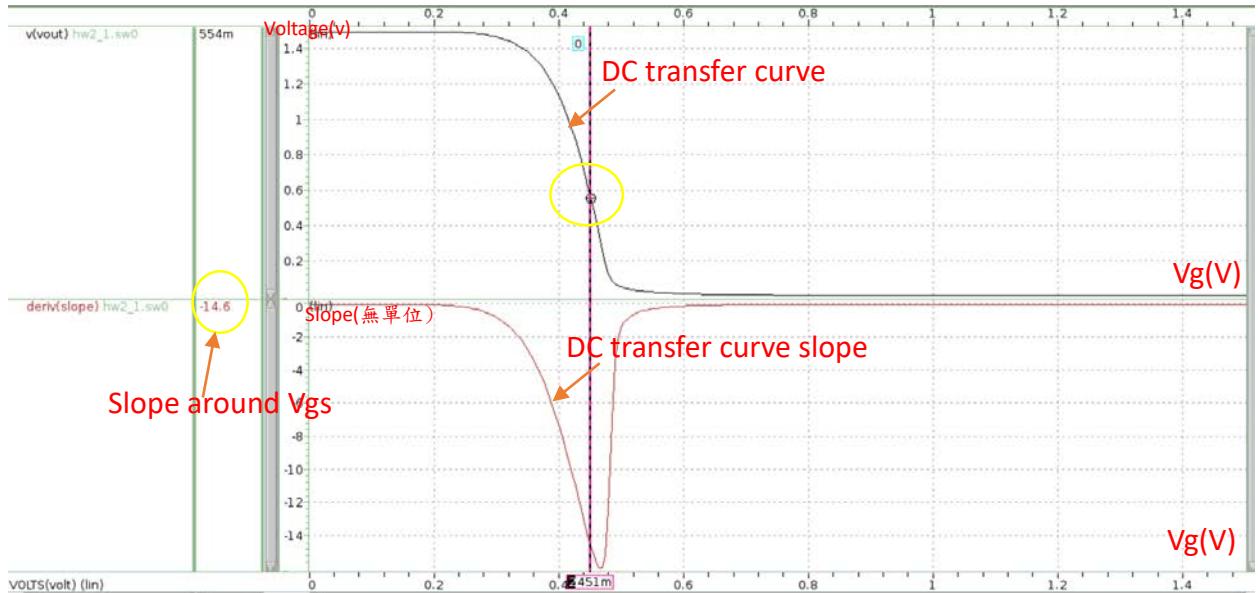


圖 2 DC transfer curve and its slope

Discussion: 可以看圖上黃色圈起來的部分，在 V_{GS} 附近的斜率是 -14.6。在 DC transfer curve 上圖形的斜率代表 voltage gain，所以與圖 1 模擬出來的結果 15 相差不大，Error rate = $\frac{14.6-15}{15} = 2.66\%$ 。誤差來源可能是在寫 hspice 的時候，DC SWEEP 掃的範圍不夠細，或是在 waveform viewer 裡頭 cursor 的精準度只到小數後 3 位，所以才有微小的差異

(f)

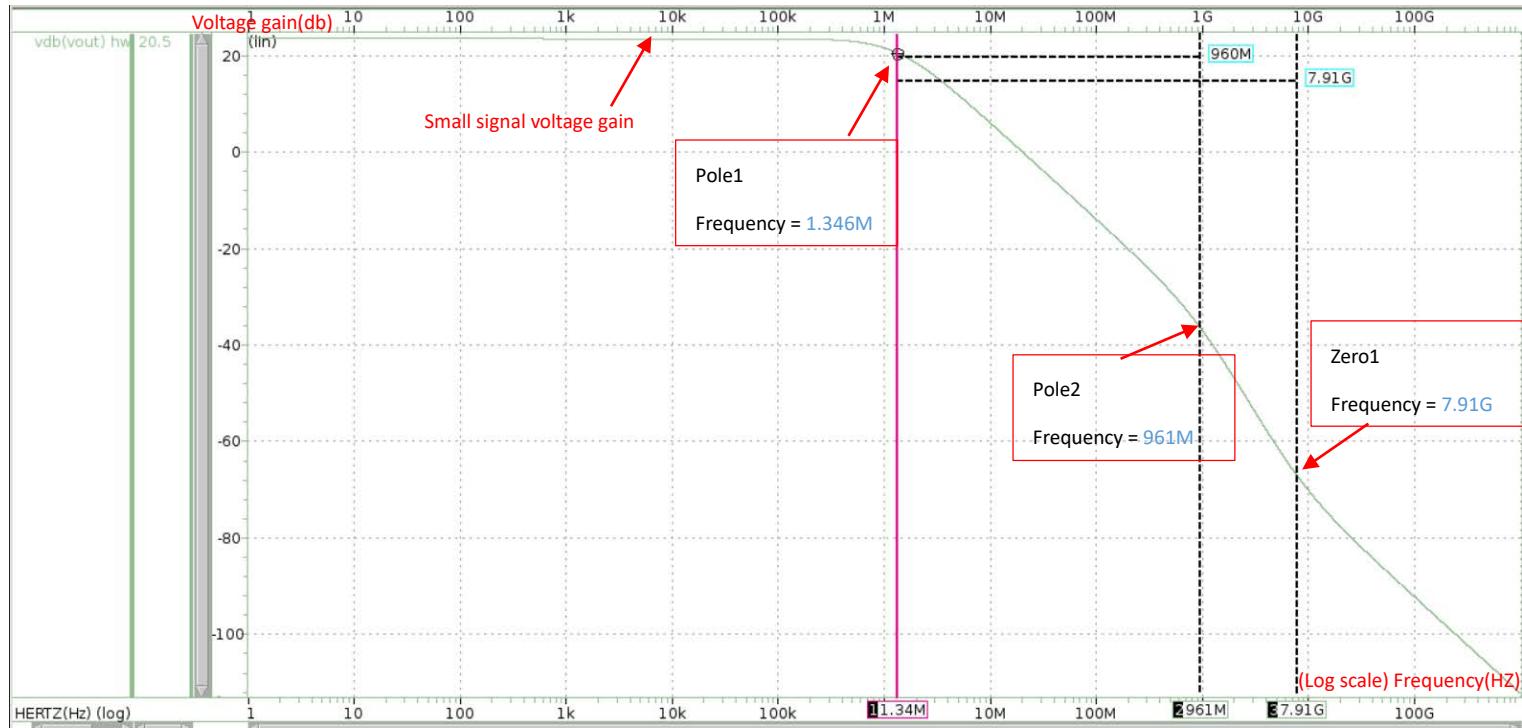


圖 3 DC pole zero analysis

The 1th iter
>temperature = 25

poles (rad/sec)		poles (hertz)	
real	imag	real	
-8.45860x	0.	-1.34623x	0.
-6.03668g	0.	-960.768x	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
49.7205g	0.	7.91326g	0.

圖 4 part of *.pz0 file

hand calculation: 使用 high frequency model of Common source, (Notation: $R = R_L//r_o$)

$$\frac{V_{out}}{V_{in}} \frac{(C_{GD} - g_m)R}{as^2 + bs + 1}, \text{ where } \begin{cases} a = R_s R (C_{GS} C_{GD} + C_{DB} C_{GD} + C_{GS} C_{DB} + C_{GD} C_L + C_{GS} C_L) \\ b = (1 + g_m R) C_{GD} R_S + R_S C_{GS} + R (C_{DB} + C_{GD} + C_L) \end{cases}$$

There is a zero

$$w_z = \frac{g_m}{C_{GD}}, f_z = \frac{128.183 \times 10^{-6}}{2.470 \times 10^{-15} \times 2\pi} = 8.26\text{GHz}$$

There are two poles, supposed $w_{p2} \gg w_{p1}$ (dominant pole approximation)

$$w_{p1} = \frac{1}{b} = \frac{1}{(1+g_m R) C_{GD} R_S + R_S C_{GS} + R (C_{DB} + C_{GD} + C_L)}$$

$$w_{p2} = \frac{b}{a} = \frac{(1+g_m R) C_{GD} R_S + R_S C_{GS} + R (C_{DB} + C_{GD} + C_L)}{R_S (C_{GS} C_{GD} + C_{DB} C_{GD} + C_{GS} C_{DB} + C_{GD} C_L + C_{GS} C_L)}$$

Using the value from 圖 5, I can get two poles: (Note: $C_L = 1\text{pF}$, $R_s = 10\text{kohm}$)

$$f_{p1} = \frac{w_{p1}}{2\pi} = 1.305\text{MHz}$$

$$f_{p2} = \frac{w_{p2}}{2\pi} = 1234.6\text{MHz}$$

可以發現跟 simulation results 仍然有些許的誤差，可能來自於手算過程簡略了一些數字或者是 $w_{p2} \gg w_{p1}$ 這個假設，但 w_{p2} 的值相對於 w_{p1} 還不夠大，所以有誤差。不過整體來說 hand calculation 跟 simulation results 的數量級還算是對的。 f_{p1} 差不多都在 1M 這個數量級； f_{p2} 差不多都在 1000M 這個數量級； f_z 也差不多在 7~8G 左右的數量級。

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vdsat	71.4434m
vod	2.3601m
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gam_eff	507.4460m
gm	128.1826u
gds	2.0262u
gmb	24.8738u
cdtot	9.0578f
cgtot	16.6239f
cstot	19.7697f
cbtot	19.0138f
cgs	11.0421f
cgd	2.4695f

圖 5 small signal parameter list

(g) The followings are my observations of how to maximize FOM1.

1. -3db bandwidth in CS is $\frac{1}{R_L \times C_L}$. So in the only thing I can change is R_L . Therefore, I try to make R_L small.

However it cannot be too small, or the current would be large because $I = \frac{VDD - V_{out}}{R_L}$, assume NMOS is in saturation,

V_{out} and R_L decreases so current increases)

2. The bias current is proportional to $\frac{W}{L}$ 、 $(V_{GS} - V_{th})$. I try to minimize $\frac{W}{L}$ ratio and avoid the NMOS to

be in cutoff region at the same time. Also I want to make sure is equal to 15. So I decrease the $(V_{GS} - V_{th})$. And try to find a balance point between these influences.

(The reason why I decrease $(V_{GS} - V_{th})$: without consideration of r_o , voltage is $gm * RL$. $gm = \frac{I_D}{V_{ov}/2}$, $VDD - I_d * RL > V_{ov}$ to make sure NMOS is in the saturation region. So, $RL < \frac{VDD - V_{ov}}{I_D}$. Voltage gain = $gm \times R_L <$

$\frac{2(VDD - V_{ov})}{V_{ov}}$. So the smaller V_{ov} is the larger voltage gain becomes.)

Problem 2 (FOM2)

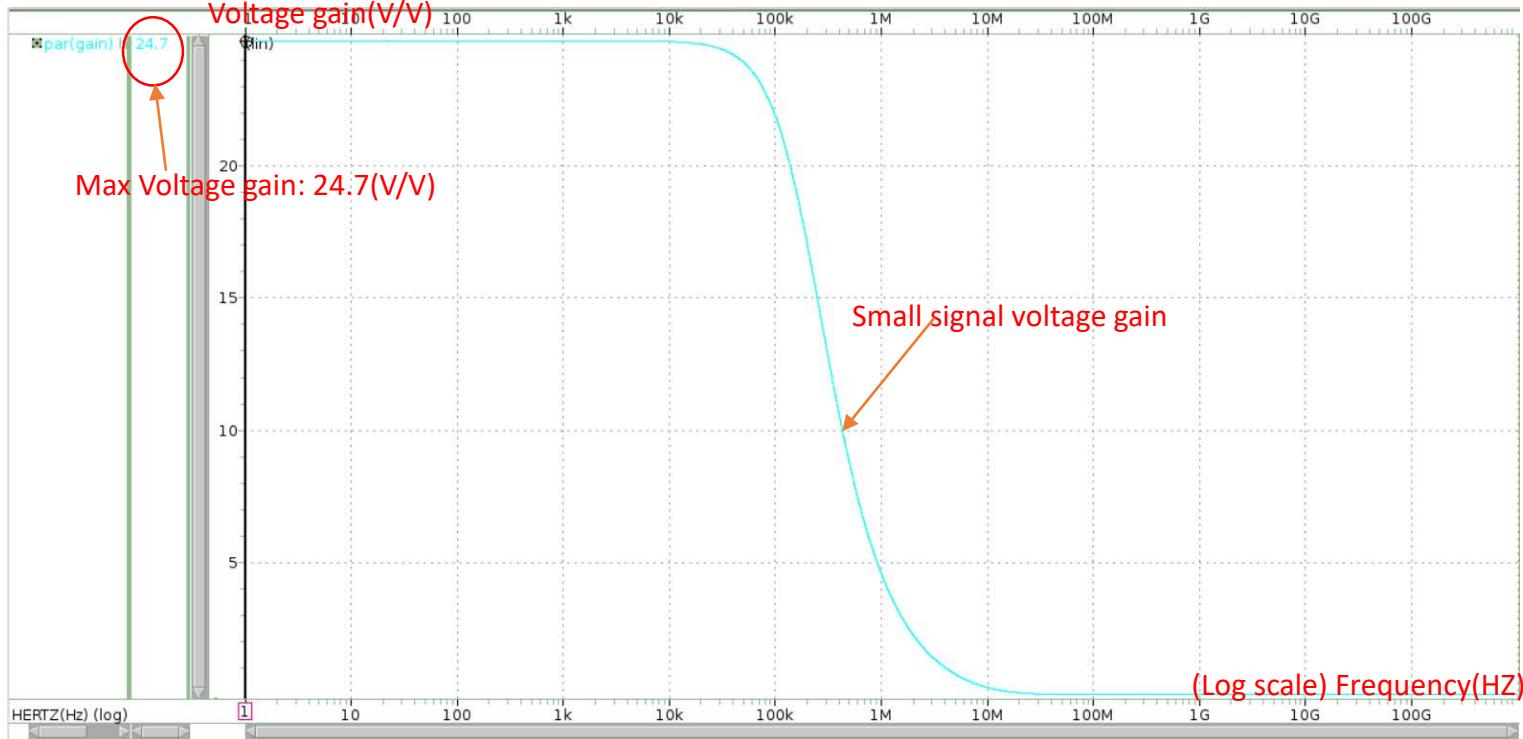


圖 6 frequency response of NMOS

The followings are my observations of how to maximize FOM2:

$$Av = gm \times (R_L // r_o)$$

1. I noticed the V_{GS} can dramatically influence the gain. As initially I set V_{GS} at around 0.45V. I try my best to maximize the gain, but gain was always around 16~17(V/V). And when I set V_{GS} at around 0.35, the voltage gain increased dramatically. So I try to make the V_{GS} as small as possible.
2. By decreasing V_{GS} , it also reduced current but increase r_o . So the difference between R_L and r_o becomes larger. Therefore I can increase R_L , the value of $R_L // r_o$ will be close to R_L as long as r_o is still very large. In my design r_o is around 6.37Mohm, and $R_L=880\text{kohm}$.
3. Also I try to make V_{GS} as close to V_{th} as much. According to my analysis in (g), the smaller V_{ov} is, the bigger the voltage gain becomes. So in my

design Vov is only 3.55mV.

Hspice code

*****problem 1 (FOM1)*****

```
.prot
.lib "cic018.l" TT
.unprot
.temp 25
.option post

M1 Vout Vg gnd gnd n_18 w = 6.6u l = 0.47u m = 1
v1 Vdd 0 1.5
v2 Vgs 0 DC 0.4515 AC 1
v3 gnd 0 0
C1 Vout 0 1p
Rs Vgs Vg 10k
RL VDD Vout 153k $gain = gm*(RL//ro), but ro > RL, RL < 19076 to be in
saturation, RL the bigger the better
```

```
.DC v2 0 1.5 0.005
.probe DC
+current = I(M1)
+vth = vth(M1)
+vov = par(' V(Vg)-Vth(M1)' )
+vsat = par(' V(Vg)-Vth(M1)-V(Vout)' )
+slope = deriv(' V(Vout)' )

.AC DEC 10k 1 1T
.probe AC
+gain = par("V(Vout)" )
.pz V(Vout) v2    $pole zero analysis
.op
.meas AC Gainmax MAX vdb(Vout)
.meas AC bandwidth WHEN Vdb(Vout) = 'Gainmax-3'
.end
*****problem 2 (FOM2)*****
.prot
.lib "cic018.1" TT
.unprot
```

```
.temp 25

.option post

M1 Vout Vg gnd gnd n_18 w = 49u l = 10u m = 1
v1 Vdd 0 1.5
v2 Vgs 0 DC 0.32 AC 1
v3 gnd 0 0
C1 Vout 0 1p
Rs Vgs Vg 10k
RL VDD Vout 880k
.DC v2 0 1.5 0.1
.probe DC
+current = I(M1)
+vth = vth(M1)
.AC DEC 10k 1 1T
.probe AC
+gain = par('V(Vout)')
+cdb = 1x29(M1)
.pz V(Vout) v2 $pole zero analysis
.op
```

```
.meas Gainmax MAX Vdb(Vout)
```

```
.meas bandwidth when Vdb(Vout) = 'Gainmax-3'
```

```
.end
```