NTHUEE

EE3235 Analog IC Analysis & Design - I 2019. Fall.

HW1

Due date : 2019. 10.11 (Friday) 23:59pm (upload to iLMS System)

First release : 2019. 09. 25

HW1 –MOS Device Performance

This homework is for you to get familiar to HSPICE. The results should include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulations for hand calculations.

Please note:

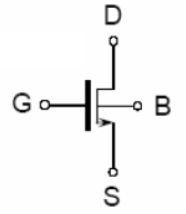
1. Please hand in your report using LMS.
2. Please note, **no delay allowed!!!**
3. **Please generate your report with *pdf* format (AIC_HW{X}_StudentID.pdf). At first page please add your student ID and name. Try to make the information "readable".** (Note: Don't use black color in background for your screen capture figures).
4. Please **hand in the spice code file (AIC_HW{X}_StudentID. sp)** with your report for each work. Do not include output file.
5. Do not zip your whole package.

Please attach your spice code at the end of report.

1. In the following we will use two different sizes with same W/L ratio,

   M1A: W/L=5µm/0.18µm, m=2

   M1B: W/L=5µm/0.36µm, m=4



In the simulation, VS=VB=0V, VD=1.8V Please sweep VG from 0V to 1.8V and draw two curves in a same figure, from (a) to (e). Compare device simulations with your calculation, and add your discussions.

(a) V_{th} vs. V_G : (threshold voltage)

(b) I_D vs. V_G : (on-off current ratio)

Please use log scale for I_D axis, and observe the current level under

off/subthreshold/strong inversion operation.

(c) gm/I_D vs. V_G : (power efficiency)

(d) gm*ro vs. V_G : (intrinsic gain)

(e) gm/Cg vs. V_G : (speed)

部分參考範例

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*輸出小訊號模型

.DC VG 0 1 0.01                    $change different value
.plot Vth=LV9(M1A)                 $plot M1 device threshold voltage
.plot Gid=par('(LX7(M1A)/I(M1A)')  $plot M1 device gm/ID
:
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2. Use hspice to simulate the capacitance characteristic of pMOS as shown in figure with body connected to vdd=1.8V. (***hint***: .probe DC ctot=par("lx18(MN)"))

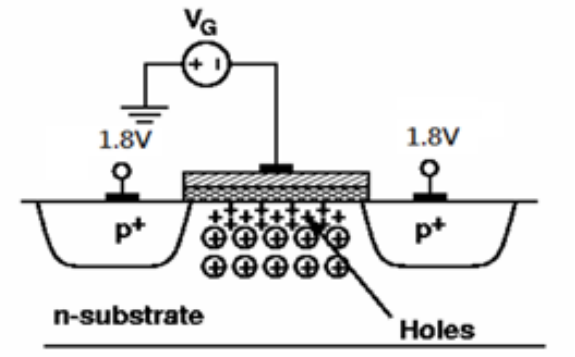
(a) Assume:

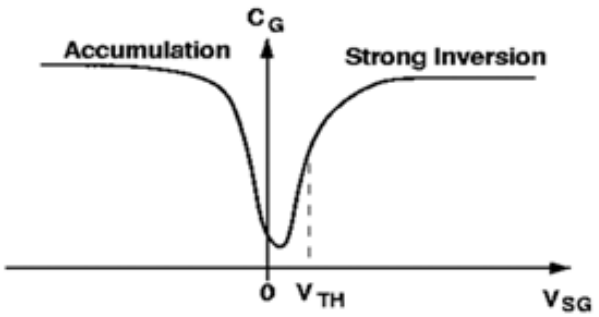
PMOS1: W/L = 10um/0.5um, m=5, V_G = 0V ~ 3.6V.

PMOS2: W/L = 50um/0.5um, m=1, V_G = 0V ~ 3.6V.

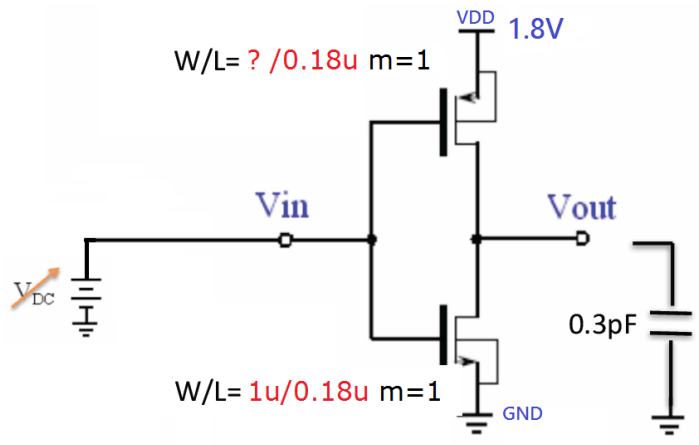
Do the simulation and plot and make comments the capacitance difference.

(b) **PMOS3: W/L =5um/5um, m=1.** Do the simulation and plot and make comments the capacitance difference compared with PMOS1 and PMOS2.





3. This is an analog amplifier or a digital driver, with the MOS device sizes as:



(a) (At TT corner, 25℃) Please use .DC sweep command to find the PMOS width so that Vin = Vout = $\frac{VDD}{2}$ and draw the input-output DC transfer curve under the condition of the size you find. (Be care of resolution issues) (width with accuracy to the 3rd decimal places at most) pmos width = 3.15u

(b) Repeat the steps in (a), find the PMOS width so that Vin = Vout = $\frac{VDD}{2}$ under 5 corner (SS, SF, TT, FS, FF) and 3 temperatures (-40℃, 25℃, 125℃). Fill the following table and make comments.

	SS	SF	TT	FS	FF
-40℃	3.646	0.889	3.575	2.543	3.419
25℃	3.105	0.759	3.15	2.271	3.04
125℃	2.562	0.627	2.68	1.959	2.604

(unit: um)

4. Fig. 2(a) shows the pseudo-NMOS logic inverter. The gate of PMOS is always connected to ground and always ON. The large-signal transfer curve of vout versus vin of this circuit is given in Fig. 2(b). Determine the three operation regions (cutoff, linear, and saturation) of Mp and Mn in the four different regions.(AB, BC, CD, and DE) Use the inequality to prove your answer. (ex. Vgs < Vth)

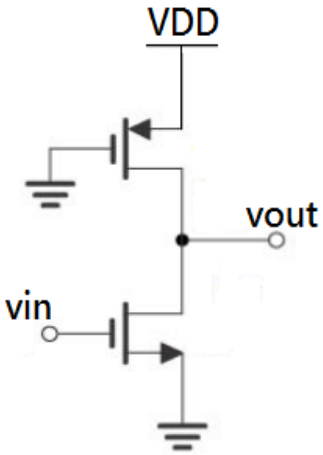


Fig. 2(a)

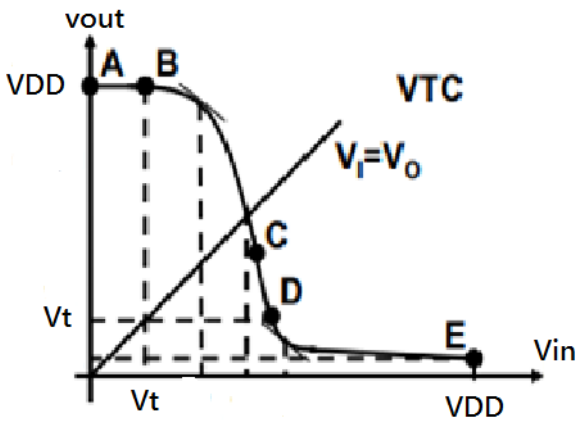


Fig. 2(b)