EE3235 Analog IC Analysis & Design-I Final Project

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I. Schematic

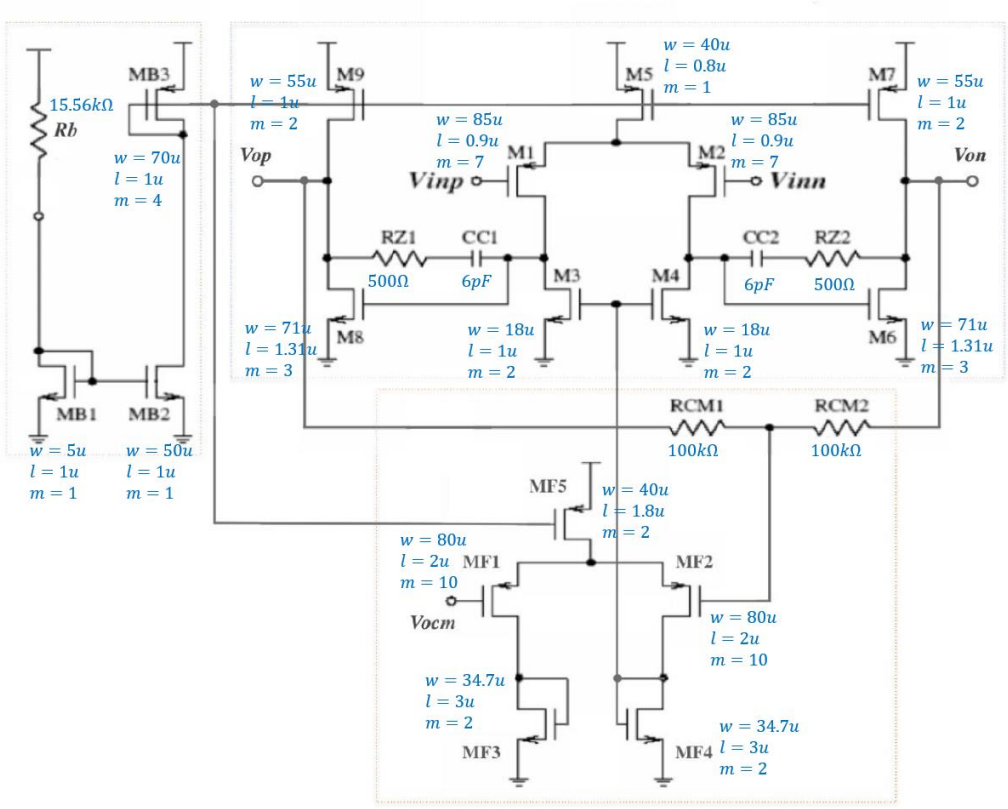


Fig. 1(a) Whole circuit schematic (Device size & component value)

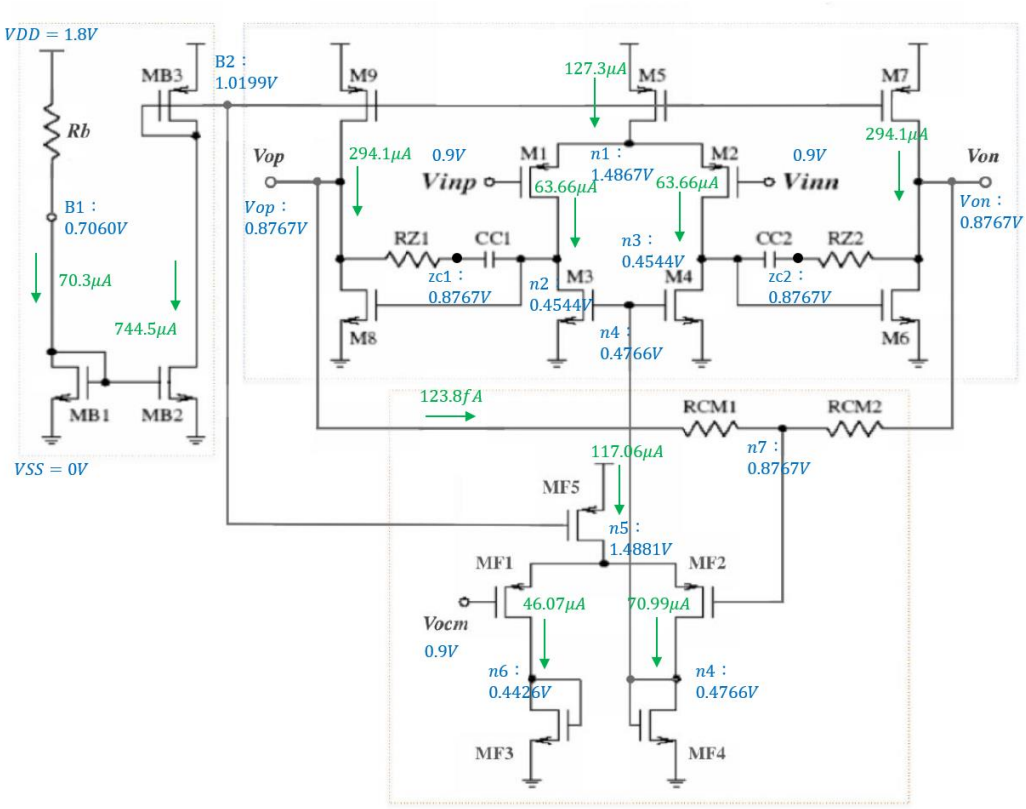


Fig. 1(b) Whole circuit schematic (Node voltage & Branch current)

List. 1：Small signal parameters

subckt	xop	xop	xop	xop	xop	xop
element	1:mb1	1:mb2	1:mb3	1:m1	1:m2	1:m3
model	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	70.3103u	744.4851u	-744.4851u	-63.6574u	-63.6574u	63.6574u
ibs	-1.244e-20	-1.115e-19	6.873e-20	8.2531f	8.2531f	-9.873e-21
ibd	-300.3082a	-3.6702f	9.6956f	35.4487f	35.4487f	-1.2198f
vgs	705.9723m	705.9723m	-780.1290m	-586.7226m	-586.7226m	476.5957m
vds	705.9723m	1.0199	-780.1290m	-1.0323	-1.0323	454.4118m
vbs	0.	0.	0.	313.2774m	313.2774m	0.
vth	386.4914m	380.6097m	-494.5475m	-583.1972m	-583.1972m	385.5881m
vdsat	272.9791m	280.5251m	-262.4845m	-70.9223m	-70.9223m	112.2055m
vod	319.4809m	325.3626m	-285.5816m	-3.5255m	-3.5255m	91.0076m
beta	1.5575m	15.5999m	19.3865m	46.3646m	46.3646m	11.2067m
gam eff	507.4467m	507.4468m	557.0846m	554.9654m	554.9654m	507.4460m
gm	400.0522u	4.1616m	4.6067m	1.2803m	1.2803m	928.7941u
gds	5.9938u	52.2643u	34.5461u	3.3910u	3.3910u	11.3127u
gmb	76.7272u	795.6866u	1.4299m	339.5449u	339.5449u	189.3256u
cdtot	6.7583f	63.0054f	315.1920f	615.7555f	615.7555f	50.2290f
cgtot	34.4539f	343.3496f	1.8298p	2.4192p	2.4192p	242.6747f
cstot	38.7766f	386.2963f	2.1417p	2.4433p	2.4433p	271.2222f
cbtot	18.5052f	179.8744f	1.0140p	1.7710p	1.7710p	136.5383f
cgs	30.2944f	301.3118f	1.6138p	1.7158p	1.7158p	209.4780f
cgd	1.7908f	17.7523f	101.1553f	213.5052f	213.5052f	12.8738f

subckt	xop	xop	xop	xop	xop	xop
element	1:m4	1:m5	1:m6	1:m8	1:m7	1:m9
model	0:n_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	63.6574u	-127.3148u	276.6036u	276.6036u	-294.1384u	-294.1383u
ibs	-9.873e-21	1.188e-20	-4.116e-20	-4.116e-20	2.726e-20	2.726e-20
ibd	-1.2198f	562.0979a	-13.3607f	-13.3607f	4.5252f	4.5252f
vgs	476.5957m	-780.1290m	454.4118m	454.4118m	-780.1290m	-780.1290m
vds	454.4118m	-313.2774m	876.7381m	876.7382m	-923.2619m	-923.2618m
vbs	0.	0.	0.	0.	0.	0.
vth	385.5881m	-497.2500m	365.4641m	365.4641m	-494.5502m	-494.5502m
vdsat	112.2055m	-263.8330m	109.3102m	109.3102m	-262.5519m	-262.5519m
vod	91.0076m	-282.8790m	88.9477m	88.9477m	-285.5789m	-285.5789m
beta	11.2067m	3.4771m	50.0747m	50.0747m	7.6110m	7.6110m
gam eff	507.4460m	557.0846m	507.4460m	507.4460m	557.0846m	557.0846m
gm	928.7941u	768.1608u	4.0855m	4.0855m	1.8206m	1.8206m
gds	11.3127u	41.1120u	39.6930u	39.6930u	11.5926u	11.5926u
gmb	189.3256u	238.0253u	827.6464u	827.6464u	565.2546u	565.2546u
cdtot	50.2290f	56.0532f	273.5125f	273.5125f	120.8197f	120.8197f
cgtot	242.6747f	213.3931f	1.8487p	1.8487p	718.6353f	718.6353f
cstot	271.2222f	250.3837f	2.0202p	2.0202p	841.5311f	841.5311f
cbtot	136.5383f	133.4876f	899.7764f	899.7764f	395.7123f	395.7123f
cgs	209.4780f	183.9531f	1.6099p	1.6099p	633.8385f	633.8385f
cgd	12.8738f	17.0786f	74.9312f	74.9312f	39.6124f	39.6124f

subckt	xop	xop	xop	xop	xop
element	1:mf1	1:mf2	1:mf3	1:mf4	1:mf5
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	-46.0681u	-70.9965u	46.0681u	70.9965u	-117.0646u
ibs	11.0546f	11.0547f	-6.958e-21	-1.072e-20	1.092e-20
ibd	48.1164f	46.9105f	-2.2304f	-2.4019f	1.1191f
vgs	-588.1349m	-611.3968m	442.5767m	476.5957m	-780.1290m
vds	-1.0456	-1.0115	442.5767m	476.5957m	-311.8651m
vbs	311.8651m	311.8651m	0.	0.	0.
vth	-571.0396m	-571.0396m	335.4172m	335.2822m	-484.9224m
vdsat	-73.5384m	-85.0865m	116.2919m	139.3552m	-263.9577m
vod	-17.0953m	-40.3572m	107.1595m	141.3135m	-295.2067m
beta	27.8584m	27.7439m	6.9834m	6.9949m	3.0549m
gam eff	554.9743m	554.9743m	507.4460m	507.4460m	557.0846m
gm	895.4521u	1.2639m	631.8135u	823.3312u	689.4067u
gds	1.1196u	1.6588u	4.6706u	6.3455u	31.7812u
gmb	240.0314u	338.8393u	127.8271u	164.6264u	217.5127u
cdtot	827.0262f	830.5055f	98.4380f	98.1450f	140.2201f
cgtot	7.6025p	8.6467p	1.3660p	1.3787p	945.5096f
cstot	7.5291p	9.0574p	1.4335p	1.4512p	1.0623p
cbtot	3.9972p	4.0335p	506.0617f	503.2851f	436.2085f
cgs	5.9404p	7.2675p	1.2220p	1.2395p	842.3276f
cgd	287.0980f	287.1796f	23.9367f	24.0462f	46.2861f

II. Spice code

```
****op****
.subckt op vinp vinn vdd vss vop von vocm

***Bias MOS***
MB1 B1 B1 vss vss N_18 w=5u l=1u m=1
MB2 B2 B1 vss vss N_18 w=50u l=1u m=1
MB3 B2 B2 vdd vdd P_18 w=70u l=1u m=4

***Amp MOS***
M1 n2 vinp n1 vdd P_18 w=85u l=0.9u m=7
M2 n3 vinn n1 vdd P_18 w=85u l=0.9u m=7
M3 n2 n4 vss vss N_18 w=18u l=1u m=2
M4 n3 n4 vss vss N_18 w=18u l=1u m=2
M5 n1 B2 vdd vdd P_18 w=40u l=0.8u m=1
M6 von n3 vss vss N_18 w=71u l=1.31u m=3
M8 vop n2 vss vss N_18 w=71u l=1.31u m=3
M7 von B2 vdd vdd P_18 w=55u l=1u m=2
M9 vop B2 vdd vdd P_18 w=55u l=1u m=2

***Feedback MOS***
MF1 n6 vocm n5 vdd P_18 w=80u l=2u m=10
MF2 n4 n7 n5 vdd P_18 w=80u l=2u m=10
MF3 n6 n6 vss vss N_18 w=34.7u l=3u m=2
MF4 n4 n4 vss vss N_18 w=34.7u l=3u m=2
MF5 n5 B2 vdd vdd P_18 w=40u l=1.8u m=2

***Resistor***
RZ1 vop zc1 500
RZ2 von zc2 500
RCM1 vop n7 100k
RCM2 von n7 100k
Rb vdd B1 15.56k

***Capacitor***
CC1 zc1 n2 6p
CC2 n3 zc2 6p

.ends
```

III. Simulations

3.1 Open-loop differential mode AC response

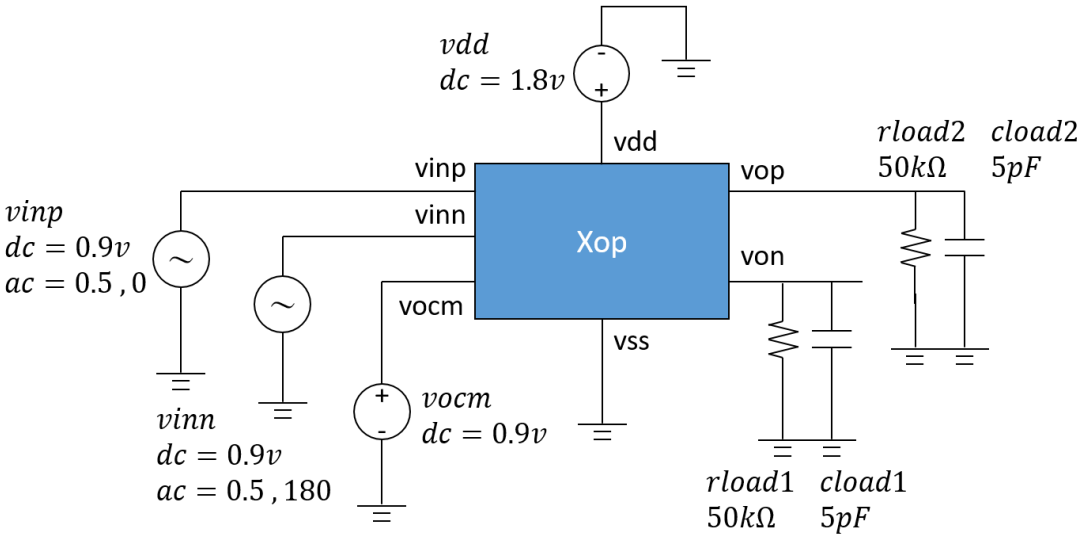
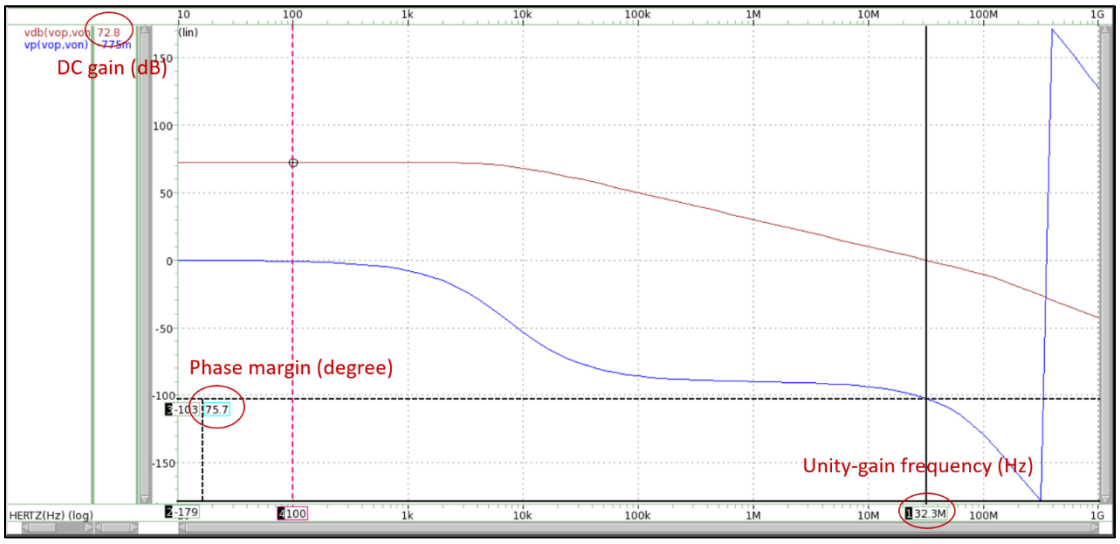


Fig. 3.1(a) Test circuit of 3.1




```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  72.8230     at=  10.0000
               from=  10.0000     to=   1.0000g
dcgain=   4.3767k    at=  10.0000
               from=  10.0000     to=   1.0000g
adm_in_db_10k=  68.3165
unity_frequency=  32.3093x
phase=-102.5294
phase_margin=  77.4706
```

Fig. 3.1(b) AC magnitude and phase response of differential mode gain

```
Output first 10 Poles, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      poles (rad/sec)                poles ( hertz)
real             imag            real             imag
-46.5407k        0.              -7.40718k        0.
-1.11873x        -18.4888x       -178.051k        -2.94259x
-1.11873x        18.4888x        -178.051k        2.94259x
-151.796x        0.              -24.1591x        0.
-285.635x        0.              -45.4602x        0.
-317.701x        0.              -50.5636x        0.
-663.813x        0.              -105.649x        0.
-759.983x        231.772x        -120.955x        36.8877x
-759.983x        -231.772x       -120.955x        -36.8877x
-775.835x        215.474x        -123.478x        34.2937x

Output first 10 Zeros, (total 20)
Use .option pz_num = NUM to control output number, (default:10)

      zeros (rad/sec)                zeros ( hertz)
real             imag            real             imag
-1.10475x        -18.3880x       -175.827k        -2.92654x
-1.10475x        18.3880x        -175.827k        2.92654x
-1.10599x        18.3924x        -176.023k        2.92725x
-1.10599x        -18.3924x       -176.023k        -2.92725x
-151.820x        0.              -24.1628x        0.
-285.636x        0.              -45.4605x        0.
-317.601x        0.              -50.5478x        0.
-566.094x        -3.73732k       -90.0966x        -594.813
-566.094x        3.73732k        -90.0966x        594.813
-648.898x        0.              -103.275x        0.
```

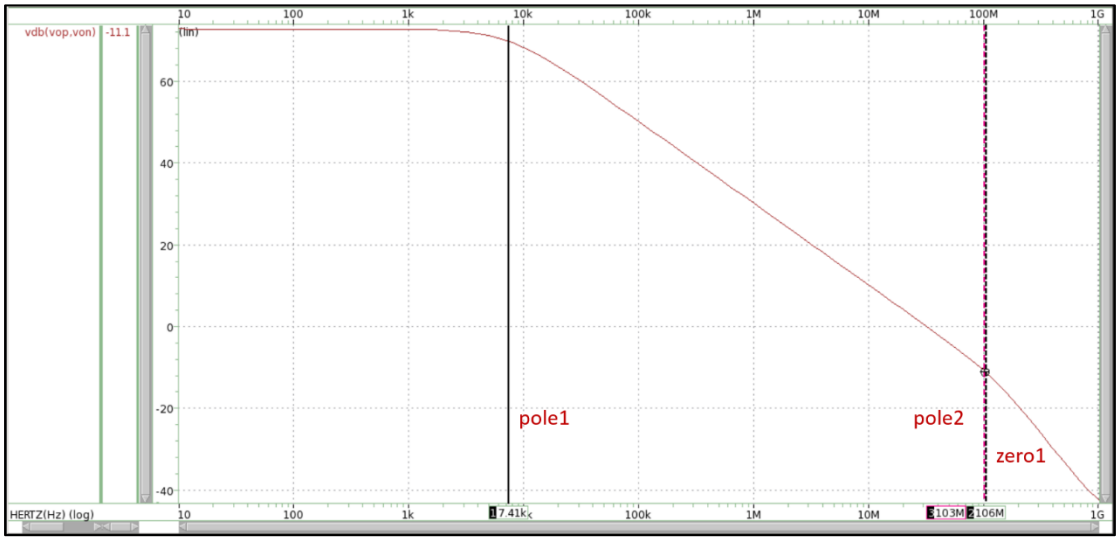


Fig. 3.1(c) Poles and zeros of differential mode

<Dis. 3.1(d)>

(i) Gain：

從 fig. 1(a)可以得知：

$\rightarrow gain = g_{m1} * (r_{o1} \parallel r_{o3}) * g_{m8} * (r_{o8} \parallel r_{o9} \parallel r_{load})$

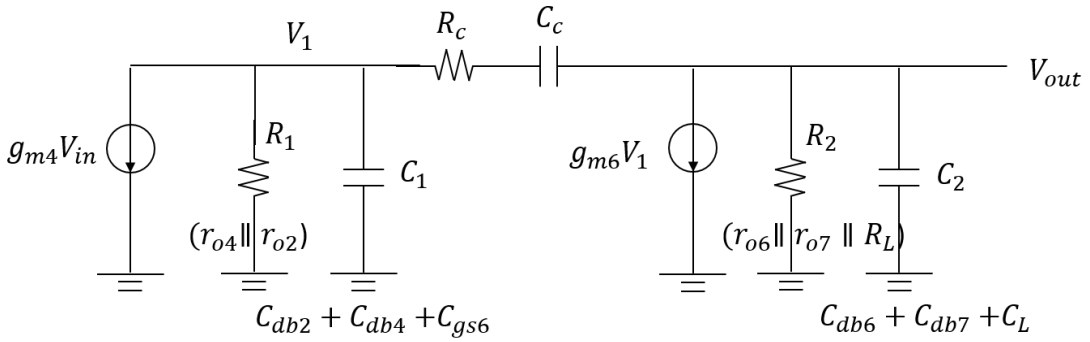
由 List. 1 可以得到以上的參數，因此我們可以計算出：

$\rightarrow gain = 1.2803m * (68010.1) * 4.0855m * (14028.0786)$

$= 4990.322 = 73.96\text{dB}$

與模擬值 72.823dB 相差不大。

(ii) Pole1：



(Figure 1)Pole analysis

$$\omega_{p1} = \frac{1}{g_{m6} * R_1 * R_2 * C_c} = \frac{1}{(4.0855m) * 68010.0927 * 14028.0786 * 6pF}$$
$$= 42759.4369(rad) = 6.805(kHz)$$

此算法並沒有考慮R_c的影響，因此所得到的值會與模擬有點誤差，而模擬結果為 7.4072kHz，與計算值相差尚在在可接受範圍。

(iii) Pole2：

```
cdb_2= 402.2627f
cdb_4=  36.0065f
cdb_6= 190.5634f
cdb_7=  80.9834f
```

(Figure 2) Measured cdb values

$$\omega_{p2} = \frac{g_{m6}}{(C_1 + C_2)} = \frac{4.0855m}{(628.9032f + 5.2715p)}$$
$$= 692.41M(rad) = 110.2(MHz)$$

$Simulation\ \ result：105.649(MHz)$

與模擬值相比，我們發現算出的 pole 是位置在較後面的，往前看此之前的 pole，可以發現幾乎都有與之對應的 zero 存在，因為 pole 與 zero 的效果抵銷，因此我們得到的 pole 是在與 zero 相消後所得到剩餘的 pole 位置。

(iv) Zero：

$$\omega_z = \frac{1}{C_c(\frac{1}{g_{m6}} - R_c)} = \frac{1}{6p(244.768 - 500)} = 653M(rad) = 103.928(MHz)$$

$Simulation\ \ result：103.275(MHz)$

與算 pole2 時相同，我們一樣發現算出的 zero 位置為較後面的 zero，往前看一樣可以發現，每個 zero 都有與之對應的 pole 存在，因此在效果相消後，我們會得到抵銷剩餘的 zero 位置。

3.2 Open-loop differential mode DC sweep

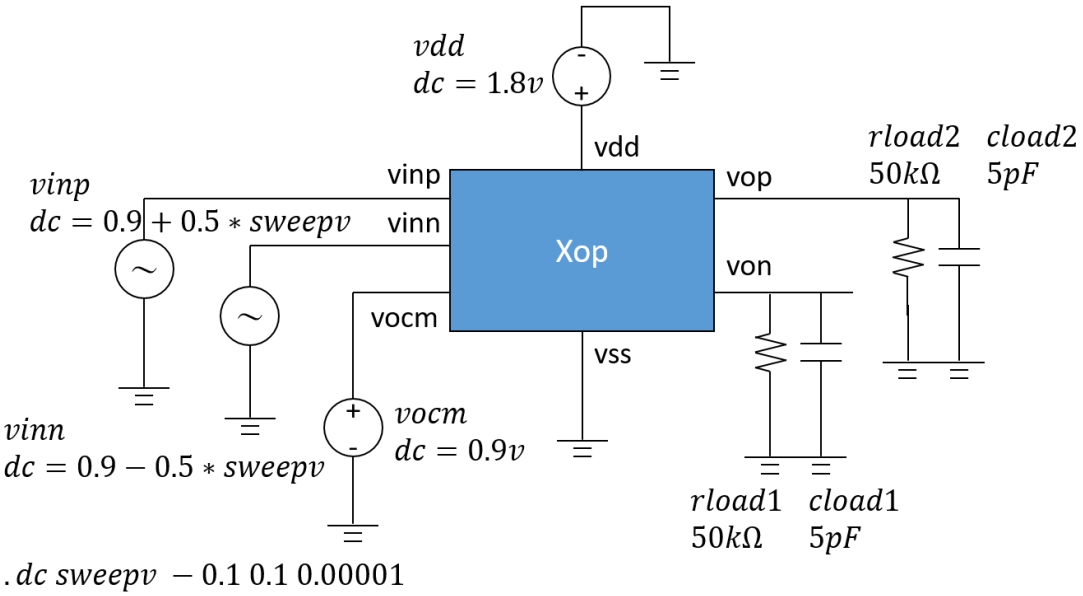


Fig. 3.2(a) Test circuit of 3.2

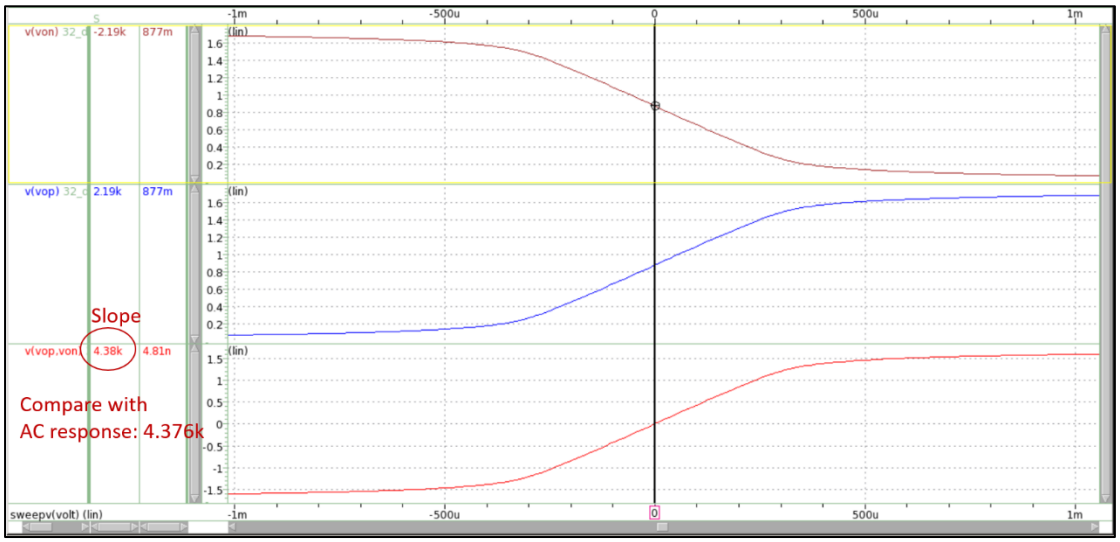


Fig. 3.2(b) Open-loop differential mode DC sweep

3.3 Open-loop common mode AC response

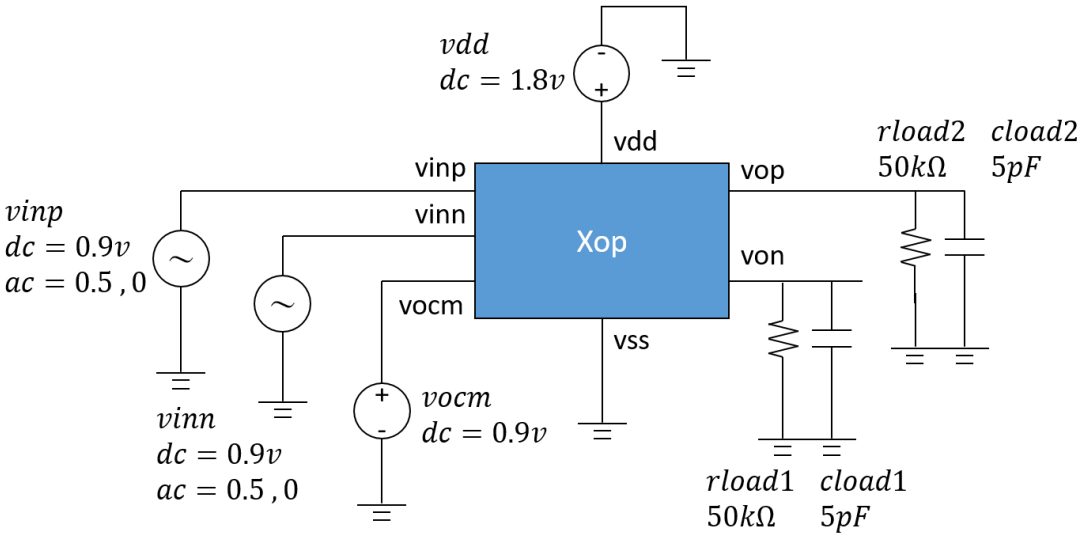
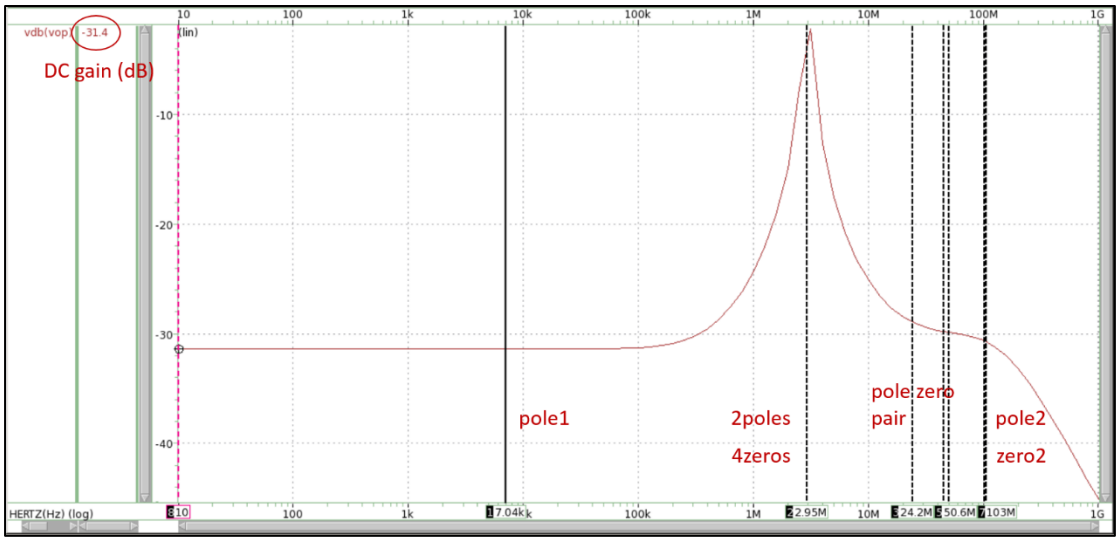


Fig. 3.3(a) Test circuit of 3.3




```
****** ac analysis tnom=  25.000 temp=  25.000 ******
acm_in_db= -31.4054
acm_in=  26.8986m
```

Fig. 3.3(b) AC magnitude response of common mode gain

<C.M.R.R. @10KHz>: 68.3165-(-31.4054) = 99.7219dB

```
Output first 10 Poles, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      poles (rad/sec)                poles ( hertz)
real            imag            real            imag
-46.5407k       0.              -7.40718k       0.
-1.11873x       -18.4888x       -178.051k       -2.94259x
-1.11873x       18.4888x        -178.051k       2.94259x
-151.796x       0.              -24.1591x       0.
-285.635x       0.              -45.4602x       0.
-317.701x       0.              -50.5636x       0.
-663.813x       0.              -105.649x       0.
-759.983x       231.772x        -120.955x       36.8877x
-759.983x       -231.772x       -120.955x       -36.8877x
-775.835x       215.474x        -123.478x       34.2937x

Output first 10 Zeros, (total 20)
Use .option pz_num = NUM to control output number, (default:10)

      zeros (rad/sec)                zeros ( hertz)
real            imag            real            imag
-1.10475x       -18.3880x       -175.827k       -2.92654x
-1.10475x       18.3880x        -175.827k       2.92654x
-1.10599x       18.3924x        -176.023k       2.92725x
-1.10599x       -18.3924x       -176.023k       -2.92725x
-151.820x       0.              -24.1628x       0.
-285.636x       0.              -45.4605x       0.
-317.601x       0.              -50.5478x       0.
-566.094x       -3.73732k       -90.0966x       -594.813
-566.094x       3.73732k        -90.0966x       594.813
-648.898x       0.              -103.275x       0.
```

Fig. 3.3(c) Poles and zeros of common mode

<Dis. 3.3(d)>

與<Dis. 3.1(d)>相同，我們可以得到：

(i) Pole1：

$$\omega_{p1} = \frac{1}{g_{m6} * R_1 * R_2 * C_c} = \frac{1}{(4.0855m) * 68010.0927 * 14028.0786 * 6pF}$$
$$= 42759.4369(rad) = 6.805(kHz)$$

與模擬值 7.4072kHz 相差在可接受範圍。

(ii) Pole2：

$$\omega_{p2} = \frac{g_{m6}}{C_1 + C_2} = \frac{4.0855m}{(628.8326f) + (5.2715p)}$$
$$= 692.4131M(rad) = 110.2(MHz)$$

$Simulation\ \ result：105.649(MHz)$

與模擬值相比，我們發現算出的 pole 是位置在較後面的，往前看此之前的 pole，可以發現幾乎都有與之對應的 zero 存在，因為 pole 與 zero 的效果抵銷，因此我們得到的 pole 是在與 zero 相消後所得到剩餘的 pole 位置。

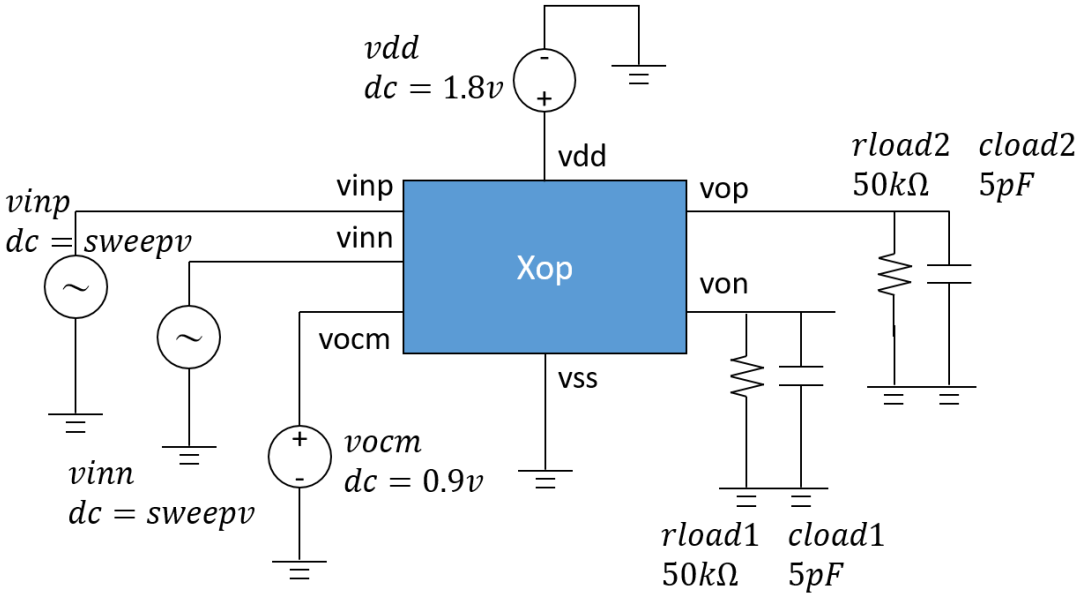
(iii) Zero：

$$\omega_z = \frac{1}{C_c(\frac{1}{g_{m6}} - R_c)} = \frac{1}{6p(244.768 - 500)} = 653M(rad) = 103.928(MHz)$$

$Simulation\ \ result：103.275(MHz)$

與算 pole2 時相同，我們一樣發現算出的 zero 位置為較後面的 zero，往前看一樣可以發現，每個 zero 都有與之對應的 pole 存在，因此在效果相消後，我們會得到抵銷剩餘的 zero 位置。

3.4 Open-loop common mode DC sweep



$.dc\ sweepv\ 0\ 'supplyp - supplyn'\ 0.001$

Fig. 3.4(a) Test circuit of 3.4

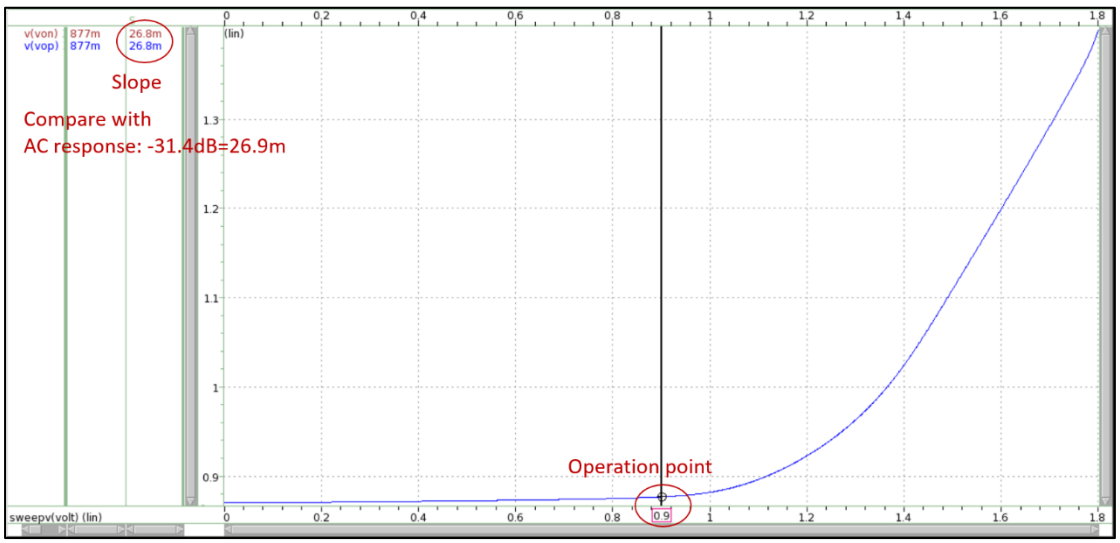


Fig. 3.4(b) Open-loop common mode DC sweep

3.5 Open-loop power supply+ AC response

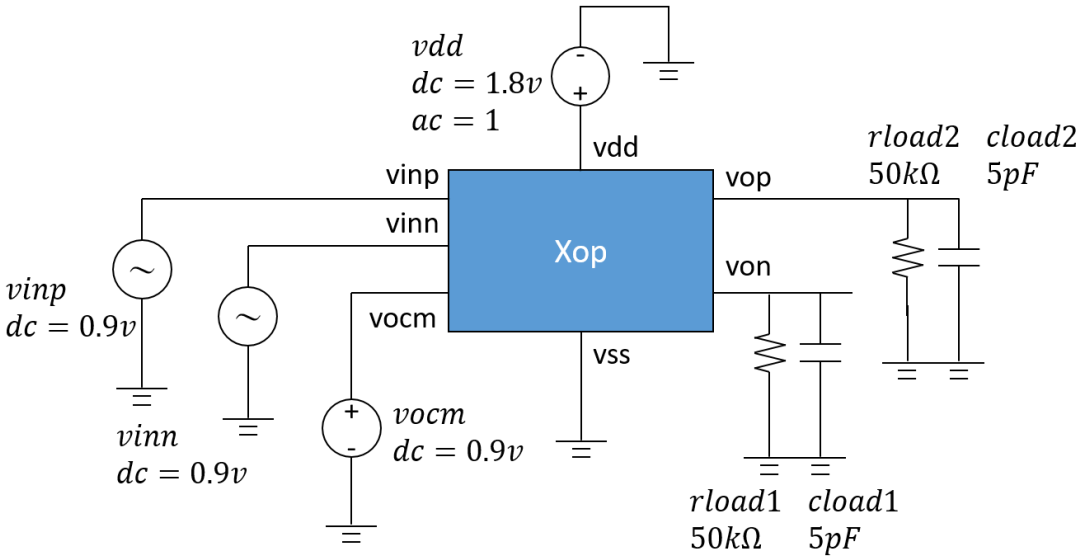
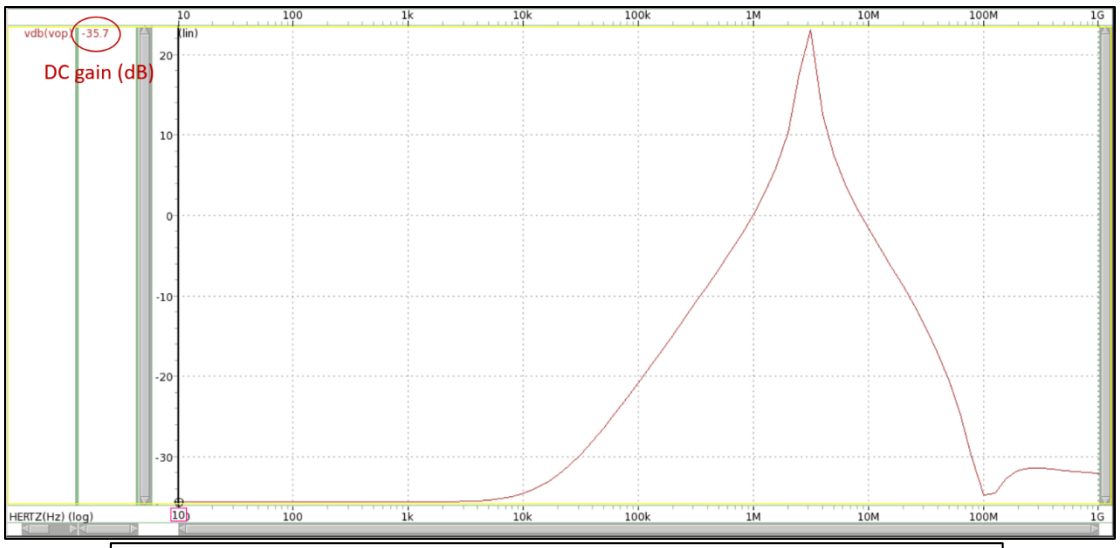


Fig. 3.5(a) Test circuit of 3.5




```
****** ac analysis tnom=  25.000 temp=  25.000 ******
psp_in_db= -34.5671
```

Fig. 3.5(b) AC magnitude response of power supply+ gain

<P.S.R.R.+ @10KHz>: 68.3165-(-34.5671) = 102.8836dB

3.6 Open-loop power supply- AC response

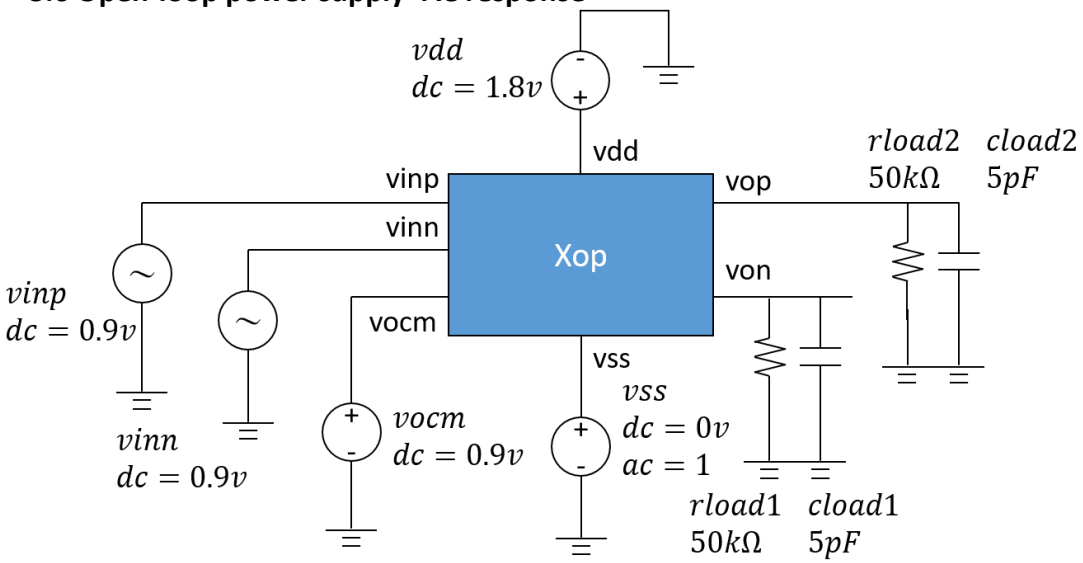
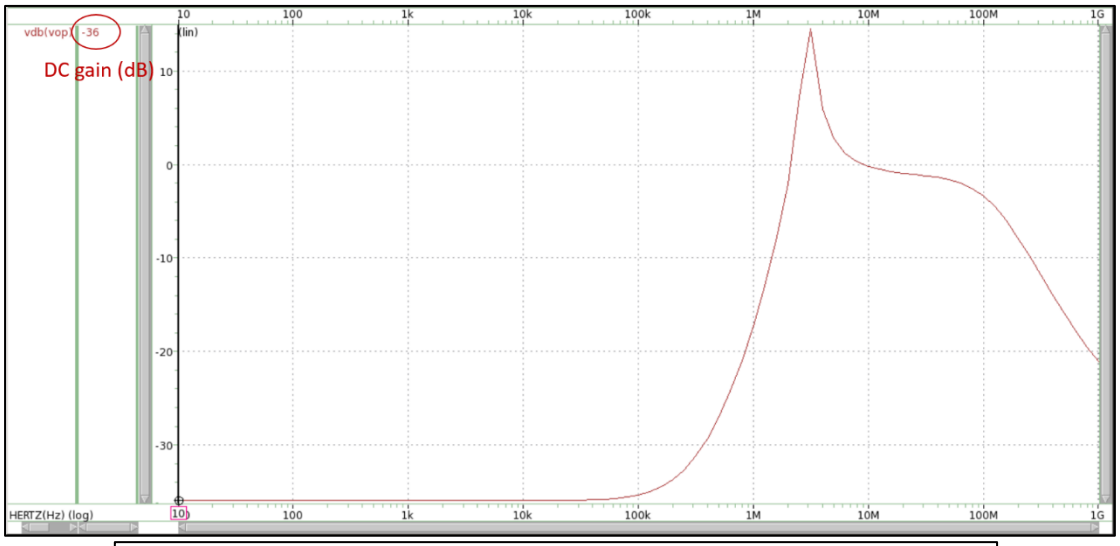


Fig. 3.6(a) Test circuit of 3.6




```
****** ac analysis tnom=  25.000 temp=  25.000 ******
psn_in_db= -35.9632
```

Fig. 3.6(b) AC magnitude response of power supply- gain

<P.S.R.R.- @10KHz>: 68.3165-(-35.9632) = 104.2797dB

3.7 Closed-loop differential mode AC response

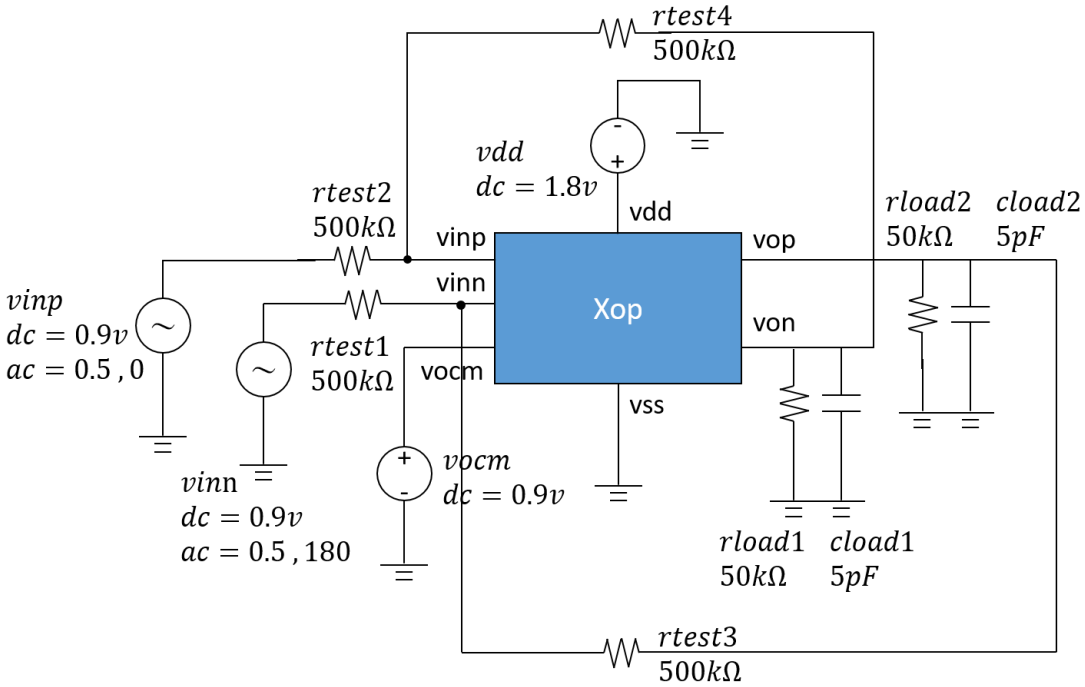


Fig. 3.7(a) Test circuit of 3.7

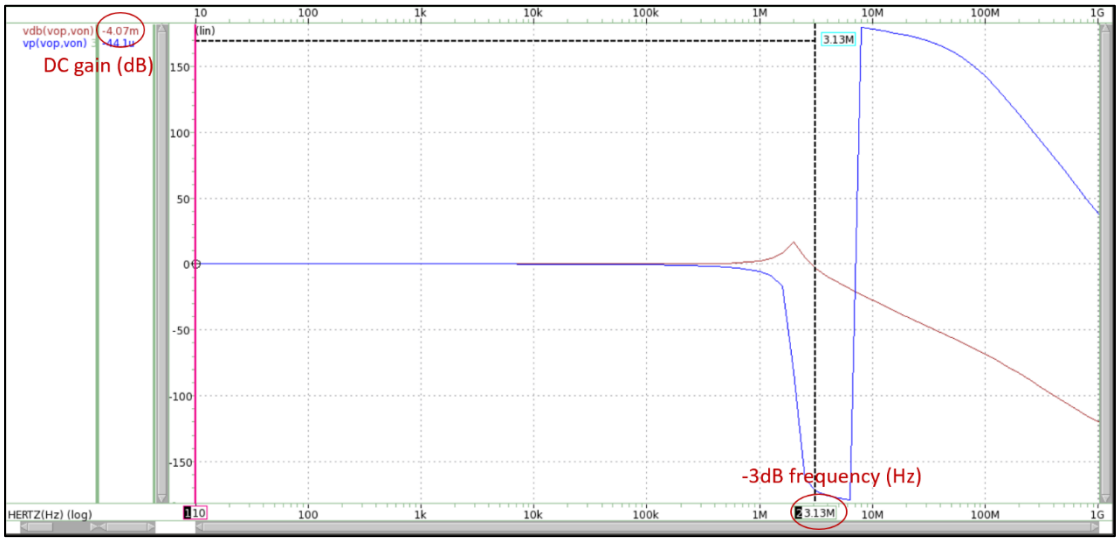


Fig. 3.7(b) AC magnitude and phase responses of differential mode gain

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:test1    = 900.0000m 0:test2    = 900.0000m 0:vdd      =   1.8000
+0:vinn     = 888.2200m 0:vinp     = 888.2200m 0:vocm     = 900.0000m
+0:von      = 876.4400m 0:vop      = 876.4400m 0:vss      =   0.
+1:b1       = 705.9723m 1:b2       =   1.0199  1:n1       =   1.4775
+1:n2       = 454.4228m 1:n3       = 454.4228m 1:n4       = 476.7865m
+1:n5       =   1.4880  1:n6       = 442.3344m 1:n7       = 876.4400m
+1:zc1      = 876.4400m 1:zc2      = 876.4400m
```

Fig. 3.7(c) Input and output node voltages

從 Fig. 3.7(c)可以得到，$vinn, vinp = 0.888V$，而$von, vop = 0.8764V$，兩者相除接近為 1，為合理的結果。

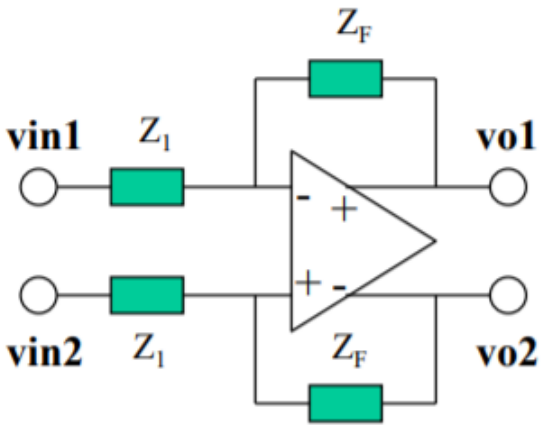
```
****     small-signal transfer characteristics

     v(vop,von)/vinn                          = -999.5319m
     input resistance at             vinn     =  669.4638k
     output resistance at v(vop,von)          =   11.2402
```

Fig. 3.7(d) .tf result of closed loop differential mode

<Dis. 3.7(e)>

(i) Gain：



(Figure 3) Closed loop circuit

$$\rightarrow Gain = \frac{Z_F}{Z_1} = \frac{500k}{500k} = 1$$

與模擬值 0.9995 相差不大。

(ii) Input impedance：

$$\rightarrow Z_{in} \cong \left((R_{CM1} + R_{CM2} + 50k) \parallel 500k\right) + 500k$$
$$= \left((200k + 50k) \parallel 500k\right) + 500k = 666.667k\Omega$$

與模擬值$669.4638k\Omega$相差不大。

(iii) output impedance：

我們知道理想的 op amp 會有 zero output impedance，而透過 CMFB 的方式我們將會得到接近於 0 的 output impedance。

3.8 Closed-loop differential mode DC sweep

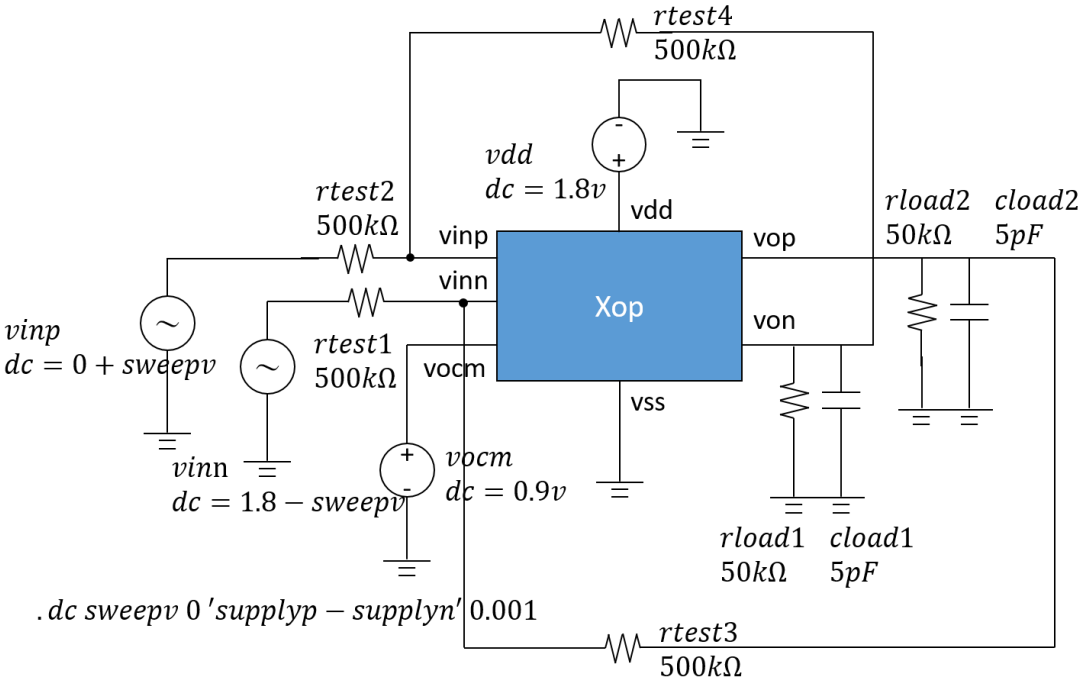


Fig. 3.8(a) Test circuit of 3.8

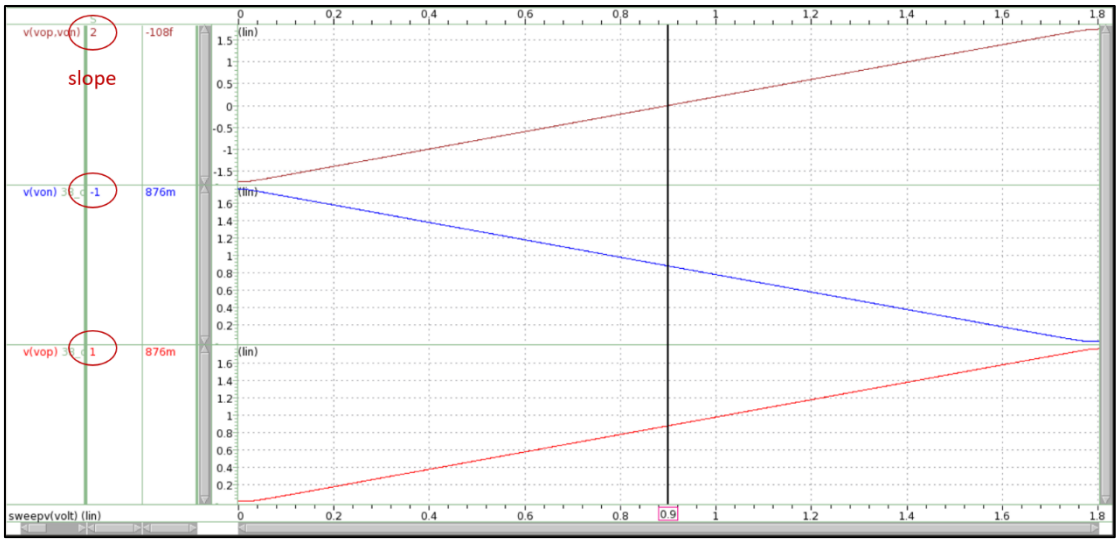


Fig. 3.8(b) Single-ended and differential outputs for differential step inputs

由 Fig. 3.8(b)我們可以發現，$v(vop, von)$的斜率為 2，而 3.7 小題中所得到的 AC response 數值 1 不同。原因為 3.8 中我們是一次 sweep 雙邊訊號，而 3.7 是只有 sweep 單邊，因此我們在 3.8 中所得到的斜率為 3.7 的兩倍。

3.9 Closed-loop step+ response

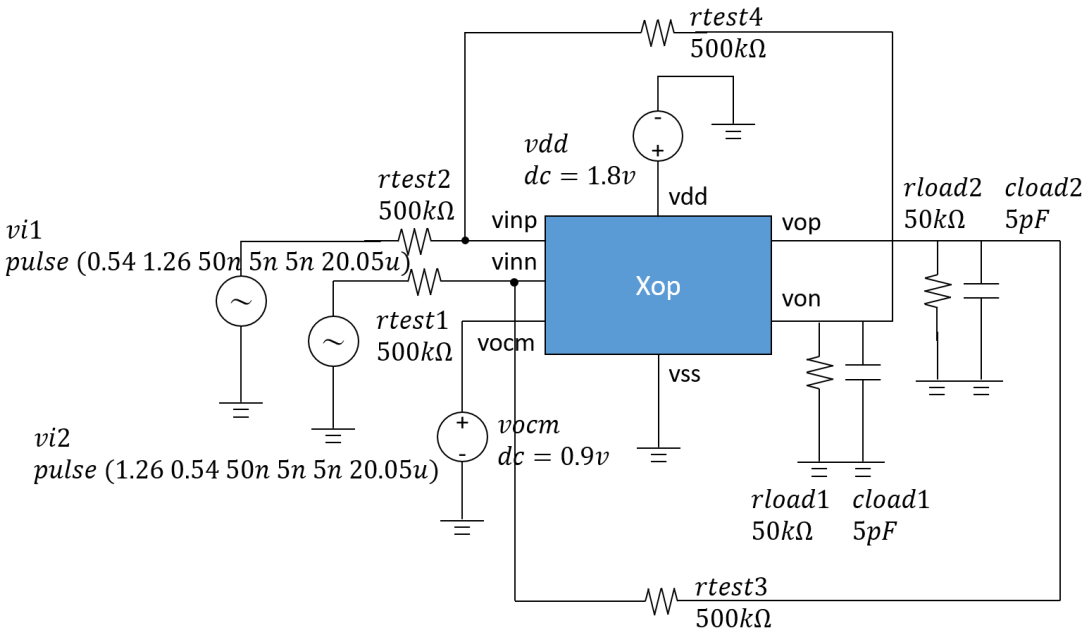


Fig. 3.9(a) Test circuit of 3.9

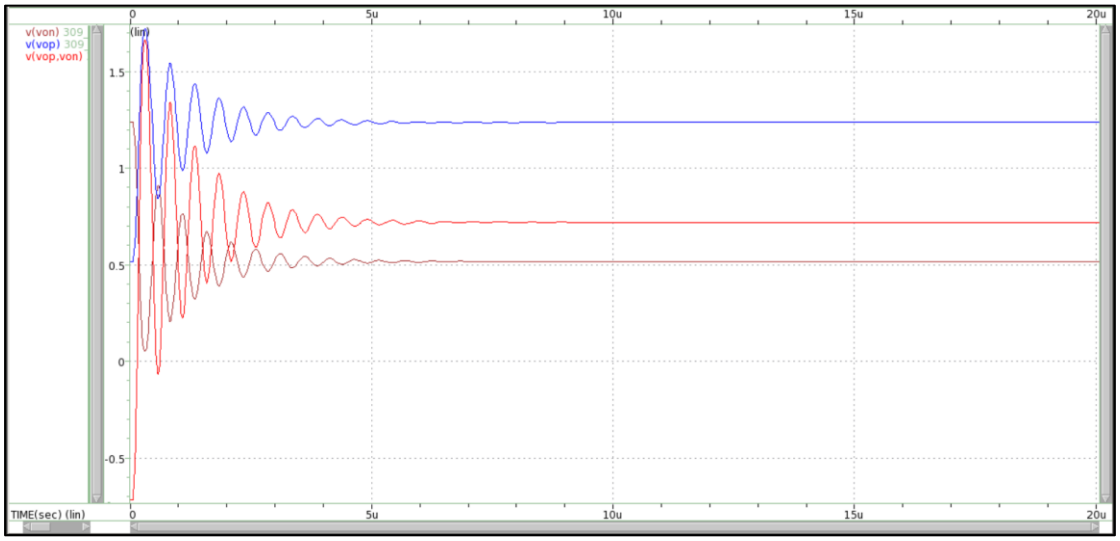


Fig. 3.9(b) Single-ended and differential outputs for +1.44V differential step inputs

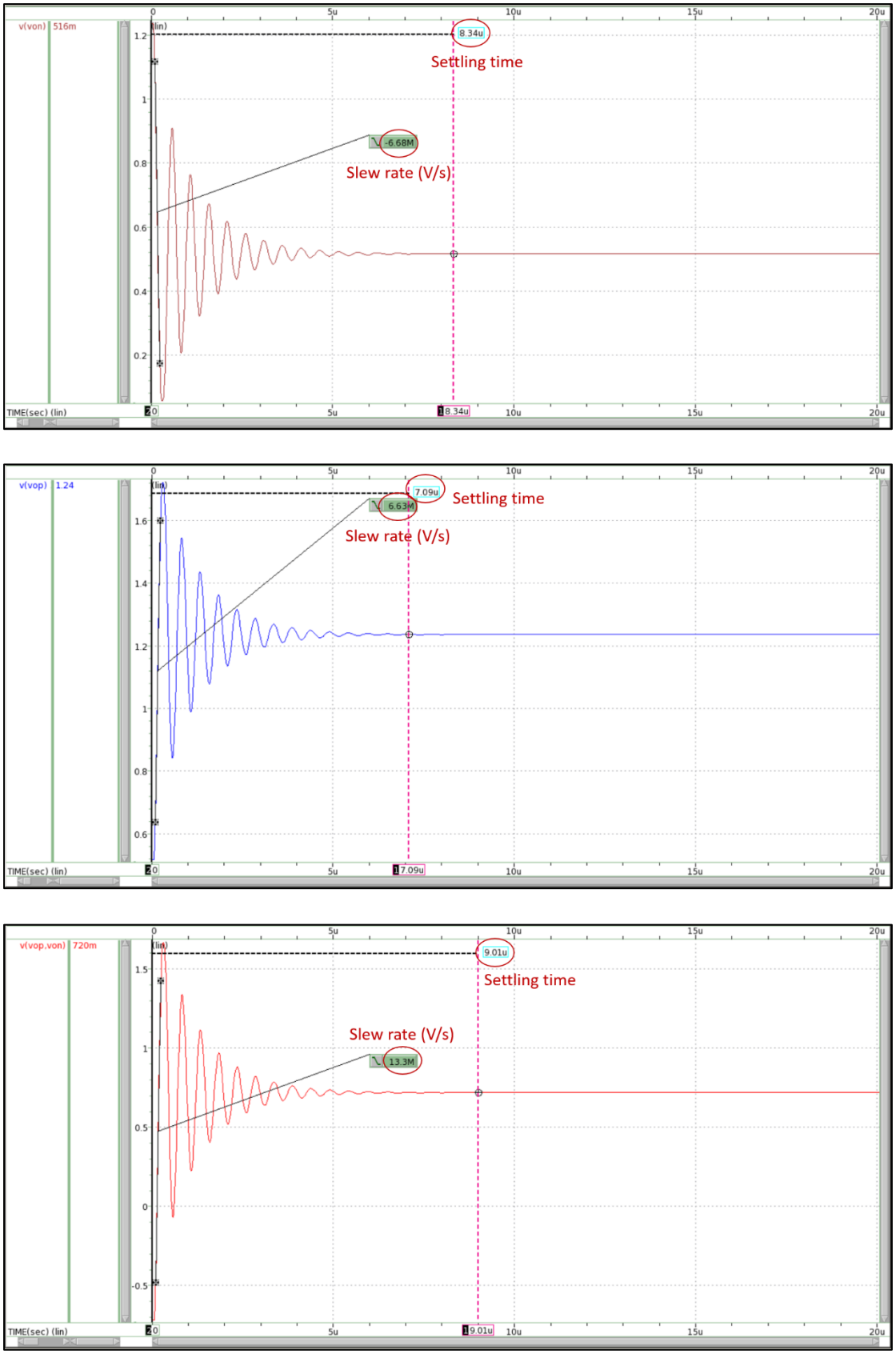


Fig. 3.9(c) Slew rate & settling time

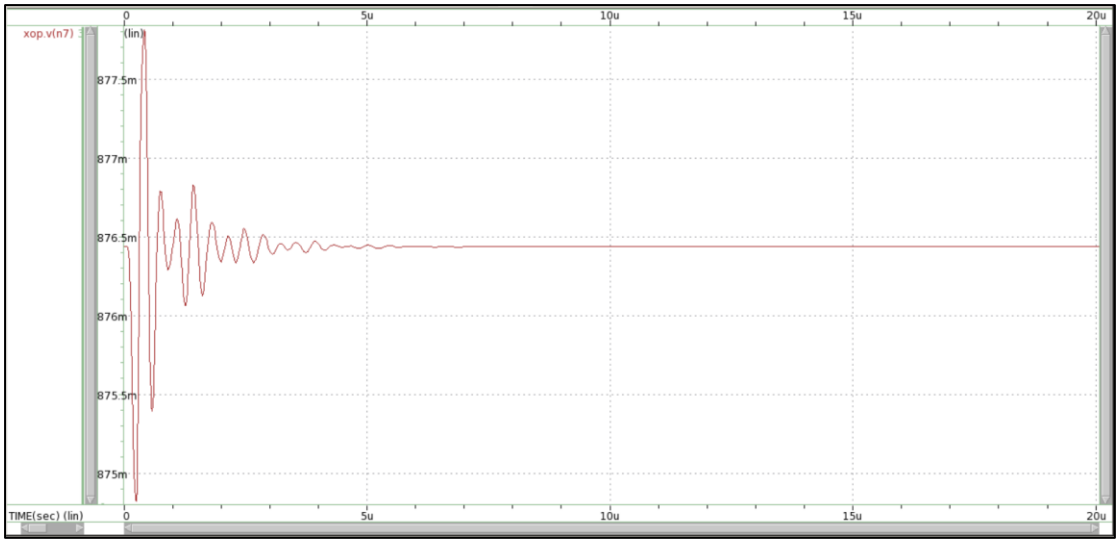


Fig. 3.9(d) Common mode sensing node waveform

<Dis. 3.9(e)>

由 Fig. 3.9(c)與 Fig. 3.9(d)我們可以發現，Common mode sensing node 會根據所感應到的 common mode 訊號，與 MF1、MF3 的訊號相比後進行調整，並將結果回傳給 M3 與 M4 的 gate，透過此 CMFB 的作用，最終我們將會得到一個穩定的 common mode voltage。

3.10 Closed-loop step- response

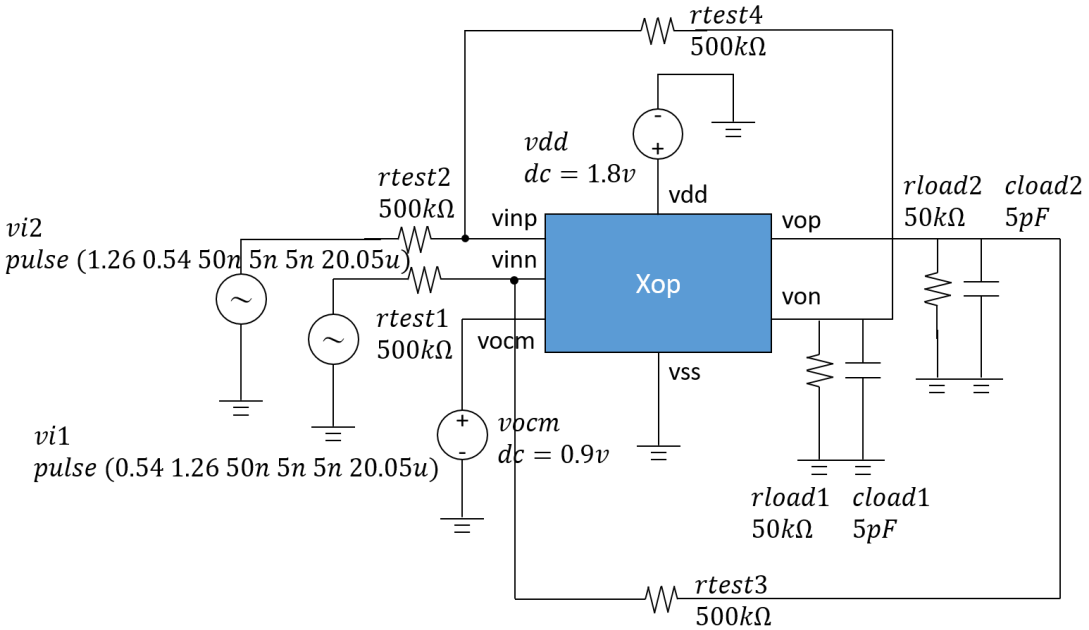


Fig. 3.10(a) Test circuit of 3.10

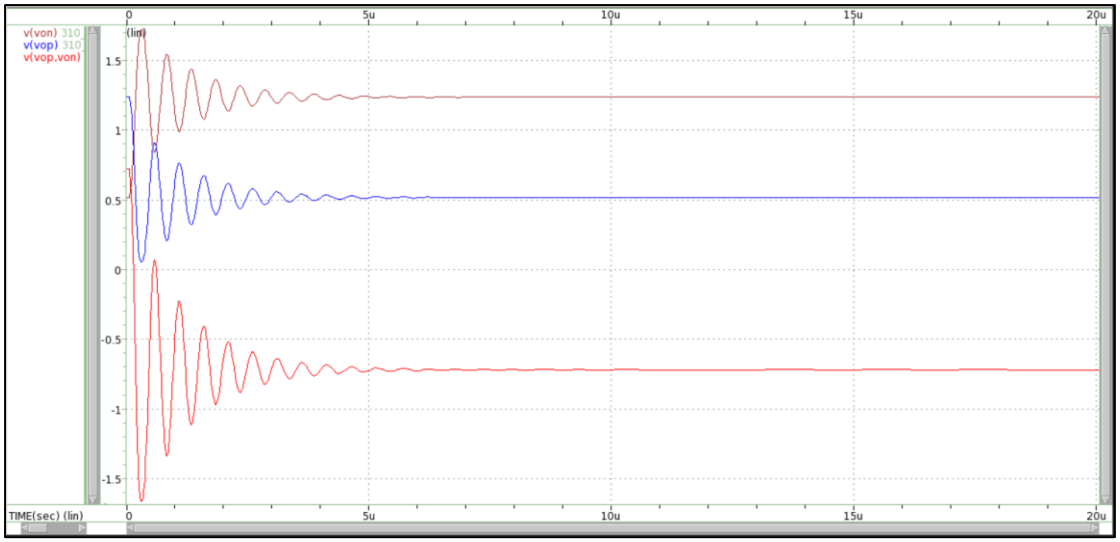
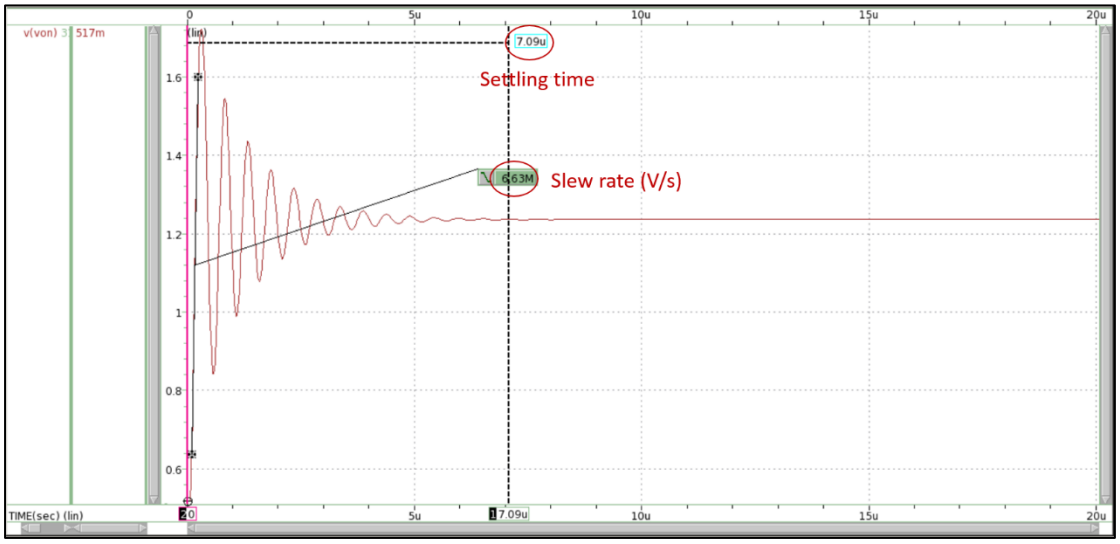
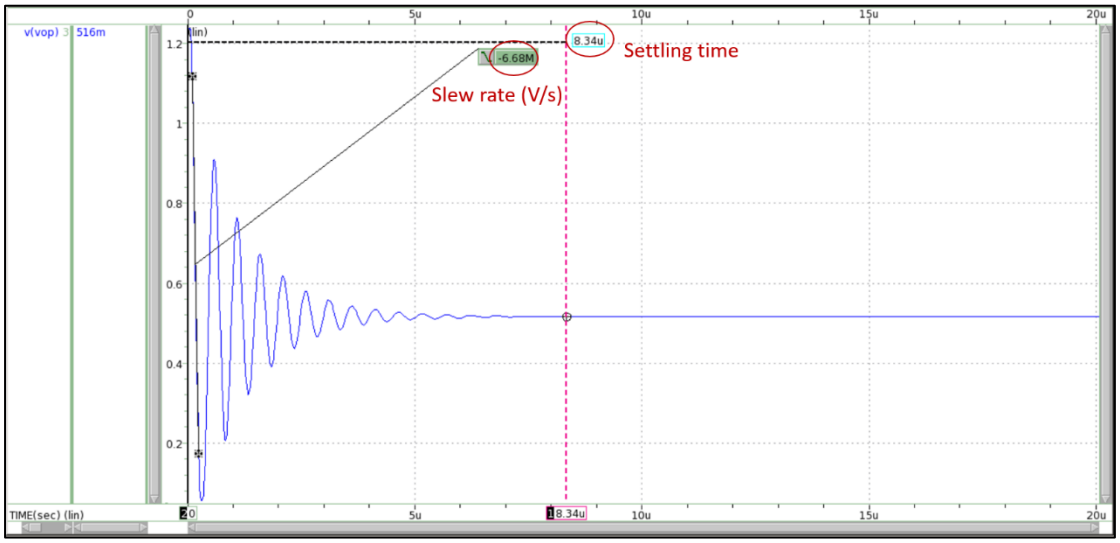


Fig. 3.10(b) Single-ended and differential outputs for -1.44V differential step inputs





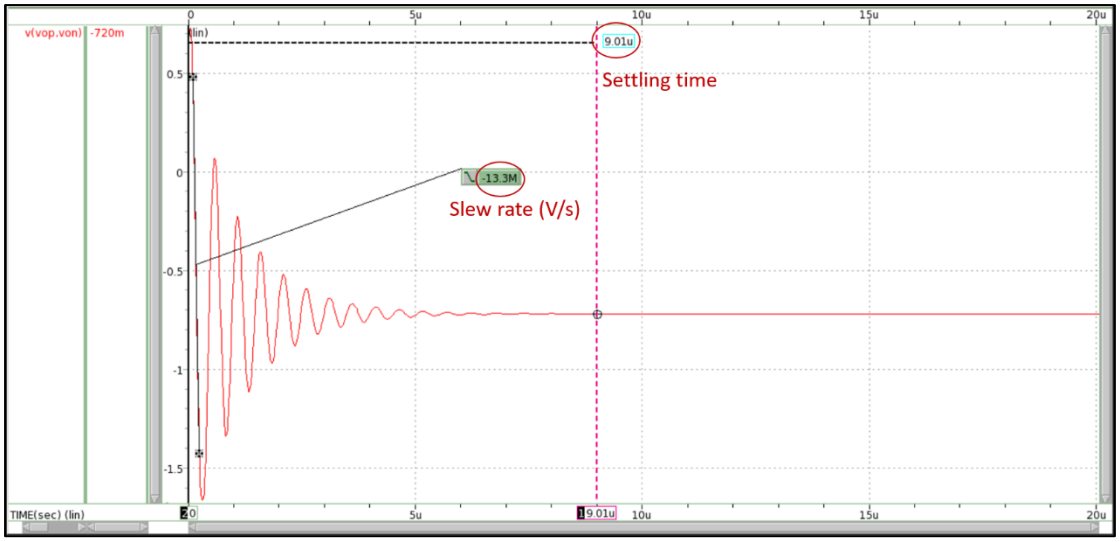


Fig. 3.10(c) Slew rate & settling time

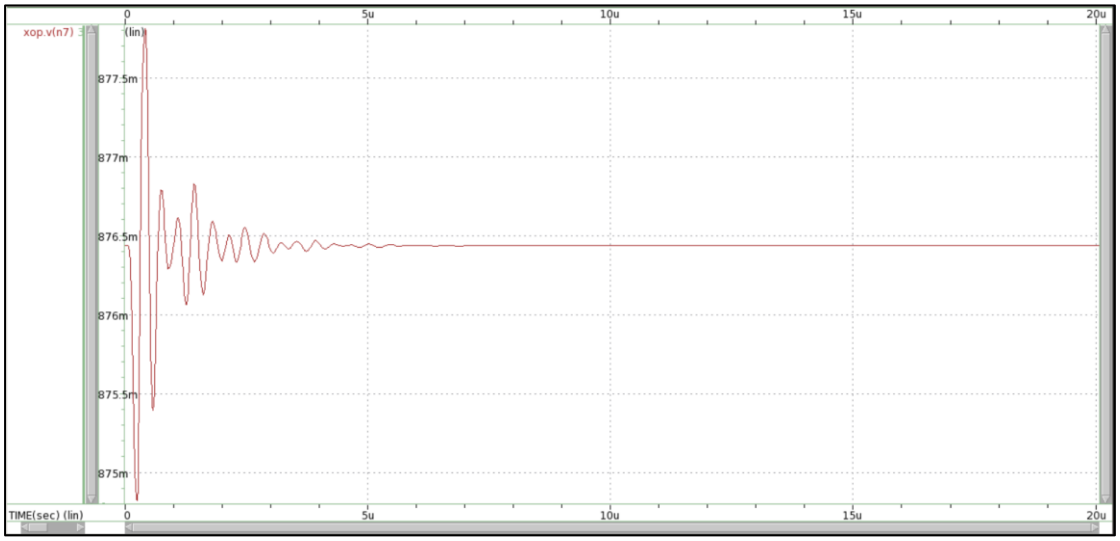


Fig. 3.10(d) Common mode sensing node waveform

IV. Performance Table

Design Items	Specifications	My work
Technology	CIC pseudo 0.18um technology	
Supply Voltage	1.8V, as small as possible	1.8V
Vicm, Vocm	0.9V/0.9V	0.9V/0.9V
Supply Current (Total)	<4mA, as small as possible	1.6475mA
Loading	5pF/50kΩ(for each output)	5pF/50kΩ
Compensation R,C	Open for design	500Ω/6pF
Open-loop simulations		
DC gain	>72dB, as large as possible	72.8230dB
Unity-GBW	>1MHz, as large as possible	32.3093MHz
P.M.	$>45^{\circ}$	77.4706°
C.M.R.R @10KHz	>80dB	99.7219dB
P.S.R.R+ @10KHz	>80dB	102.8836dB
P.S.R.R- @10KHz	>80dB	104.2797dB
Closed-loop simulation		
Differential swing of 1.44V(step signal)		
S.R.+ (10%~90%)	$>1\ ^{V}/_{us}$	$13.3^{V}/_{us}$
S.R.- (90%~10%)	$>1\ ^{V}/_{us}$	$13.3^{V}/_{us}$
Settling+ (to 0.1%)	<10us	9.0062us
Settling- (to 0.1%)	<10us	9.0062us
FoM		
Small signal	GBW(MHz)*CL(pF)/Power(mW)	54.475299
Large signal +	SR+ ($^{V}/_{us}$)*CL(pF)/Power(mW)	22.424549
Large signal -	SR- ($^{V}/_{us}$)*CL(pF)/Power(mW)	22.424549

V. Design Concerns

這次 project 有較多的 spec 要求，在調整 MOS 規格時，需要同時考慮不同的 spec 是否都有符合規定。

<Bias Circuit>:

一開始在調整 Bias Circuit 時，我先將R_b拔掉，接上一個測試電流源，當所有 MOSFET 調整到 Saturation region 後，再透過I_d公式將R_b數值求出，這樣能避免我因為調整R_b大小，而改變到 MOSFET 的 saturation 狀態。

<Amplifier Circuit>:

設計 Amplifier Circuit，主要需要調整 size 使其 gain 達到 spec 要求的 72dB，其中將 M1 跟 M2 的$\left(\frac{W}{L}\right)ratio$提高、或是將 M3、M4 的$\left(\frac{W}{L}\right)ratio$降低，都可以使 gain 增加。另外 RCM1 與 RCM2 則需要設計一個較大的電阻，這樣才能確保 Feedback 能有效的進行回授。

<Feedback Circuit>:

在 Feedback Circuit 中，由於 MF1 是接上不變的v_{ocm}，因此 MF1 與 MF5 較容易因為調整其他參數而離開 saturation 狀態，所以在選擇這兩個 MOSFET 的 size 時需要特別注意。

<Spec concern>

在這次的設計中，我發現 Phase margin 與 Settling time 是較難達到的兩個規定。當我在調整數值以達到較高的 gain 時，往往 phase margin 就會隨之下降，雖然我們可以利用增加C_c的方法來增加 phase margin，但是會伴隨著 Unity-gain frequency 下降的問題，因此在選擇C_c時需要特別小心。而 Settling time 的部分，我發現微調一點點數值，Settling time 就會有較大的變化，且 Settling time 與數據調大調小並沒有絕對的關係，例如在某一 size 附近，先微微調大 MOS 的 size，此時 settling time 可能會減少，但如果我繼續調大他的 size，此時 settling time 可能反而會上升，因此我試了幾次才成功調到符合規定的規格。

VI. Discussions

這次 Final project 有非常多的參數可以讓我們設計，一開始要調整到使每個 MOSFET 都進入 saturation 狀態就花了我不少功夫，而在全部調整完後，感謝助教提供的.sp 檔，使我在作圖上快上許多。這次的電路共有三部分，分析時難度提高了不少，為了縮減分析的難度，有些影響因素我就沒有考慮，因為如此，所以有些數值算出來誤差也較大。透過這次的 project，我發現我對於 feedback 電路還不是很熟悉，因此在分析時常常卡了許久不知從何下手，甚至使用了較差的分析方法，期許自己之後能夠更加理解 feedback 的運作機制。

這學期的 AIC 課程，使我對於類比電路的操作與相關應用有了初步的了解，藉由 7 次作業，也讓我認識與學會基礎的 Hspice 操作，但有時候會覺得作業內容與老師該周所教的課程部分不是十分相關，我會建議另外出一些與該周相關的題目，這樣能使我們對於上課的內容更加理解，最後特別謝謝助教們總是不厭其煩地為我講解作業問題。