Analog Integrated Circuit Design _ Final Project

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Design Items	Specifications	My Work
Technology	CIC pseudo 0.18um technology	
Supply Voltage	**1.8V**, as small as possible	1.8V
Vicm, Vocm	**0.9V / 0.9V**	0.9V / 0.9V
Supply Current (Total)	**< 4mA**, as small as possible	-224.22u
Loading	**5pF / 50KΩ (for each output)**	5pF / 50KΩ
Compensation R, C	Open for design	35KΩ / 1pF
Open-loop simulation		
DC gain	**> 72dB**, as large a possible	74.32 dB
Unity-GBW	**> 1MHz**, as large as possible	18.81 MHz
P.M.	**> 45°**	55.5493
C.M.R.R. @10KHz	> 80dB	112.1 dB
P.S.R.R.+ @10KHz	> 80dB	112.5 dB
P.S.R.R.- @10KHz	> 80dB	116.8 dB
Closed-loop simulation		
Differential swing of 1.44V (step signal)		
S.R.+ (10% ~ 90%)	> 1 V/us	3.8 V/us
S.R.- (10% ~ 90%)	> 1 V/us	3.8 V/us
Settling+ (to 0.1%)	< 10 us	9.41 u
Settling- (to 0.1%)	< 10 us	9.41 u
FoM		
Small signal	GBW (MHz) * CL (pF) / Power(mW)	233.03
Large signal +	SR+(V/us) * CL (pF) / Power(mW)	47.08
Large signal -	SR-(V/us) * CL (pF) / Power(mW)	47.08

1. Schematic

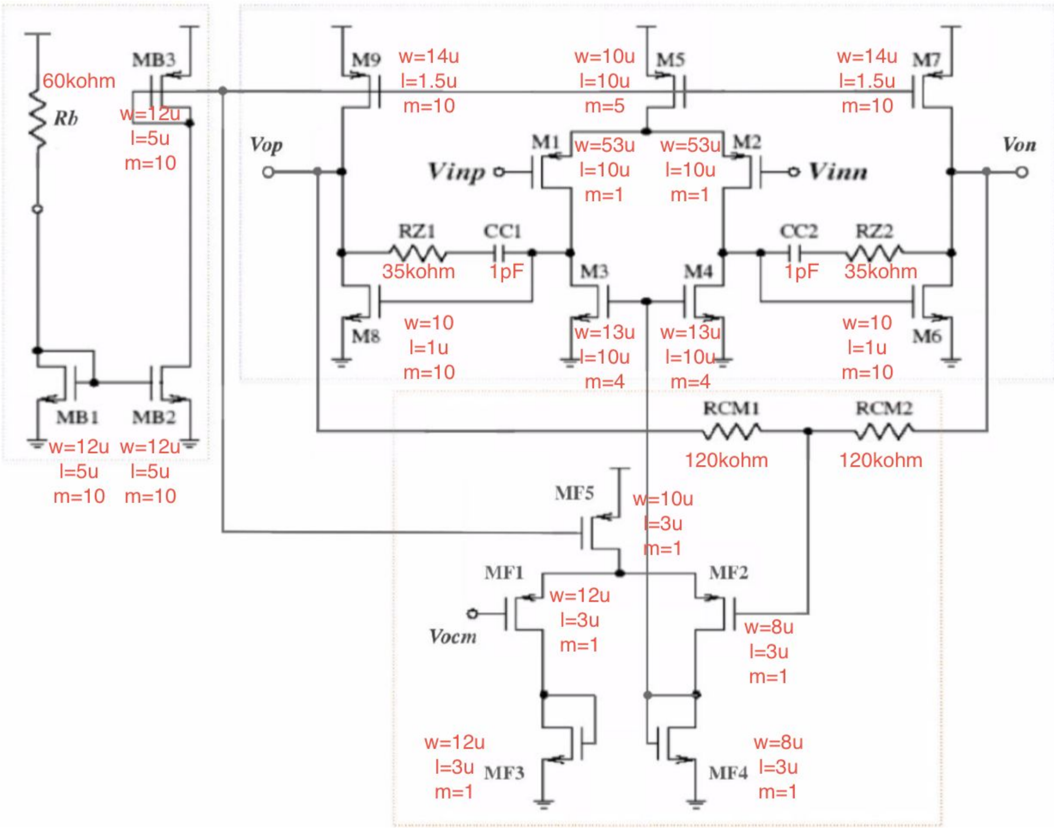

Fig. 1(a) active device size and passive component value

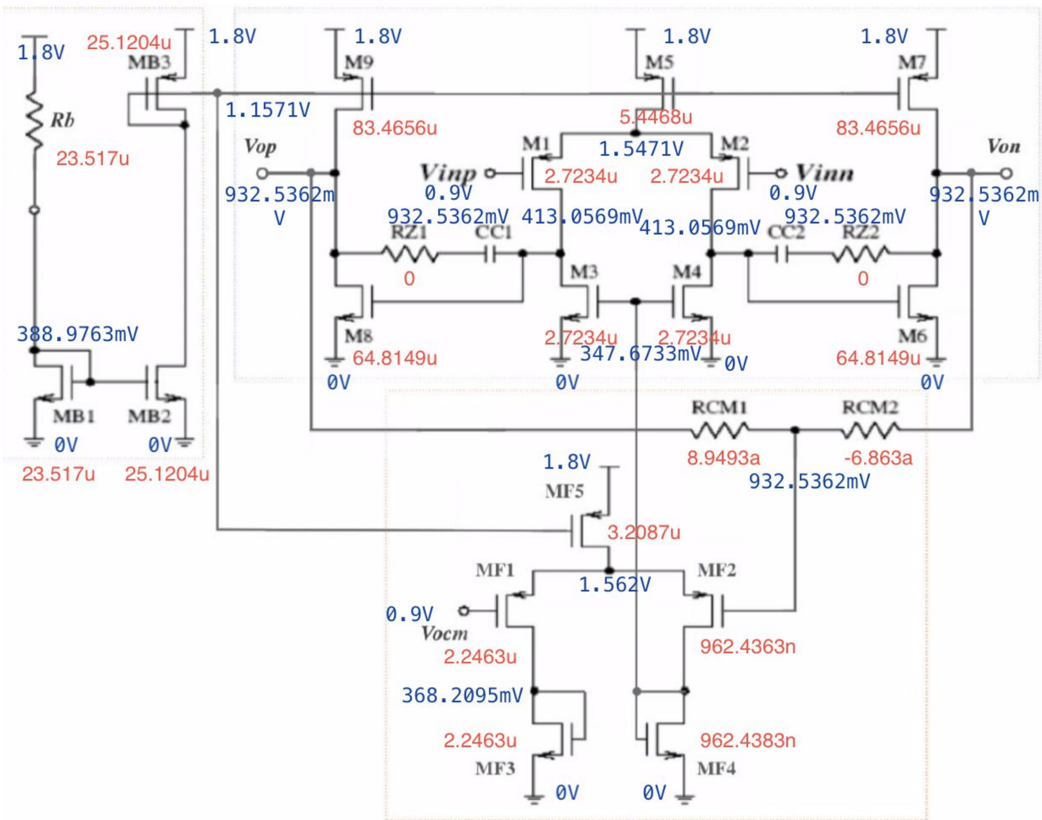

Fig. 1(b) Each node voltage and branch current

subckt	xop	xop	xop	xop	xop	xop
element	1:m1	1:m2	1:m3	1:m4	1:m5	1:m6
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	2.7234u	2.7234u	2.7234u	2.7234u	5.4468u	64.8149u
ibs	3.2776f	3.2776f	-4.312e-22	-4.312e-22	608.8452a	-1.049e-20
ibd	597.6495a	597.6495a	-1.6350f	-1.6350f	5.455e-22	-7.2551f
vgs	486.9431m	486.9431m	347.6733m	347.6733m	-390.0284m	413.0569m
vds	1.1340	1.1340	413.0569m	413.0569m	252.9017m	932.5362m
vbs	1.3869	1.3869	0.	0.	252.9017m	0.
vth	-534.5825m	-534.5825m	317.1202m	317.1202m	-462.1852m	382.8485m
vdsat	-126.0448m	-126.0448m	69.8080m	69.8080m	-171.2001m	76.7574m
vod	-112.5158m	-112.5158m	30.5531m	30.5531m	-180.7450m	30.2084m
beta	368.6994u	368.6994u	1.5431m	1.5431m	355.1377u	31.0478m
gam eff	555.3506m	555.3506m	507.4459m	507.4459m	557.0847m	507.4460m
gm	35.1338u	35.1338u	53.9851u	53.9851u	50.9218u	1.2474m
gds	11.4444n	11.4444n	180.5556n	180.5556n	818.5108n	13.1502u
gmb	9.7030u	9.7030u	11.1786u	11.1786u	15.8173u	255.8184u
cdtot	3.5981p	3.5981p	74.7044f	74.7044f	3.5642p	128.1937f
cgtot	3.2803p	3.2803p	2.7983p	2.7983p	3.2319p	576.9051f
cstot	54.9342f	54.9342f	2.6841p	2.6841p	164.8826f	622.6395f
cbtot	1.1074p	1.1074p	1.0245p	1.0245p	1.1821p	369.1207f
cgs	19.1527f	19.1527f	2.3381p	2.3381p	64.1233f	460.9226f
cgd	2.9919p	2.9919p	16.8903f	16.8903f	2.9249p	36.2352f

List. 1-1 small signal parameters in .lis file (part1)

subckt	xop	xop	xop	xop	xop	xop
element	1:m7	1:m8	1:m9	1:mb1	1:mb2	1:mb3
model	0:p_18.1	0:n_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	83.4656u	64.8149u	83.4656u	23.5170u	25.1204u	25.1204u
ibs	5.6951f	-1.049e-20	5.6951f	-3.746e-21	-4.002e-21	3.6583f
ibd	8.141e-21	-7.2551f	8.141e-21	-3.5749f	-10.6339f	2.478e-21
vgs	224.5336m	413.0569m	224.5336m	388.9793m	388.9793m	0.
vds	867.4638m	932.5362m	867.4638m	388.9793m	1.1571	642.9302m
vbs	867.4638m	0.	867.4638m	0.	0.	642.9302m
vth	-488.3153m	382.8485m	-488.3153m	325.6876m	323.3081m	-468.2571m
vdsat	-158.0686m	76.7574m	-158.0686m	87.4768m	88.8165m	-167.7474m
vod	-154.6149m	30.2084m	-154.6149m	63.2917m	65.6711m	-174.6731m
beta	6.6147m	31.0478m	6.6147m	7.1737m	7.1723m	1.7041m
gam eff	557.0846m	507.4460m	557.0846m	507.4459m	507.4459m	557.0847m
gm	878.4099u	1.2474m	878.4099u	401.9397u	423.4070u	243.2761u
gds	2.4072u	13.1502u	2.4072u	2.1712u	2.1058u	310.2243n
gmb	269.2899u	255.8184u	269.2899u	82.4058u	85.5970u	75.4036u
cdtot	1.5511p	128.1937f	1.5511p	173.9879f	149.0597f	4.3135p
cgtot	1.3506p	576.9051f	1.3506p	3.7122p	3.7263p	3.8339p
cstot	156.0117f	622.6395f	156.0117f	3.7782p	3.8010p	142.5848f
cbtot	661.1329f	369.1207f	661.1329f	1.3061p	1.2850p	1.4882p
cgs	50.3778f	460.9226f	50.3778f	3.2707p	3.2821p	44.7227f
cgd	1.2018p	36.2352f	1.2018p	40.3776f	38.4621f	3.4908p

List. 1-2 small signal parameters in .lis file (part2)

subckt	xop	xop	xop	xop	xop
element	1:mf1	1:mf2	1:mf3	1:mf4	1:mf5
model	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati
id	2.2463u	962.4363n	2.2463u	962.4383n	3.2087u
ibs	814.7000a	572.1702a	-3.578e-22	-1.594e-22	114.6058a
ibd	135.4383a	93.7743a	-338.3989a	-221.4538a	3.213e-22
vgs	531.7905m	584.8630m	368.2095m	347.6733m	-404.9053m
vds	1.1938	1.2143	368.2095m	347.6733m	238.0249m
vbs	1.4318	1.4523	0.	0.	238.0249m
vth	-544.1698m	-544.2165m	336.7759m	337.6572m	-475.7465m
vdsat	-132.4385m	-110.7203m	72.1517m	62.6320m	-164.0167m
vod	-117.8053m	-85.2224m	31.4336m	10.0161m	-167.1837m
beta	273.9905u	183.1022u	1.2022m	800.3696u	235.7004u
gam eff	555.4471m	555.4471m	507.4459m	507.4459m	557.0847m
gm	28.0976u	14.0259u	44.0542u	20.4779u	31.6605u
gds	28.5847n	12.8750n	302.6780n	139.0773n	649.7072n
gmb	7.8146u	3.8888u	9.1298u	4.2679u	9.8103u
cdtot	248.8767f	159.3236f	17.1845f	11.5168f	216.4340f
cgtot	225.1971f	145.5780f	198.9607f	113.2476f	194.6943f
cstot	12.4212f	8.2995f	196.9800f	104.9343f	18.4462f
cbtot	86.1989f	57.5405f	87.9876f	58.5429f	81.8943f
cgs	4.3124f	2.8732f	165.2078f	86.3007f	6.0926f
cgd	203.7942f	129.9254f	4.2079f	2.8684f	174.7737f

List. 1-3 small signal parameters in .lis file (part3)

2. Spice Code

```
.param vdd=1.8V          $Your positive supply voltage
.param vss=0V            $Your negative supply voltage
.param vocm=0.9V         $Your output common mode voltage (for CMFB)

.subckt op vinp vinn vdd vss vop von vocm

*** First stage ***

M1 M1_M2_M5 vinp M1_M3 vdd      p_18 w=53u l=10u m=1
M2 M1_M2_M5 vinn M2_M4 vdd      p_18 w=53u l=10u m=1
M3 M1_M3 M3_M4_feed vss vss     n_18 w=13u l=10u m=4
M4 M2_M4 M3_M4_feed vss vss     n_18 w=13u l=10u m=4
M5 vdd cross M1_M2_M5 vdd       p_18 w=10u l=10u m=5

*** Second stage ***

M6 von M2_M4 vss vss            n_18 w=10u l=1u m=10
M7 vdd cross von vdd            p_18 w=14u l=1.5u m=10
M8 vop M1_M3 vss vss            n_18 w=10u l=1u m=10
M9 vdd cross vop vdd            p_18 w=14u l=1.5u m=10

*** Compensation ***

RZ1 vop RZ1_CC1 35k
RZ2 von RZ2_CC2 35k
CC1 M1_M3 RZ1_CC1 1p
CC2 M2_M4 RZ2_CC2 1p

*** Bias Circuit ***

Rb MB1_MB2 vdd 60k
MB1 MB1_MB2 MB1_MB2 vss vss     n_18 w=12u l=5u m=10
MB2 cross MB1_MB2 vss vss       n_18 w=12u l=5u m=10
MB3 vdd cross cross vdd         p_18 w=12u l=5u m=10

*** Feedback Circuit ***

RCM1 RCM1_RCM2 vop 120k
RCM2 RCM1_RCM2 von 120k
MF1 MF1_MF2_MF5 vocm MF1_MF3 vdd                p_18 w=12u l=3u m=1
MF2 MF1_MF2_MF5 RCM1_RCM2 M3_M4_feed vdd        p_18 w=8u l=3u m=1
MF3 MF1_MF3 MF1_MF3 vss vss                     n_18 w=12u l=3u m=1
MF4 M3_M4_feed M3_M4_feed vss vss               n_18 w=8u l=3u m=1
MF5 vdd cross MF1_MF2_MF5 vdd                   p_18 w=10u l=3u m=1

.ends
```

Fig. 2 Spice code (op.sp)

3. Simulations

3.1 Open-loop differential mode AC response

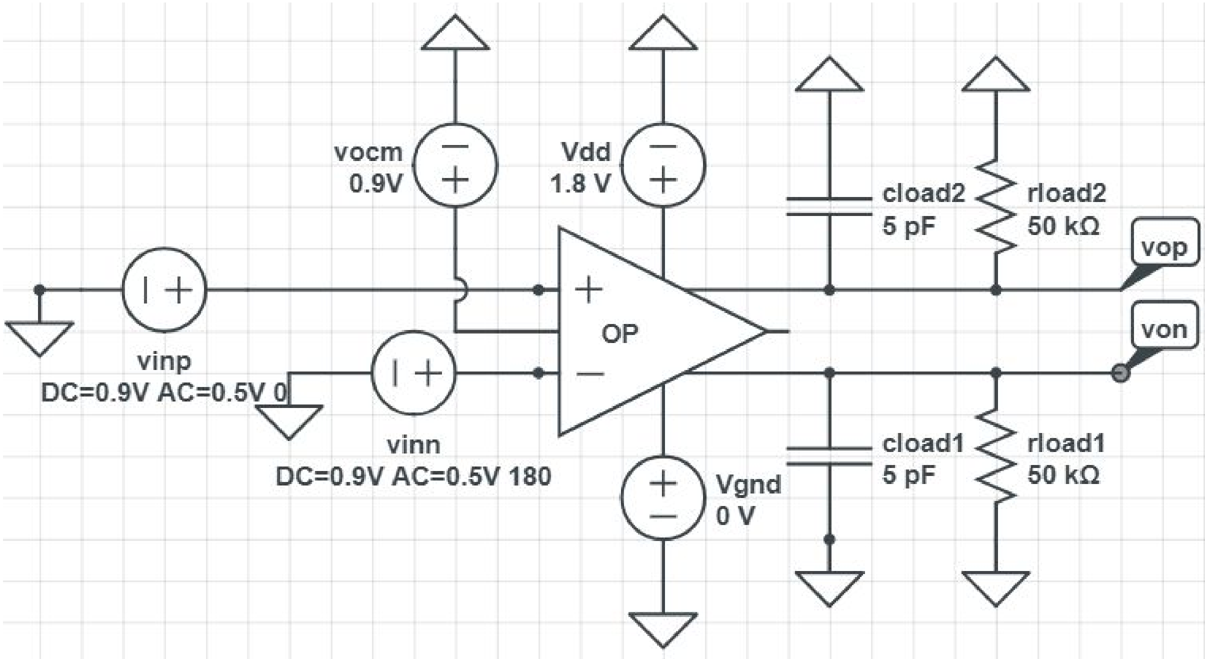

Fig. 3.1(a)

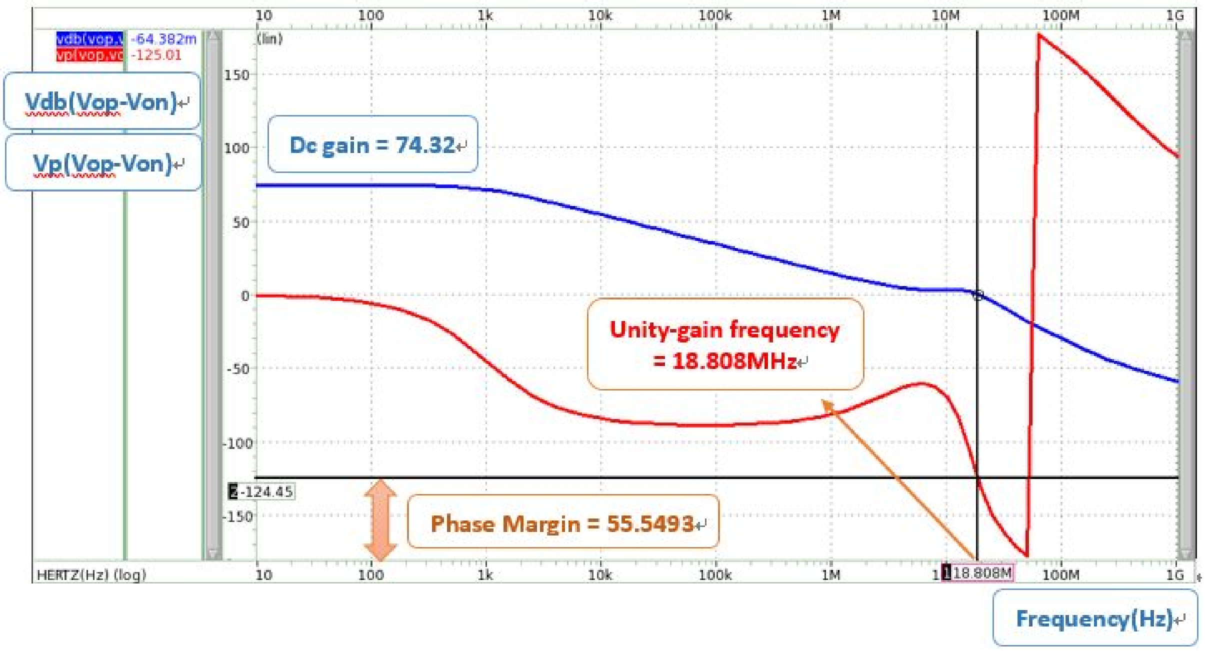

Fig. 3.1(b)

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**************************************************
  ******   pole/zero analysis


   input =  0:vinn          output = v(vop,von)

Output first 10 Poles, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      poles (rad/sec)              poles ( hertz)
real            imag            real            imag
-6.15619k       0.              -979.787        0.
-2.56440x       -8.88054x       -408.137k       -1.41338x
-2.56440x       8.88054x        -408.137k       1.41338x
-12.1461x       0.              -1.93312x       0.
-23.9576x       0.              -3.81297x       0.
-47.2717x       90.8016x        -7.52352x       14.4515x
-47.2717x       -90.8016x       -7.52352x       -14.4515x
-48.0077x       -88.4583x       -7.64066x       -14.0786x
-48.0077x       88.4583x        -7.64066x       14.0786x
-56.3974x       0.              -8.97593x       0.

Output first 10 Zeros, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      zeros (rad/sec)              zeros ( hertz)
real            imag            real            imag
-2.62538x       8.96222x        -417.843k       1.42638x
-2.62538x       -8.96222x       -417.843k       -1.42638x
-12.3477x       0.              -1.96520x       0.
-24.2303x       0.              -3.85637x       0.
-28.7640x       0.              -4.57793x       0.
-48.1891x       -88.3511x       -7.66954x       -14.0615x
-48.1891x       88.3511x        -7.66954x       14.0615x
-56.3956x       0.              -8.97565x       0.
-115.426x       0.              -18.3707x       0.
-167.845x       0.              -26.7133x       0.

 ***** constant factor = 286.872m
```

Fig. 3.1(c)

Dis. 3.1(d) :

gain = $gm3(ro1//ro3) * gm8(ro8//ro9//Rcm2//rload) = 7990$

gain(dB) = 20 * log 7950 = 78.1

$pole\ 1 = \frac{gm1}{2\pi AvCc}$ = -1.08 k

$pole\ 2 = \frac{gm8}{2\pi(Cc1+Cc2)}$ = 9.93 * 10^7

$zero = \frac{1}{2\pi Cc(\frac{1}{gm6}-RZ1)}$ = 930776.04

gain error = $\frac{78.1-74}{78.1} = 8.12\%$

pole1 error = $\frac{1080-979}{1080} = 9.35\%$

pole2 error = $\frac{115.426-99.3}{99.3} = 16.23\%$

zero error = $\frac{1486321-930776.04}{930776.04} = 59.7\%$

zero 都與模擬值有蠻大的誤差，我認為可能是因為有些parasitic capacitance 導致這些誤差，因為這次電路也比較大一些。或者也有可能是公式本身就帶有的誤差，加劇了誤差的情形。

3.2 Open-loop differential mode DC sweep

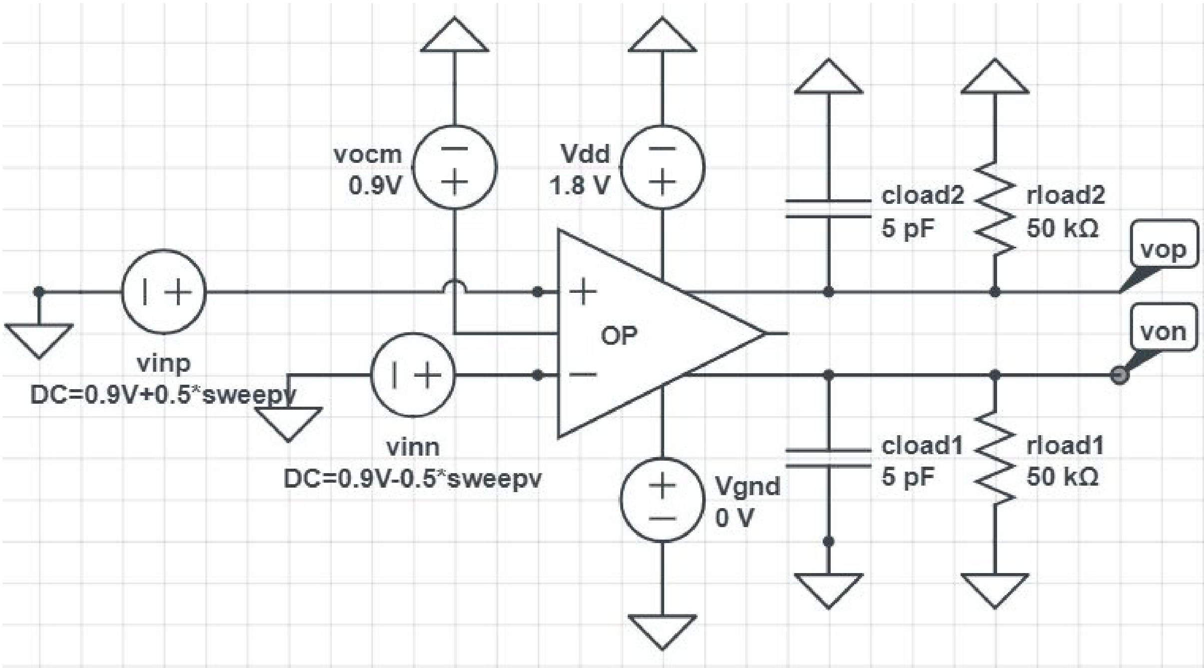

Fig. 3.2(a)

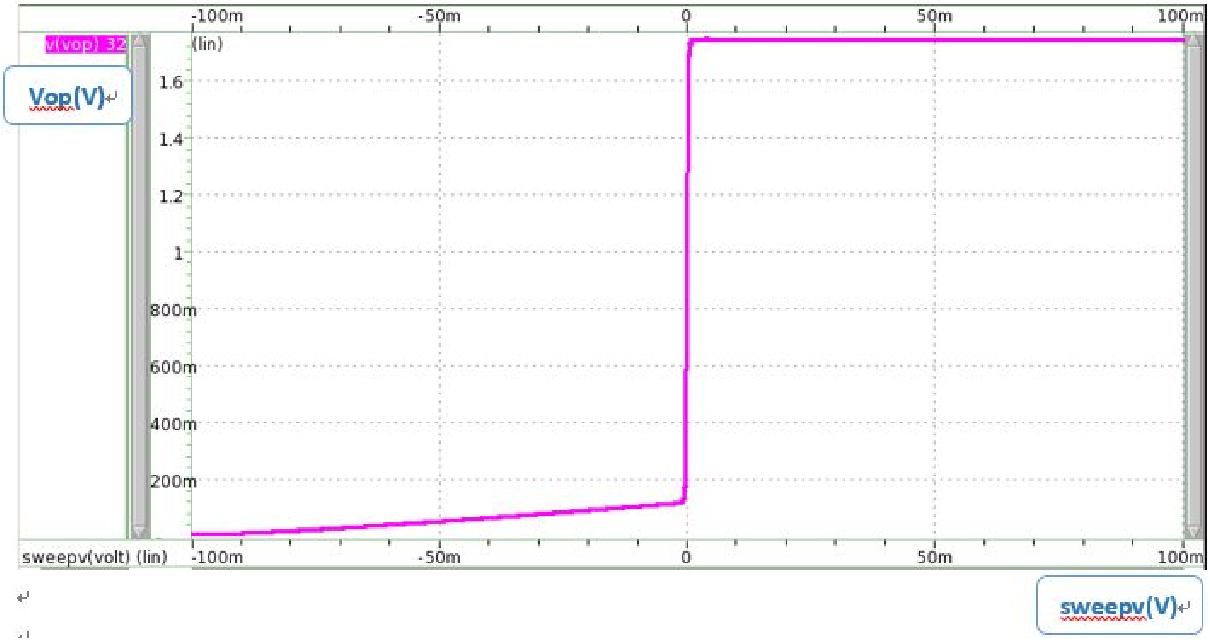

Fig. 3.2(b)-Vop

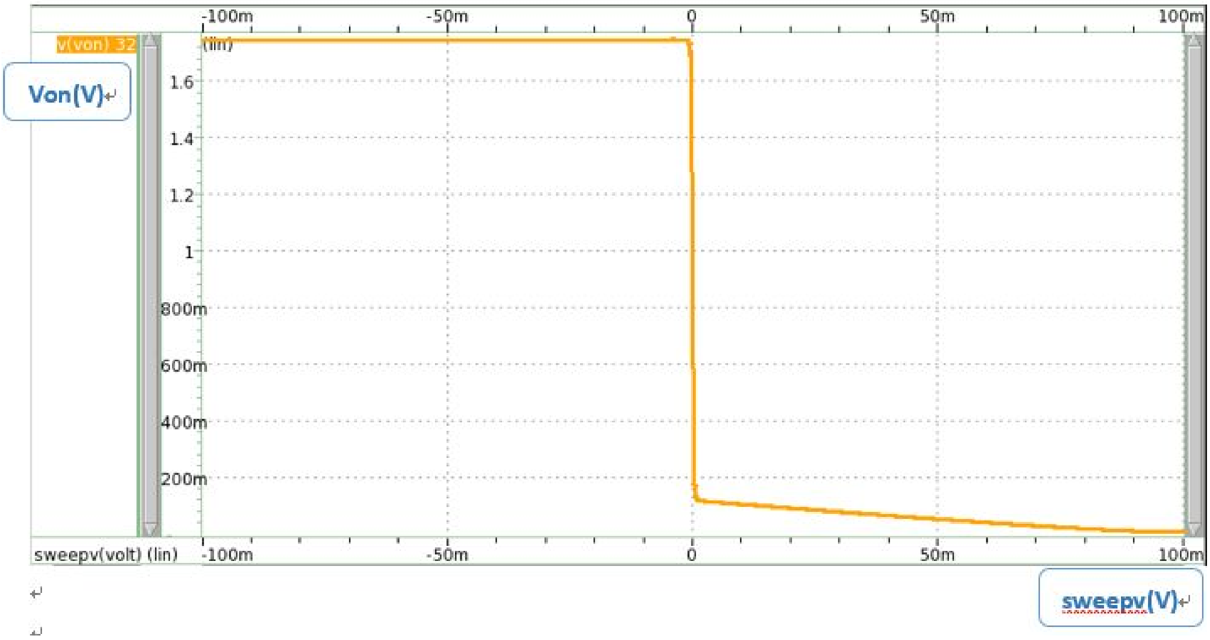

Fig. 3.2(b)-Von

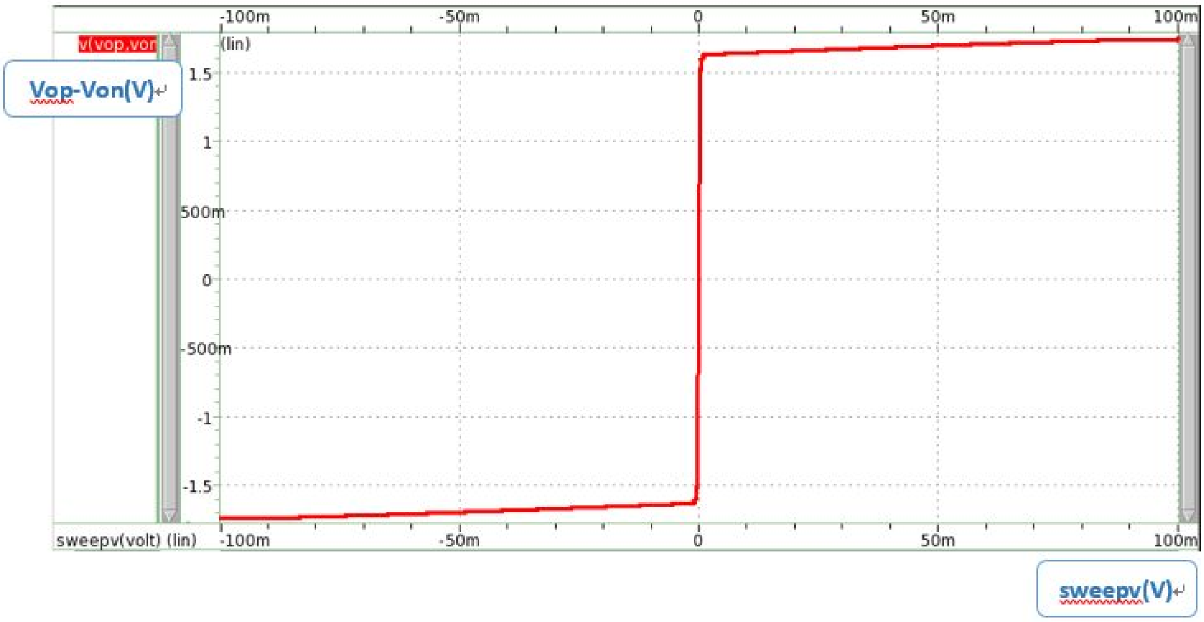

Fig. 3.2(b)-Vop-Von

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:32_dc-dm_v2.sw0	slope(v(von),0)			-2.5999k		
D0:32_dc-dm_v2.sw0	slope(v(vop),0)			2.5999k		
D0:32_dc-dm_v2.sw0	slope(v(vop,von),0)			5.1998k		

Fig. 3.2(b)-slope

3.3 Open-loop differential mode AC response

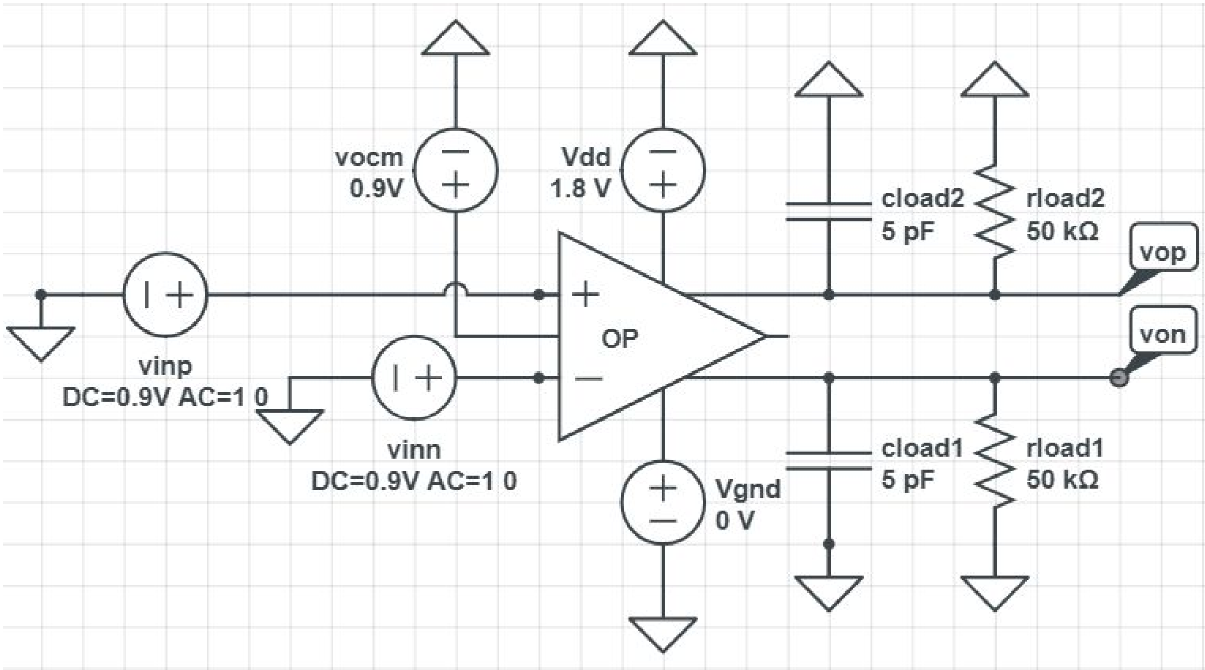

Fig. 3.3(a)

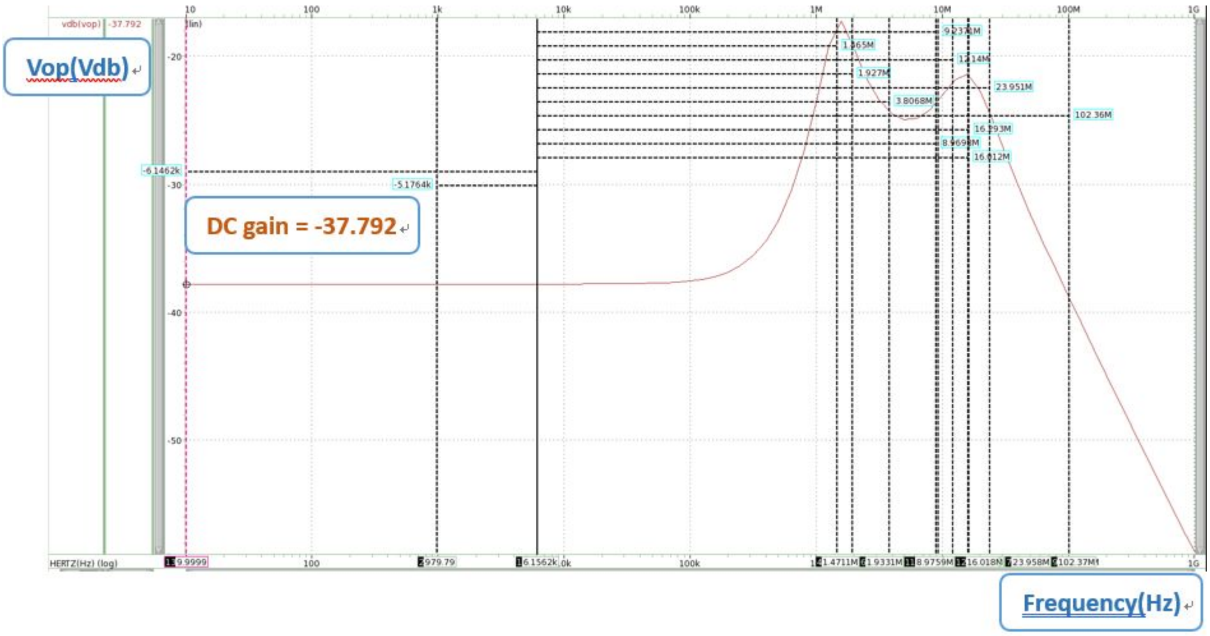

Fig. 3.3(b)-poles

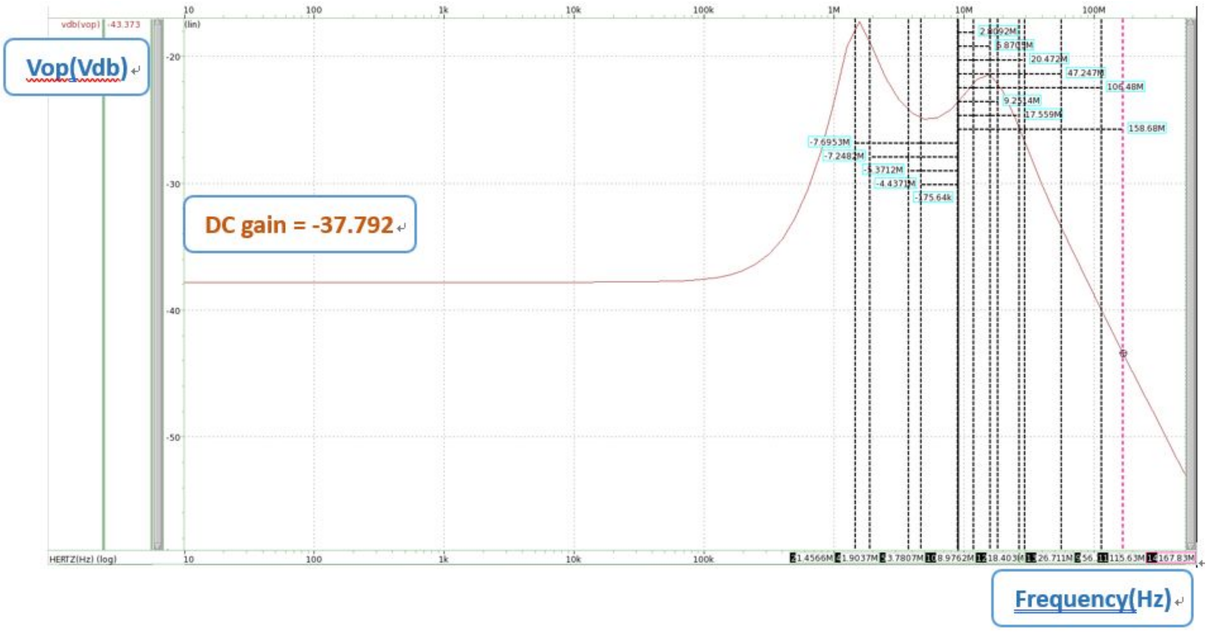

Fig. 3.3(b)-zeros

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****************************************************
  ******   pole/zero analysis


   input =  0:vinp          output = v(vop)

Output first 10 Poles, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      poles (rad/sec)                poles ( hertz)
real             imag              real             imag
-6.15619k        0.                -979.787         0.
-2.56440x        8.88054x          -408.137k        1.41338x
-2.56440x        -8.88054x         -408.137k        -1.41338x
-12.1461x        0.                -1.93312x        0.
-23.9576x        0.                -3.81297x        0.
-47.2717x        90.8016x          -7.52352x        14.4515x
-47.2717x        -90.8016x         -7.52352x        -14.4515x
-48.0077x        88.4583x          -7.64066x        14.0786x
-48.0077x        -88.4583x         -7.64066x        -14.0786x
-56.3974x        0.                -8.97593x        0.

Output first 10 Zeros, (total 13)
Use .option pz_num = NUM to control output number, (default:10)

      zeros (rad/sec)                zeros ( hertz)
real             imag              real             imag
-2.50717x        8.80170x          -399.028k        1.40083x
-2.50717x        -8.80170x         -399.028k        -1.40083x
-11.9610x        0.                -1.90366x        0.
-23.7546x        0.                -3.78066x        0.
-29.6238x        0.                -4.71477x        0.
-47.8578x        -88.5681x         -7.61680x        -14.0961x
-47.8578x        88.5681x          -7.61680x        14.0961x
-56.3990x        0.                -8.97618x        0.
-115.630x        0.                -18.4032x        0.
-167.832x        0.                -26.7113x        0.

 ***** constant factor = 304.689m
```

Fig. 3.3(c)

$$pole\ 1 = \frac{gm1}{2\pi AvCc}$$ = -1.08 k

$$pole\ 2 = \frac{gm8}{2\pi(Cc1+Cc2)}$$ = 9.93 * 10^7

$$zero = \frac{1}{2\pi Cc(\frac{1}{gm6}-RZ1)}$$ = 930776.04

pole1 error = $\frac{1080-979}{1080} = 9.35\%$

pole2 error = $\frac{115.63-99.3}{99.3} = 16.23\%$

zero error = $\frac{1341930-930776.04}{930776.04} = 44.2\%$

這裡的pole 與 zero 應該是要與3-1一樣的，造成不一樣的原因可能跟輸入的訊號不同有關係。

Fig. 3.3(d)

3.4 Open-loop common mode DC sweep

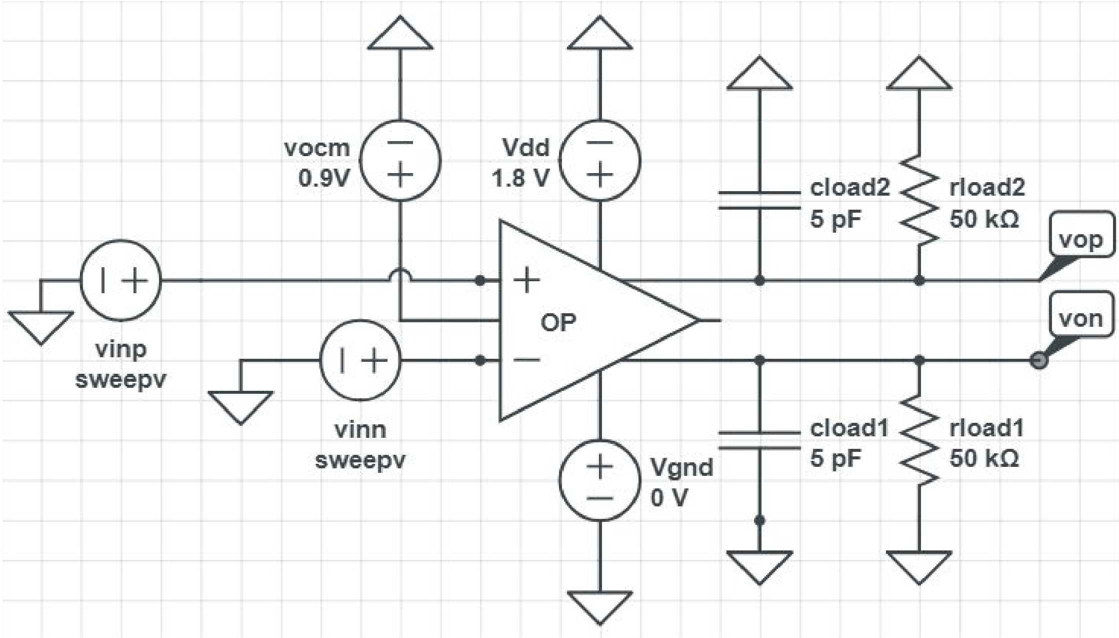

Fig. 3.4(a)

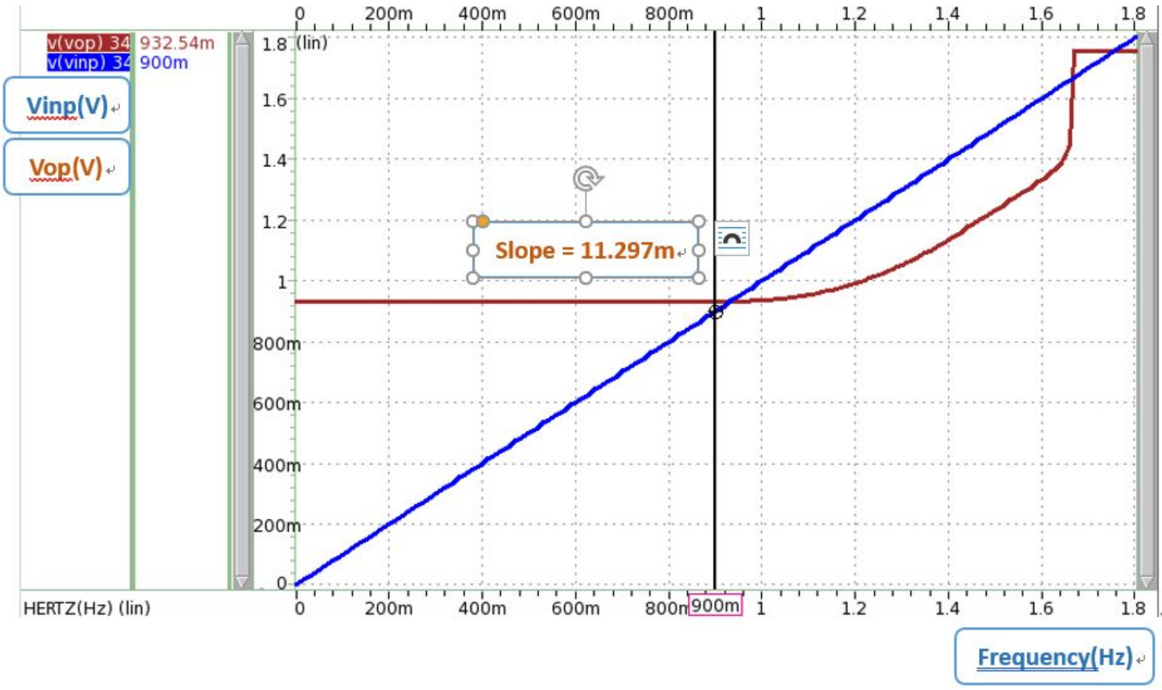

Fig. 3.4(b)

$20 * log11.297m \simeq -38.469$。與上題結果十分接近。

3.5 Open-loop power supply+ AC response

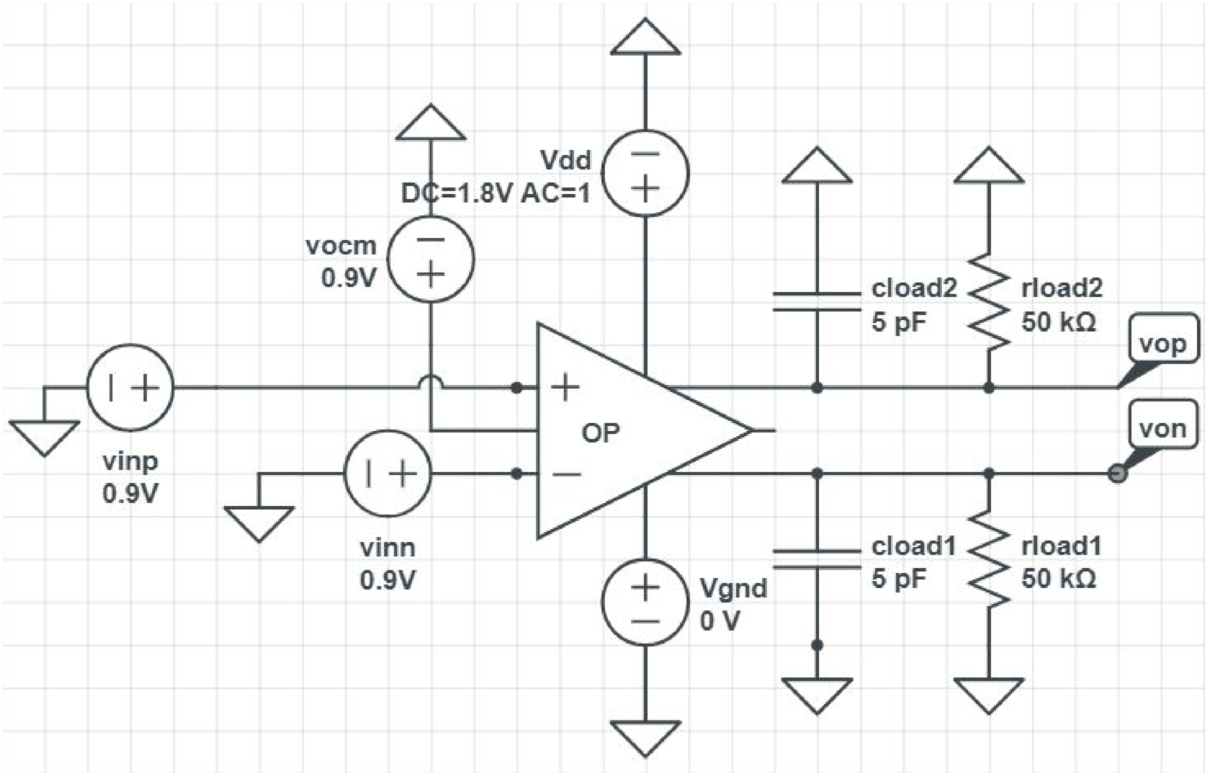

Fig. 3.5(a)

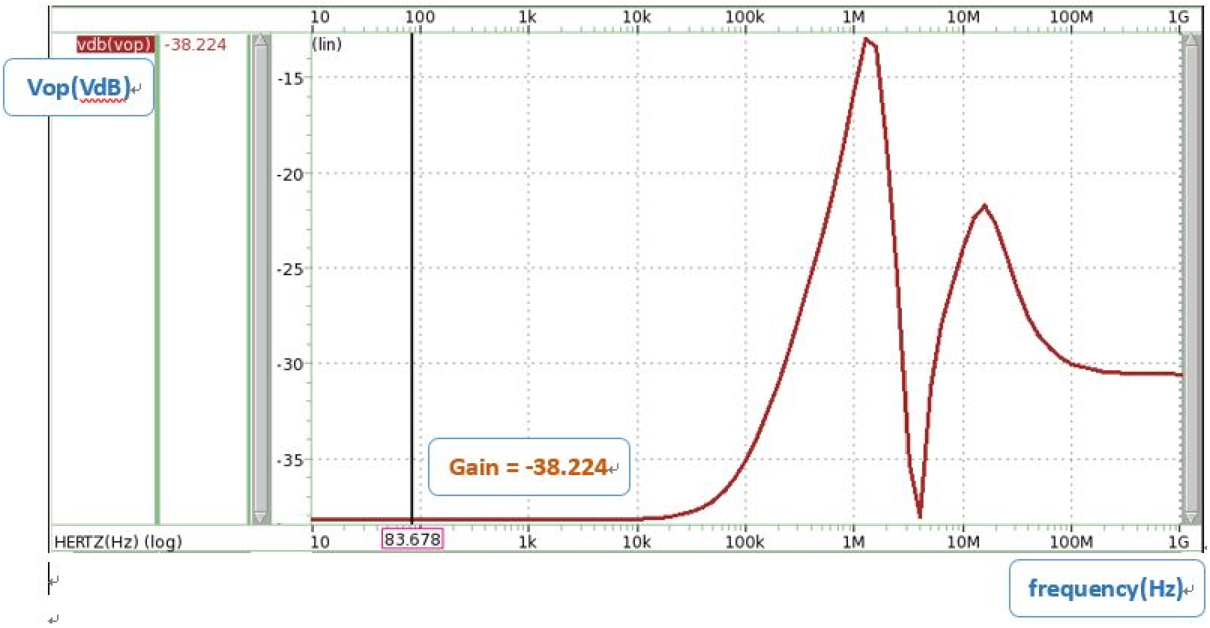

Fig. 3.5(b)

3.6 Open-loop power supply- AC response

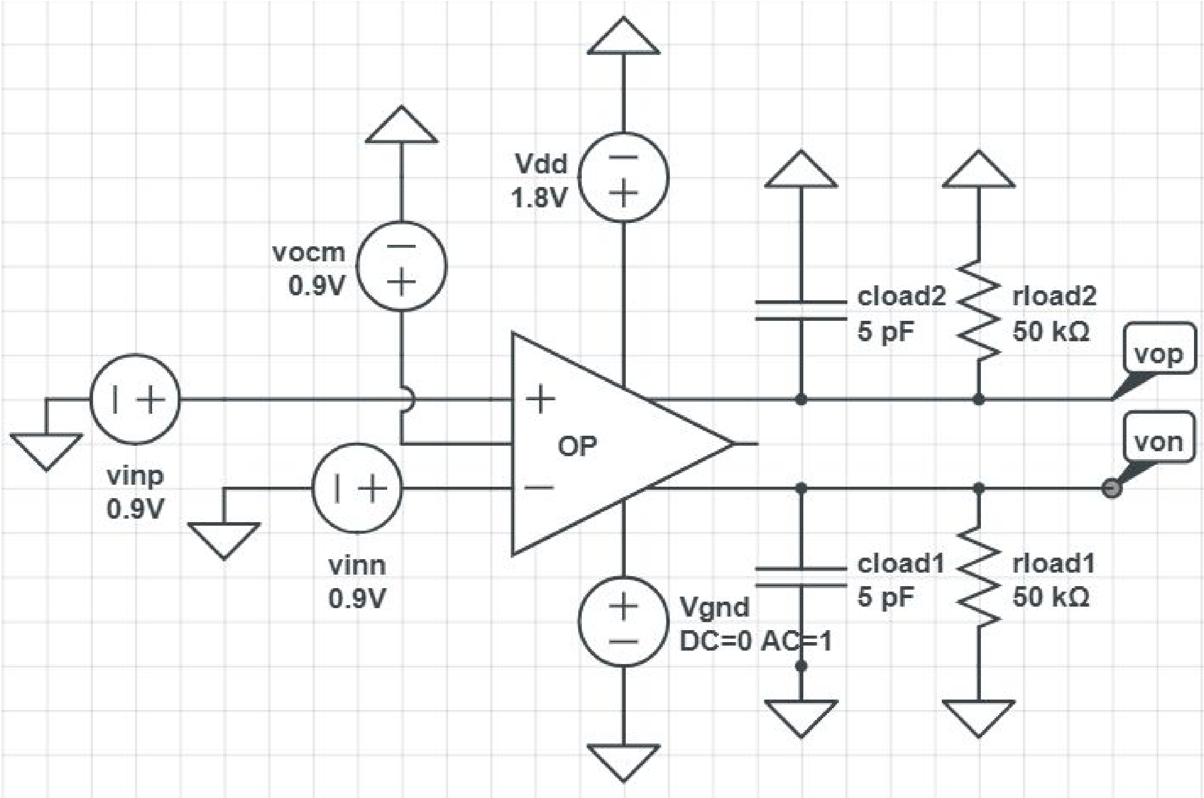

Fig. 3.6(a)

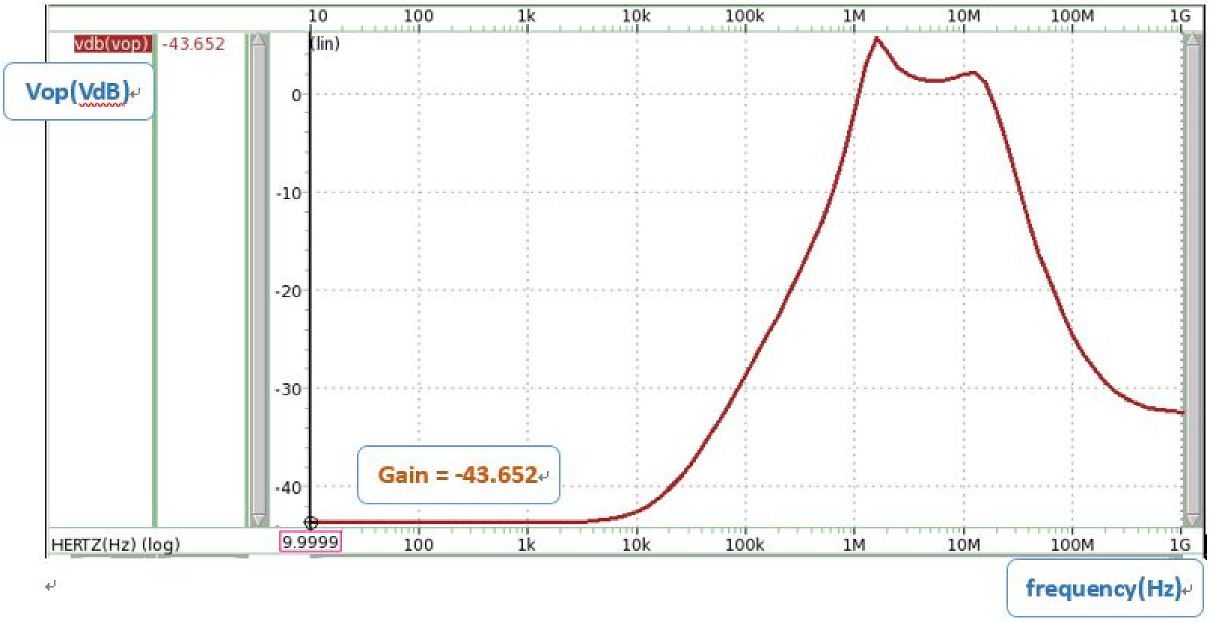

Fig. 3.6(b)

3.7 Closed-loop differential mode AC response

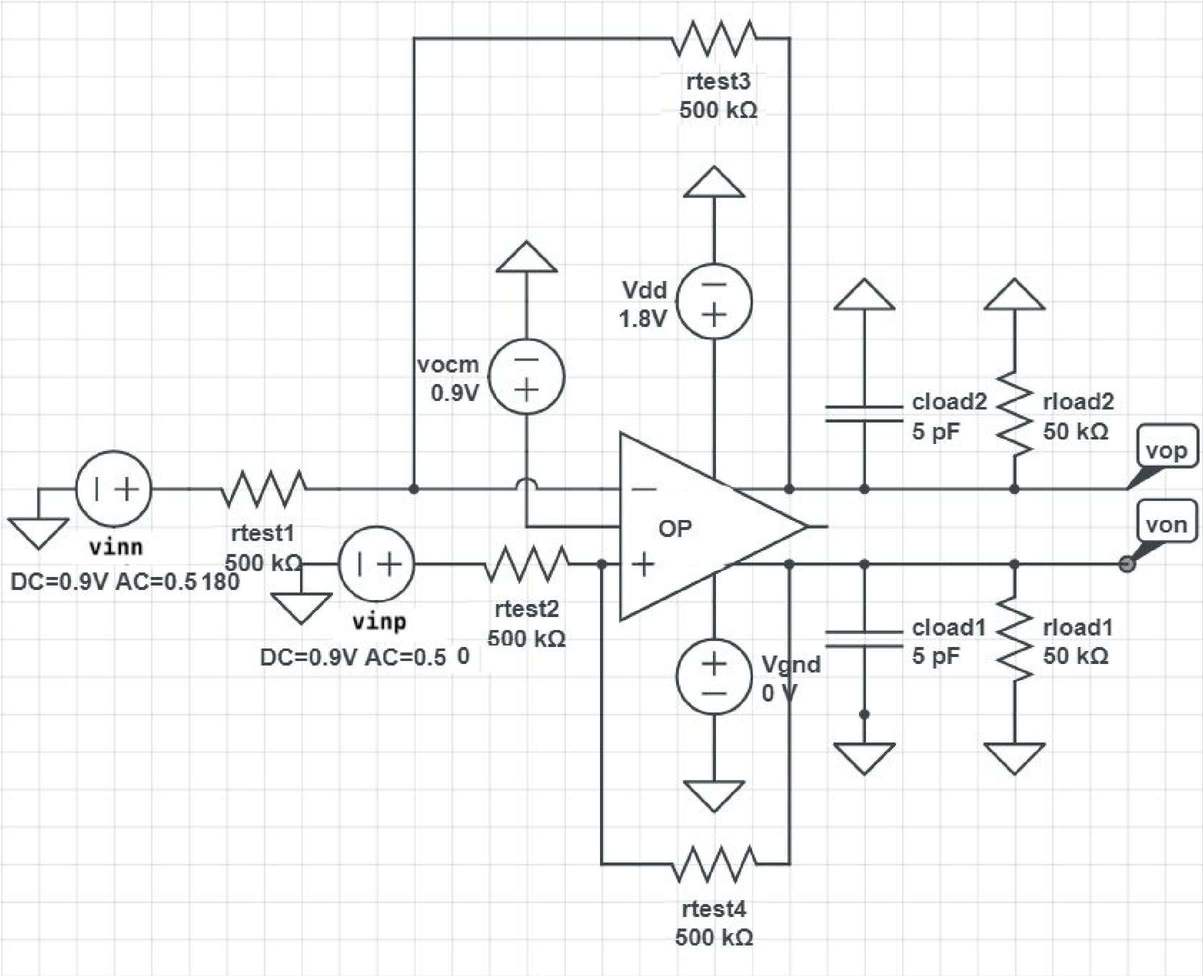

Fig. 3.7(a)

Fig. 3.7(b)

```
test1    = 900.0000m 0:test2    = 900.0000m
vinn     = 916.3893m 0:vinp     = 916.3893m
von      = 932.7785m 0:vop      = 932.7785m
```

Fig. 3.7(c)

$$20 * log\frac{von}{test1} = 20 * log\frac{932.7785}{900} \simeq 0.311$$

算出來的結果與圖片的DC gain非常相近

input output node的值很合理。

```
****     small-signal transfer characteristics

     v(vop,von)/vinp                            =  999.5984m
     input resistance at             vinp       =  668.6595k
     output resistance at v(vop,von)            =   17.5050
```

Fig. 3.7(d)

Dis. 3.7(e) :

從feedback的電路開始分析，他的放大倍率是

$$K = \frac{RCM2}{RCM2+RCM1} = \frac{120K}{240K} = 0.5$$

再來，

openloop gain = 5200，

就可以算出

$$\text{closed loop gain} = \frac{1-K}{K} * \frac{1}{1+\frac{1}{AK}} = 0.9996$$

$$20 * log0.9996 = -3.34m$$

，與模擬結果非常接近。

第二個，

Zin = (ro1//ro3) = 521k

最後，Zout在理想中應該是會等於0，但是因為我們加上了feedback 的電路，才導致了output impedance有些微的上升。

3.8 Closed-loop differential mode DC sweep

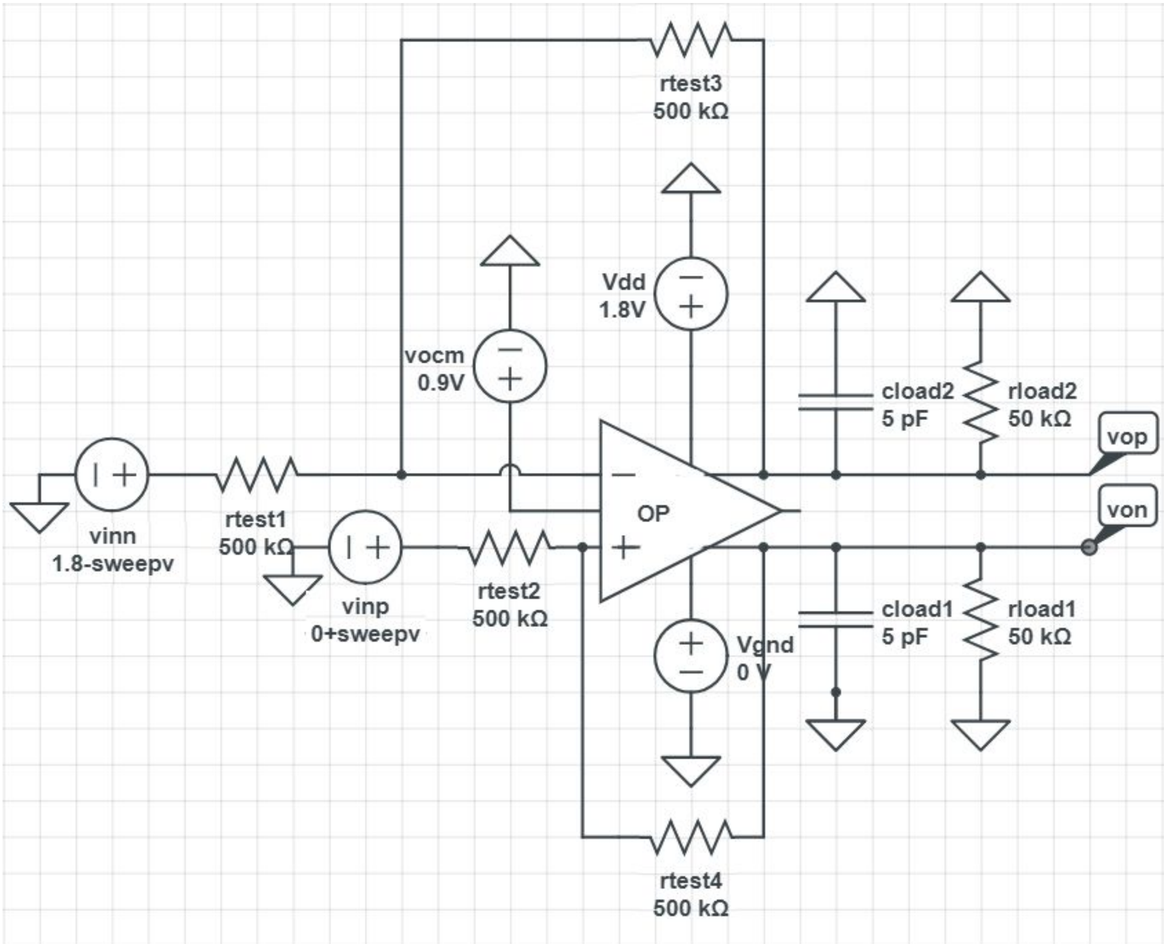

Fig. 3.8(a)

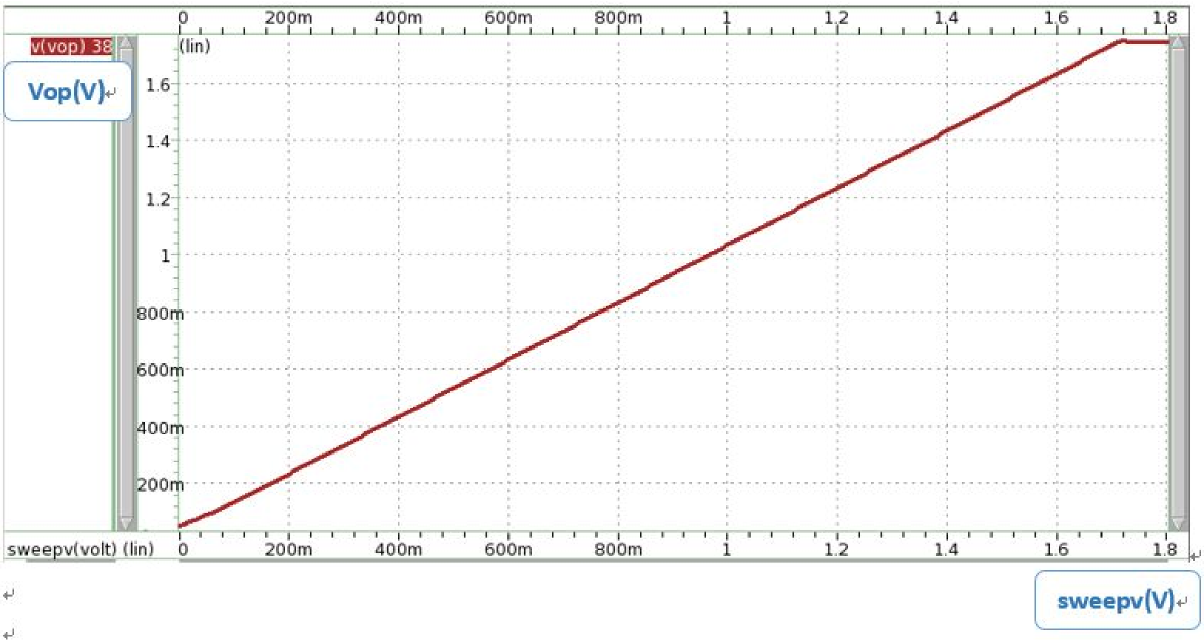

Fig. 3.8(b)-1

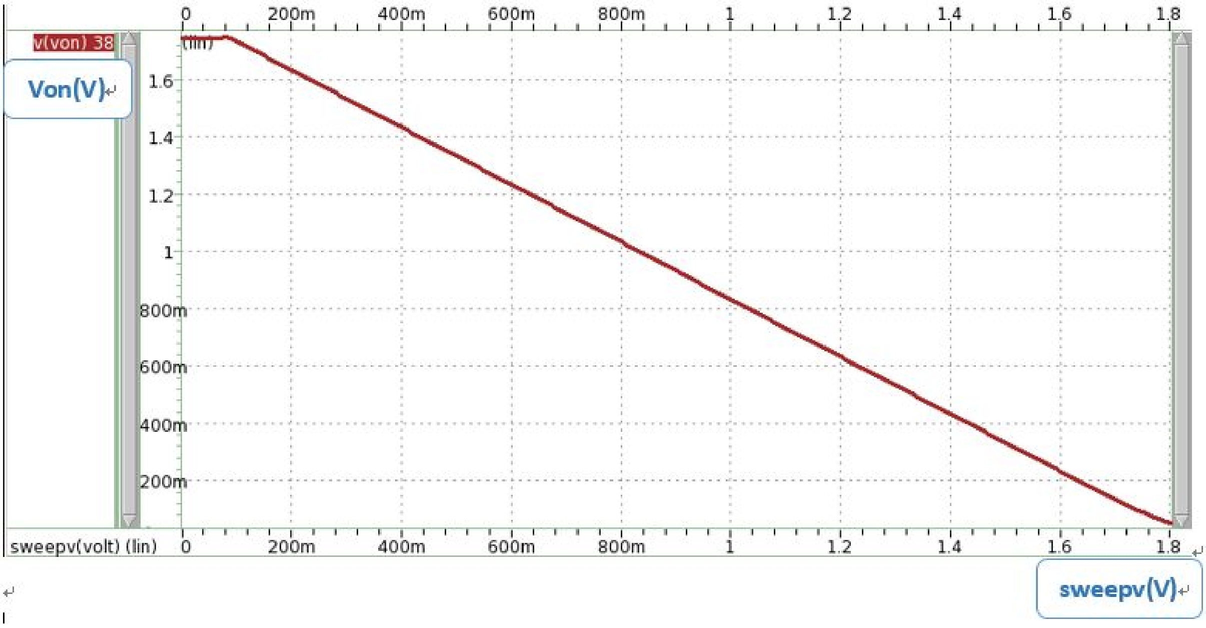

Fig. 3.8(b)-2

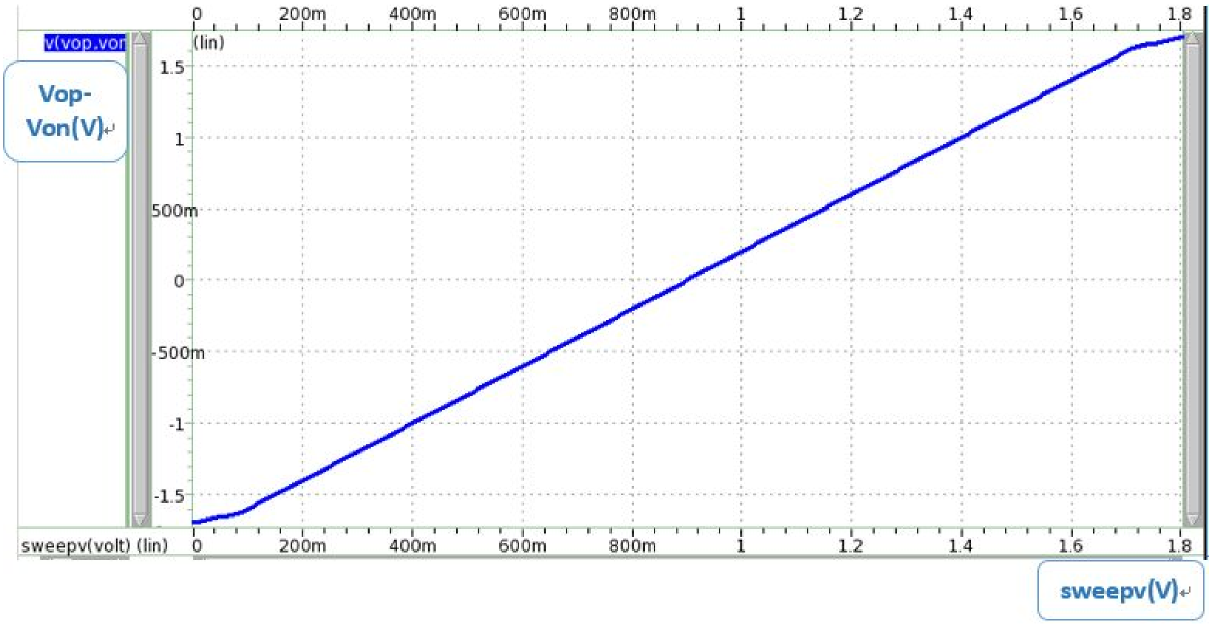

Fig. 3.8(b)-3

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:38_closed-dc_dm.sw0	slope(v(vop),0.9)			999.6m		
D0:38_closed-dc_dm.sw0	slope(v(von),0.9)			-999.6m		
D0:38_closed-dc_dm.sw0	slope(v(vop,von),0.9)			1.9992		

Fig. 3.8(b)-4

3.9 Closed-loop step+ response

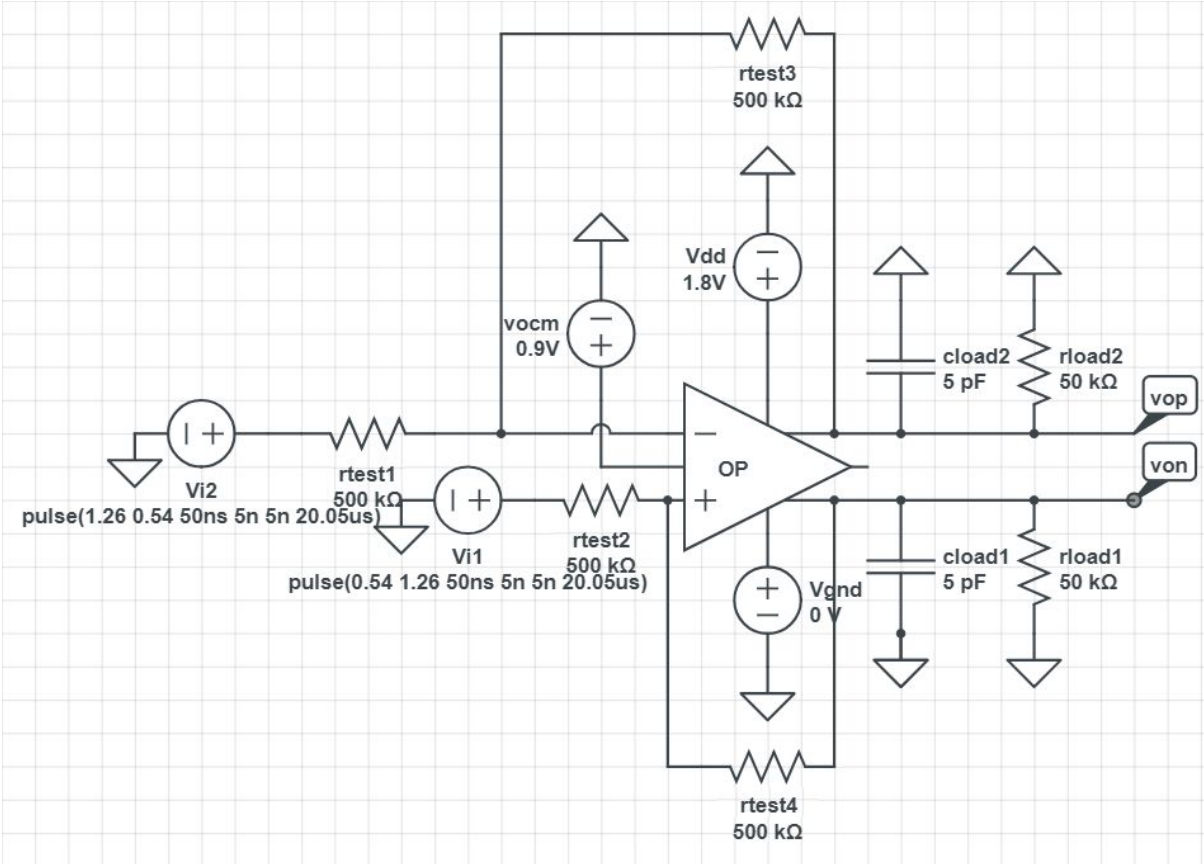

Fig. 3.9(a)

Fig. 3.9(b&c)-Vop

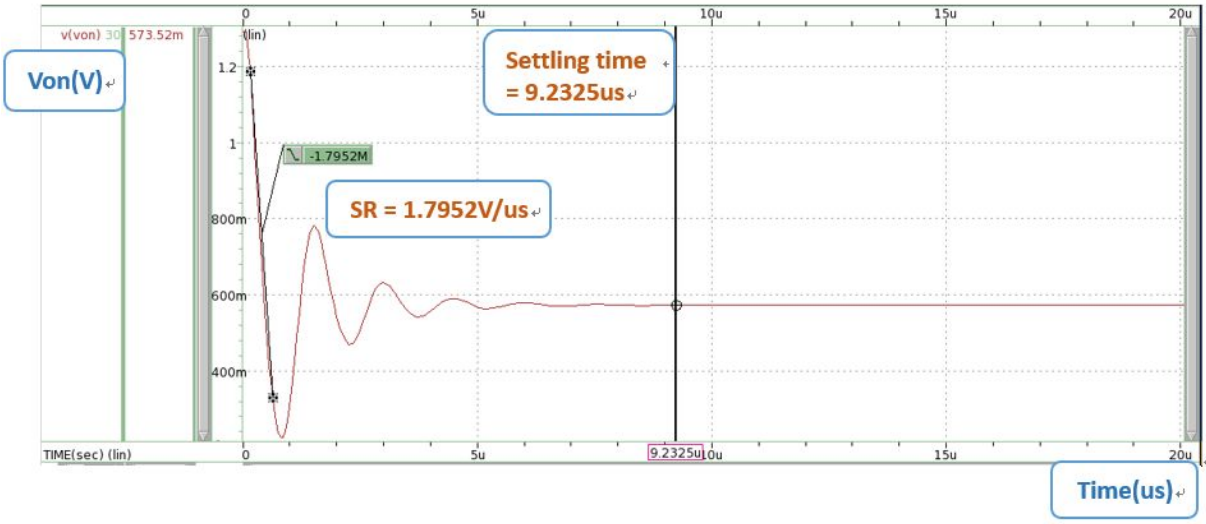

Fig. 3.9(b&c)-Von

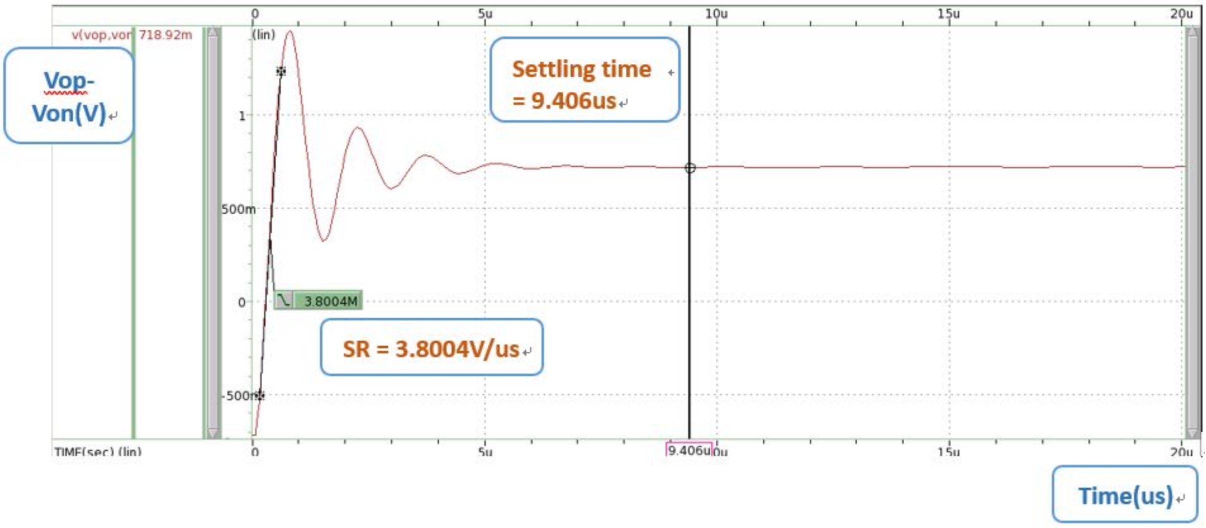

Fig. 3.9(b&c)-(Vop-Von)

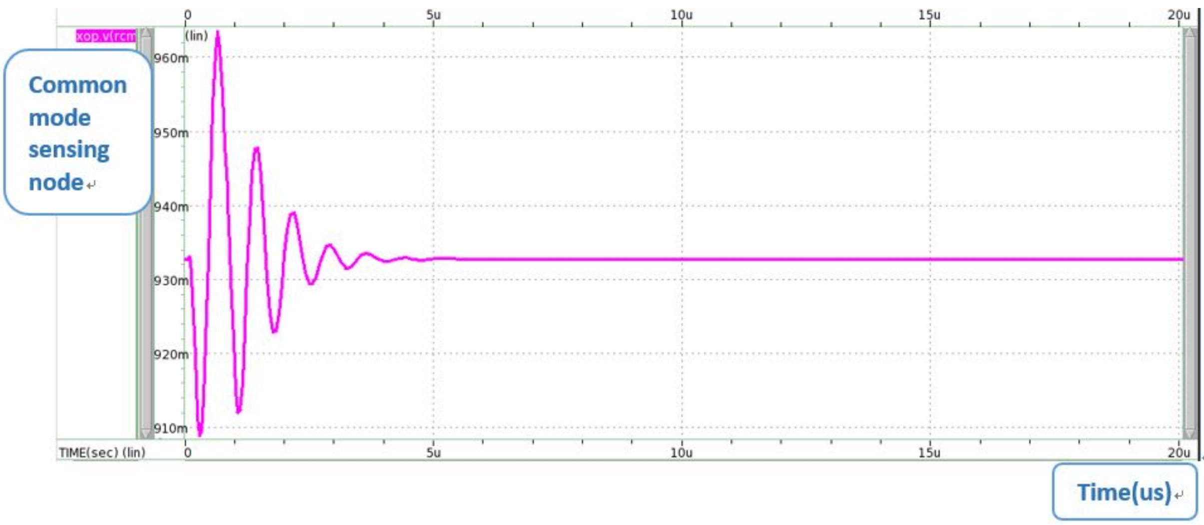

Fig. 3.9(d)

因為電路本身會存在process variation，所以可能會導致電路本身的運作無法保持預期(output common mode voltage可能會產生偏差)，所以我們加上CMFB可以讓電路維持我們的預期去運作。CMFB運作的原理是把common mode sensing node (RCM1_RCM2) 這一點的電壓往下送到CMFB當中，然後他會跟參考電壓(vocm)做比較，把誤差的值再送到bias的電路裡面，給differential amplifier一個feedback，也就成功地讓CMFB運作。

Fig. 3.9(e)

3.10 Closed-loop step- response

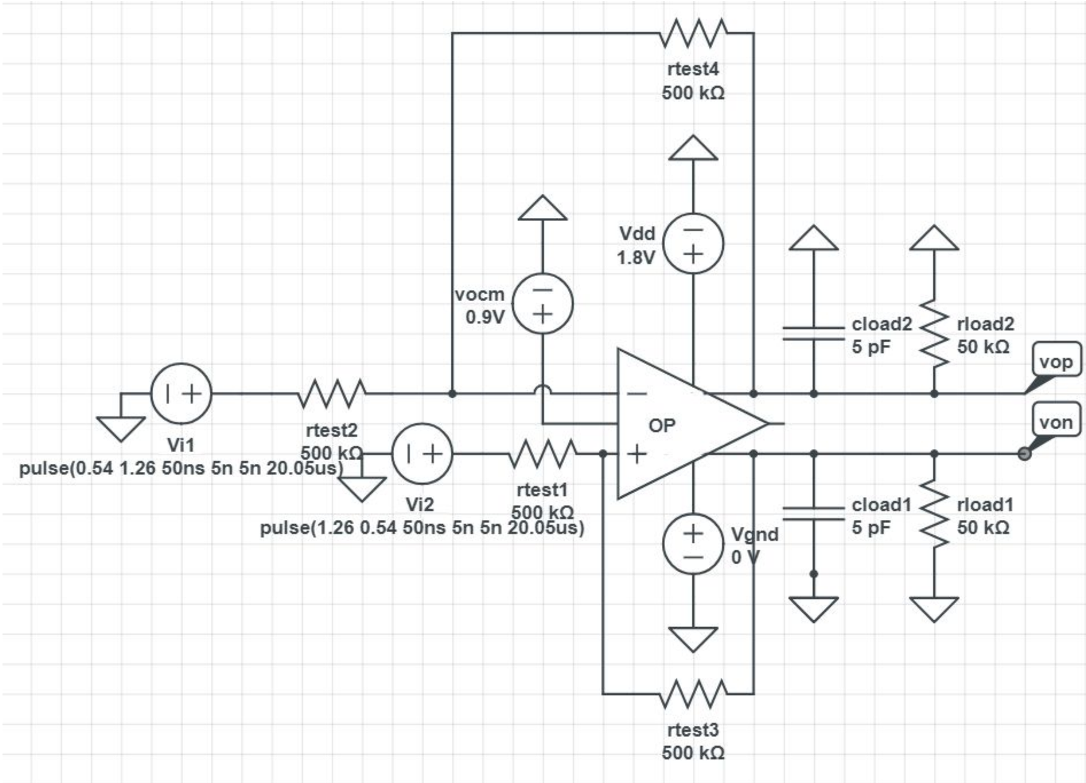

Fig. 3.10(a)

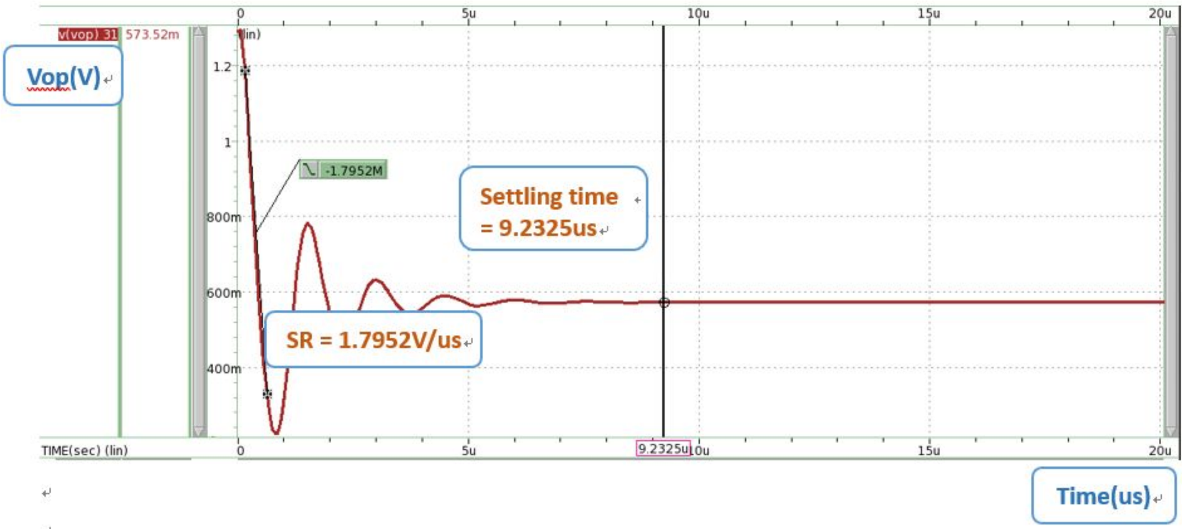

Fig. 3.10(b&c)-Vop

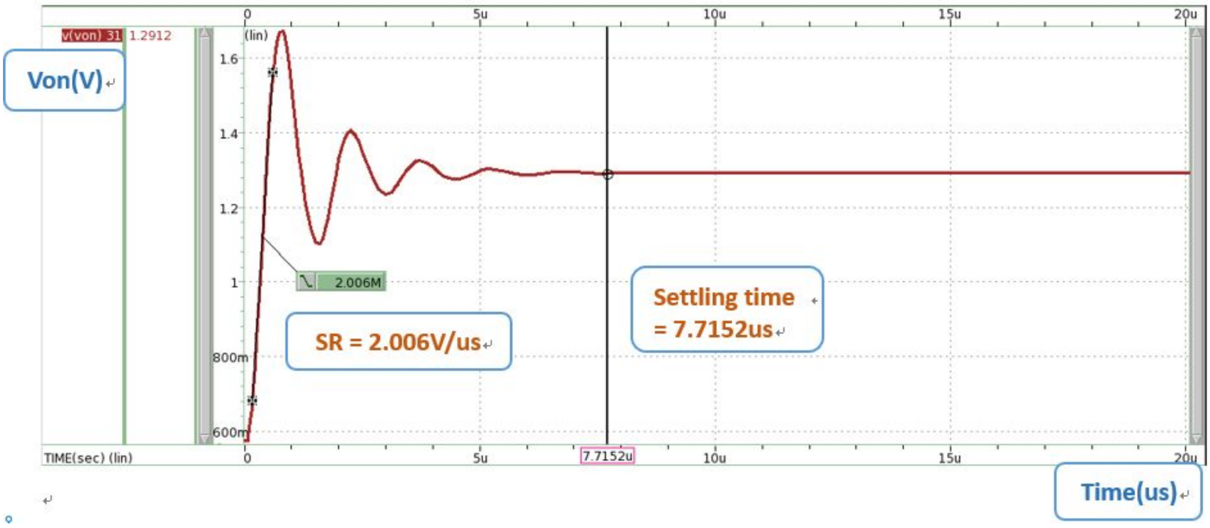

Fig. 3.10(b&c)-Von

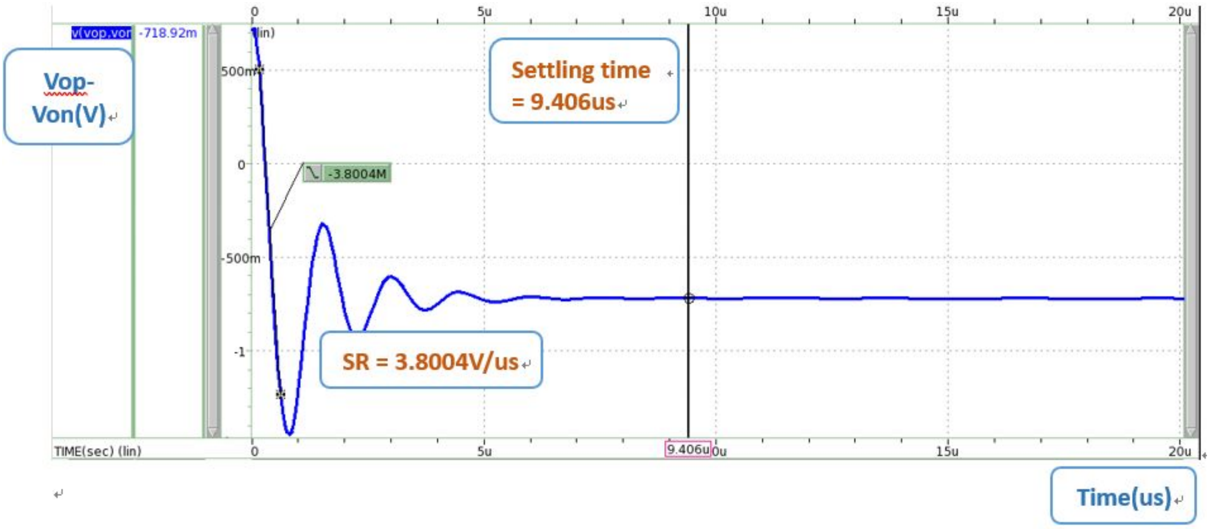

Fig. 3.10(b&c)-(Vop-Von)

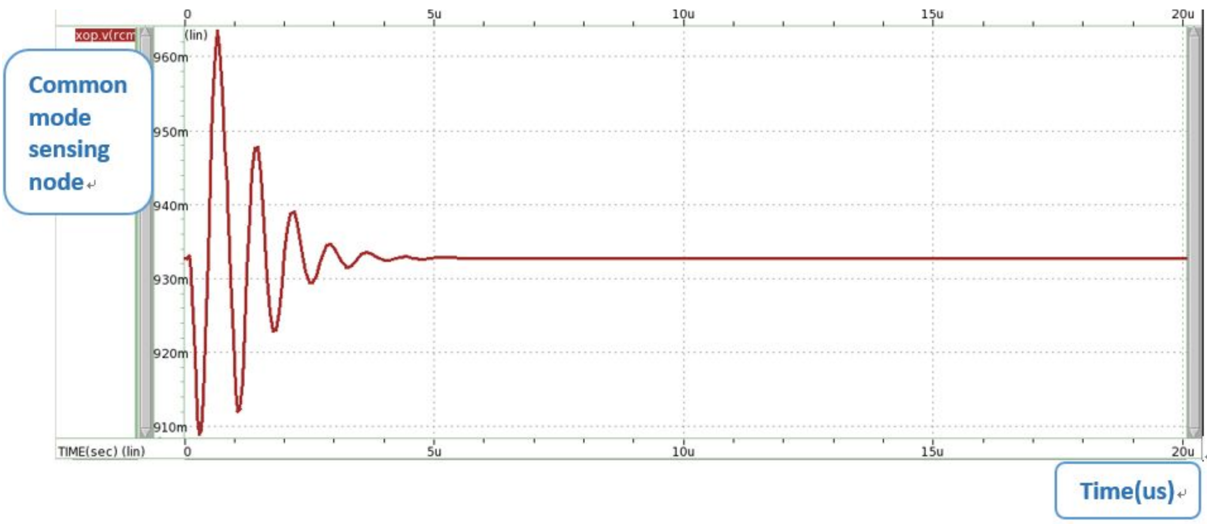

Fig. 3.10(d)

4. Performance Table

Design Items	Specifications	My Work
Technology	CIC pseudo 0.18um technology	
Supply Voltage	**1.8V**, as small as possible	1.8V
Vicm, Vocm	**0.9V / 0.9V**	0.9V / 0.9V
Supply Current (Total)	**< 4mA**, as small as possible	224.22u
Loading	**5pF / 50KΩ (for each output)**	5pF / 50KΩ
Compensation R, C	Open for design	35KΩ / 1pF
Open-loop simulation		
DC gain	**> 72dB**, as large a possible	74.32 dB
Unity-GBW	**> 1MHz**, as large as possible	18.81 MHz
P.M.	**> 45°**	55.5493
C.M.R.R. @10KHz	> 80dB	112.1 dB
P.S.R.R.+ @10KHz	> 80dB	112.5 dB
P.S.R.R.- @10KHz	> 80dB	116.8 dB
Closed-loop simulation		
Differential swing of 1.44V (step signal)		
S.R.+ (10% ~ 90%)	> 1 V/us	3.8 V/us
S.R.- (10% ~ 90%)	> 1 V/us	3.8 V/us
Settling+ (to 0.1%)	< 10 us	9.41 u
Settling- (to 0.1%)	< 10 us	9.41 u
FoM		
Small signal	GBW (MHz) * CL (pF) / Power(mW)	233.26
Large signal +	SR+(V/us) * CL (pF) / Power(mW)	47.12
Large signal -	SR-(V/us) * CL (pF) / Power(mW)	47.12

Table1. summary table

5. Design Concerns

一開始我先將Bias Circuit拔除，接上一個電壓源，等到設計完剩下的電路之後，最後才把Bias的circuit調成後來接上的電壓源的值。要達成所有的spec並不是一件太難的事情，只要調將gain調到>72dB之後，後面的spec都不太難達成，因此我想要將重點放在優化FoM的部分。

FoM:

FoM1正比於Bandwidth,CL，反比於power，因為CL是給定的值，因此我們努力的方向是把Bandwidth提高並把power降低。首先，我想要把power降低，因此，我會需要去降低MB1的size，以讓他的電流不要那麼大，但是又要顧及不要讓gain掉到72dB以下，所以調整起來有點綁手綁腳。再來，因為要讓gain達標，所以我有稍微去增加First stage那些size，讓他們的ro增加一些，會比較好達成gain。第二，我們可以讓Bandwidth提升，要讓Bandwidth提升，最直接的想法就是盡量調小Cc的值，但是也不能無限制地去調小Cc的值，不然會因為太小而沒辦法compensate，所以在調整的時候也要注意一下。

至於FoM2與FoM3的話，power的部分跟FoM1的部分差不多，slew rate的話則是越大越好，要加大slew rate最直接的關係是降低Cc，這個與FoM1需要努力的目標是一致的。

6. Discussions

Experience and problem:

在調整電路時沒遇到什麼大問題，只要達成第一項spec的gain，後面就只需要一些微調就可以達成，比較麻煩的地方是在於優化我的FoM，因為這次的要求不算是很嚴格，才可以如此輕鬆地達成所有的spec，但是在優化FoM的過程當中我遇到了許多的麻煩，好不容易加大了FoM，但是SR或settling time，甚至是gain都會跑到沒有辦法滿足spec的值，最後終於找到一組還不錯的值，因為還要預留時間給報告，所以就沒有再繼續嘗試下去了，如果有更多時間的話，應該可以取到更好的performance，這方面是我以後應該要檢討的。

What I get and suggest:

修完這們課讓我對於Mos的運作以及類比電路的操作原理有了更進一步的認識，在修這門課以前我總認為電子學很簡單，沒有什麼困難的，也時常耳聞設計類比電路最重要的就是經驗，之前的我一值無法了解，直到修了這門課之後，才知道類比電路分析與設計是一門很深奧的學問，要如何去實現一個電路，真的是需要很豐富的經驗，才能夠知道要改變那些地方，才能夠解決電路上所遇到的問題，類比電路的博大精深是現在的我還無法完全透徹的。

建議以後作業與上課的內容能夠更契合一些，因為我在做作業時常常不知道該往哪裡前進，都要摸索很長一段時間才能夠真正開始那次的作業。

```
.param vdd=1.8V            $Your positive supply voltage
.param vss=0V              $Your negative supply voltage
.param vocm=0.9V    $Your output common mode voltage (for CMFB)

.subckt op vinp vinn vdd vss vop von vocm

*** First stage ***

M1 M1_M2_M5 vinp M1_M3 vdd          p_18 w=53u l=10u m=1
M2 M1_M2_M5 vinn M2_M4 vdd          p_18 w=53u l=10u m=1
M3 M1_M3 M3_M4_feed vss vss         n_18 w=13u l=10u m=4
M4 M2_M4 M3_M4_feed vss vss         n_18 w=13u l=10u m=4
M5 vdd cross M1_M2_M5 vdd           p_18 w=10u l=10u m=5

*** Second stage ***

M6 von M2_M4 vss vss                n_18 w=10u l=1u m=10
M7 vdd cross von vdd                p_18 w=14u l=1.5u m=10
M8 vop M1_M3 vss vss                n_18 w=10u l=1u m=10
M9 vdd cross vop vdd                p_18 w=14u l=1.5u m=10

*** Compensation ***

RZ1 vop RZ1_CC1 35k
RZ2 von RZ2_CC2 35k
CC1 M1_M3 RZ1_CC1 1p
CC2 M2_M4 RZ2_CC2 1p

*** Bias Circuit ***

Rb MB1_MB2 vdd 60k
MB1 MB1_MB2 MB1_MB2 vss vss         n_18 w=12u l=5u m=10
MB2 cross MB1_MB2 vss vss           n_18 w=12u l=5u m=10
MB3 vdd cross cross vdd             p_18 w=12u l=5u m=10

*** Feedback Circuit ***

RCM1 RCM1_RCM2 vop 120k
RCM2 RCM1_RCM2 von 120k
MF1 MF1_MF2_MF5 vocm MF1_MF3 vdd                   p_18 w=12u l=3u m=1
MF2 MF1_MF2_MF5 RCM1_RCM2 M3_M4_feed vdd           p_18 w=8u l=3u m=1
MF3 MF1_MF3 MF1_MF3 vss vss                        n_18 w=12u l=3u m=1
MF4 M3_M4_feed M3_M4_feed vss vss                  n_18 w=8u l=3u m=1
MF5 vdd cross MF1_MF2_MF5 vdd                      p_18 w=10u l=3u m=1

.ends
```