Schematic Building &
Hspice Simulation Tutorial

Full-Custom Design Auxiliary Materials

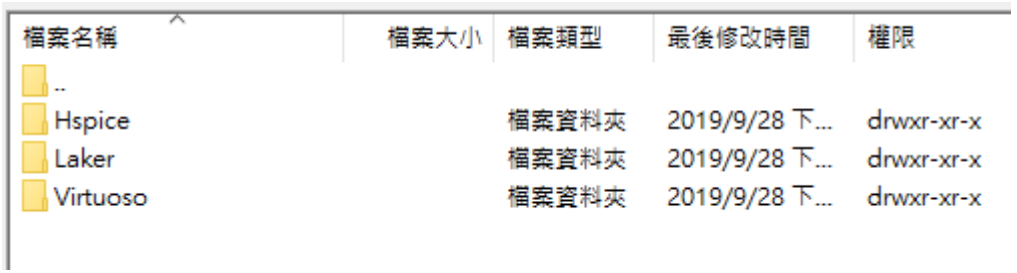
- Model
  - Device parameter
  - Ex : cic018.l
  - For Virtuoso, Hspice
- Technology file
  - Layer definition
  - Ex : laker.tf
  - For laker
- DRC command file
  - Verify Layout
  - Ex : Rule.drc
  - Calibre
- LVS command file
  - Layout Versus Schematic
  - Ex : Rule.lvs
  - Calibre

Simulation Flow

#0 : 先建立一目錄包含以下資料夾(做好檔案管理)

- Virtuoso : (Schematic)
  - 在此層開 icfb 利用 virtuoso (composer) 建立 schematic
- Laker : (Layout)
  - Layout
- Hspice : (Simulation)
  - 需包含 model 檔 (ex : cic018.l)
  - Pre-sim
  - Post-sim

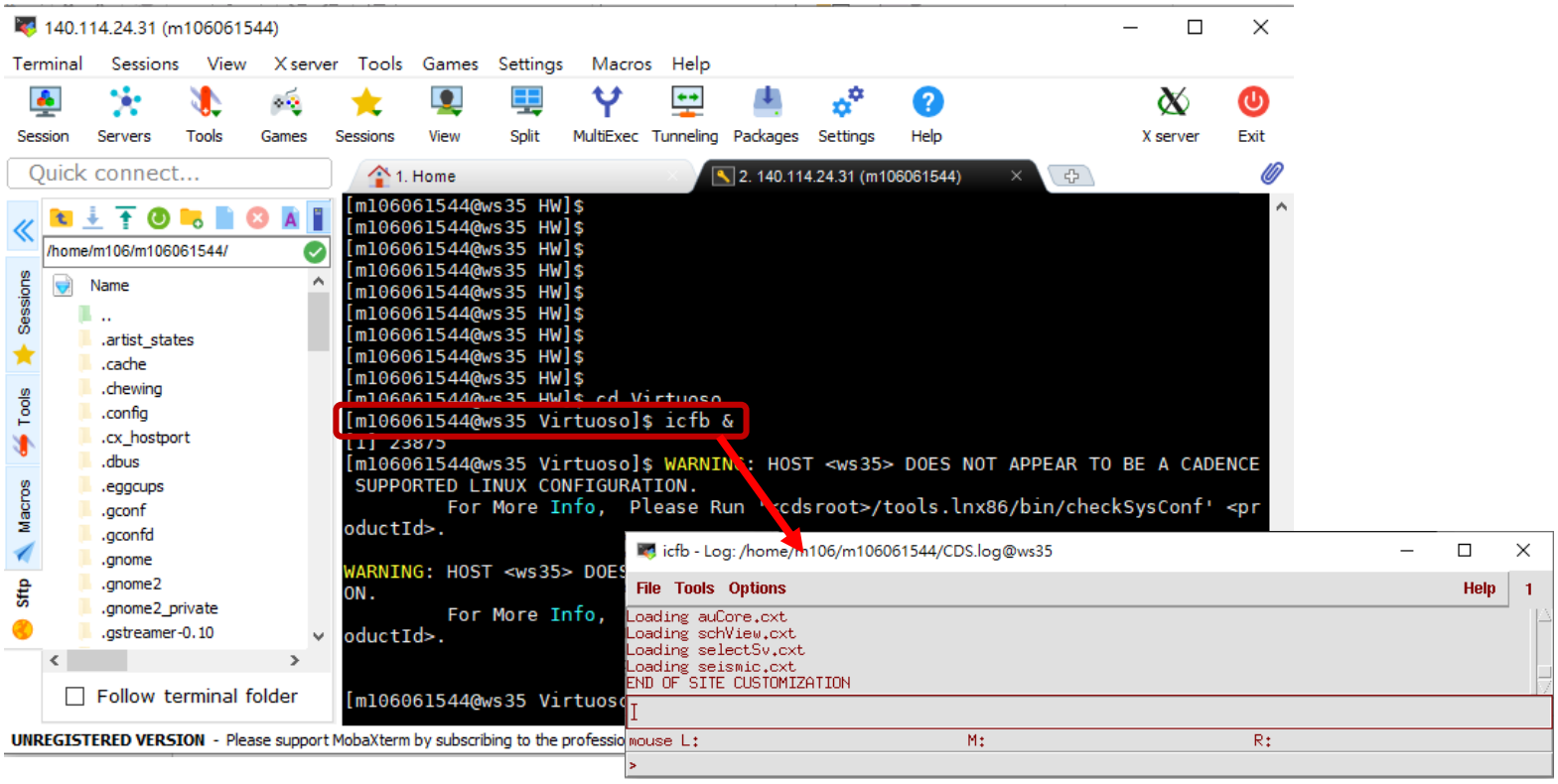
- P.s 可利用 FileZilla 直接建立目錄



Simulation Flow

#1 : 建立 Schematic

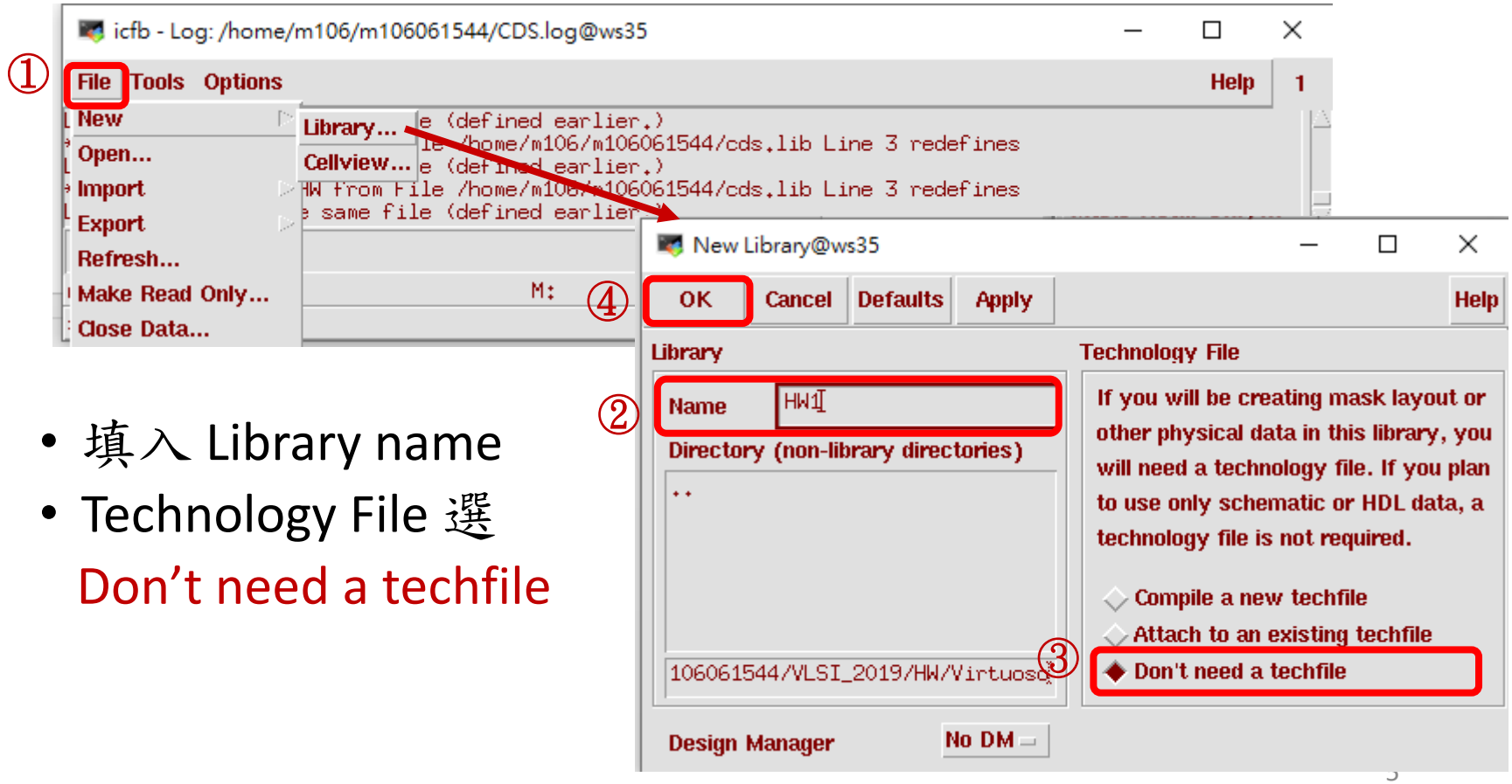
- 利用 MobaXterm 於己所建的目錄 (此處為 HW) 下
- 鍵入 cd Virtuoso ，進入 Virtuoso 資料夾
- 然後開啟鍵入 icfb & 開啟 Virtuoso



Simulation Flow

#1 : 建立 Schematic

- 於 icfb 視窗建立新的 library : File/New/Library…

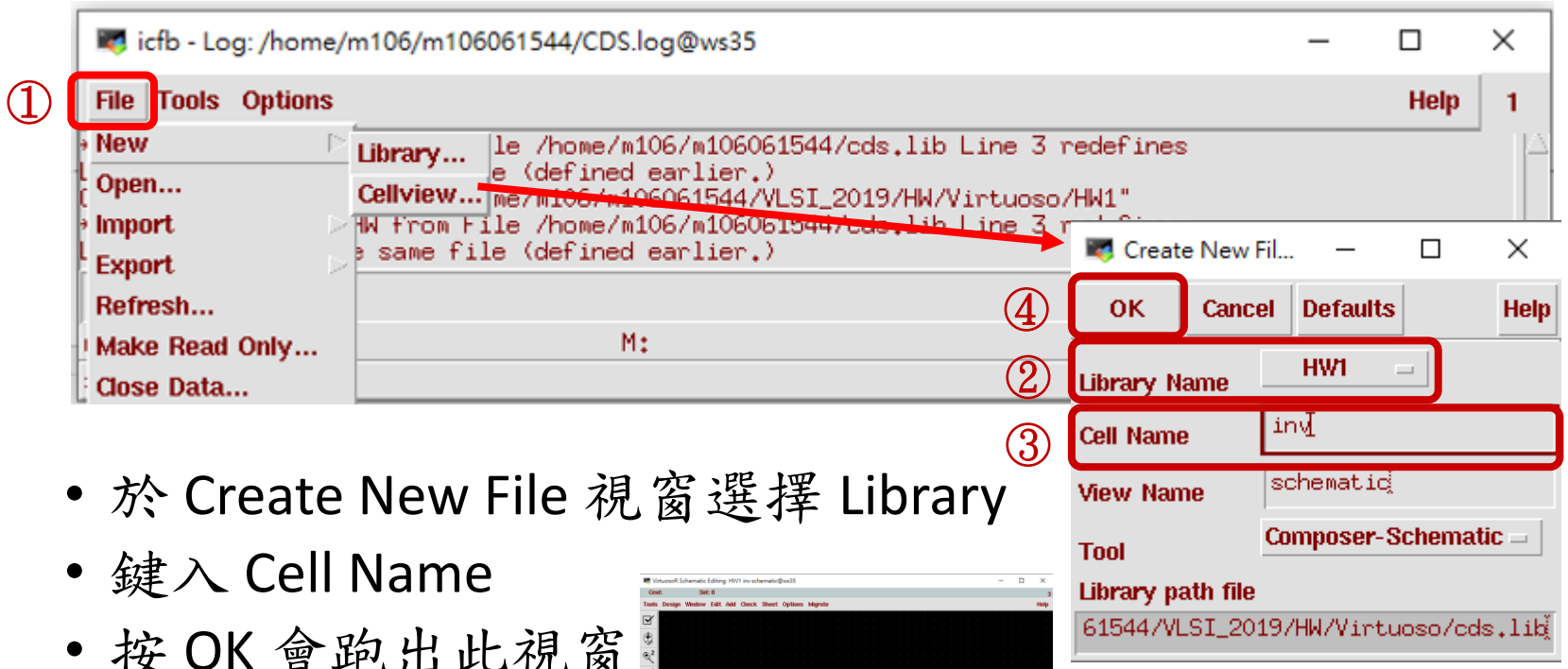


- 填入 Library name
- Technology File 選
  Don’t need a techfile

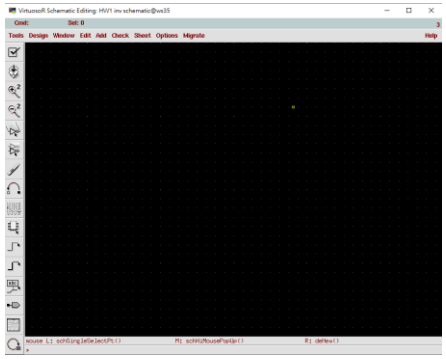
Simulation Flow

#1 : 建立 Schematic

- 於 icfb 視窗建立新的schematic : File/New/Cellview…



- 於 Create New File 視窗選擇 Library
- 鍵入 Cell Name
- 按 OK 會跑出此視窗

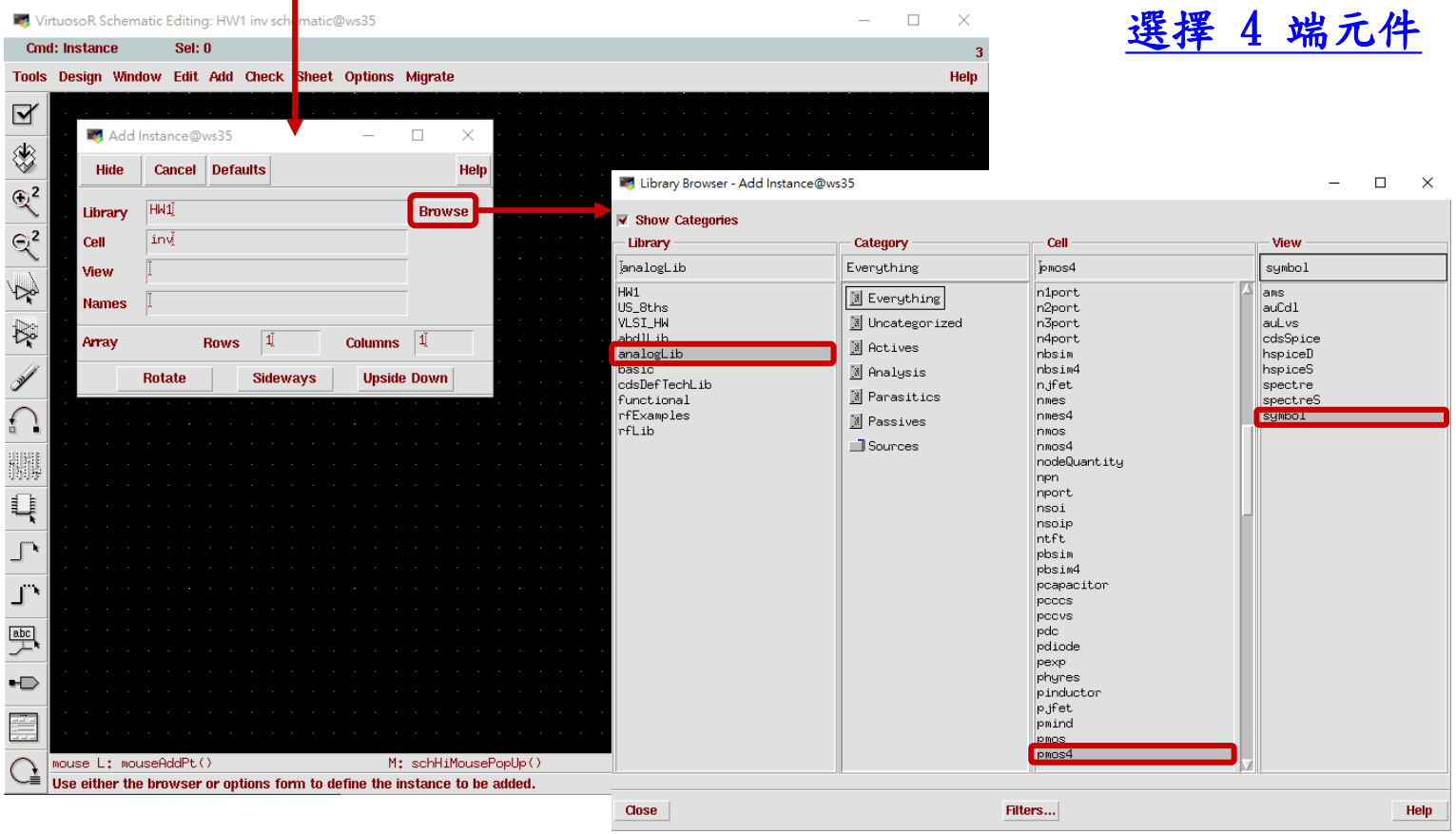


Simulation Flow

#1 : 建立 Schematic

- 於 VirtuosoR Schematic 視窗建立電路
- 利用快捷鍵 i 呼叫 device → 按 Browse → 呼叫 pmos4

選擇 4 端元件

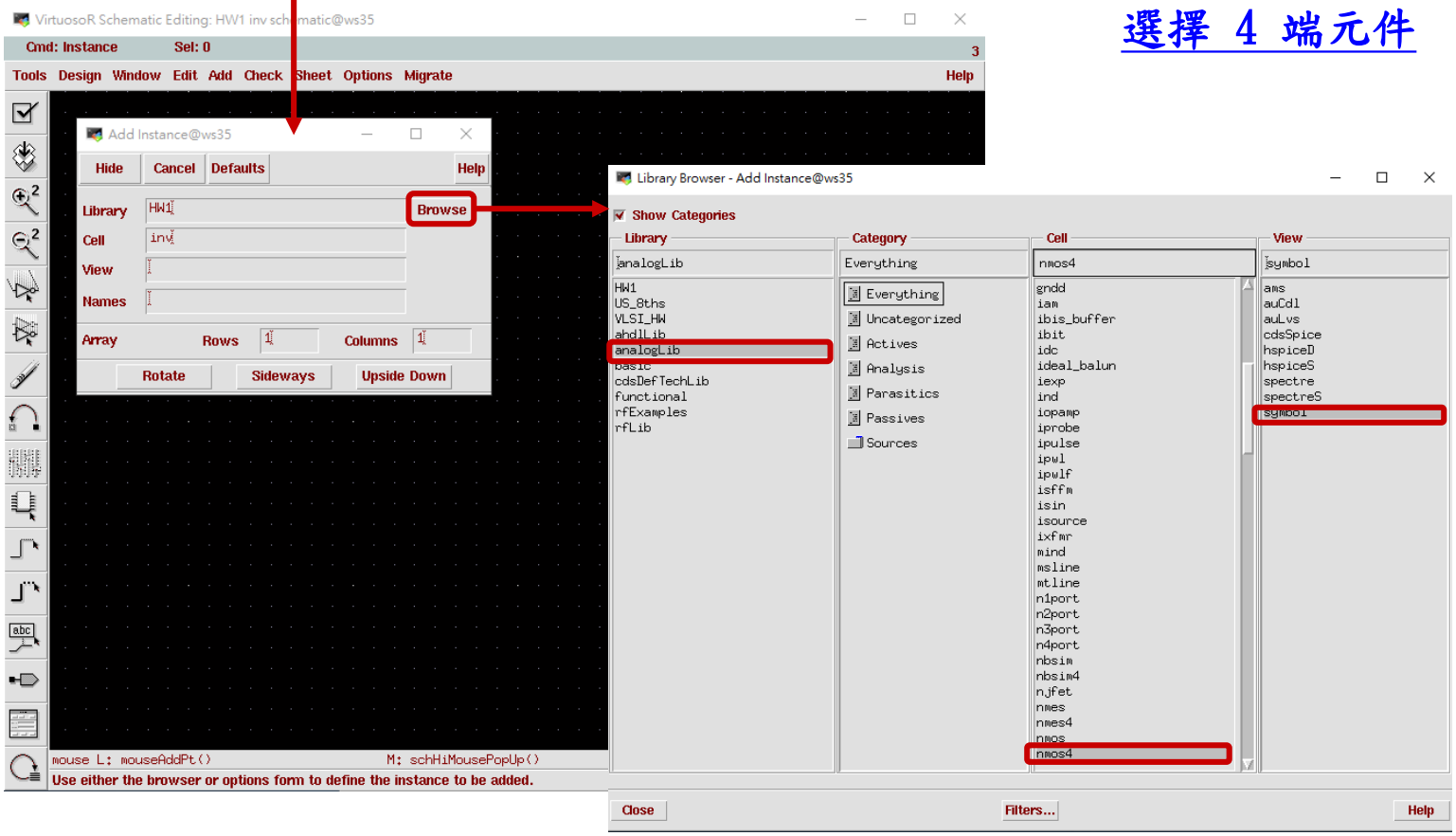


Simulation Flow

#1 : 建立 Schematic

- 於 VirtuosoR Schematic 視窗建立電路
- 利用快捷鍵 i 呼叫 device → 按 Browse → 呼叫 nmos4

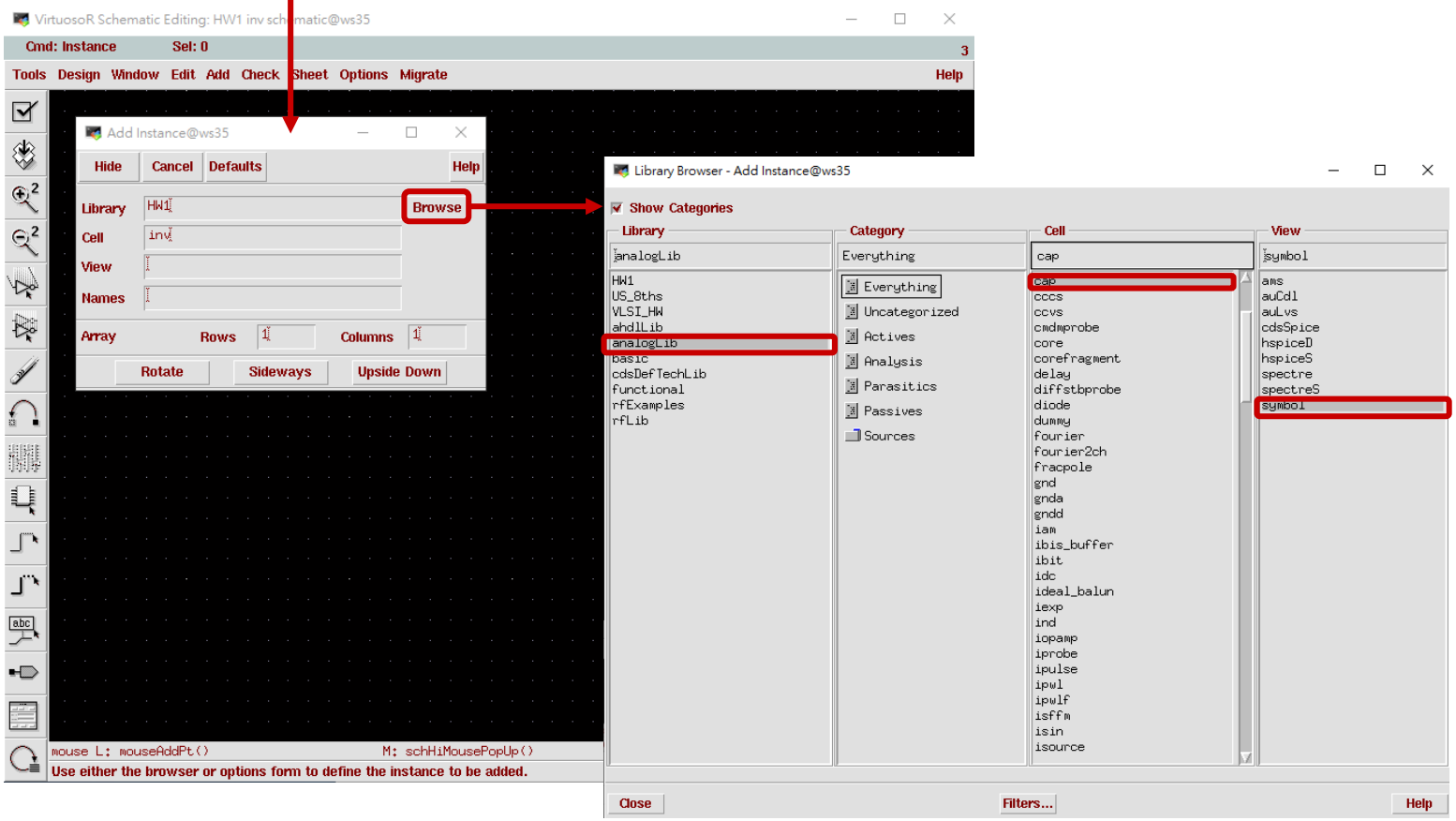
選擇 4 端元件



Simulation Flow

#1 : 建立 Schematic

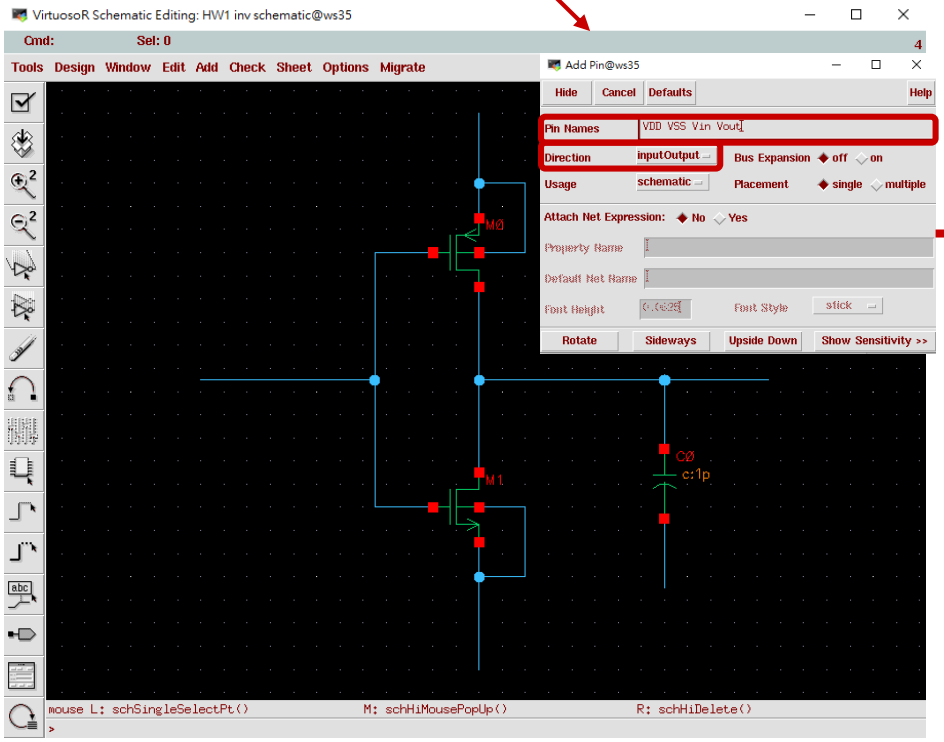
- 於 VirtuosoR Schematic 視窗建立電路
- 利用快捷鍵 i 呼叫 device → 按 Browse → 呼叫 cap

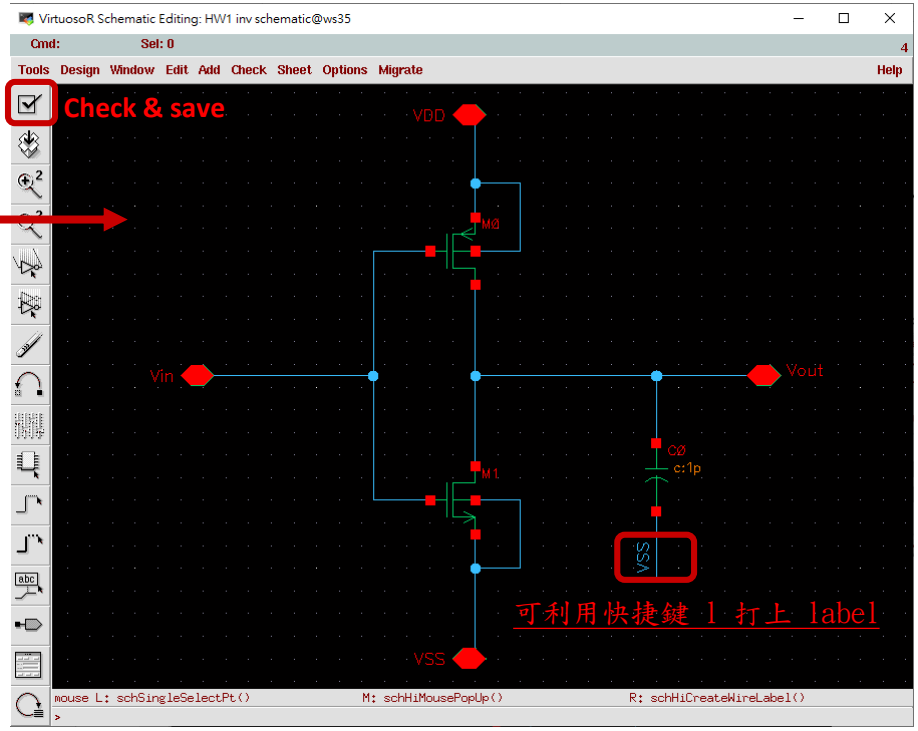


Simulation Flow

#1 : 建立 Schematic

- 擺放 device
- 按快捷鍵 w 畫連接線，連接元件
- 按快捷鍵 p 放置 I/O PIN ，鍵入 PIN name，選 InputOutput



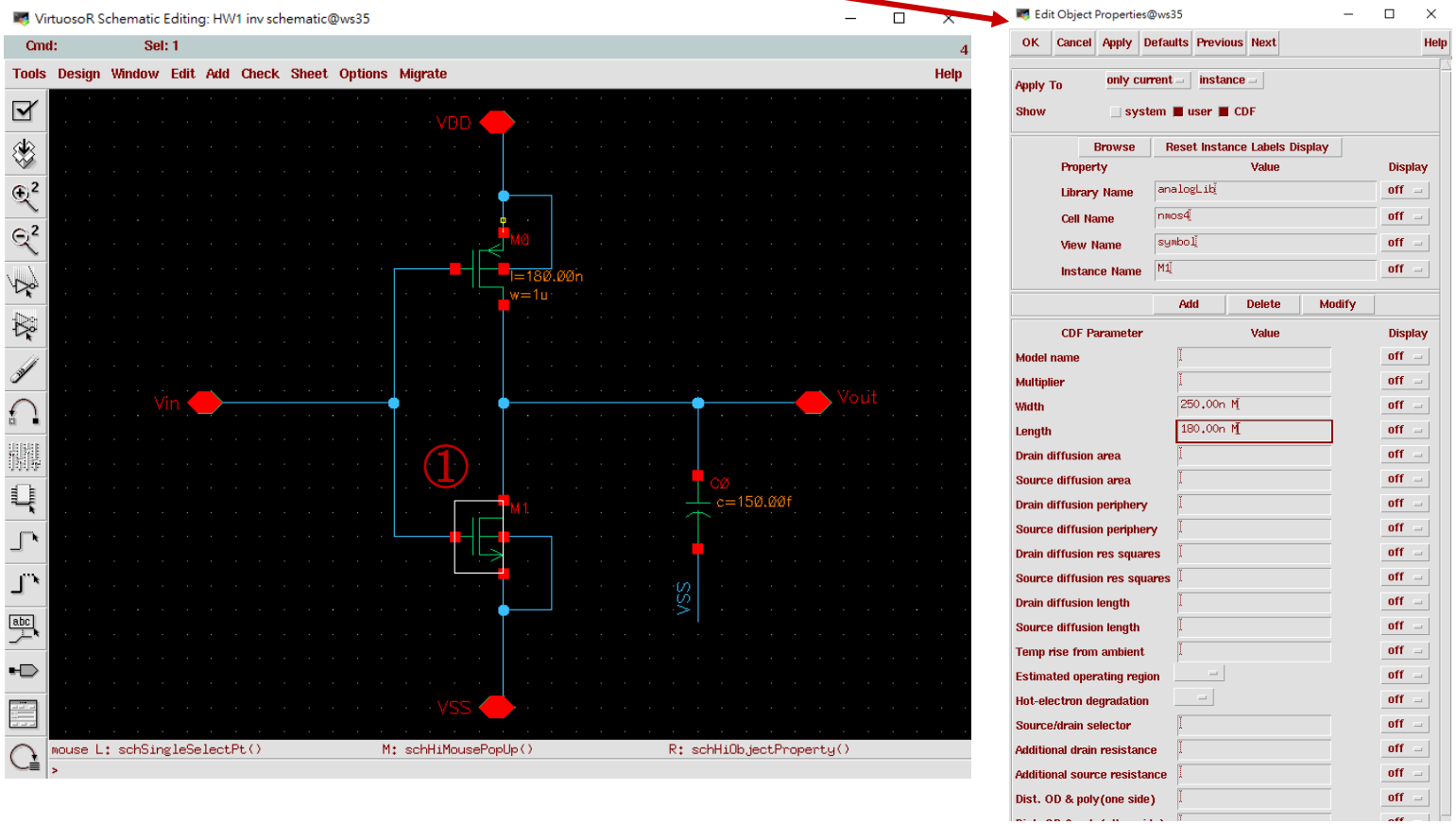


Simulation Flow

#1 : 建立 Schematic

- 選擇元件按 q 可以設定其參數 (W, L, m...)

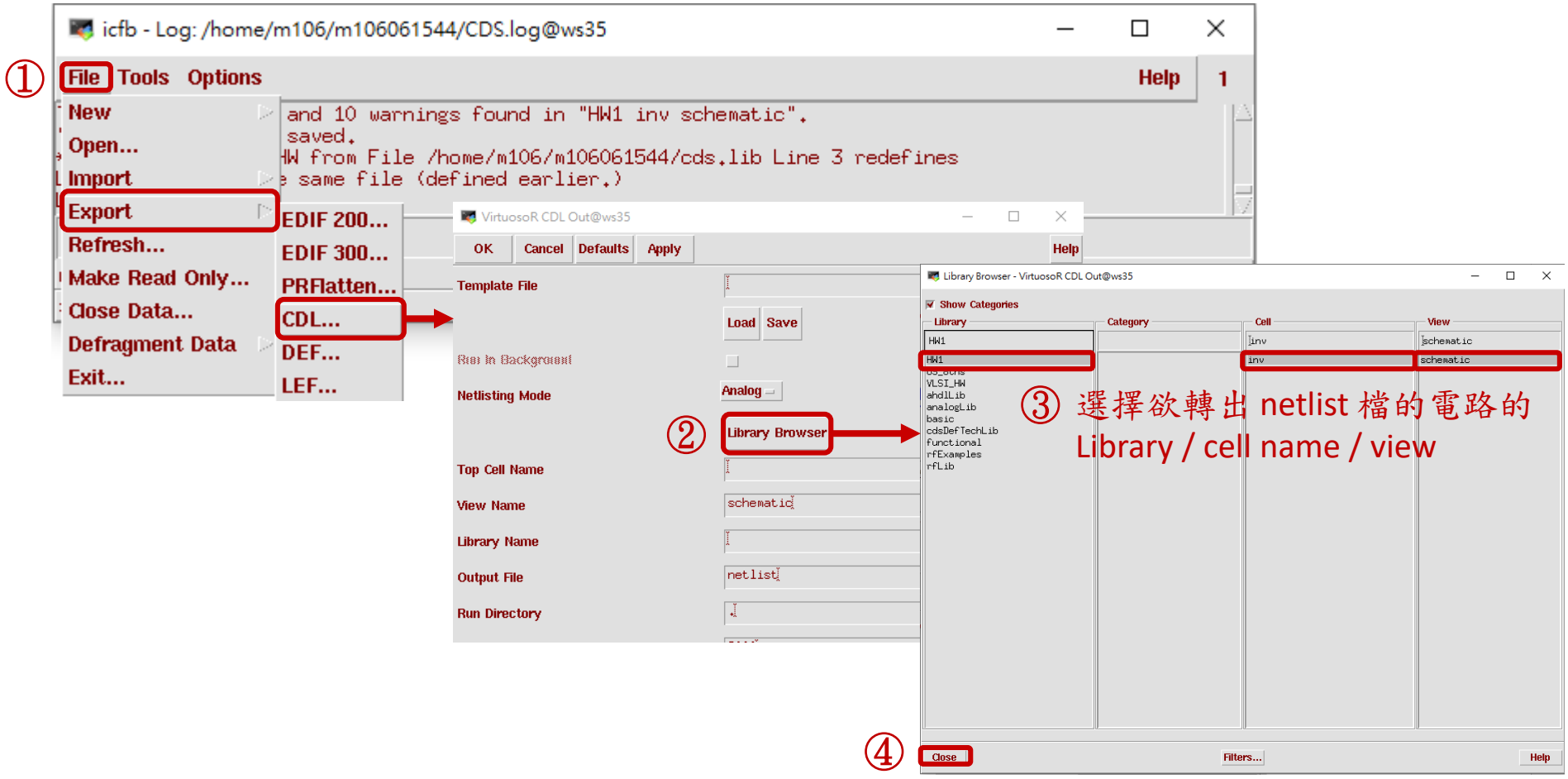
②



Simulation Flow

#2 : 轉出 schematic netlist 檔

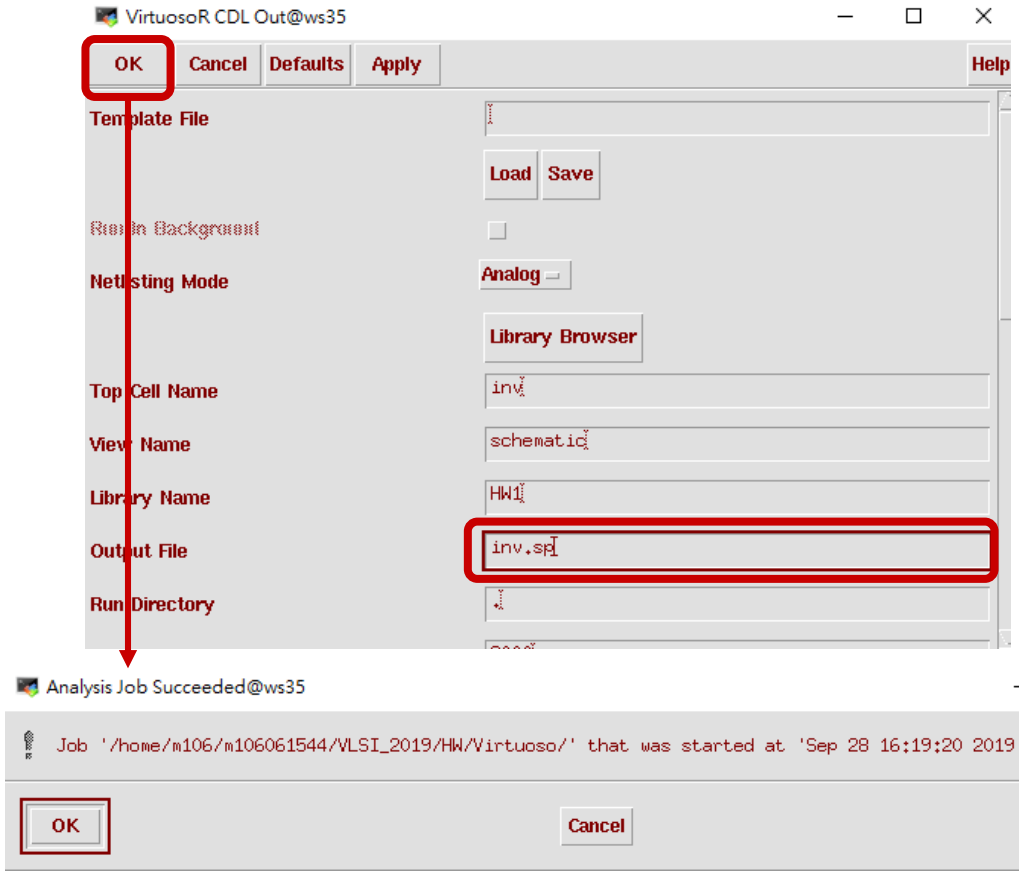
- 於 icfb 主視窗/File/Export/CDL…



Simulation Flow

#2 : 轉出 schematic netlist 檔

- 回到 Virtuoso CDL out 視窗，於 Output File 鍵入轉出檔案名稱 XXX.sp → 按左上角 OK



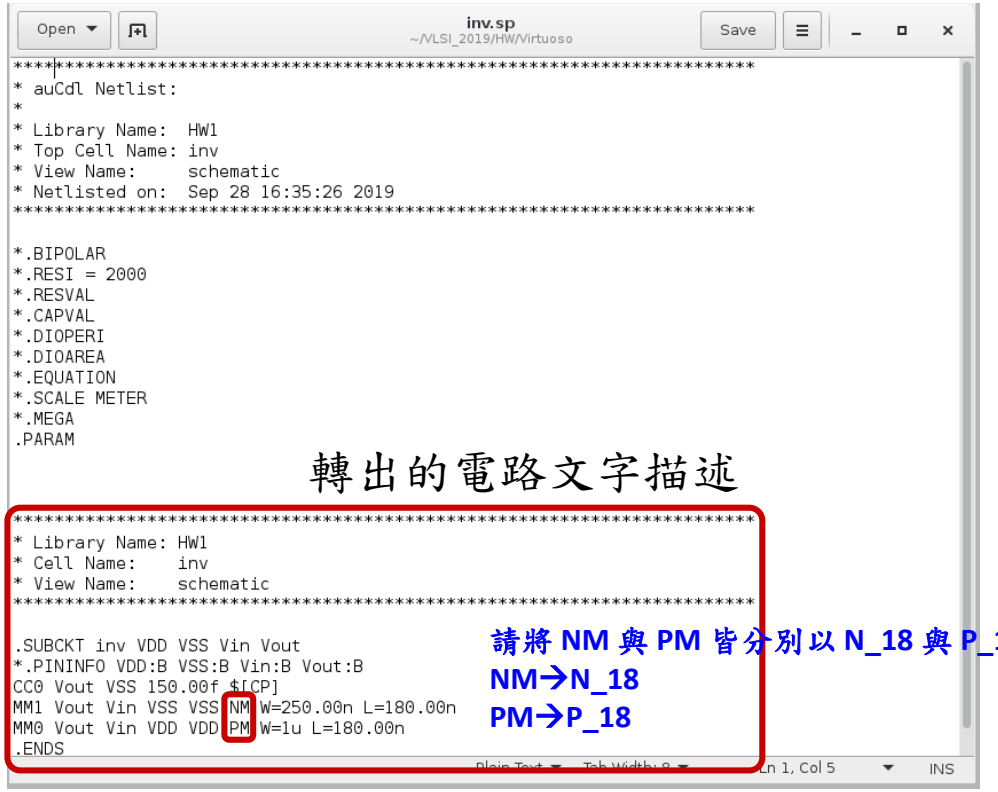
P.S 這邊如果有錯誤，通常是因為電路沒有事先做 check and save 的動作，可以先存檔再回來轉

Simulation Flow

#2 : 轉出 schematic netlist 檔

- 打開電路 netlist 檔：在 MobaXterm 上鍵入 gedit XXX.sp & (XXX為檔案名稱)

```
[m106061544@ws35 Virtuoso]$ gedit inv.sp &
```

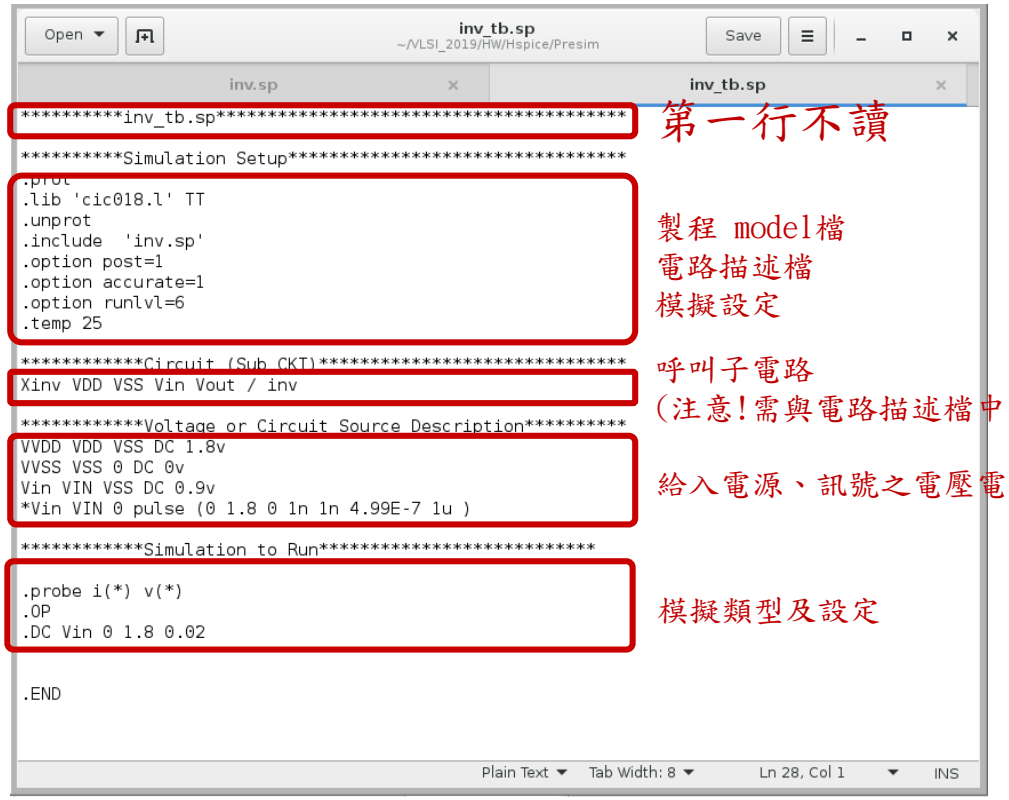


Simulation Flow

關於 Hspice 語法等可以參考下列網址
http://access.ee.ntu.edu.tw/course/vlsi_design_90second/data/spice2001_07.pdf

#3: Prepare for simulation

- 將製程 model 檔(cic018.l)、電路 .sp 檔 (inv.sp) 放至跑模擬的資料夾 (ex: presim 資料夾)
- 建立跑模擬的 testbench (ex: inv_tb.sp)



Simulation Flow

#4: Simulation

- 編輯完 testbench 後，可以藉由
  hspice -i inv_tb.sp -o inv_tb.lis & 跑模擬

```
[m106061544@ws35 Presim]$ hspice -i inv_tb.sp -o inv_tb.lis &
```

- 若顯示結果為 hspice job aborted，則表示模擬未完成，可以依造 inv_tb.lis 檔案內容中的 error information，更正錯誤

```
>info:          ***** hspice job aborted
```

- 若顯示為 hspice job concluded ，則表示模擬完成，可於 inv_tb.lis 查看部分分析結果

```
>info:          ***** hspice job concluded
```

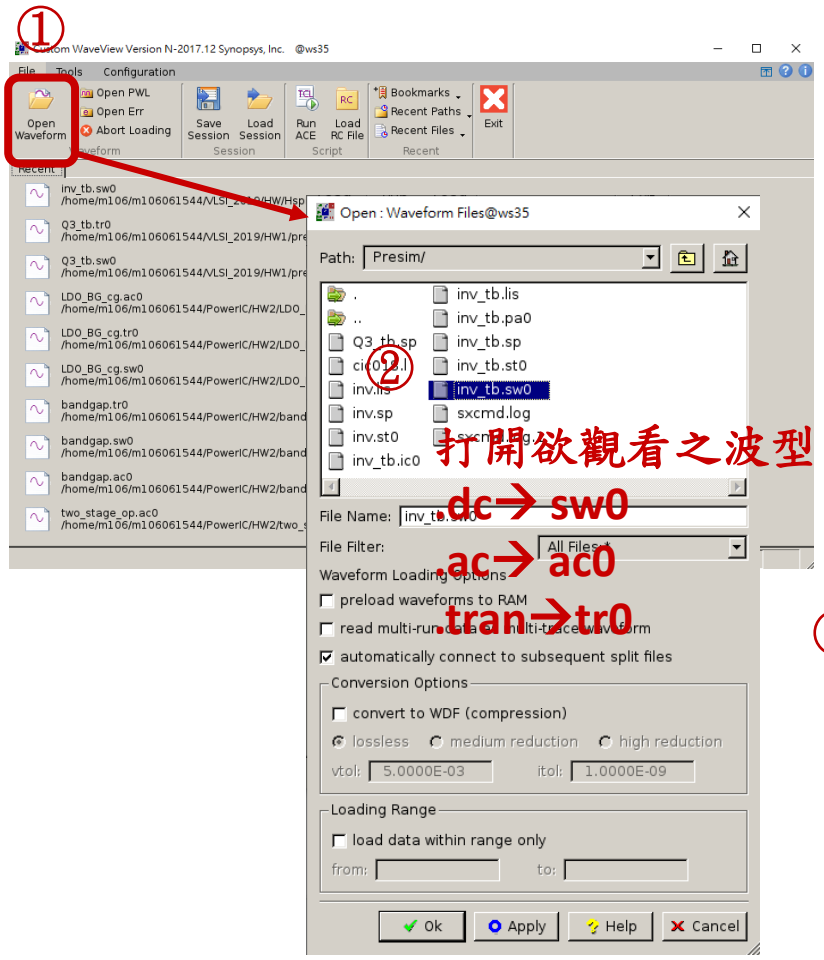
- 若模擬需要查看波型，可以藉由 wv & 指令顯示波型

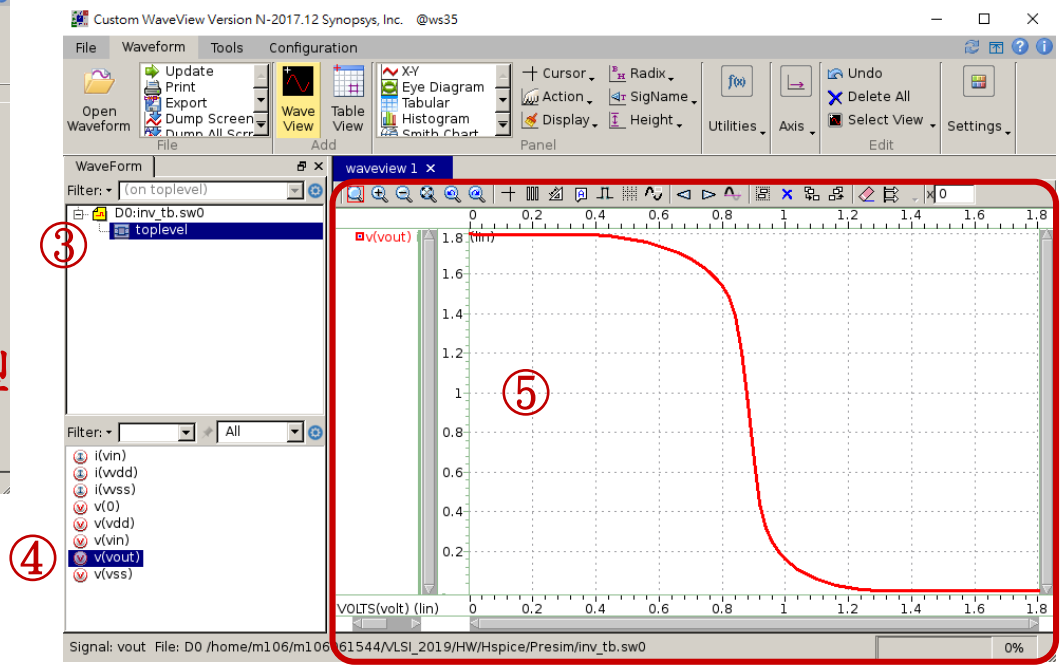
```
[m106061544@ws35 Presim]$ wv &
```

Simulation Flow

#5: Open Waveform

- 點擊 open Waveform





可藉由上方頁籤
Configuration/Preferences/Canvas Background
選擇白底或黑底

Thank you!