

Schematic Building & Hspice Simulation Tutorial

Full-Custom Design Auxiliary Materials

- Model
 - Device parameter
 - Ex : cic018.l
 - For Virtuoso, Hspice
- Technology file
 - Layer definition
 - Ex : laker.tf
 - For laker
- DRC command file
 - Verify Layout
 - Ex : Rule.drc
 - Calibre
- LVS command file
 - Layout Versus Schematic
 - Ex : Rule.lvs
 - Calibre

Simulation Flow

#0 : 先建立一目錄包含以下資料夾(做好檔案管理)

- Virtuoso : (Schematic)
 - 在此層開 icfb 利用 virtuoso (composer) 建立 schematic
- Laker : (Layout)
 - Layout
- Hspice : (Simulation)
 - 需包含 model 檔 (ex : cic018.l)
 - Pre-sim
 - Post-sim

- P.s 可利用 FileZilla 直接建立目錄

檔案名稱	檔案大小	檔案類型	最後修改時間	權限
..				
Hspice		檔案資料夾	2019/9/28 下...	drwxr-xr-x
Laker		檔案資料夾	2019/9/28 下...	drwxr-xr-x
Virtuoso		檔案資料夾	2019/9/28 下...	drwxr-xr-x

Simulation Flow

#1 : 建立 Schematic

- 於 icfb 視窗 **建立新的 library** : File/New/Library...

① File Tools Options Help 1

New Library@ws35

OK Cancel Defaults Apply Help

Library

Name HW1

Directory (non-library directories)

106061544/VLSI_2019/HW/Virtuos

Technology File

If you will be creating mask layout or other physical data in this library, you will need a technology file. If you plan to use only schematic or HDL data, a technology file is not required.

Compile a new techfile

Attach to an existing techfile

Don't need a techfile

Design Manager No DM

②

③

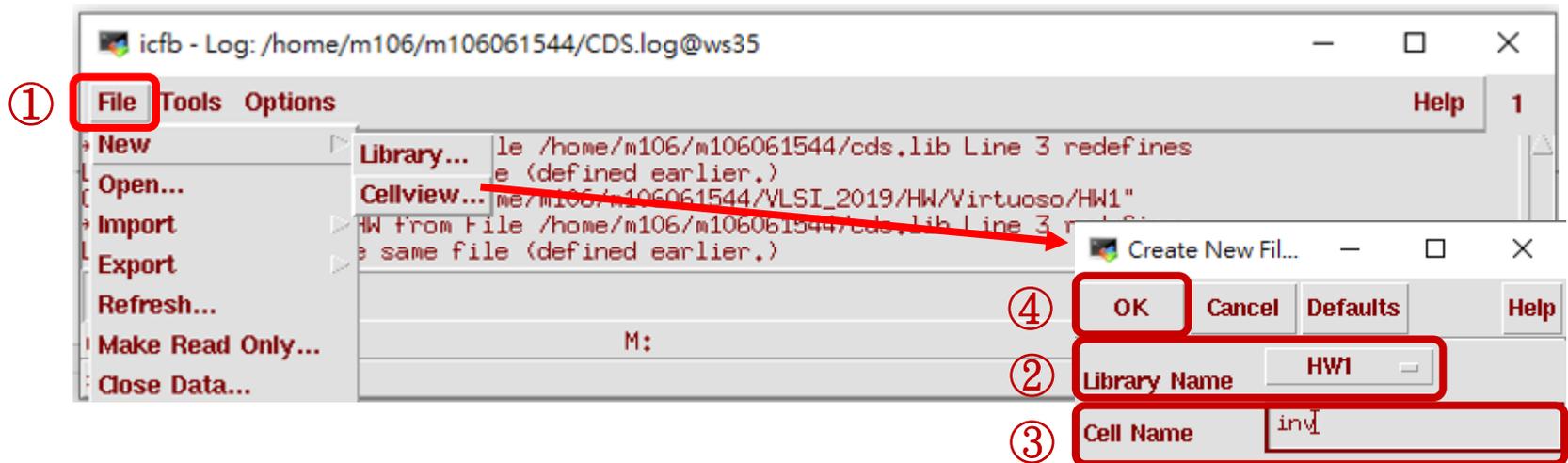
④

- 填入 Library name
- Technology File 選
Don't need a techfile

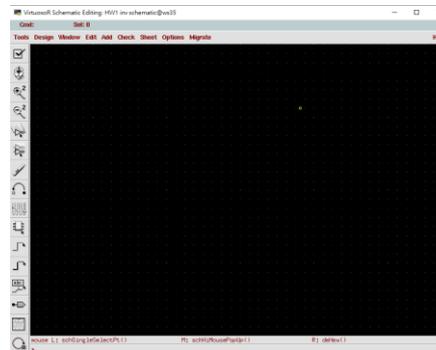
Simulation Flow

#1 : 建立 Schematic

- 於 icfb 視窗 **建立新的schematic** : File/New/Cellview...



- 於 Create New File 視窗選擇 Library
- 鍵入 Cell Name
- 按 OK 會跑出此視窗



Simulation Flow

#1 : 建立 Schematic

- 於 VirtuosoR Schematic 視窗建立電路
- 利用 快捷鍵 i 呼叫 device → 按 Browse → 呼叫 pmos4

選擇 4 端元件

The screenshot shows the VirtuosoR Schematic Editing interface. The main window is titled "VirtuosoR Schematic Editing: HW1 inv schematic@ws35". A dialog box titled "Add Instance@ws35" is open, with the "Library" field set to "HW1" and the "Cell" field set to "inv". A red box highlights the "Browse" button in the "Add Instance" dialog. A red arrow points from the "Browse" button to the "Library Browser" window. The "Library Browser" window is titled "Library Browser - Add Instance@ws35" and shows a list of components. The "Library" column has "analogLib" selected. The "Category" column has "Everything" selected. The "Cell" column has "pmos4" selected. The "View" column has "symbol" selected. A red box highlights the "pmos4" entry in the "Cell" column. A red box highlights the "symbol" entry in the "View" column. The "Library" column also has a red box around "analogLib".

Library	Category	Cell	View
analogLib	Everything	pmos4	symbol
HW1	Everything	n1port	ans
US_8ths	Uncategorized	n2port	auCd1
VLSI_HW	Uncategorized	n3port	auLvs
abdllib	Actives	n4port	cdsSpice
basic	Analysis	nbs1m	hspiceD
cdsDefTechLib	Parasitics	nbs1m4	hspiceS
functional	Passives	njet	spectre
rfExamples	Sources	nnes	spectreS
rfLib		nnes4	
		nncs	
		nncs4	
		nodeQuantity	
		rpn	
		rport	
		nsol	
		nsqip	
		ntft	
		pbs1m	
		pbs1m4	
		pcapacitor	
		pcccs	
		pccvs	
		pdic	
		pdiodic	
		pexp	
		phyres	
		pinductor	
		pjfet	
		pwind	
		pnics	
		pmos4	

Simulation Flow

#1 : 建立 Schematic

- 於 VirtuosoR Schematic 視窗建立電路
- 利用 快捷鍵 i 呼叫 device → 按 Browse → 呼叫 nmos4

選擇 4 端元件

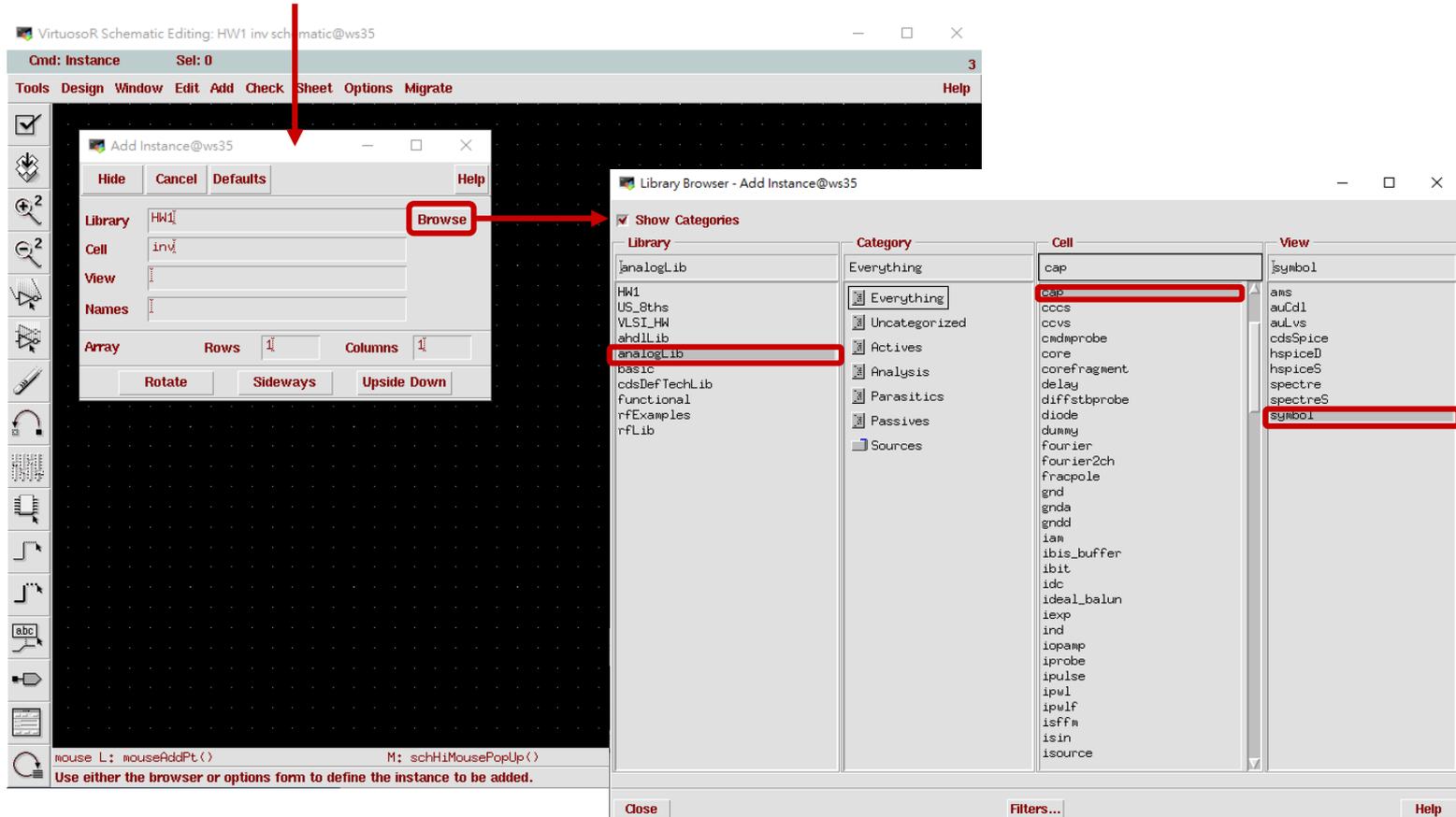
The screenshot shows the VirtuosoR Schematic Editing interface. The main window is titled "VirtuosoR Schematic Editing: HW1 inv schematic@ws35". The "Add Instance@ws35" dialog is open, showing the "Library" field set to "HW1" and the "Cell" field set to "inv". The "Browse" button is highlighted with a red box. The "Library Browser - Add Instance@ws35" window is also open, showing a list of libraries with "analogLib" selected. The "Cell" column shows a list of cells with "nmos4" selected. The "View" column shows "symbol" and "isymoot".

Library	Category	Cell	View
analogLib	Everything	nmos4	symbol
HW1	Everything	gndd	ams
US_0ths	Uncategorized	ian	auCd1
VLSI_HW	Uncategorized	ibis_buffer	auLvs
ahd1Lib	Actives	ibit	cdsSpice
analogLib	Analysis	idc	hspiceD
basic	Parasitics	ideal_balun	hspiceS
cdsDefTechLib	Passives	iexp	spectre
functional	Sources	ind	spectreS
rfeExamples		iopamp	
rflib		iprobe	
		ipulse	
		ipwl	
		ipwlf	
		isffn	
		isin	
		isource	
		ixfwn	
		mind	
		ms1line	
		wt1line	
		n1port	
		n2port	
		n3port	
		n4port	
		nbsim	
		nbsim4	
		njfet	
		nmes	
		nmes4	
		nmos	
		nmos4	
		nmos	
		nmos4	

Simulation Flow

#1 : 建立 Schematic

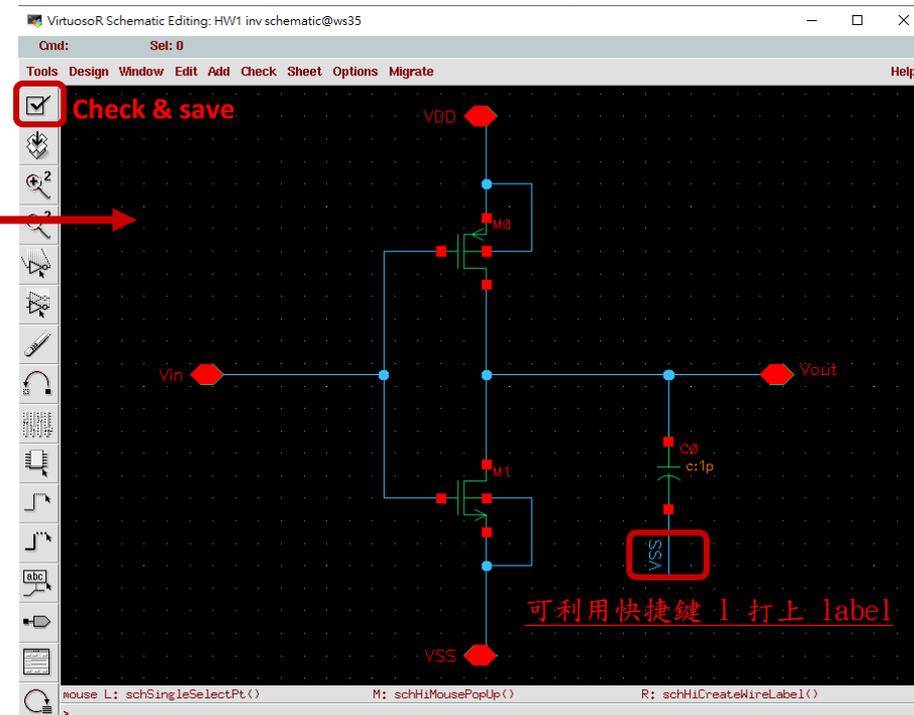
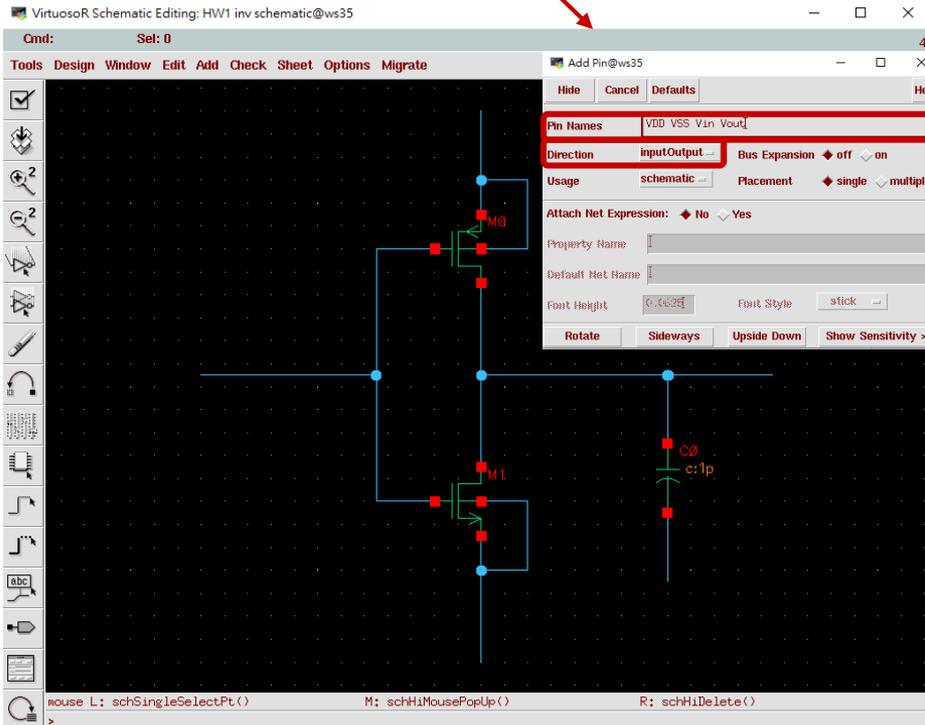
- 於 VirtuosoR Schematic 視窗建立電路
- 利用 快捷鍵 i 呼叫 device → 按 Browse → 呼叫 cap



Simulation Flow

#1 : 建立 Schematic

- 擺放 device
- 按快捷鍵 w 畫連接線，連接元件
- 按快捷鍵 p 放置 I/O PIN，鍵入 PIN name，選 InputOutput



Simulation Flow

#1 : 建立 Schematic

- 選擇元件按 q 可以設定其參數 (W, L, m...)
②

The image shows two windows from the Virtuoso Schematic Editing software. The left window, titled "VirtuosoR Schematic Editing: HW1 inv schematic@ws35", displays a schematic diagram of a common-source amplifier. The circuit includes an input terminal V_{in} , a PMOS transistor $M0$ with parameters $l=180.00n$ and $w=1u$, an NMOS transistor $M1$, a load capacitor $C0$ with value $c=150.00f$, and output terminal V_{out} . Power supply terminals VDD and VSS are also shown. A red circle with the number "1" is placed around the NMOS transistor $M1$. The right window, titled "Edit Object Properties@ws35", shows the properties for the selected NMOS transistor. The "CDF Parameter" table is as follows:

CDF Parameter	Value	Display
Model name		off
Multiplier		off
Width	250.00n M	off
Length	180.00n M	off
Drain diffusion area		off
Source diffusion area		off
Drain diffusion periphery		off
Source diffusion periphery		off
Drain diffusion res squares		off
Source diffusion res squares		off
Drain diffusion length		off
Source diffusion length		off
Temp rise from ambient		off
Estimated operating region		off
Hot-electron degradation		off
Source/drain selector		off
Additional drain resistance		off
Additional source resistance		off
Dist. OD & poly (one side)		off

Simulation Flow

#2 : 轉出 schematic netlist 檔

- 於 icfb 主視窗/File/Export/CDL...

The screenshot illustrates the steps to export a schematic netlist in CDL format. It shows the main window with the File menu open, the Export submenu expanded, and the CDL... option selected. A secondary window for the CDL export options is visible, with the Library Browser button highlighted. A third window, the Library Browser, is shown with the Library field set to 'HM1', the Cell field set to 'inv', and the View field set to 'schematic'. Red circles and arrows indicate the sequence of actions: 1. Clicking File, 2. Clicking Library Browser, 3. Selecting the circuit in the Library Browser, and 4. Clicking Close.

① File → Export → CDL...

② Library Browser

③ 選擇欲轉出 netlist 檔的電路的 Library / cell name / view

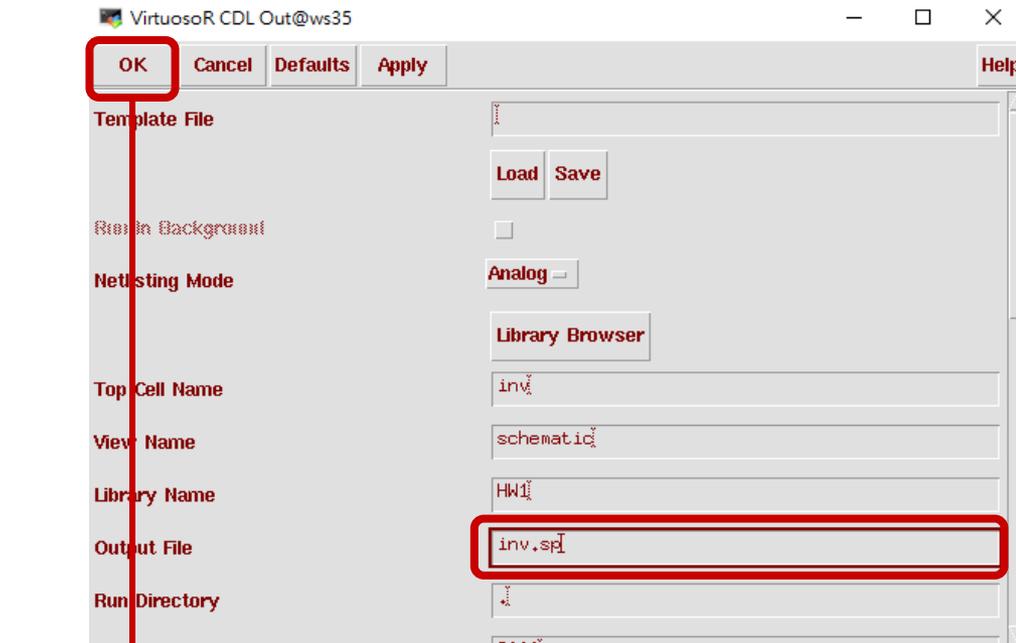
Library	Category	Cell	View
HM1		inv	schematic
HM1		inv	schematic

④ Close

Simulation Flow

#2 : 轉出 schematic netlist 檔

- 回到 Virtuoso CDL out 視窗，於 Output File 鍵入轉出檔案名稱 XXX.sp → 按左上角 OK



P.S 這邊如果有錯誤，通常是因為電路沒有事先做 check and save 的動作，可以先存檔再回來轉

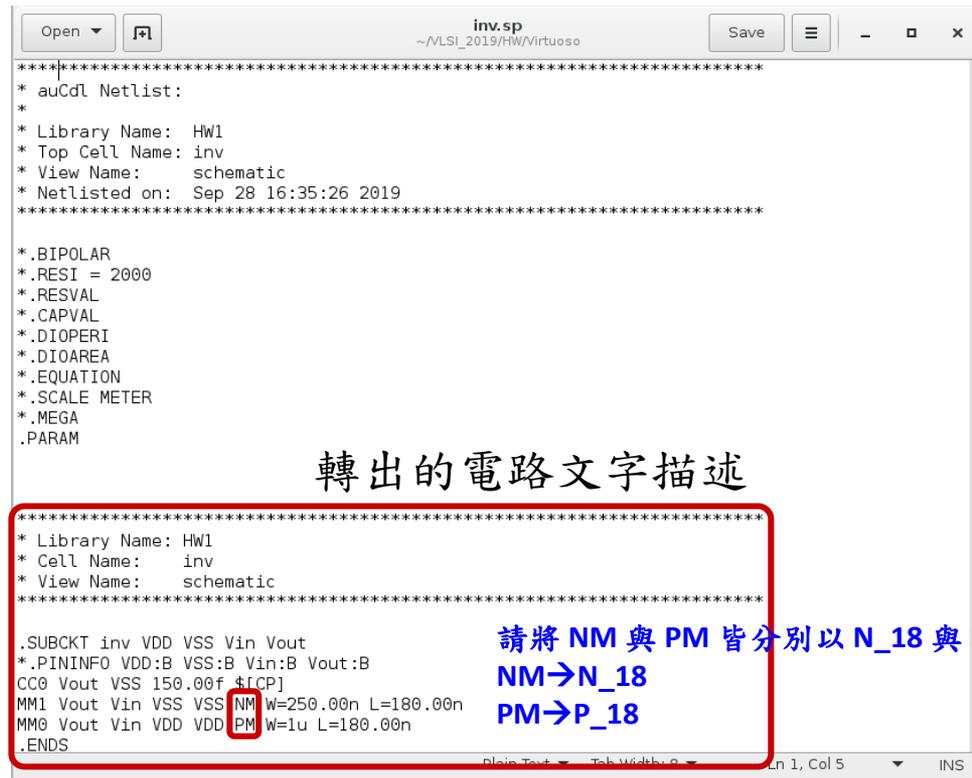


Simulation Flow

#2 : 轉出 schematic netlist 檔

- 打開電路 netlist 檔 : 在 MobaXterm 上鍵入 gedit XXX.sp & (XXX為檔案名稱)

```
[m106061544@ws35 Virtuoso]$ gedit inv.sp &
```



```
*****
* auCdI Netlist:
*
* Library Name: HW1
* Top Cell Name: inv
* View Name: schematic
* Netlisted on: Sep 28 16:35:26 2019
*****

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

*****
* Library Name: HW1
* Cell Name: inv
* View Name: schematic
*****

.SUBCKT inv VDD VSS Vin Vout
*.PININFO VDD:B VSS:B Vin:B Vout:B
CC0 Vout VSS 150.00f $[CP]
MM1 Vout Vin VSS VSS NM W=250.00n L=180.00n
MM0 Vout Vin VDD VDD PM W=1u L=180.00n
.ENDS
```

轉出的電路文字描述

請將 NM 與 PM 皆分別以 N_18 與 P_18 代替
NM→N_18
PM→P_18

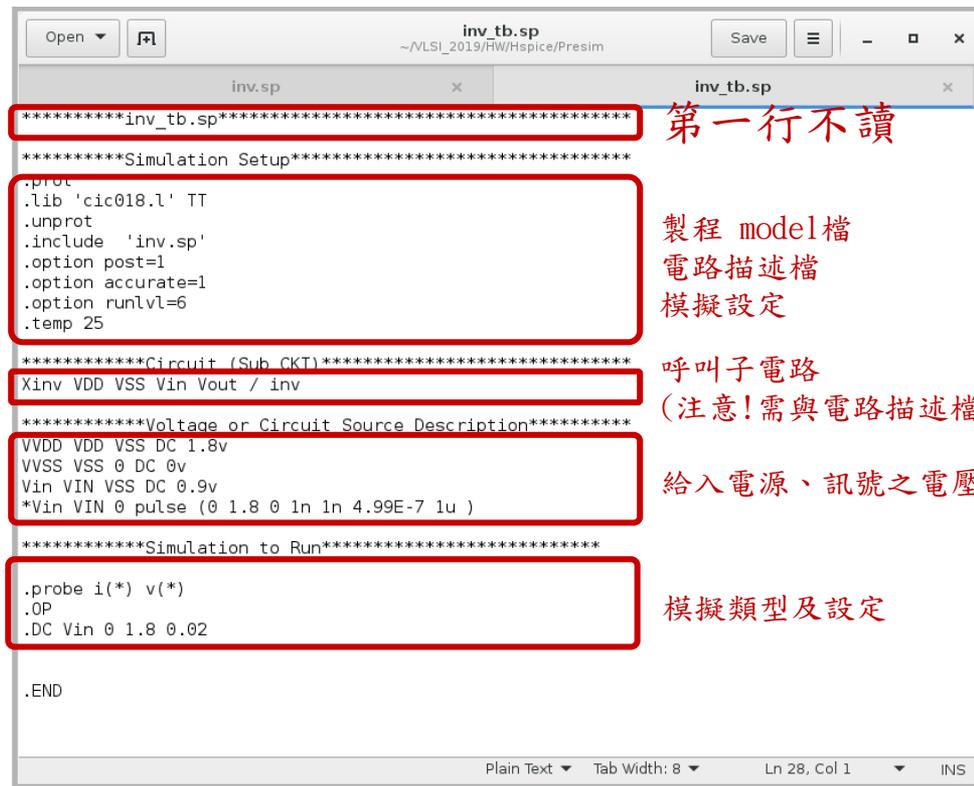
Simulation Flow

關於 Hspice 語法等可以參考下列網址

http://access.ee.ntu.edu.tw/course/vlsi_design_90second/data/spice2001_07.pdf

#3: Prepare for simulation

- 將製程 model 檔(cic018.l)、電路 .sp 檔 (inv.sp) 放至跑模擬的資料夾 (ex: presim資料夾)
- 建立跑模擬的 testbench (ex: inv_tb.sp)



```
*****inv_tb.sp*****
*****Simulation Setup*****
.proct
.lib 'cic018.l' TT
.unprot
.include 'inv.sp'
.option post=1
.option accurate=1
.option runlvl=6
.temp 25

*****Circuit (Sub CKT)*****
Xinv VDD VSS Vin Vout / inv

*****Voltage or Circuit Source Description*****
VVDD VDD VSS DC 1.8v
VVSS VSS 0 DC 0v
Vin VIN VSS DC 0.9v
*Vin VIN 0 pulse (0 1.8 0 1n 1n 4.99E-7 1u )

*****Simulation to Run*****
.probe i(*) v(*)
.OP
.DC Vin 0 1.8 0.02

.END
```

第一行不讀

製程 model 檔
電路描述檔
模擬設定

呼叫子電路
(注意!需與電路描述檔中 I/O PIN 順序一致)

給入電源、訊號之電壓電流描述

模擬類型及設定

Simulation Flow

#4: Simulation

- 編輯完 testbench 後，可以藉由
hspice -i inv_tb.sp -o inv_tb.lis & 跑模擬

```
[m106061544@ws35 Presim]$ hspice -i inv_tb.sp -o inv_tb.lis &
```

- 若顯示結果為 hspice job aborted，則表示模擬未完成，可以依造 inv_tb.lis 檔案內容中的 error information，更正錯誤

```
>info:          ***** hspice job aborted
```

- 若顯示為 hspice job concluded，則表示模擬完成，可於 inv_tb.lis 查看部分分析結果

```
>info:          ***** hspice job concluded
```

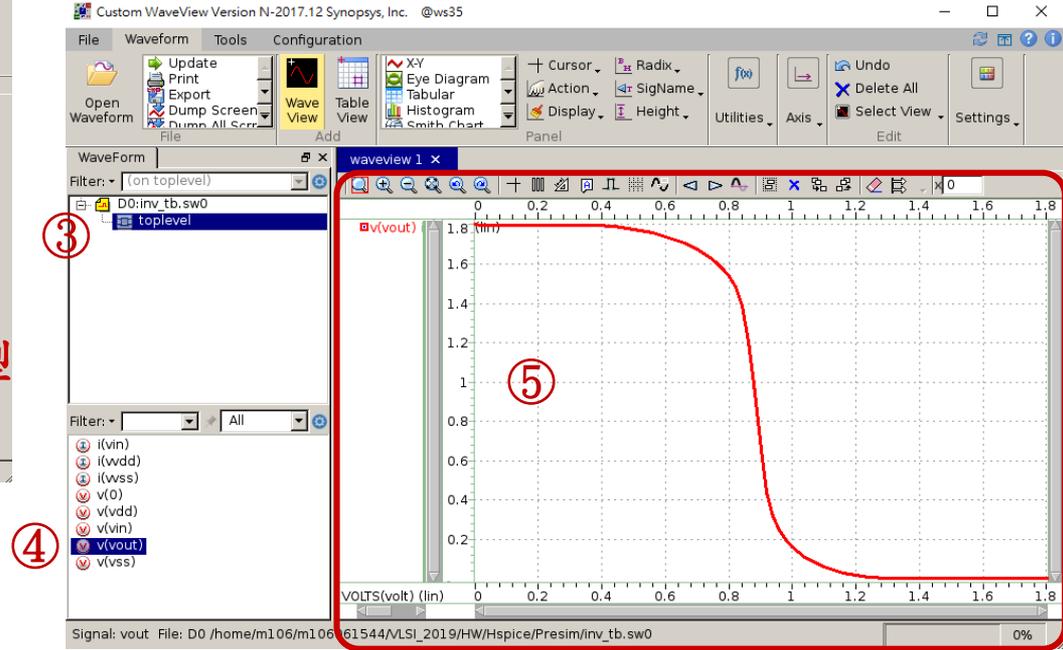
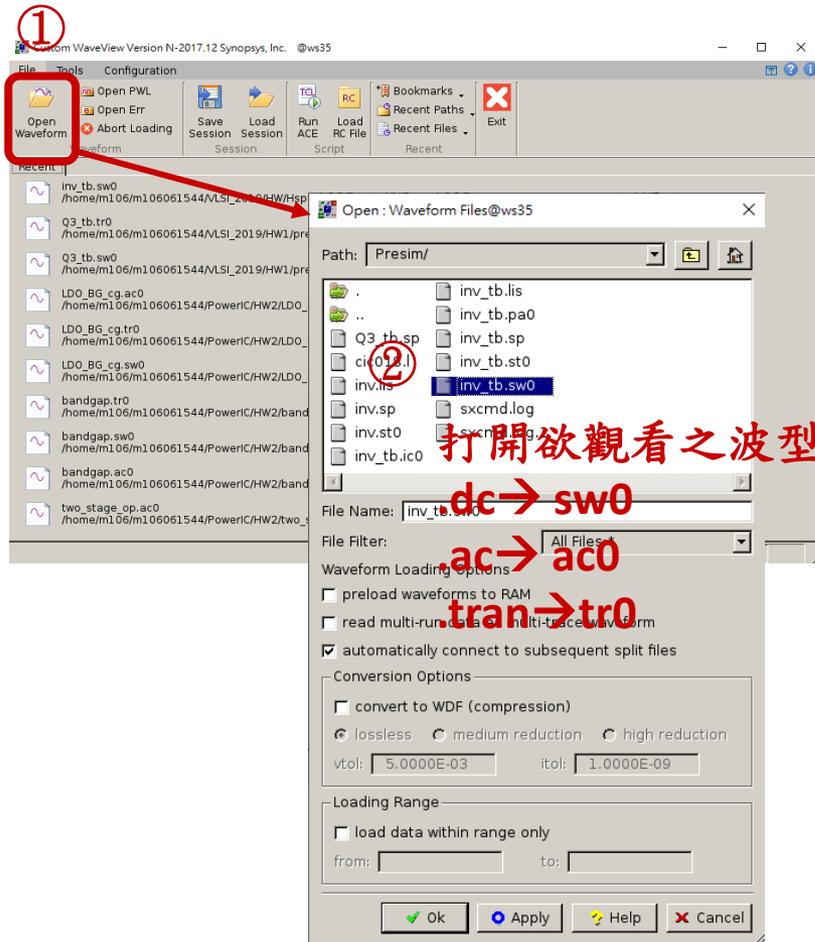
- 若模擬需要查看波型，可以藉由 wv & 指令顯示波型

```
[m106061544@ws35 Presim]$ wv &
```

Simulation Flow

#5: Open Waveform

- 點擊 open Waveform



可藉由上方頁籤
Configuration/Preferences/Canvas Background
選擇白底或黑底

Thank you!