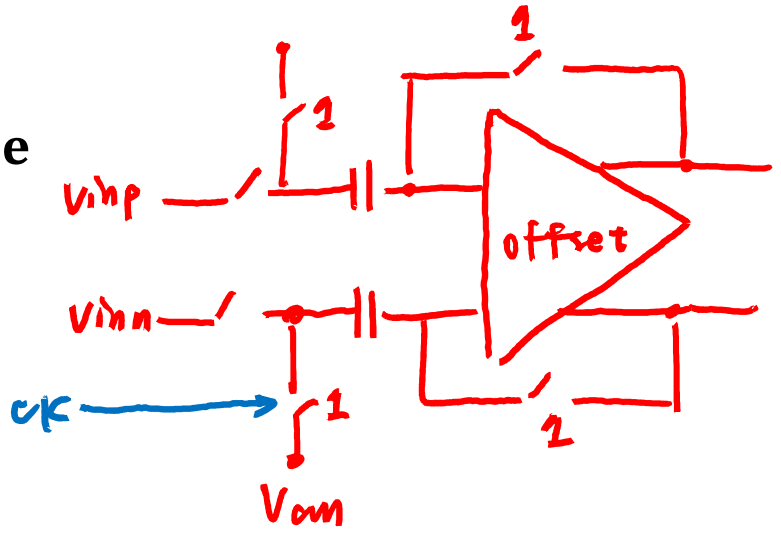
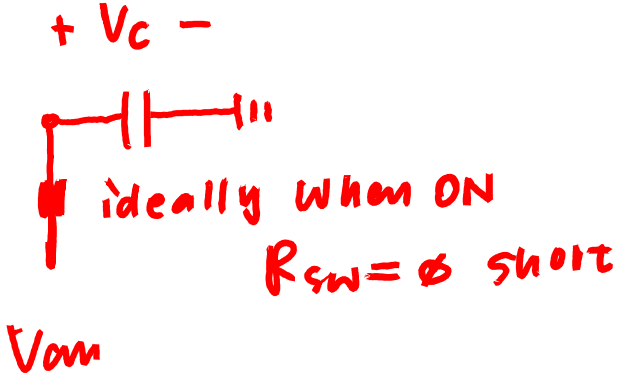
Switches

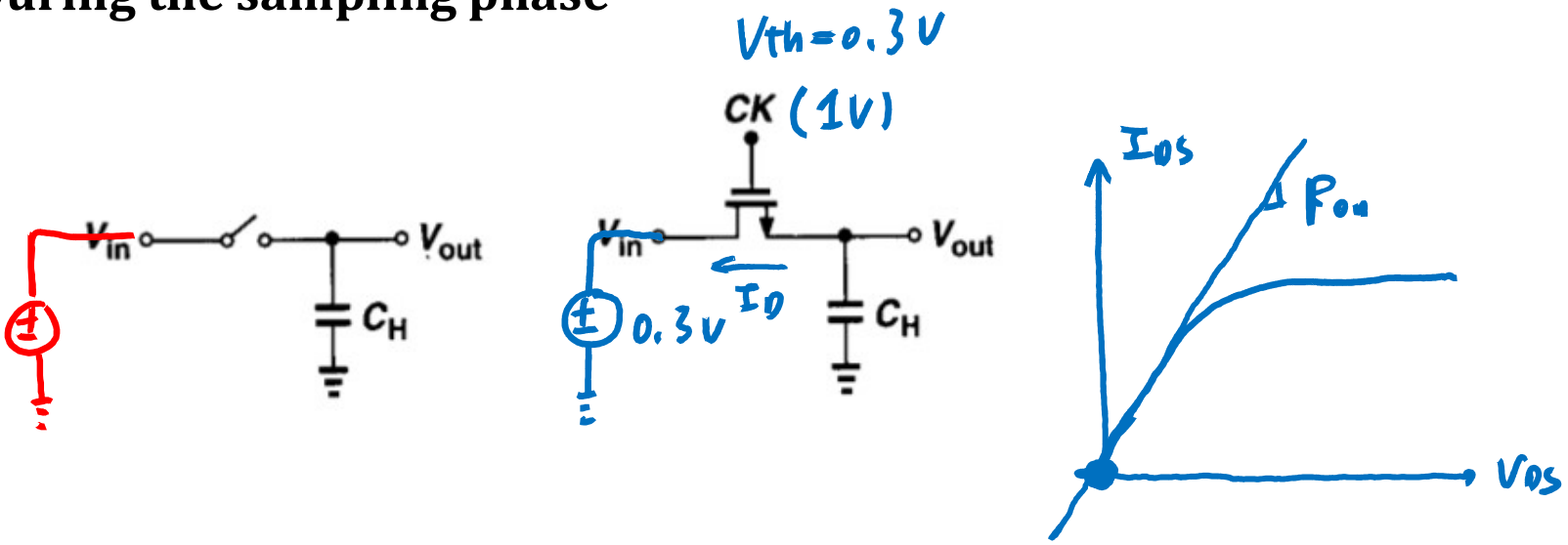
- During the sampling phase





Switches

- **During the sampling phase**



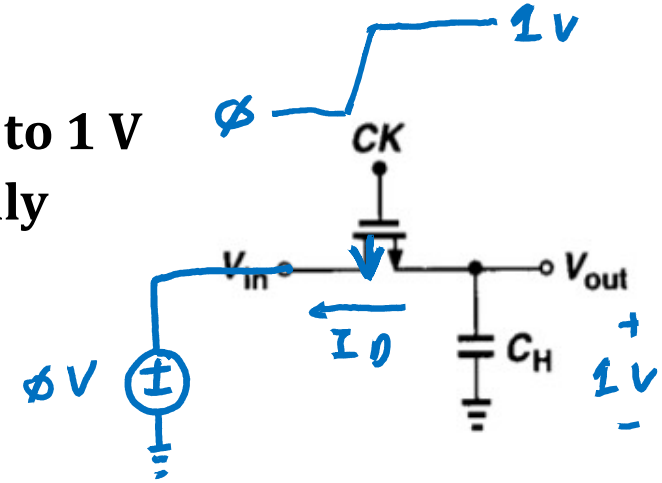
- With VCK of some high value, Vth of 0.3 V, and Vin of 0.3 V
- Once reaching steady state
  - Vout = 0.3
  - The transistor current = 0 → the transistor is ON, but flows no current
  - The transistor operating in deep triode region with certain Ron

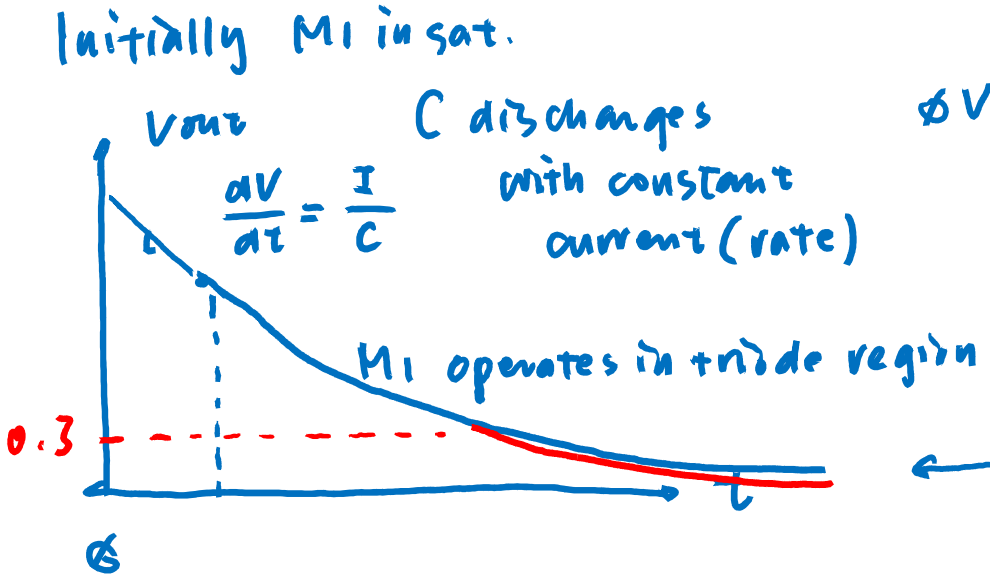
- With VCK=0 the switch is turned OFF

Switches – A Few Cases (I)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

1. **Vin = 0 V while Vout = 1.0 V initially**

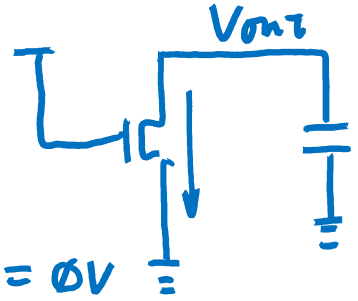




as $t \to \infty$

M1 in deep triode region

$I_D \to 0$

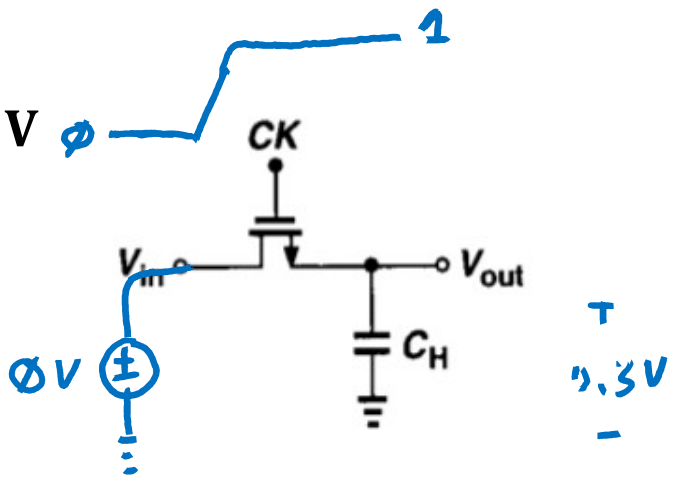


- Through the settling transient
  - The transistor current direction
  - The transistor operating region

Switches – A Few Cases (II)

- Vth of 0.3 V and VCK goes from 0 V to 1 V

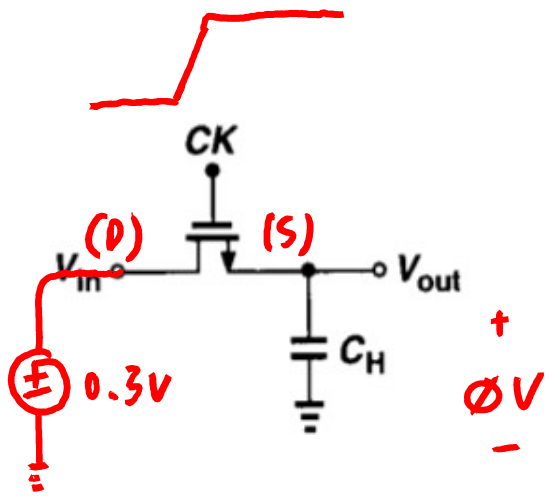
1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially

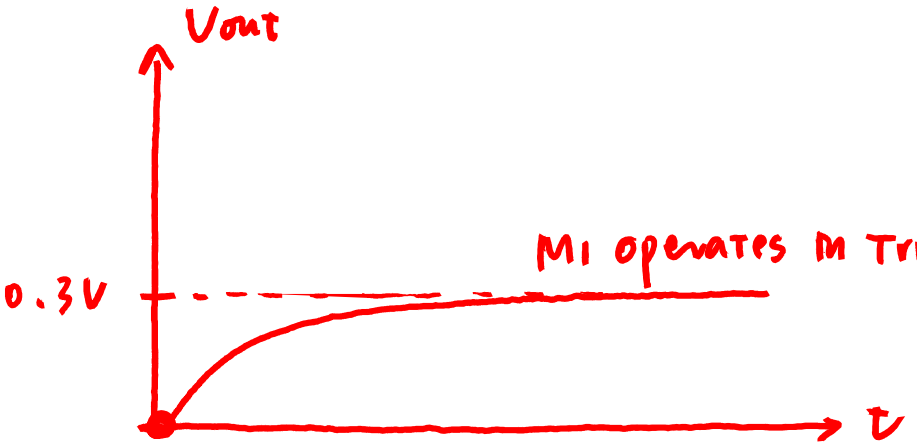


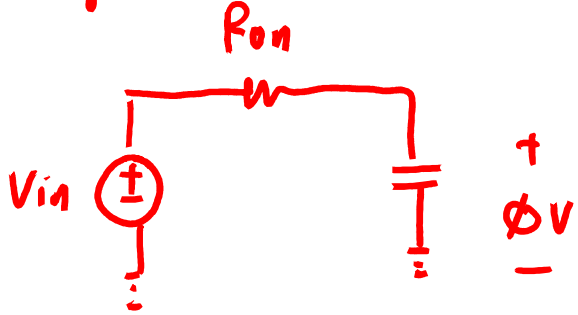
Switches – A Few Cases (III)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

1. **Vin = 0 V while Vout = 1.0 V initially**
2. **Vin = 0 V while Vout = 0.3 V initially**
3. **Vin = 0.3 V while Vout = 0 V initially**





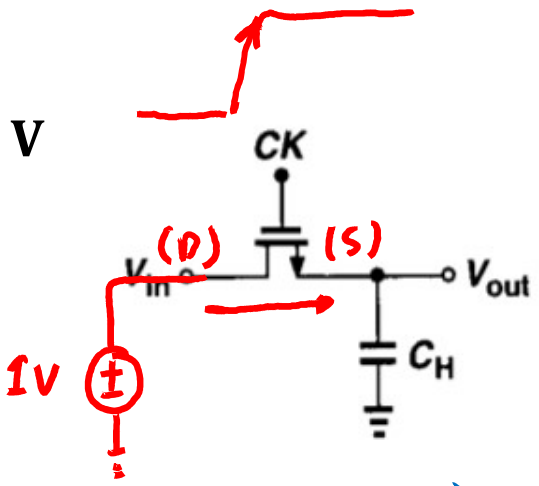


- Through the settling transient
  - The transistor current direction
  - The transistor operating region

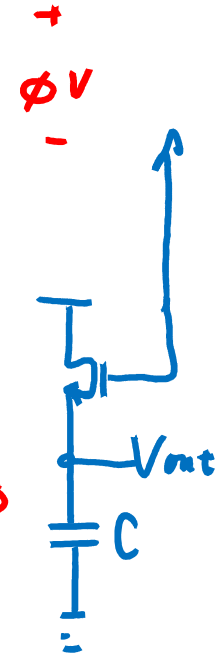
Switches – A Few Cases (IV)

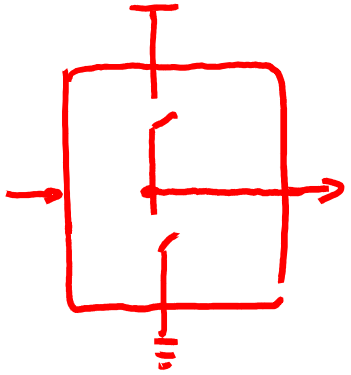
- Vth of 0.3 V and VCK goes from 0 V to 1 V

1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially
3. Vin = 0.3 V while Vout = 0 V initially
4. Vin = 1.0 V while Vout = 0 V initially



$$\frac{dV}{dt} = \frac{I}{C} = f(V_{GS}) = f(V_{DD} - V_{out})$$

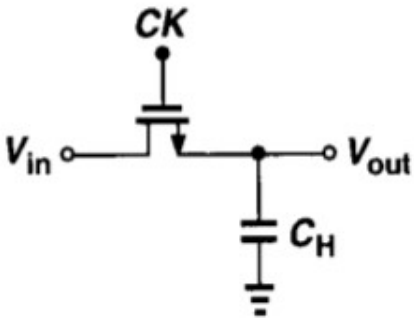




Switches – A Few Cases (IV)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

4. Vin = 1.0 V while Vout = 0 V initially

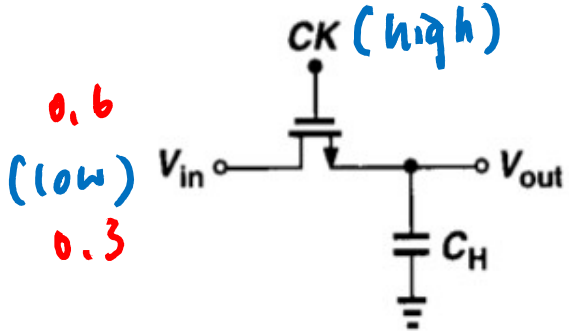


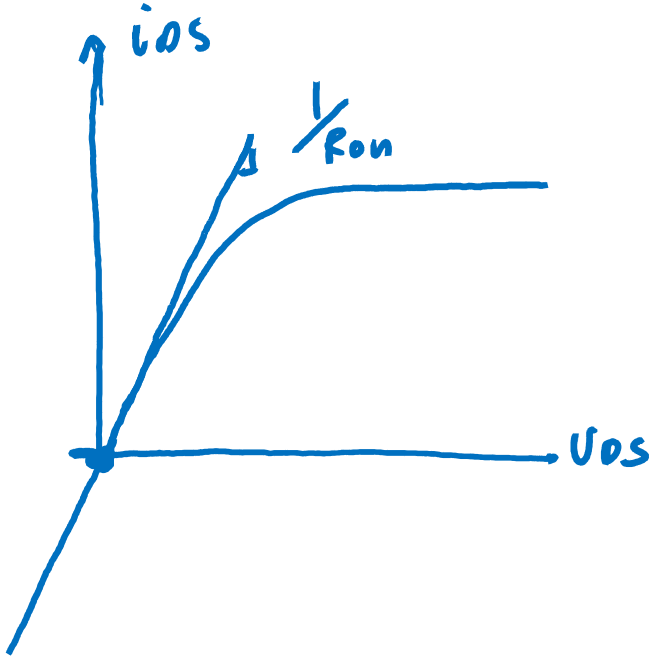
- Through the settling transient
  - The transistor current direction
  - The transistor operating region

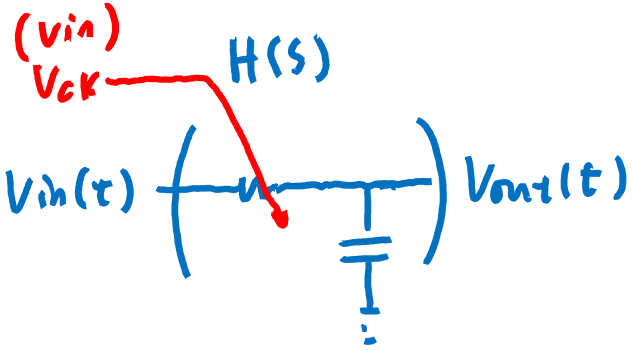
On Resistance

- **Can be viewed as a resistor equal to**

$$R_{on} = \left(\mu C_{ox} \frac{W}{L} (V_{GK} - V_{in} - V_{th}) \right)^{-1}$$

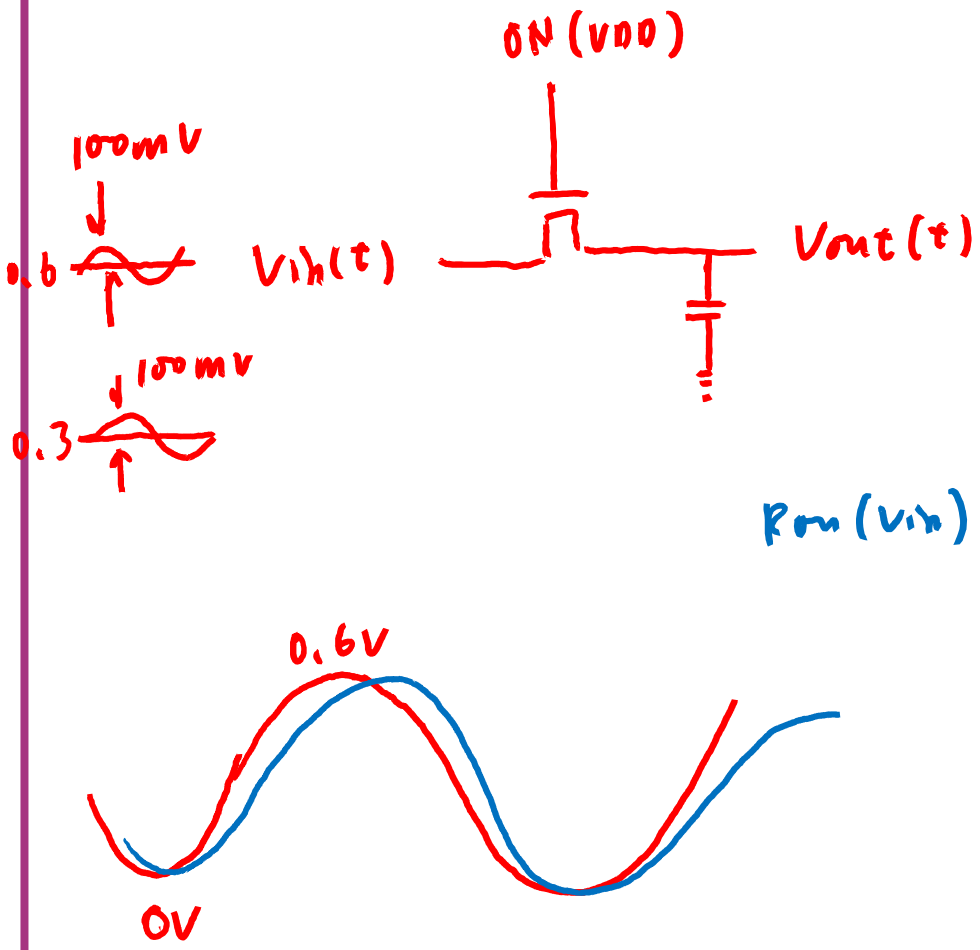






$$H(S) = \frac{\frac{1}{SC}}{R + \frac{1}{SC}} = \frac{1}{1 + SRC}$$

- On-resistance and speed depend on the input level



Nonlinearity

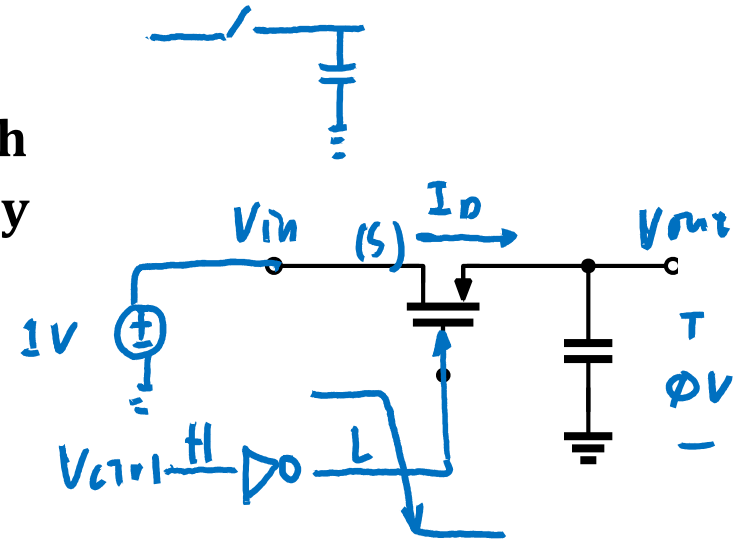
$R_{on}(V_{in})$

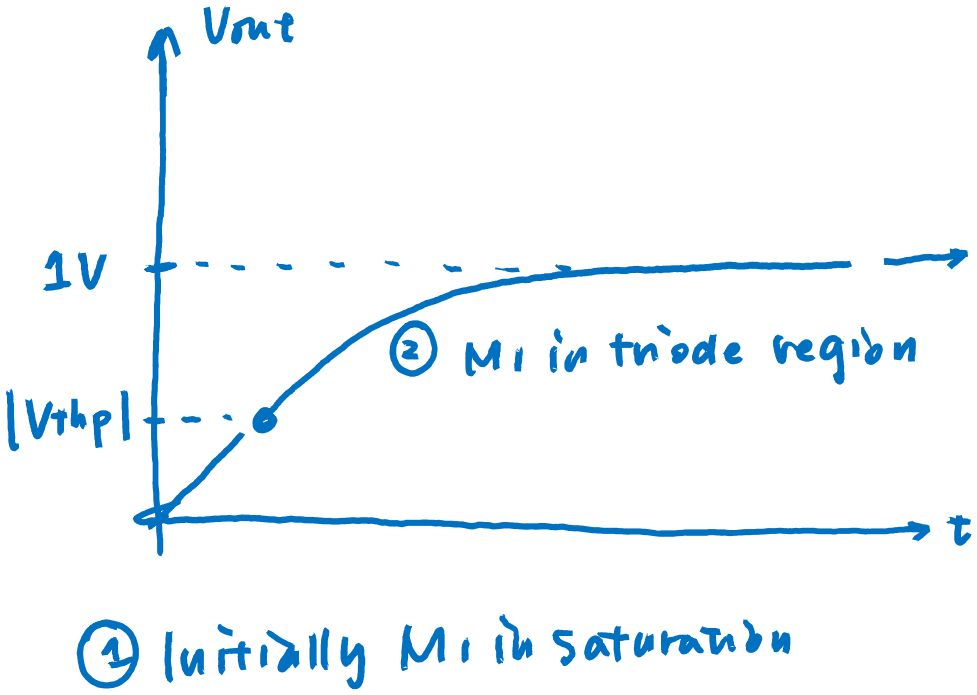
- small-signal operation
  - bias point matters
  - (common-mode)
- large-signal operation
  - waveform distortion

Using PMOS as Switch (I)

- VCK goes down to turn on the switch

1. Vin = 1.0 V while Vout = 0 V initially

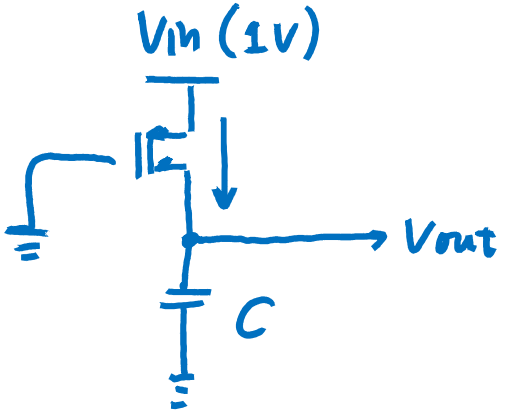




Vout → 1V

IDS → 0V

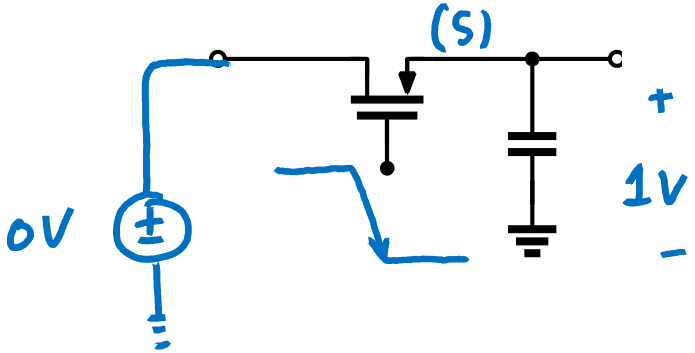
M2 in deep triode region

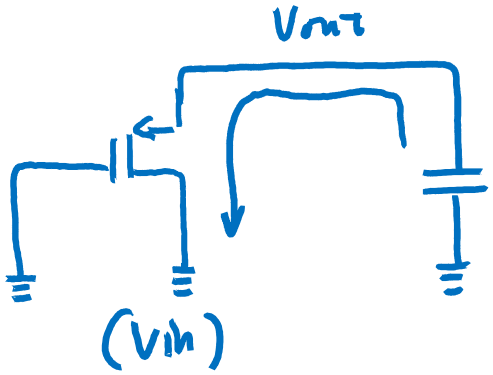


Using PMOS as Switch (II)

- VCK goes down to turn on the switch

2. Vin = 0 V while Vout = 1.0 V initially

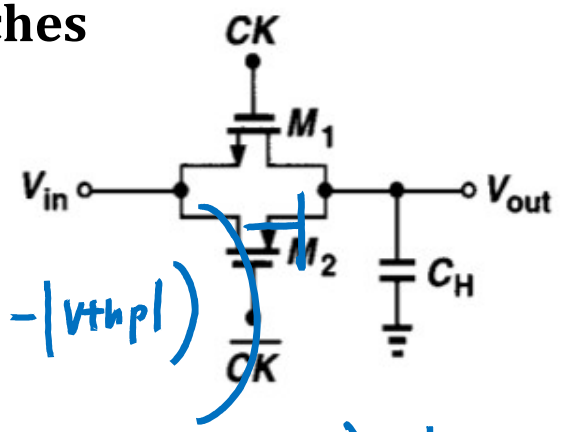




$$R_{on,p} = \left(\mu C_{ox} \frac{W}{L} \left(V_{in} - \underset{(V_{CF})}{0V} - |V_{thp}| \right) \right)^{-1}$$

Pass Transistors

- **Transmission gates or Complementary switches**
  - Complementary clock signals needed

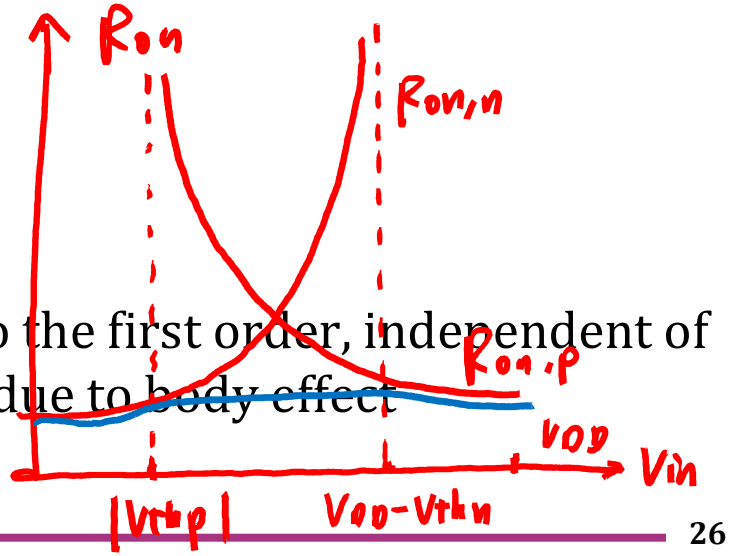


$$R_{on,eff} = R_{on,n} \parallel R_{on,p}$$

$$= \left(\mu_n C_{ox} \frac{W}{L_n} (V_{DD} - V_{in} - V_{thn}) + \mu_p C_{ox} \frac{W}{L_p} (V_{in} - |V_{thp}|) \right)^{-1}$$

$$= \left((\mu_p C_{ox} \frac{W}{L_p} - \mu_n C_{ox} \frac{W}{L_n}) V_{in} + \mu_n C_{ox} \frac{W}{L_n} (V_{DD} - V_{thn}) - \mu_p C_{ox} \frac{W}{L_p} |V_{thp}| \right)^{-1}$$

$$\Rightarrow \frac{\mu_p C_{ox} \frac{W}{L_p}}{\mu_n C_{ox} \frac{W}{L_n}} = 1 \Rightarrow \frac{\frac{W}{L_p}}{\frac{W}{L_n}} \cong \frac{\mu_n}{\mu_p}$$

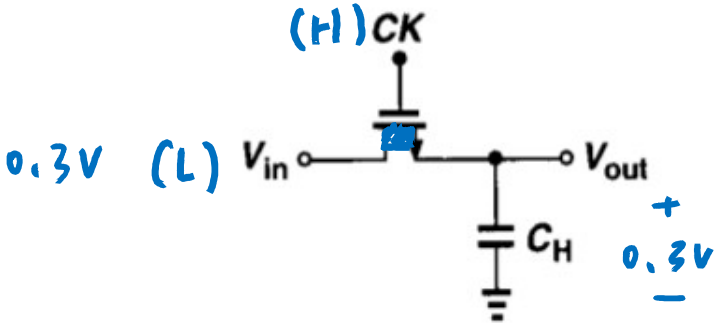


- Can be sized so that the on-resistance is, to the first order, independent of the input level → Vthp and Vthn still vary due to body effect

Charge Injection

- **In order to reduce Ron and speed up the operation**

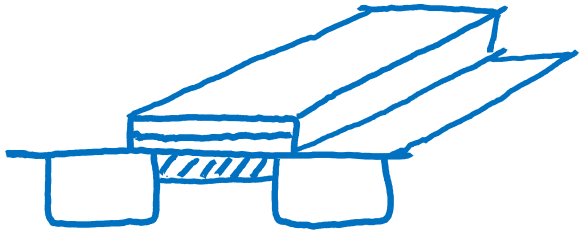
1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor



inversion layer

$Q = CV$ 其中 $C = WL \cdot C_{ox}$

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

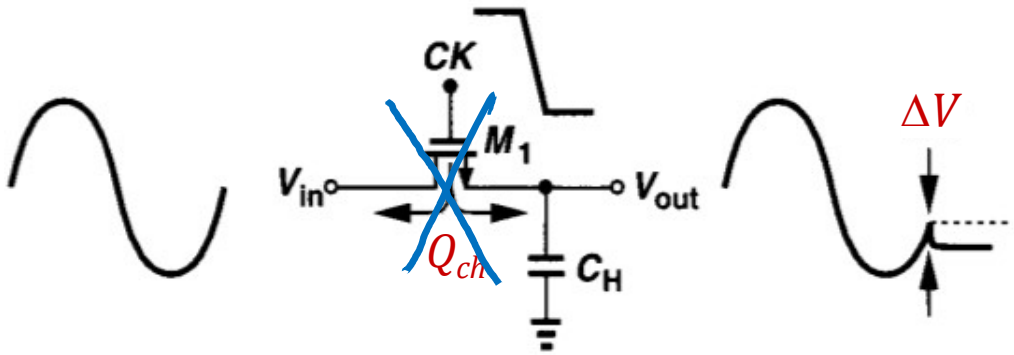


- Charge in the channel when ON

Charge Injection

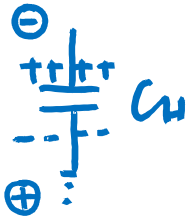
- **In order to reduce Ron and speed up the operation**

1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor



$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$



- Charge in the channel when ON

→ Causing a pedestal at the output when turning OFF