EE4280 Lecture 8: Switched-Capacitor Circuits

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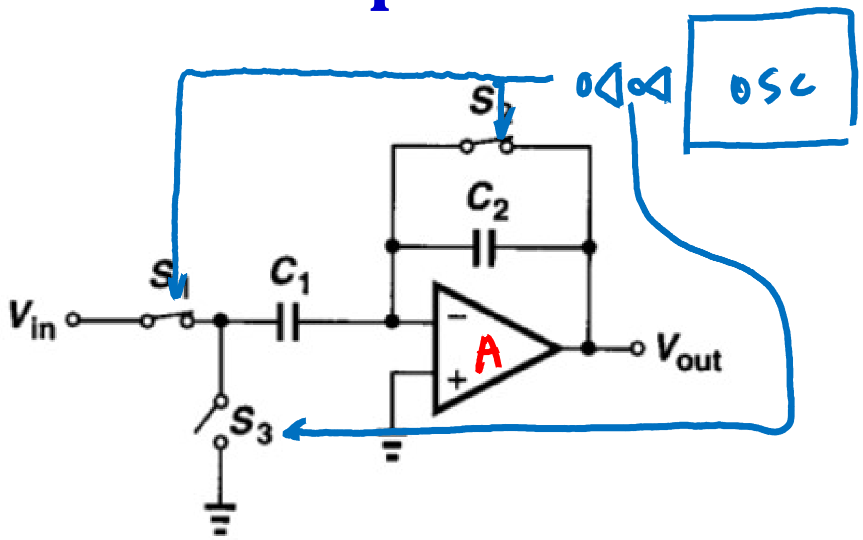
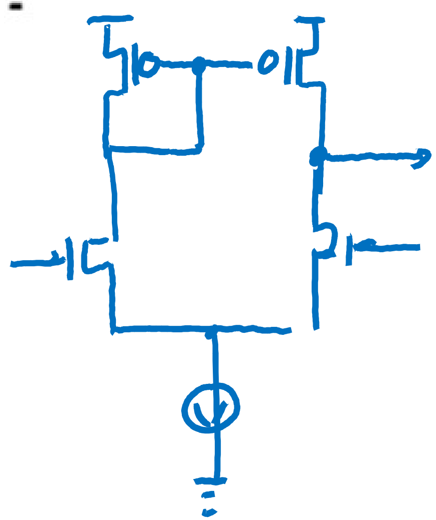
One Switched-Capacitor Circuit Example

- **Some capacitors**
- **Some switches**
  - Control signals needed
  - Typically 180° out-of-phase
  - → Two-phase operation



- **An operational amplifier**
  - High voltage gain
  - Differential input
  - Single-ended output



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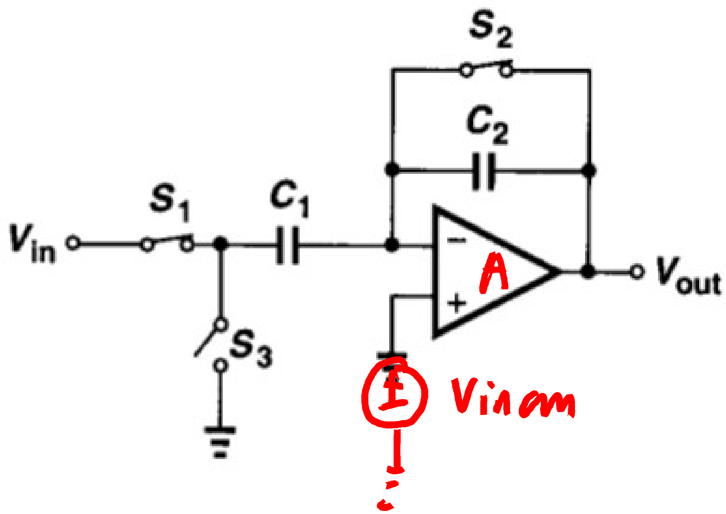

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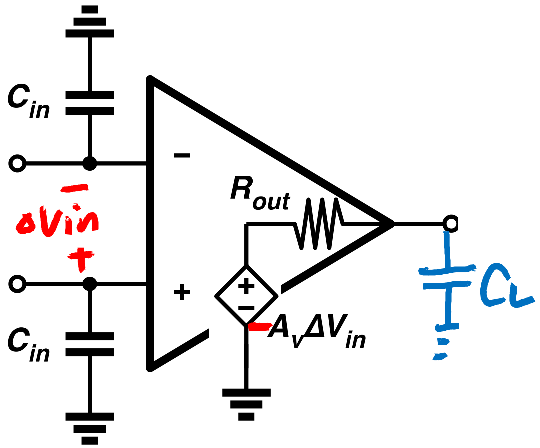
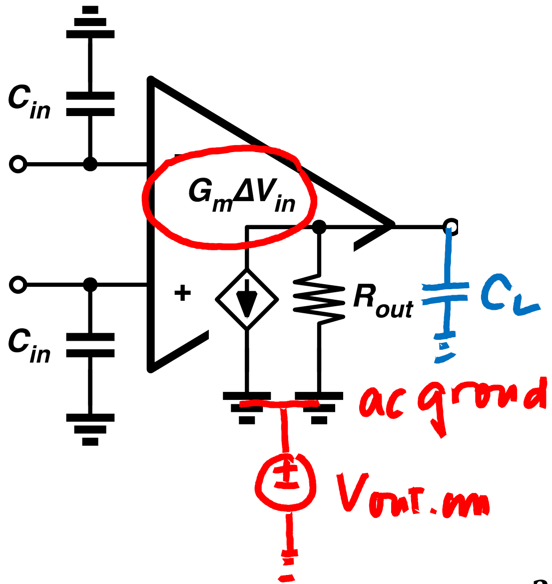
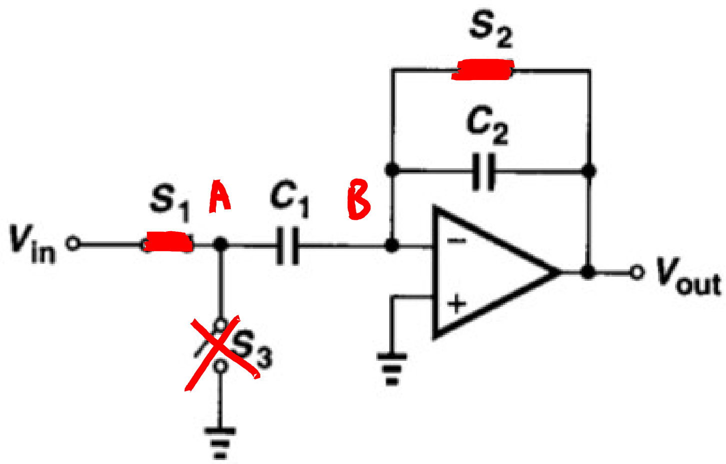




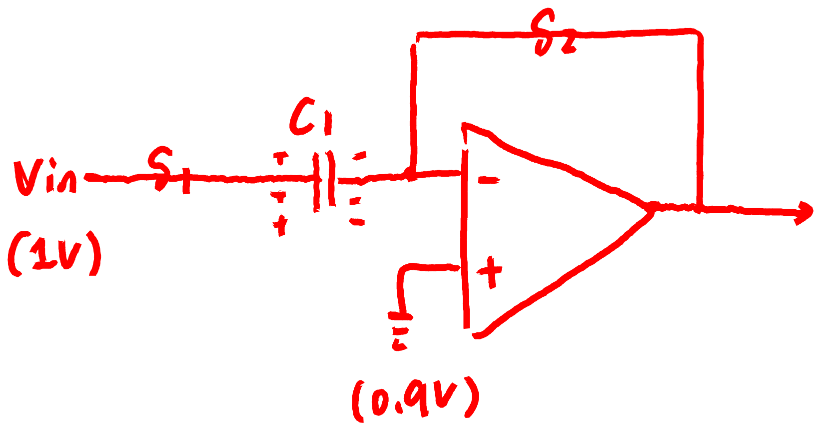
Operations – Phase #1

- **S1 and S2 are ON**

Sampling phase



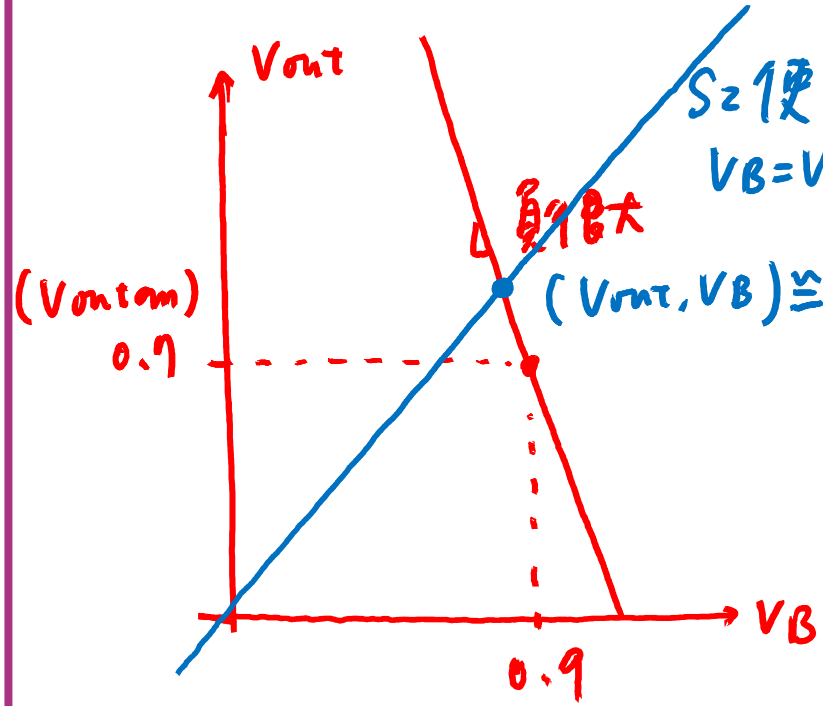
※ consider DC input

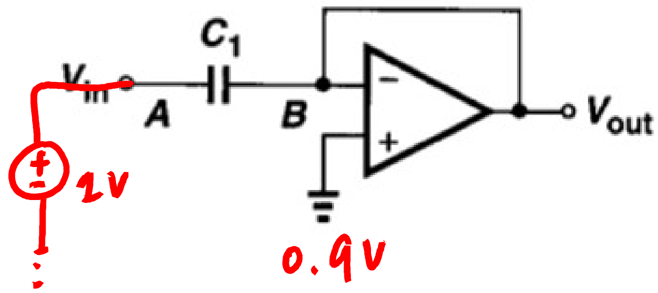


Operations – Phase #1

- **S1 and S2 are ON**
  - S2 provides a unity-gain feedback

DC input



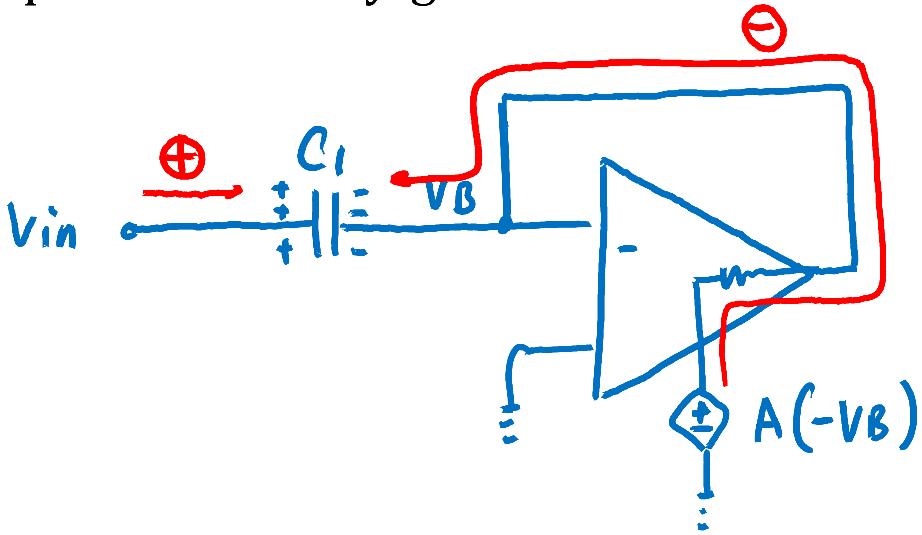


$(V_{out}, V_B) \cong (0.9, 0.9) = (V_{incm}, V_{incm})$

virtual short through nega FB

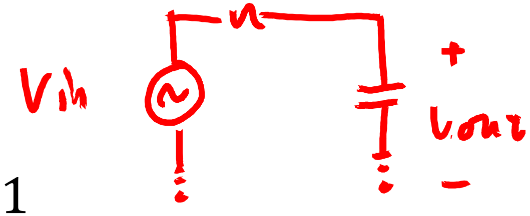
Operations – Phase #1

- **S1 and S2 are ON**
  - S2 provides a unity-gain feedback



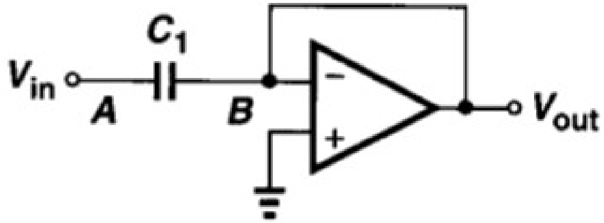
- The negative input port transient
- Once reaching steady state
  - Virtual ground or virtual short
  - No current flowing into input
  - No voltage across C2

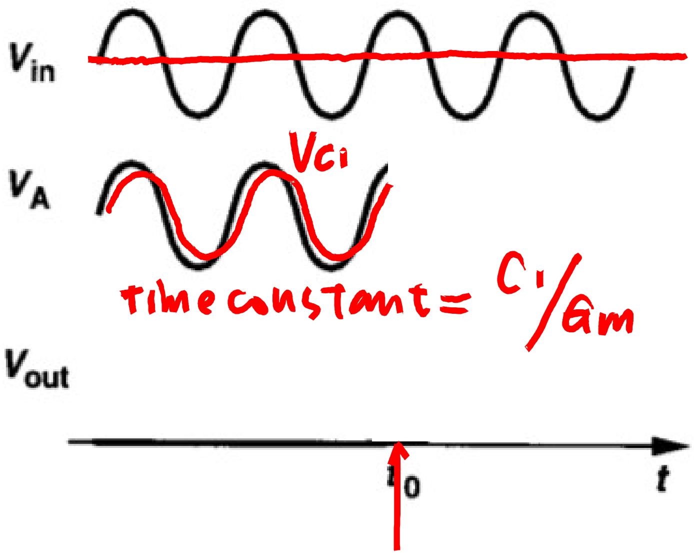
Operations – Phase #1

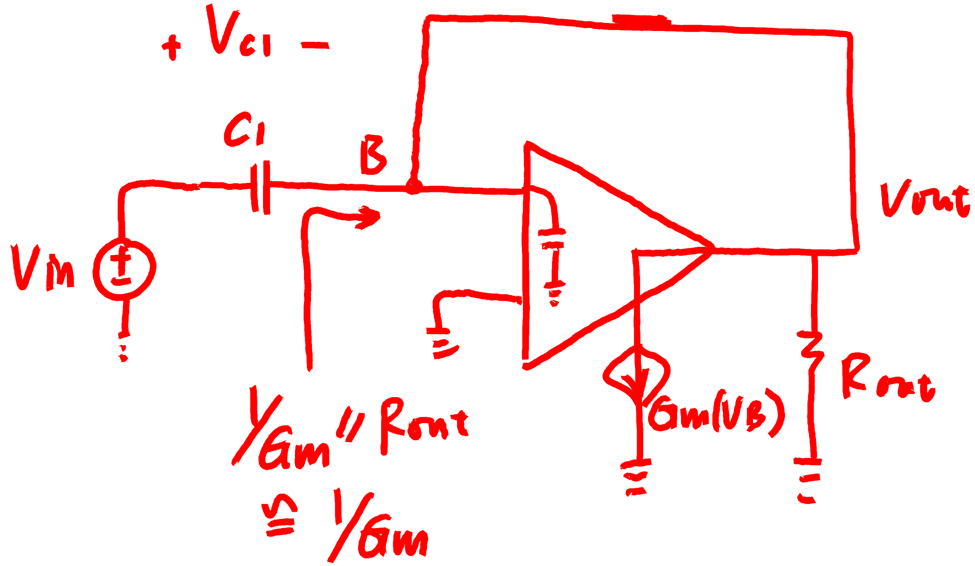


- **S1 and S2 are ON**
- S1 connects C1 to Vin → sampling Vin across C1

→ Sampling Phase





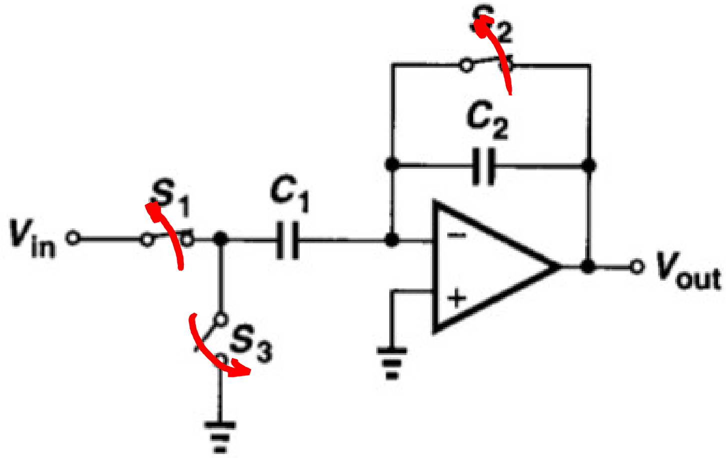


Operation – Phase #2

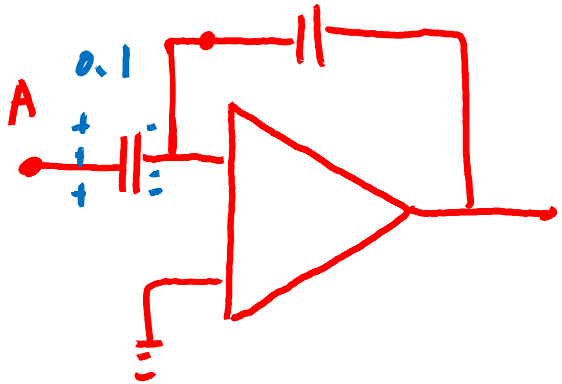
- S1 and S2 gets turned **OFF**
- S3 is then turned **ON**

有順序

一般來說 $\underline{S_2 \to S_1} \to S_3$



B becomes high-Z node

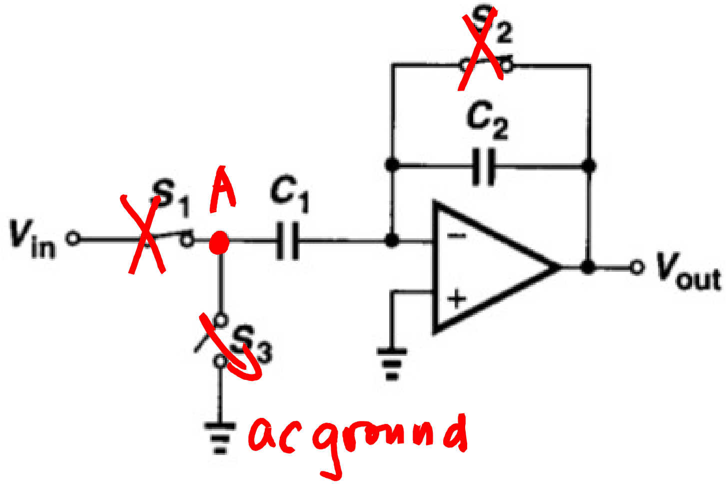


* node A becomes floating

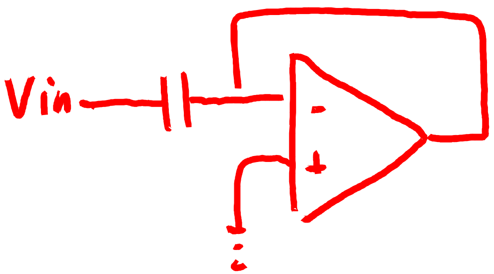
* but all voltages are the same

Operation – Phase #2

- **S1 and S2 gets turned OFF**
  - Charges remain on capacitors
- **S3 is then turned ON**
  - Pull the left plate of C1 from Vin to ground



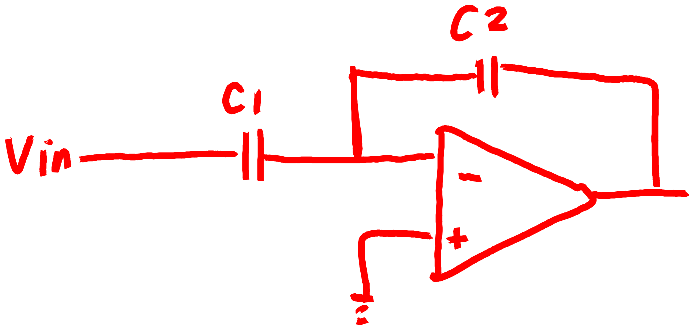
phase # 1



loop gain = A

比較有 stability concern

phase # 2



$$\text{loop gain} = \left(A \frac{C_2}{C_1 + C_2}\right)$$

Operation – Phase #2

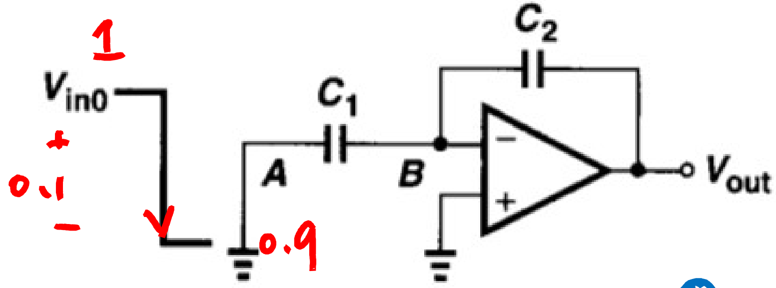
positive gain

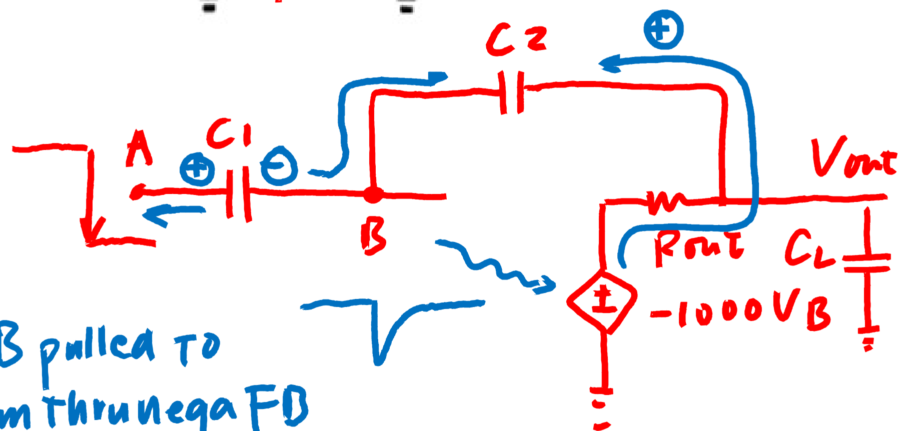
non-inverting amp

- **S1 and S2 gets turned OFF**
  - Charges remain on capacitors
- **S3 is then turned ON**
  - Pull the left plate of C1 from Vin to ground

→ Charge gets transferred

→ Amplification Phase

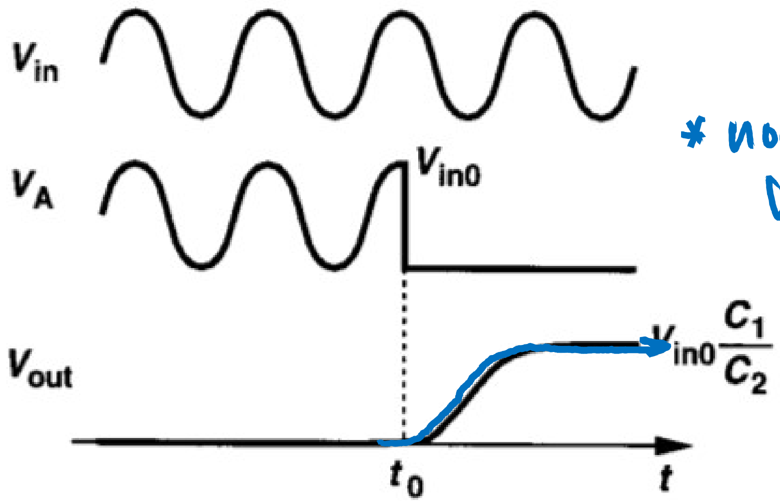




* node B pulled to Vin0 thru nega FB

* charges transferred from C1 to C2

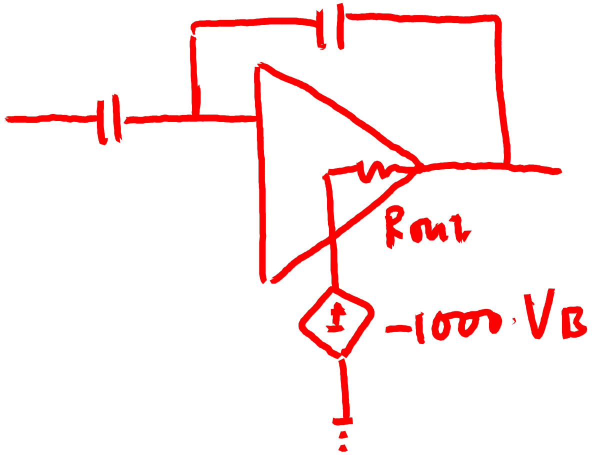
$\Delta V_{out} = \Delta V_{in} \cdot C_1/C_2$

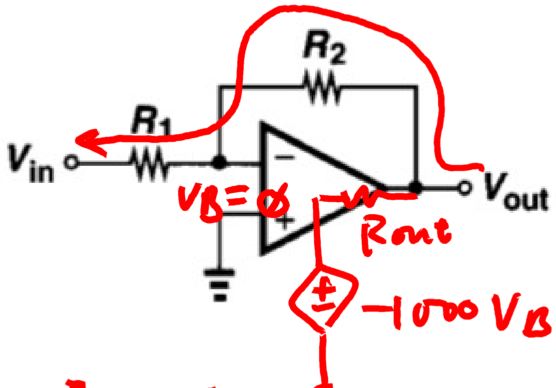


- **Non-inverting amplifier**
- **Sampling timing**
- **Stability considerations**

Continuous-Time Example

- **To amplify the input signal with resistive feedback**
  - Ideal voltage gain





$$I_{R1} = I_{R2}$$

$$\frac{V_B - V_{in}}{R_1} = \frac{V_{out} - V_B}{R_2}$$

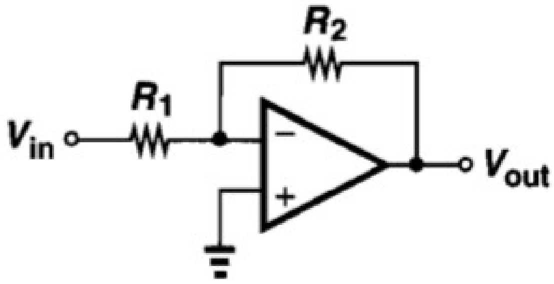
$$V_B = 0 \longleftarrow A \to \infty$$

$$\frac{V_{out}}{V_{in}} = \frac{-R_2}{R_1}$$

Continuous-Time Example

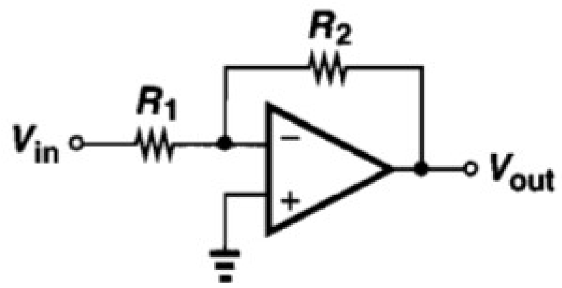
- **To amplify the input signal with resistive feedback**
  - Ideal voltage gain

- **A few more details:**
  - Voltage sensing – current feedback
  - Loading effect on open-loop gain (when considering Rout of opamp)



Continuous-Time Example

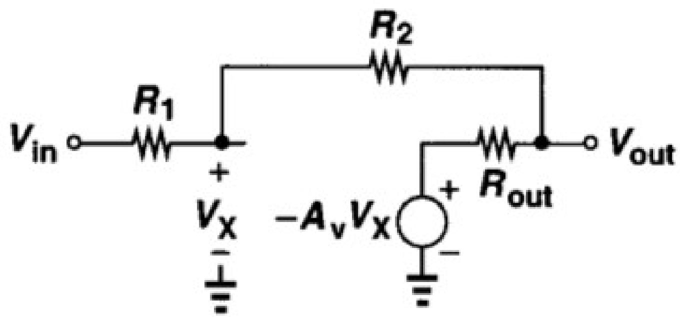
- **To amplify the input signal with resistive feedback**
  - Ideal voltage gain



- **A few more details:**
  - Voltage sensing – current feedback
  - Loading effect on open-loop gain (when considering Rout of opamp)

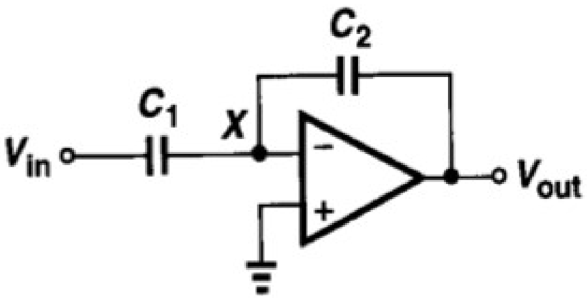
  - R2 flows current that comes from Rout

→ Degrading voltage gain from Vx to Vout



With Capacitive Feedback

- Loading effect can be avoid
- Need a mechanism to set the bias point of Vx



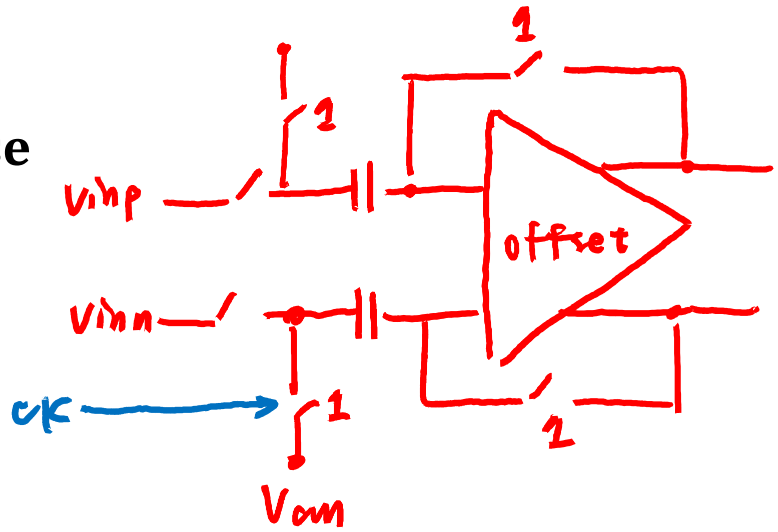
- Transfer function and Bode plot

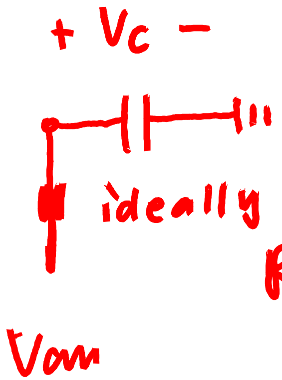
- Accuracy

Switches

offset

- During the sampling phase



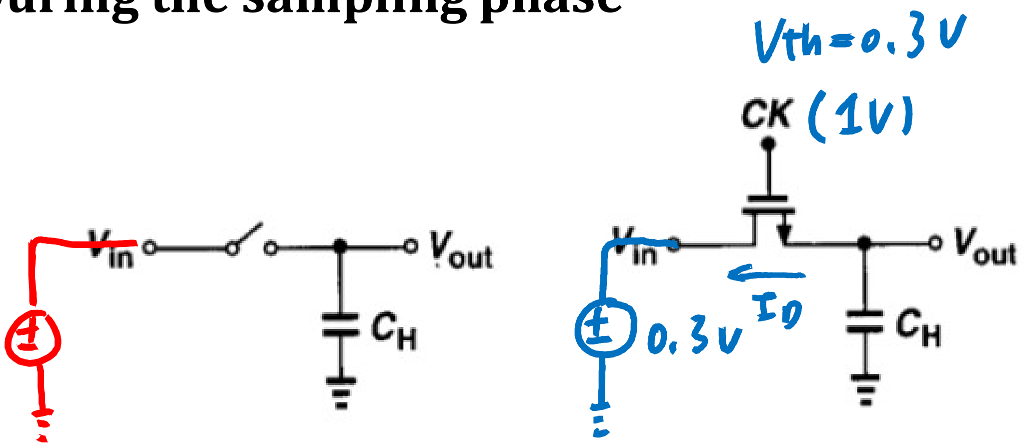


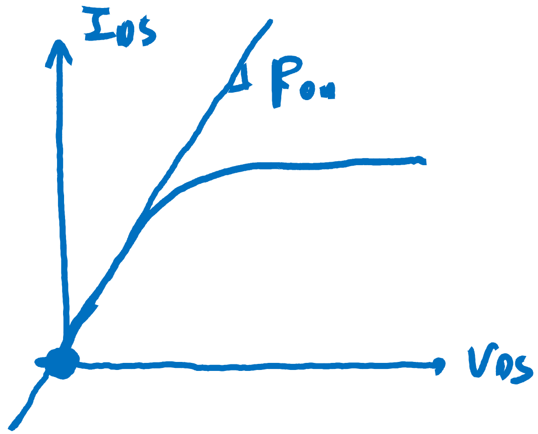
ideally when ON

$R_{sw} = \emptyset$ short

Switches

- **During the sampling phase**





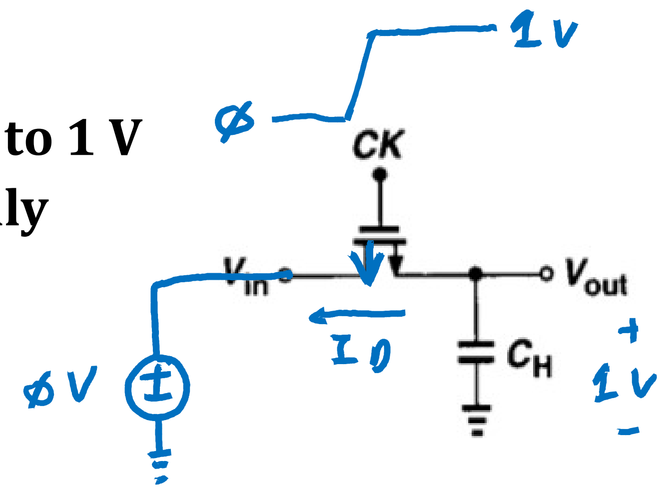
- With VCK of some high value, Vth of 0.3 V, and Vin of 0.3 V
- Once reaching steady state
  - Vout = 0.3
  - The transistor current = ∅ — the transistor is ON, but flows no current
  - The transistor operating in deep triode region with certain Ron

- With VCK=0 the switch is turned OFF

Switches – A Few Cases (I)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

1. Vin = 0 V while Vout = 1.0 V initially

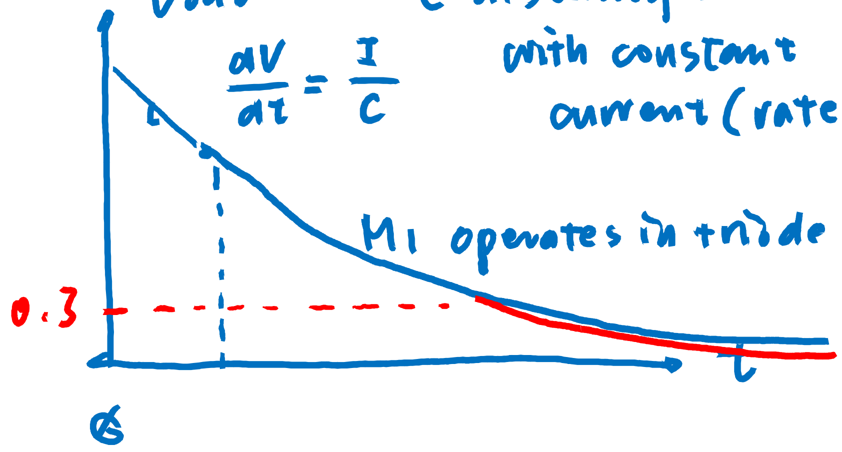


Initially M_1 in sat.

C discharges with constant current (rate)

$$\frac{dV}{dt} = \frac{I}{C}$$

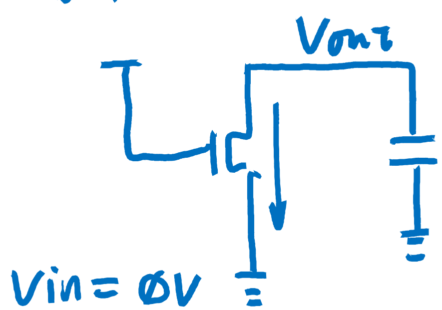
M_1 operates in triode region



as $t \to \infty$

M_1 in deep triode region

$I_D \to 0$

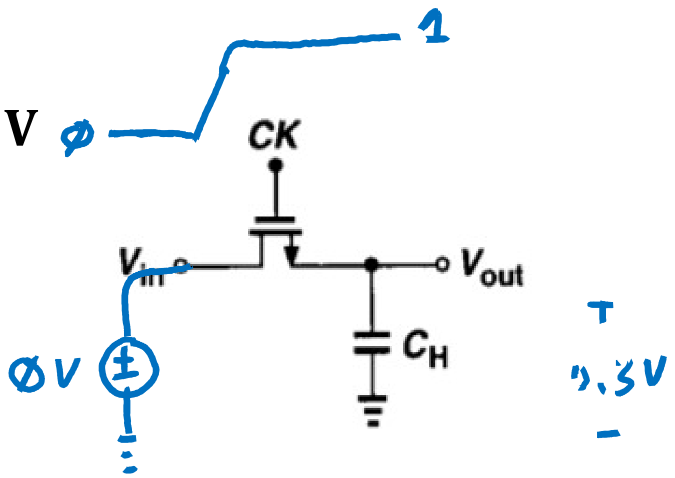


- Through the settling transient
  - The transistor current direction
  - The transistor operating region

Switches – A Few Cases (II)

- Vth of 0.3 V and VCK goes from 0 V to 1 V

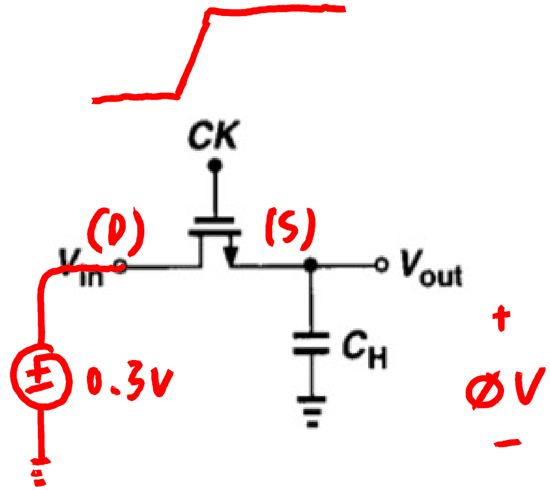
1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially

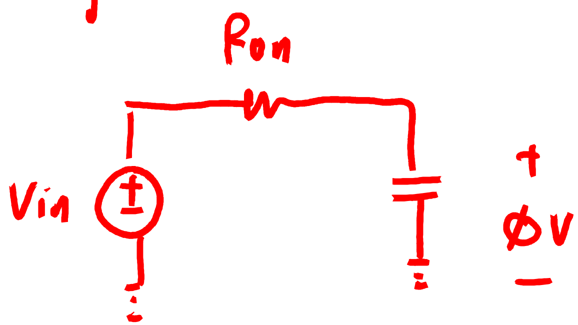


Switches – A Few Cases (III)

- Vth of 0.3 V and VCK goes from 0 V to 1 V

1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially
3. Vin = 0.3 V while Vout = 0 V initially



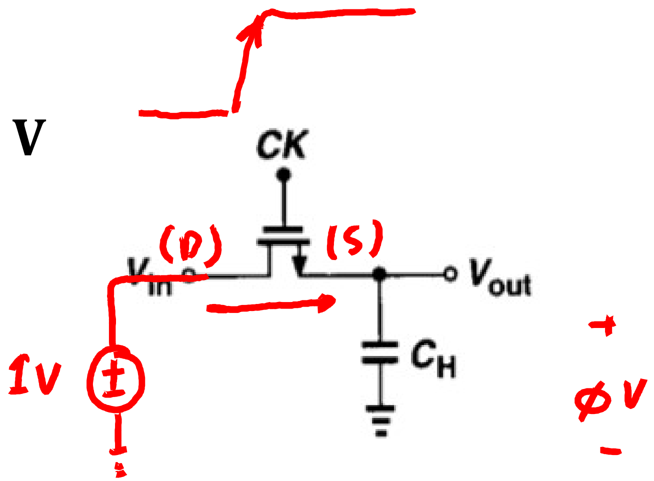


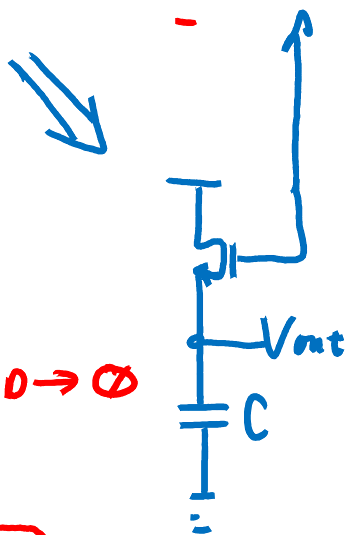
- Through the settling transient
  - The transistor current direction
  - The transistor operating region

Switches – A Few Cases (IV)

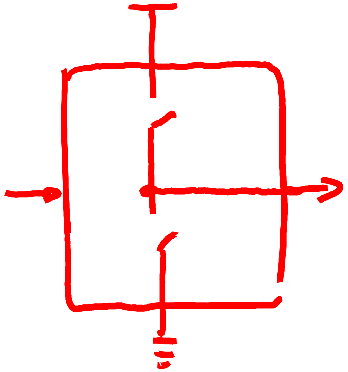
- Vth of 0.3 V and VCK goes from 0 V to 1 V

1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially
3. Vin = 0.3 V while Vout = 0 V initially
4. Vin = 1.0 V while Vout = 0 V initially





Eventually M1 gets turned OFF $I_D \to 0$

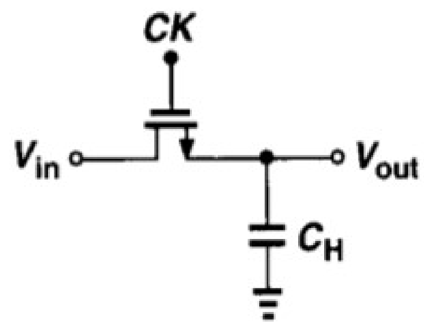


$$\frac{dV}{dt} = \frac{I}{C} = f(V_{GS}) = f(V_{DD} - \underline{V_{out}})$$

Switches – A Few Cases (IV)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

4. Vin = 1.0 V while Vout = 0 V initially

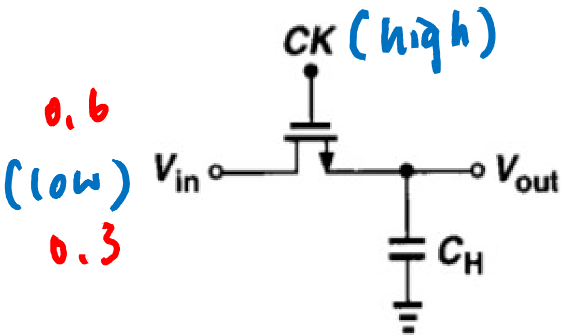


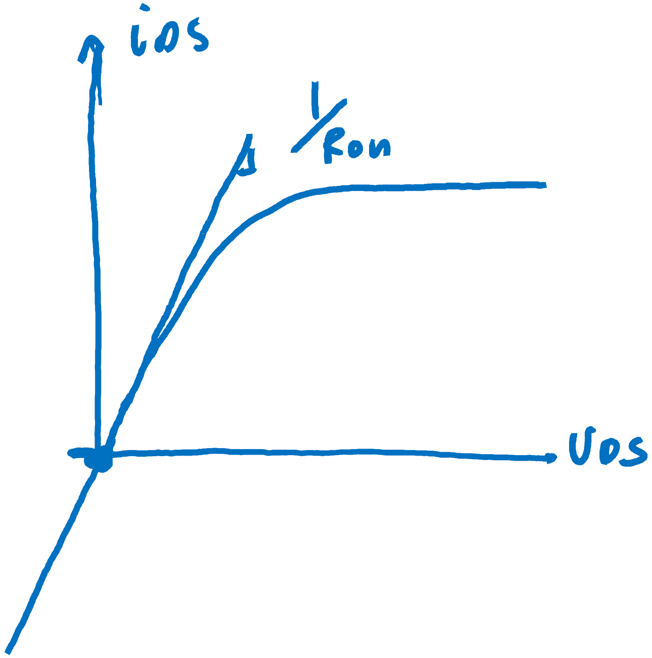
- Through the settling transient
  - The transistor current direction
  - The transistor operating region

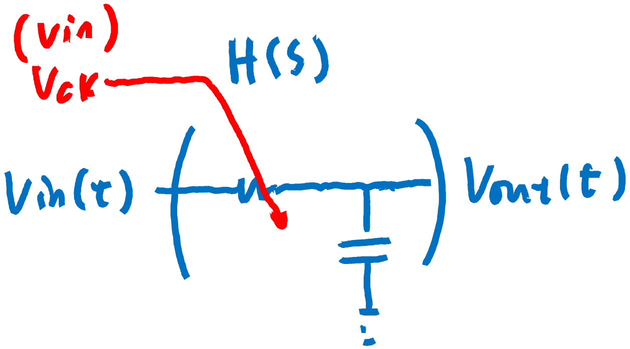
On Resistance

- **Can be viewed as a resistor equal to**

$$R_{on} = \left(\mu C_{ox}\frac{W}{L}\left(V_{CK}-V_{in}-V_{th}\right)\right)^{-1}$$

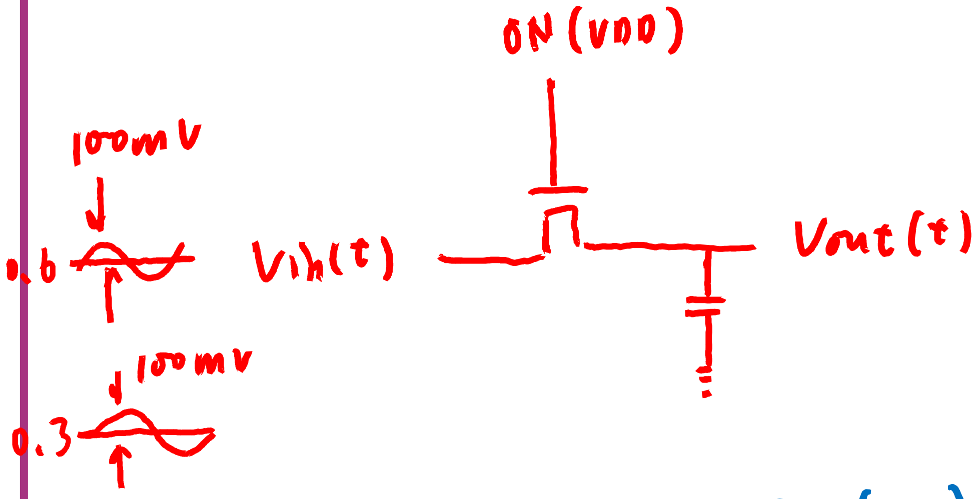


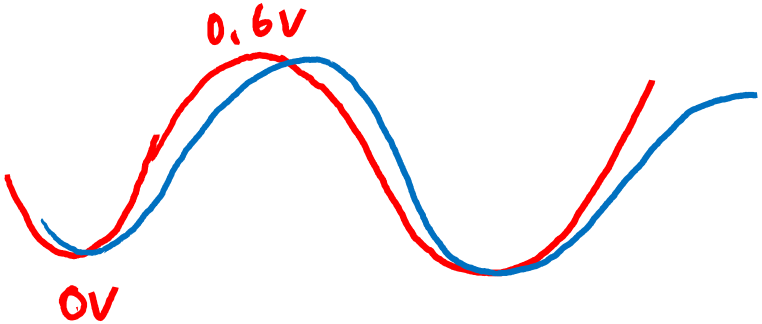




$$H(s) = \frac{\frac{1}{sC}}{R+\frac{1}{sC}} = \frac{1}{1+sRC}$$

- On-resistance and speed depend on the input level





Nonlinearity

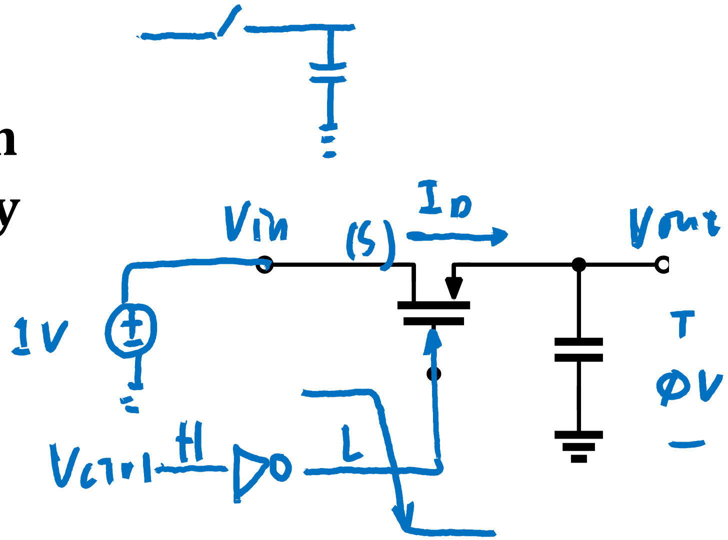
Ron(vin)

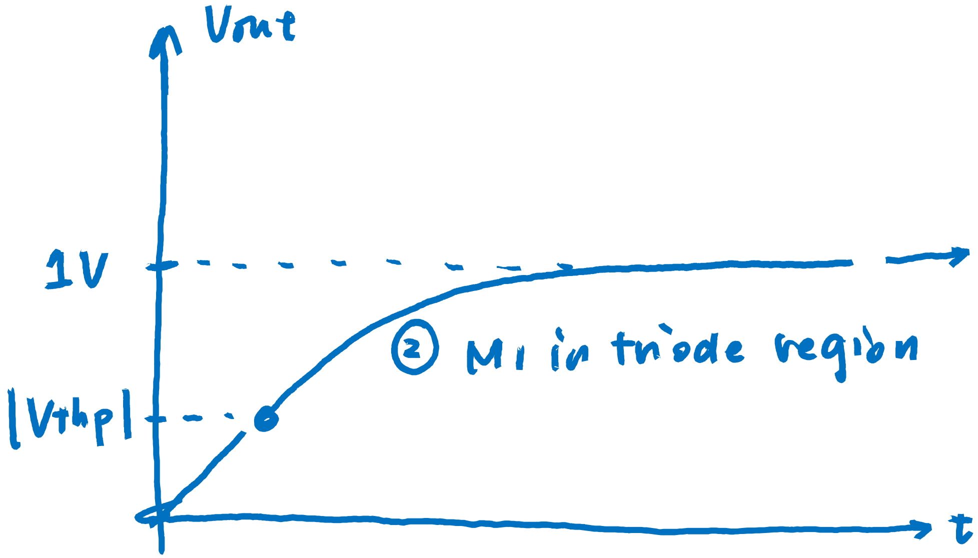
- small-signal operation
  - bias point matters (common-mode)
- large-signal operation
  - waveform distortion

Using PMOS as Switch (I)

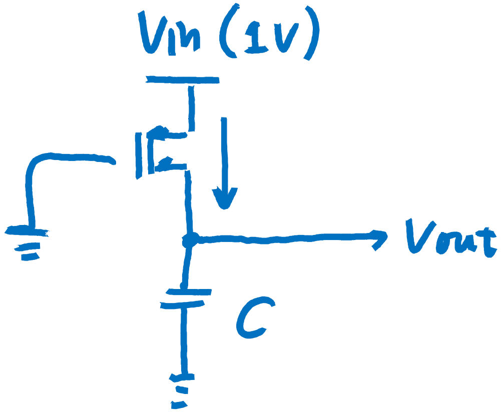
- VCK goes down to turn on the switch

1. Vin = 1.0 V while Vout = 0 V initially





Vout → 1V
IDS → ØV
M2 in deep triode region

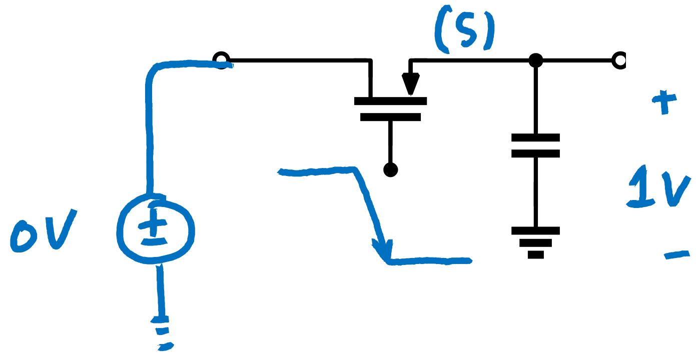


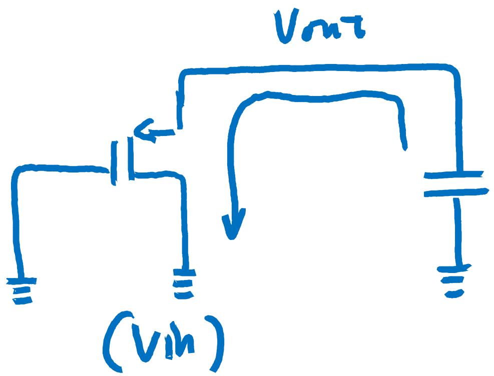
① Initially M1 in saturation

Using PMOS as Switch (II)

- VCK goes down to turn on the switch

2. Vin = 0 V while Vout = 1.0 V initially

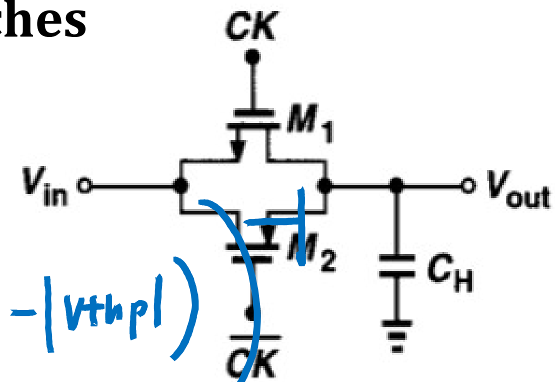




$$R_{on,p} = \left(\mu C_{ox} \frac{W}{L}\left(V_{in} - \underset{(V_{CK})}{0V} - |V_{thp}|\right)\right)^{-1}$$

Pass Transistors

- **Transmission gates or Complementary switches**
  - Complementary clock signals needed

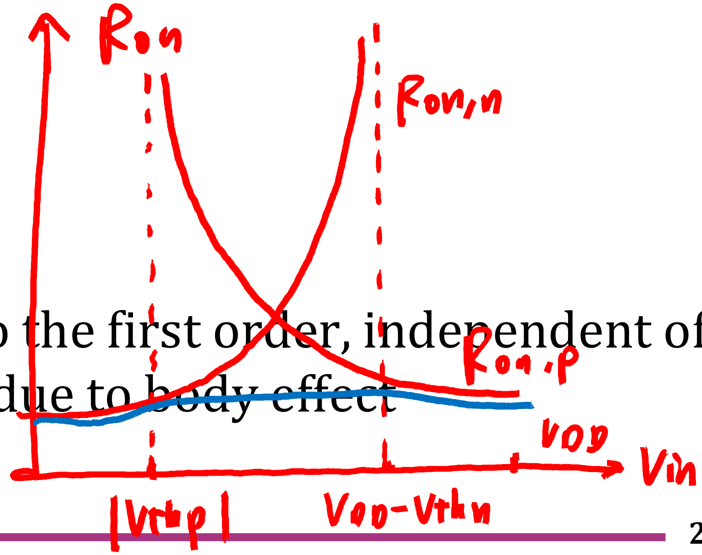


$$R_{on,eff} = R_{on,n} \,\|\, R_{on,p}$$

$$= \left(\mu_n C_{ox} \frac{W}{L}_n (V_{DD} - V_{in} - V_{thn}) + \mu_p C_{ox} \frac{W}{L}_p (V_{in} - |V_{thp}|) \right)$$

$$= \left(\left(\mu_p C_{ox} \frac{W}{L}_p - \mu_n C_{ox} \frac{W}{L}_n \right) V_{in} + \mu_n C_{ox} \frac{W}{L}_n (V_{DD} - V_{thn}) - \mu_p C_{ox} \frac{W}{L}_p |V_{thp}| \right)^{-1}$$

$$\Rightarrow \frac{\mu_p C_{ox,p} \frac{W}{L}_p}{\mu_n C_{ox,n} \frac{W}{L}_n} = 1 \Rightarrow \frac{\frac{W}{L}_p}{\frac{W}{L}_n} \simeq \frac{\mu_n}{\mu_p}$$



  - Can be sized so that the on-resistance is, to the first order, independent of the input level → Vthp and Vthn still vary due to body effect

Charge Injection

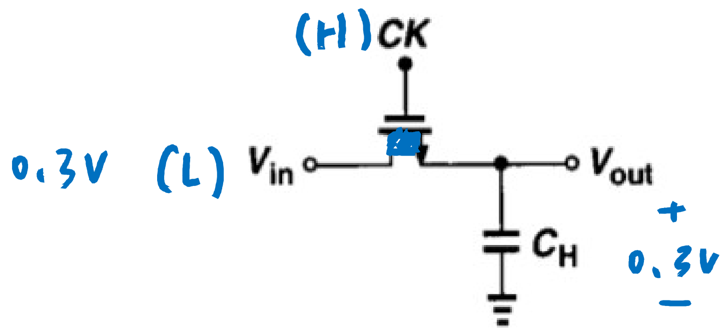
- **In order to reduce Ron and speed up the operation**

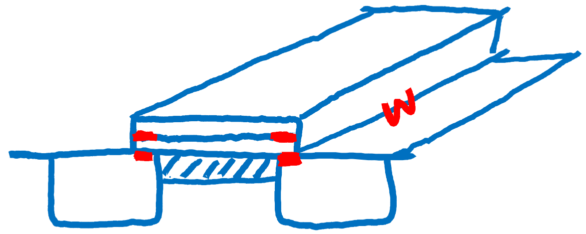
1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor

inversion layer

Q=CV 其中 C=WL·Cox

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$





- Charge in the channel when ON

Charge Injection

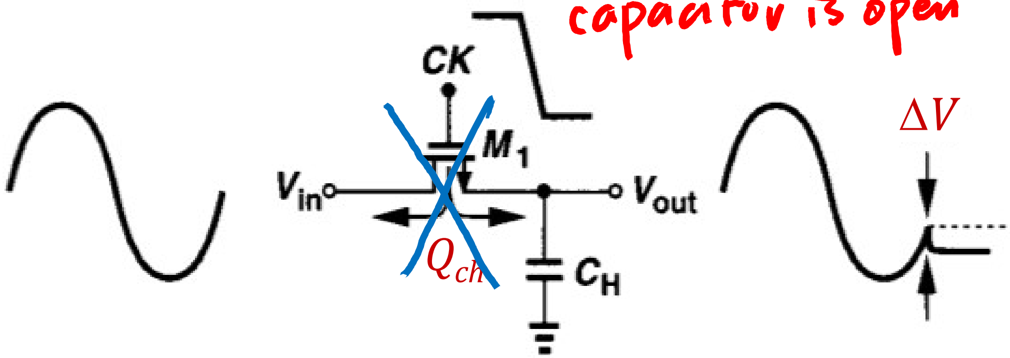
- **In order to reduce Ron and speed up the operation**

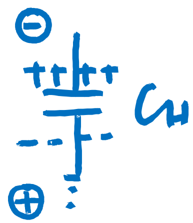
1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor

Vout becomes high-Z
capacitor is open

$$Q_{ch} = -WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

$$\Delta V = \frac{-K\,WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$





- Charge in the channel when ON

→ Causing a pedestal at the output when turning OFF

1 Charge Injection

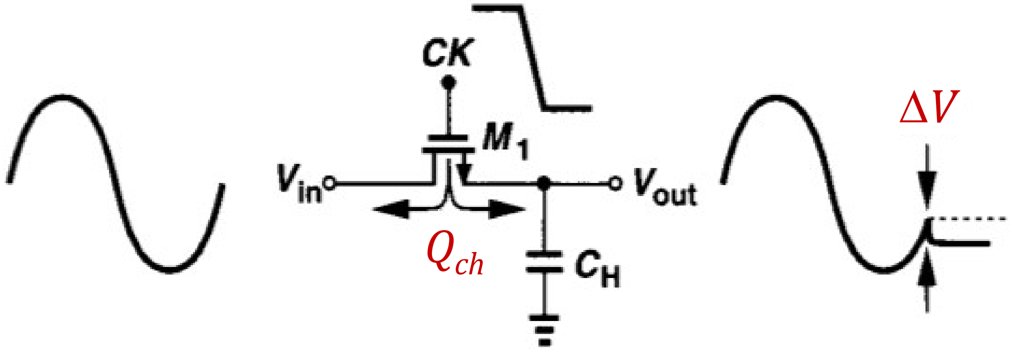
$WL\downarrow, C_H\uparrow$ direct trade off with speed

- **In order to reduce Ron and speed up the operation**

1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor

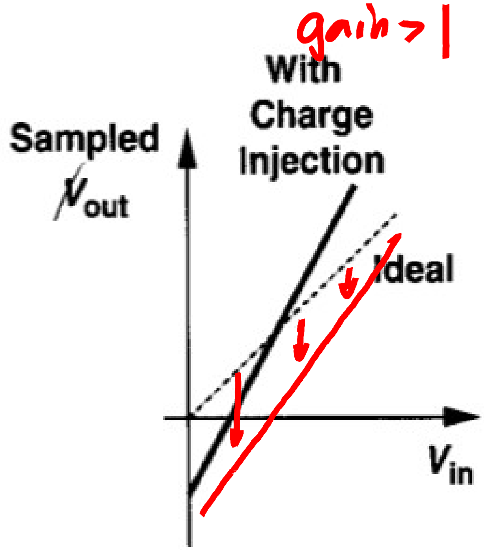
$$Q_{ch} = -WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

$$\Delta V_{max} = \frac{-WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$



- Charge in the channel when ON

→ Causing a pedestal at the output when turning OFF



$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$$

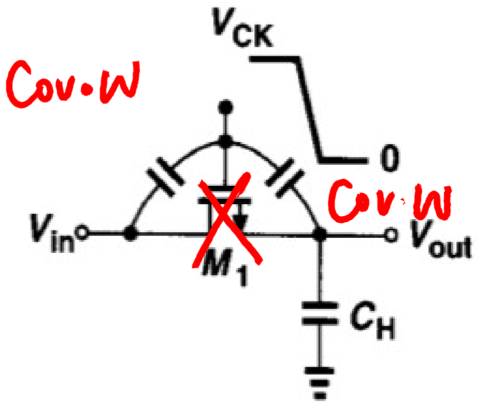
Sampling

→ Gain error and offset

Clock Feedthrough

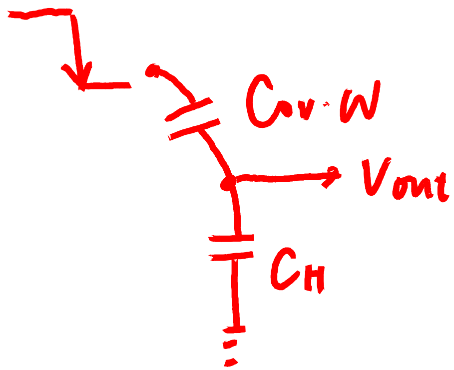
製程資料 C_{ox}, C_{ov}

- **Clock transitions get coupled to Vout through overlap capacitance**



$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov}+C_H}$$

想要W↓, C_H↑

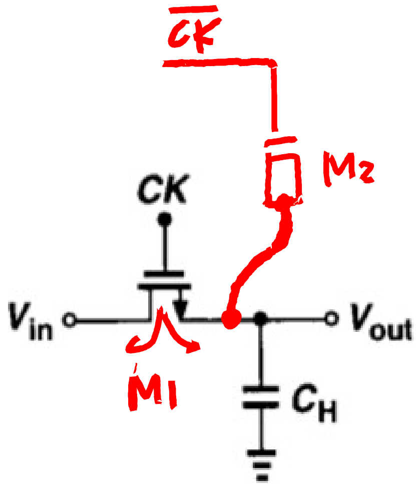


  - ΔV independent of Vin

- **Both charge injection and clock feedthrough trade-off with speed**

Charge Injection Cancellation (I)

- **Dummy switch**
  - Injected charge can be removed by means of a second transistor



as M_1 turns OFF $\Delta Q_1 = -K \cdot WL \cdot C_{ox}(V_{DD} - V_{in} - V_{th})$

M_2 turns ON (inversion layer formed in M_2)

$\Delta Q_2 = -W_2 \cdot L_2 \cdot C_{ox}(V_{DD} - V_{in} - V_{th})$

$\Rightarrow \Delta Q_1 = \Delta Q_2$

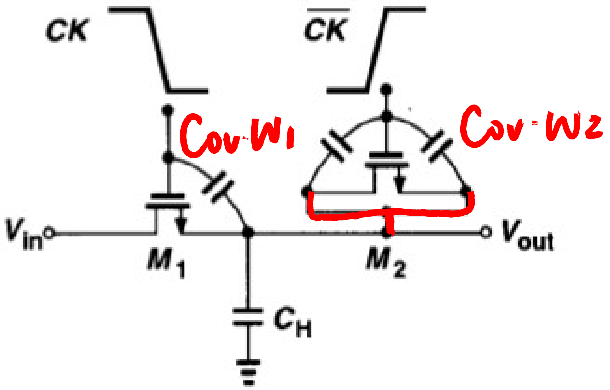
$W_2 = K \cdot W_1$

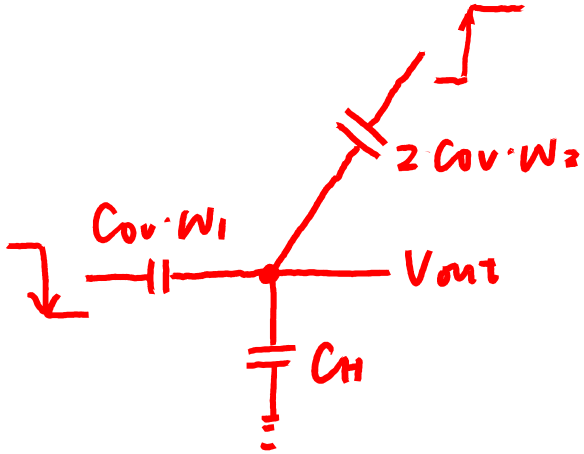
with $K = 0.5$ $W_2 = 0.5 W_1$

- However, it is hard to know the fraction of charge going towards Vout

Dummy Switch on Clock Feedthrough

- **Also suppressed**





with superposition

$$\Delta V_{out} = -V_{CK} \cdot \frac{C_{ov} \cdot W_1}{C_{ov} \cdot W_1 + 2C_{ov}W_2 + C_H} + V_{CK} \frac{2C_{ov} \cdot W_2}{C_{ov} \cdot W_1 + 2C_{ov} \cdot W_2 + C_H}$$

如果依前頁 $W_2 = 0.5W_1$

$\Delta V_{out} \rightarrow 0$

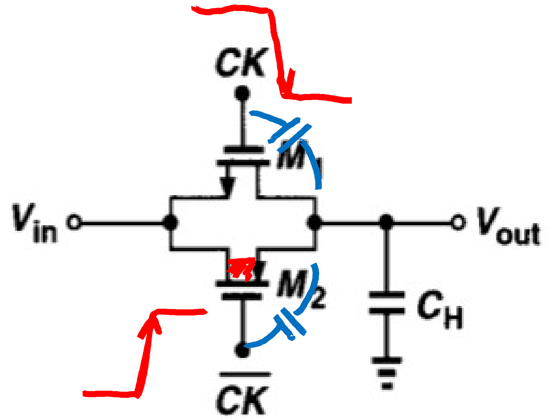
Charge Injection Cancellation (II)

- **Complementary switch** pass transistor
  - Charges from NMOS cancel partially with charges from PMOS

net charge = $\Delta Q_N + \Delta Q_P$

$= -(W \cdot L)_n C_{oxn}(V_{DD} - V_{in} - V_{th}) + (WL)_p \cdot C_{oxp}(V_{in} - |V_{thp}|)$

$= f(V_{in})$ not necessary zero



- Perfect cancellation for only one input level
- Not perfect cancellation for clock feedthrough

$C_{ovn} \neq C_{ovp}$, nevertheless, $W_n \neq W_p$ usually