EE4280 Lecture 6:
Phase-Locked Loops

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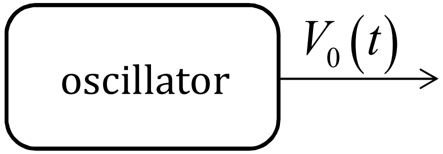
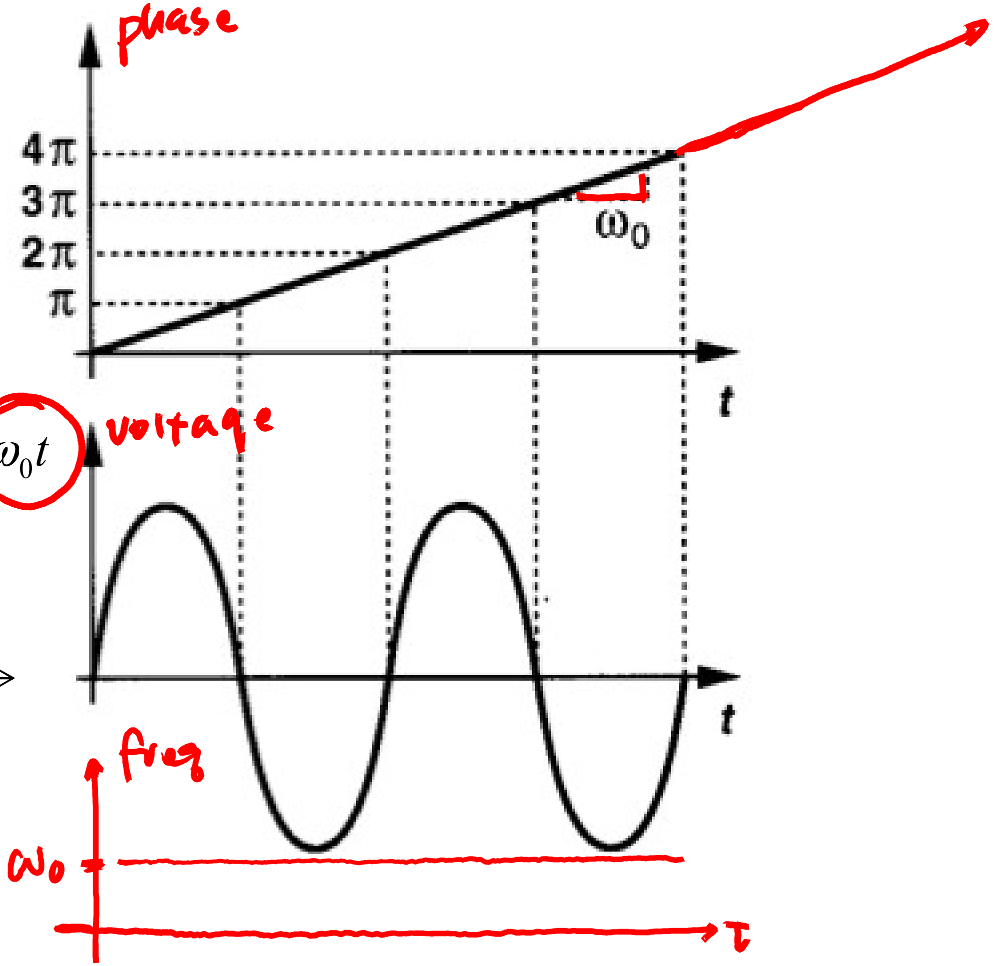
Mathematical Model of VCO

$$\phi(t) = \omega_0 t$$

$$V_0(t) = V_m \sin \omega_0 t$$



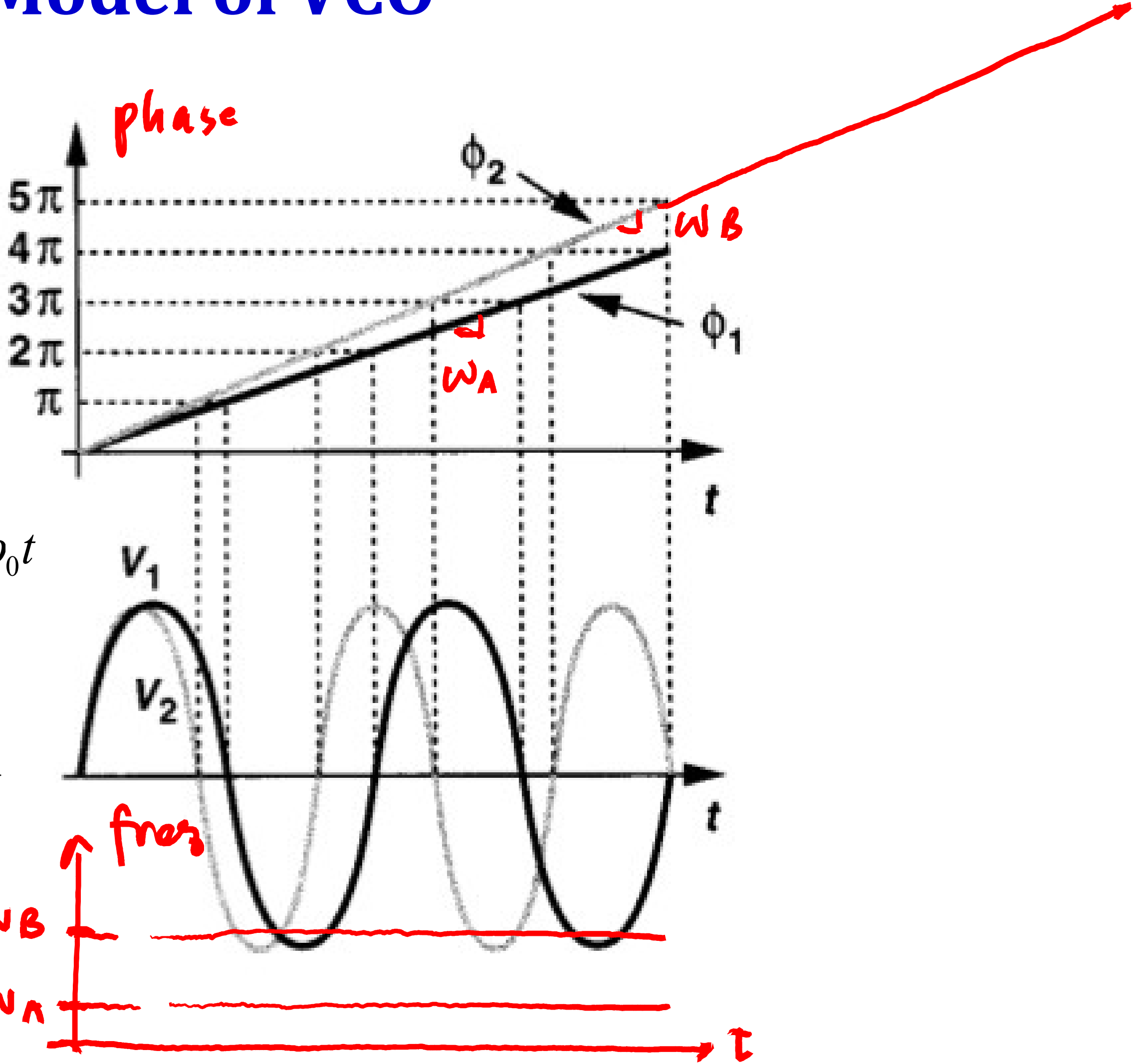


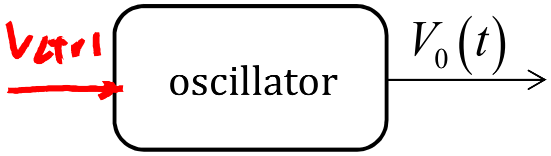
- **Oscillator's output phase is accumulated over time**

Mathematical Model of VCO

total phase $\phi(t) = \omega_0 t$

$V_0(t) = V_m \sin \omega_0 t$



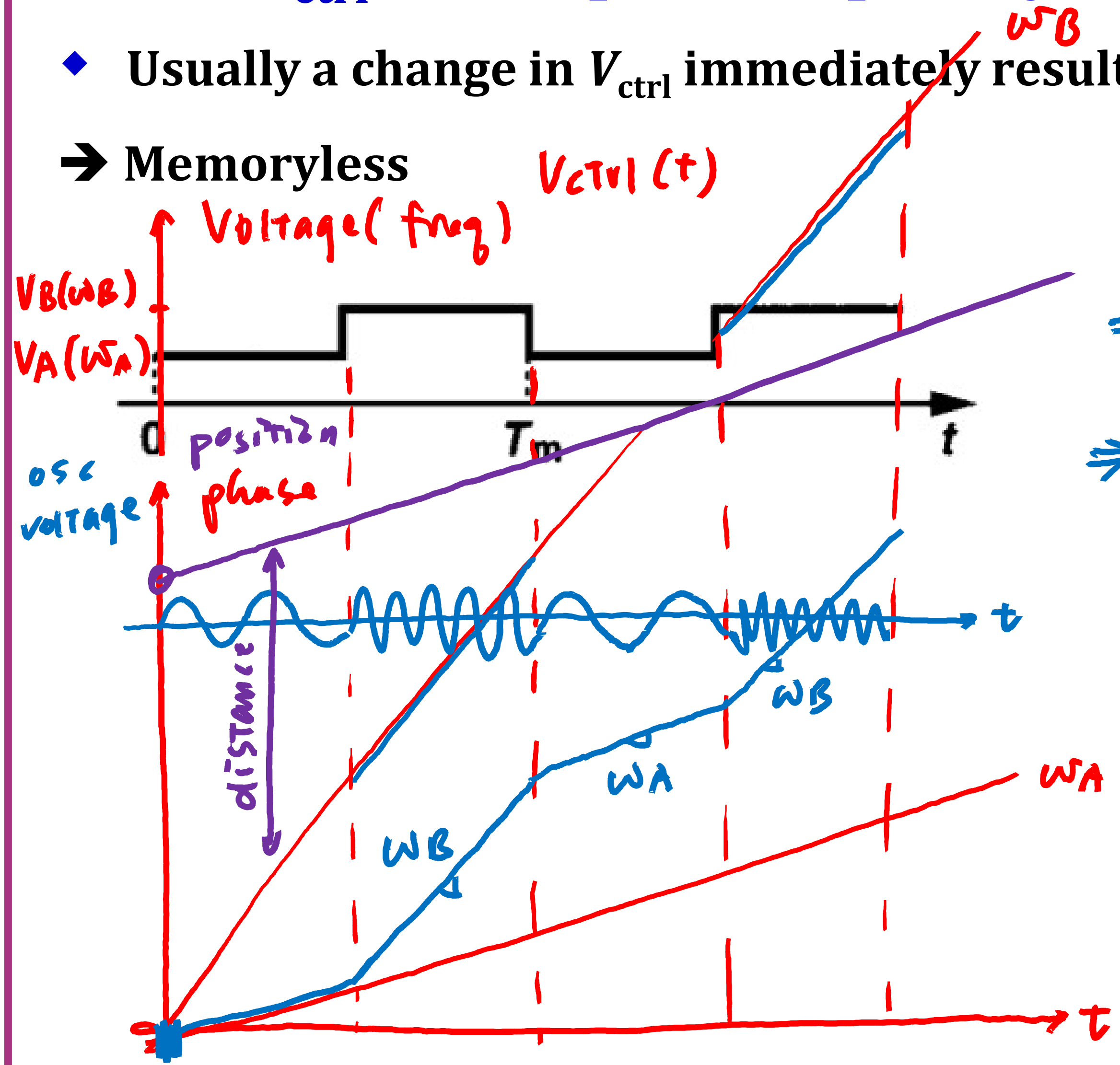


- **Oscillator's output phase is accumulated over time**
- **Faster frequency results in faster phase accumulation**

From V_{ctrl} to Output Frequency and Phase

- Usually a change in V_{ctrl} immediately results in a change in ω_{out}

➔ Memoryless



If $V_{ctrl}(t) \rightarrow \omega(t)$

$\Rightarrow \phi(t) \neq \omega(t)\cdot t$

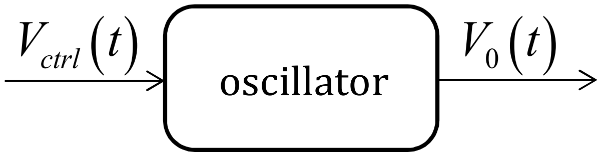
$\Rightarrow \phi(t) = \int \underline{\underline{\omega(t)}}\,dt + \underset{\overset{\|}{0}}{\phi_0}$

- If the frequency is a known function of time

$t=0$

Excessive Phase and Transfer Function

$$\therefore \omega(t)=\omega_0+K_{vco}\cdot\Delta V_{ctrl}(t)$$

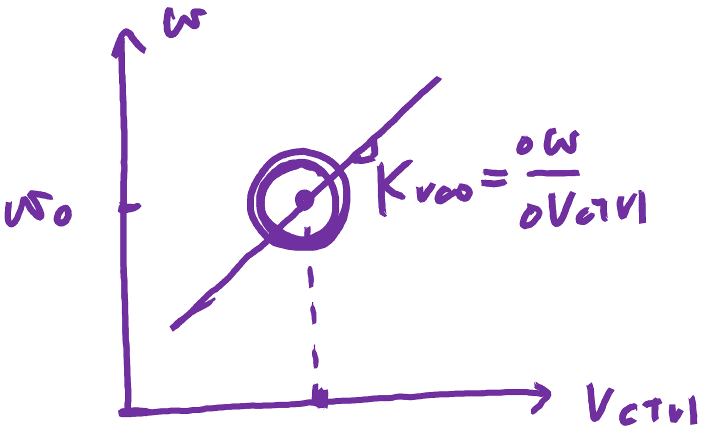


total phase

$$\phi(t)=\int\omega(t)\cdot dt+\phi_0$$

excessive phase

$$=\underline{\omega_0 t}+\overset{\phi_{ex}(t)}{\underline{\int K_{vco}\cdot\Delta V_{ctrl}(t)\cdot dt}}+\underset{0}{\underset{\|}{\underline{\phi_0}}}$$



$$V_{out}(t)=A_0\cdot\cos\left(\omega_0 t+\int K_{vco}\cdot\Delta V_{ctrl}(t)\,dt+\phi_0\right)$$

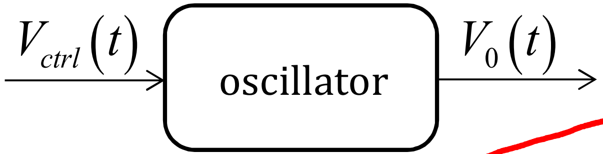
從 $V_{ctrl}(t)$ to $\phi_{ex}(t)$

- **Often times, the excessive phase is of interest** $\phi_{ex}(t)=K_{VCO}\int V_{ctrl}(t)\,\mathrm{d}t$

➔ **Transfer function:** 從 $\frac{\phi_{ex}(s)}{V_{ctrl}(s)}=\frac{K_{vco}}{s}$ #

Frequency Modulated Signal Example

- **With a small sinusoidal control voltage**



$\omega(t) = \omega_0 + K_{vco} \cdot V_m \cos \omega_m t$

$V_{cont}(t) = V_m \cos \omega_m t \;\; + V_{c0} \rightarrow V_{out}(t) = V_0 \cos(\omega_0 t + K_{VCO} \int V_{cont} dt)$

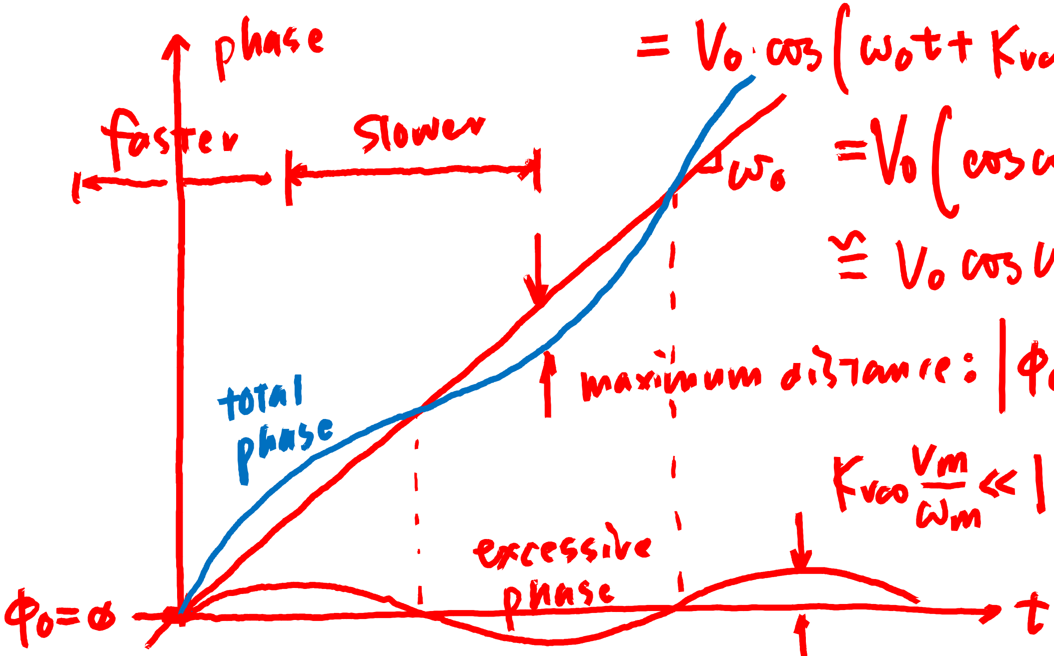
$= V_0 \cdot \cos\left(\omega_0 t + K_{vco} \cdot \frac{V_m}{\omega_m} \cdot \sin(\omega_m t) + \phi_0\right)$

$= V_0 \left(\cos \omega_0 t \cdot \cos \phi_{ex} - \sin \omega_0 t \sin \phi_{ex}(t)\right)$

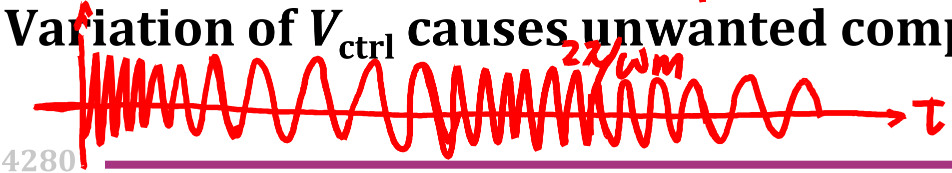
$\cong V_0 \cos \omega_0 t - V_0 \cdot K_{vco} \frac{V_m}{\omega_m} \underline{\sin \omega_0 t} \cdot \underline{\sin \omega_m t}$

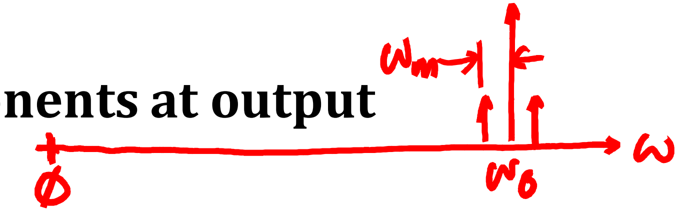
$= V_0 \cos \omega_0 t + \frac{V_0 K_{vco} \cdot V_m}{2 \omega_m} \left(\cos(\omega_0 + \omega_m) t + \cos(\omega_0 - \omega_m) t \right)$

$K_{vco} \frac{V_m}{\omega_m} \ll 1$



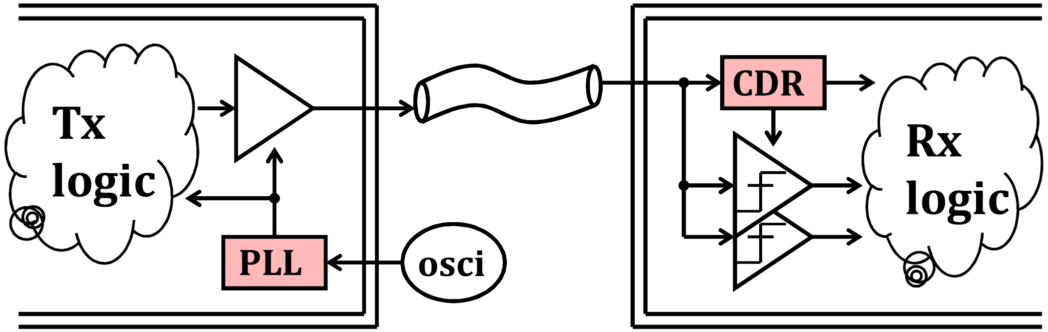
- **Variation of V_{ctrl} causes unwanted components at output**

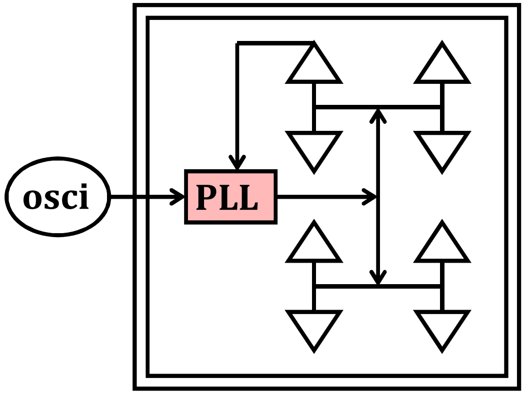




Phase-Locked Loops (I)

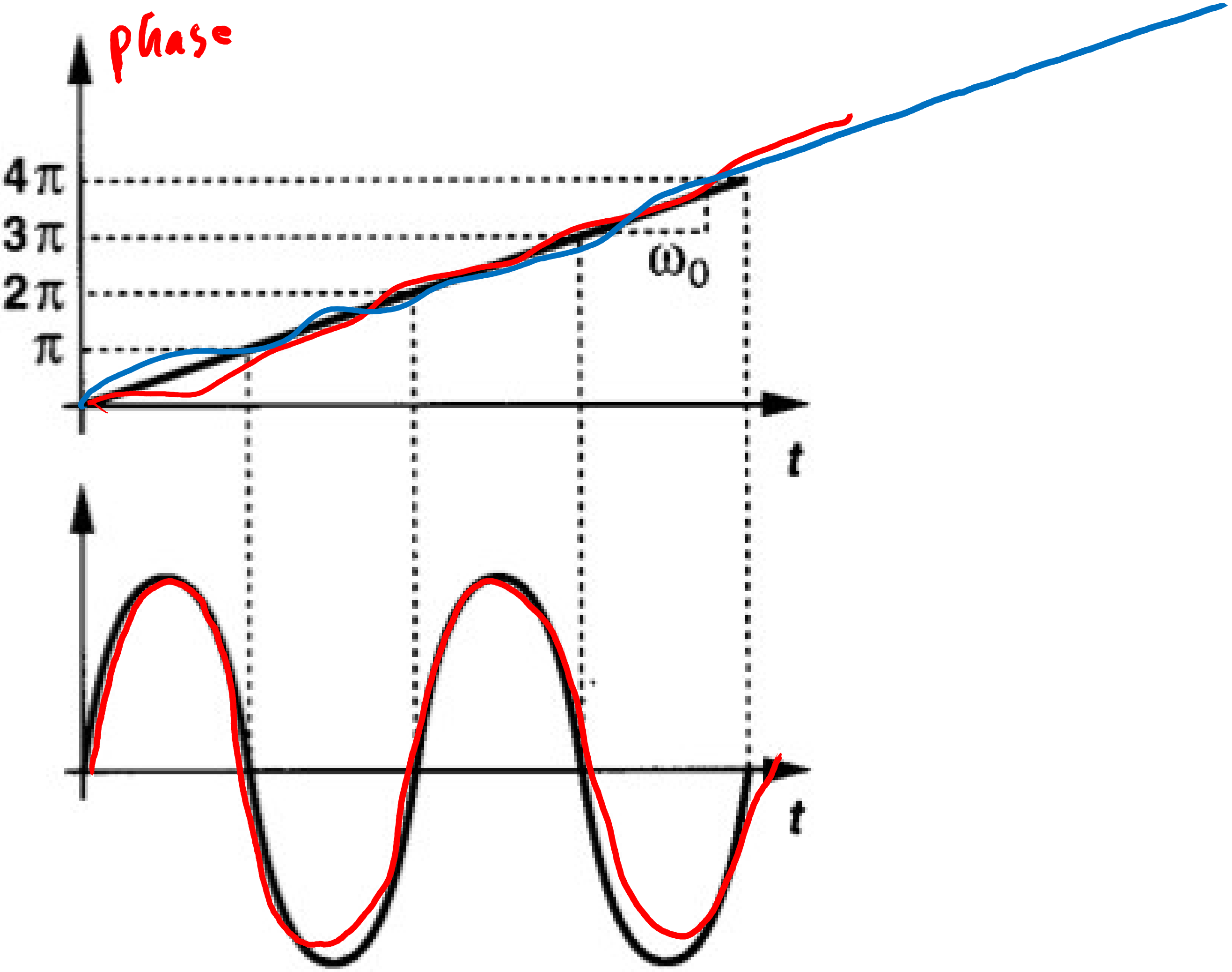
- **Phase-locked loops are used to generate a well-defined clock from a reference source**
- **Wide range of applications**
  - Clock generation and frequency synthesis
    - Generating a 10GHz clock from a 100MHz reference clock
    - Modulation/demodulation in wireless systems
  - Clock-and-data recovery
    - Extract clock frequency and optimum phase from incoming data stream
  - Skew cancellation
    - Phase aligning an internal clock to an I/O clock



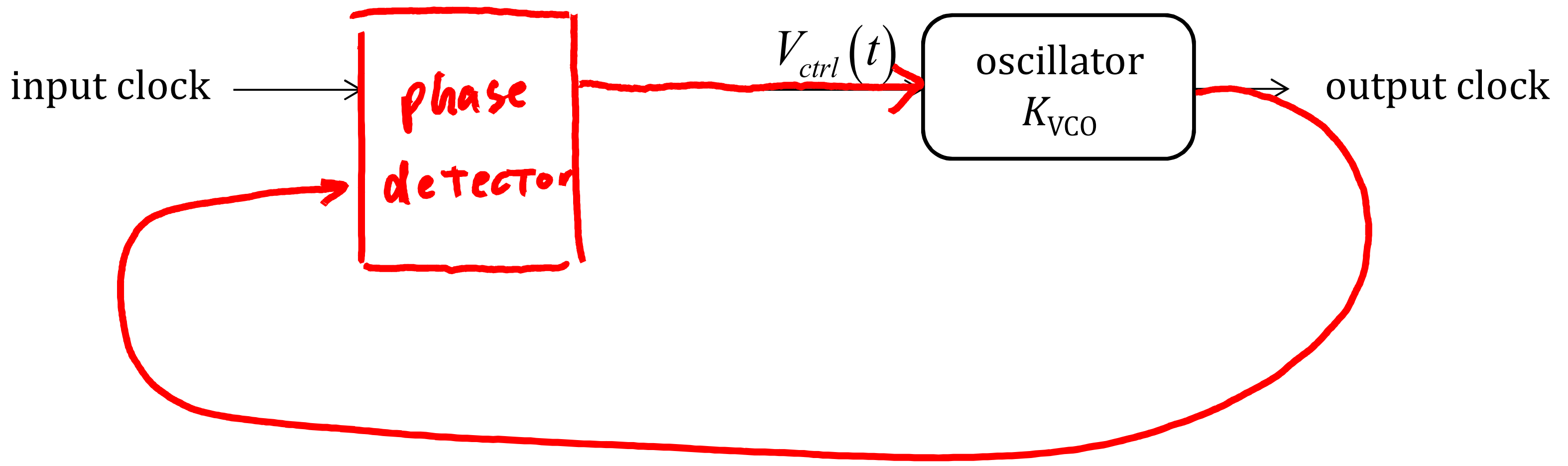


Phase-Locked Loops (II)

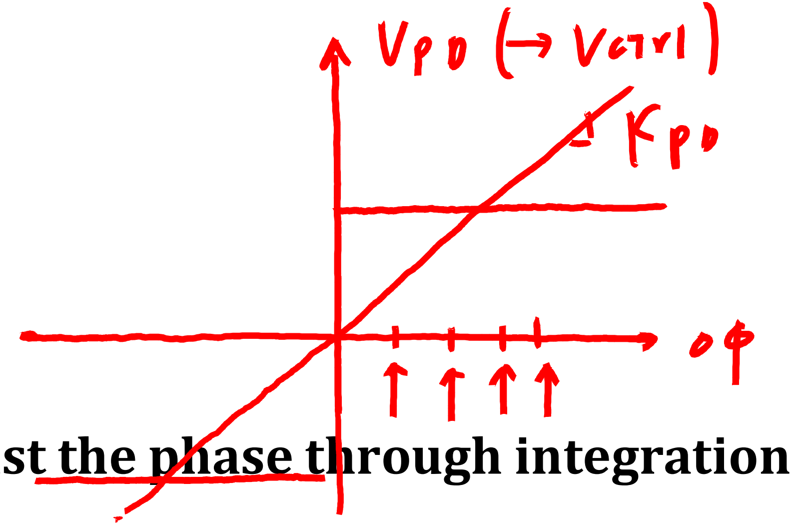
- A negative feedback system that compares and adjusts the output phase with the input phase



In Order to Achieve Phase Lock



- **Need to measure the phase difference between the two clocks**

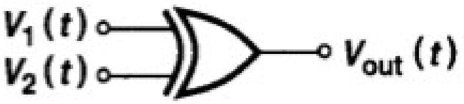


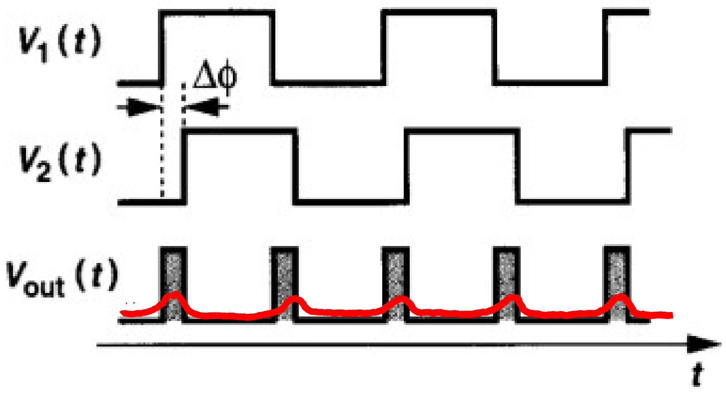
➔ **Phase detector**
A circuit whose <u>average</u> output is linearly proportional to the phase difference between the two inputs

➔ **We must vary the frequency to adjust the phase through integration**

Phase Detector Example – XOR Gate (I)

digital gate

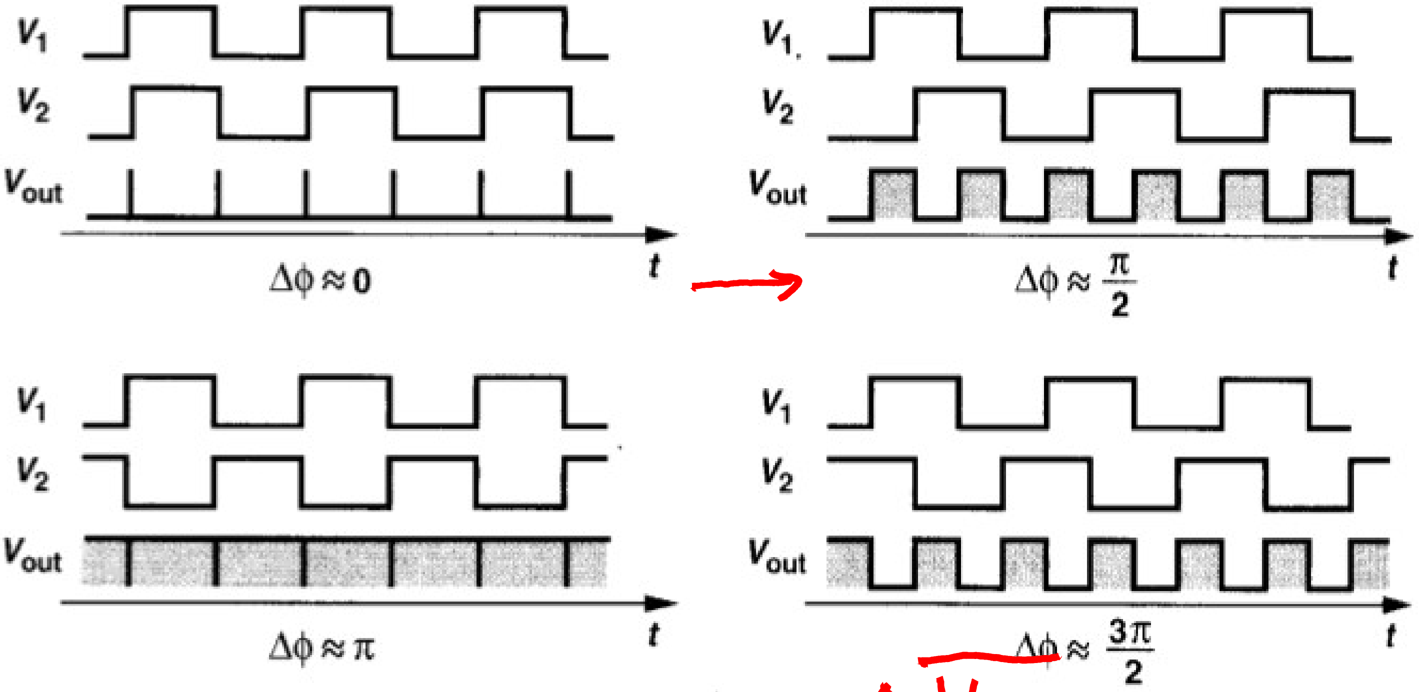


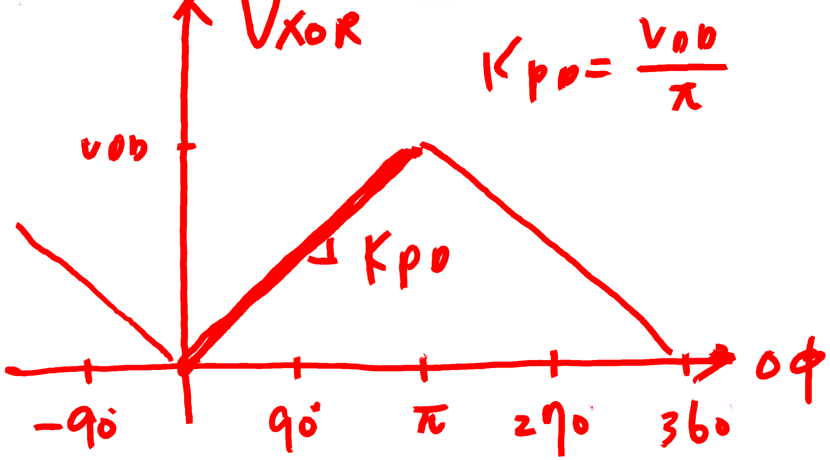


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

- Respond to both (rising and falling) edges
- As the phase difference keeps increasing …

Phase Detector Example – XOR Gate (II)



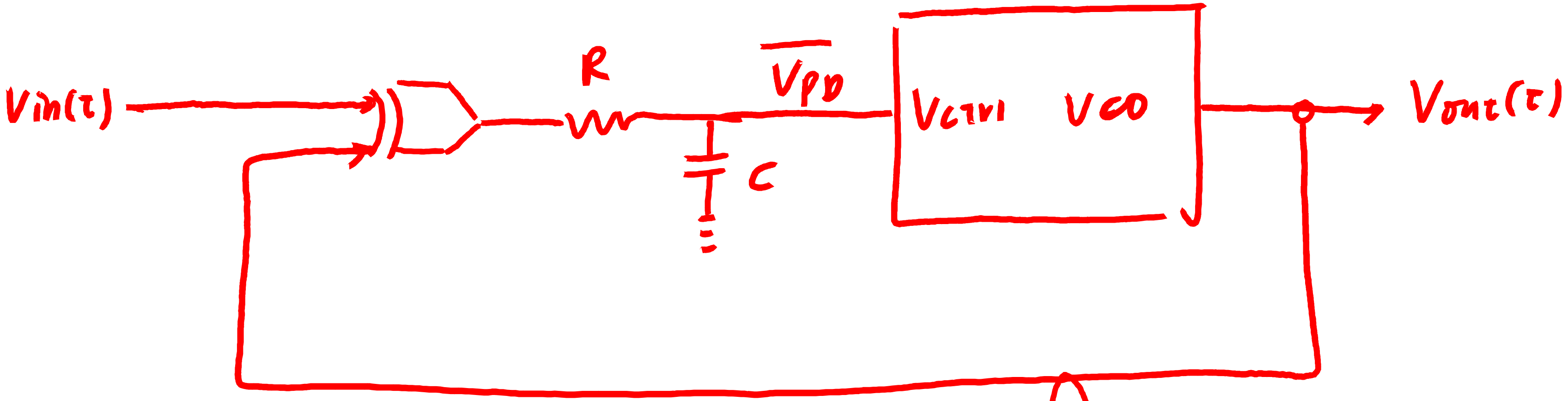


$K_{PD} = \frac{V_{DD}}{\pi}$

- The phase detector gain K_{PD} of

Basic PLL Topology

- A low-pass filter is used after the phase detector to extract the average PD output

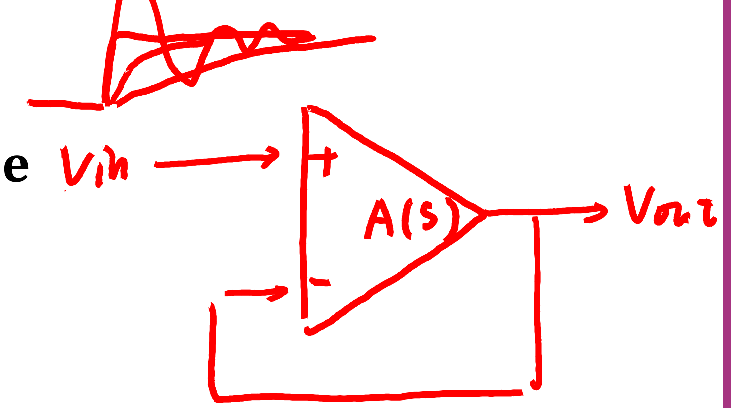


- In steady state

static phase error

➔ The phase difference settles to small value

➔ The two frequency becomes the same



Phase-Locked Loops in Steady State (I)

loop-filter

low-pass filter

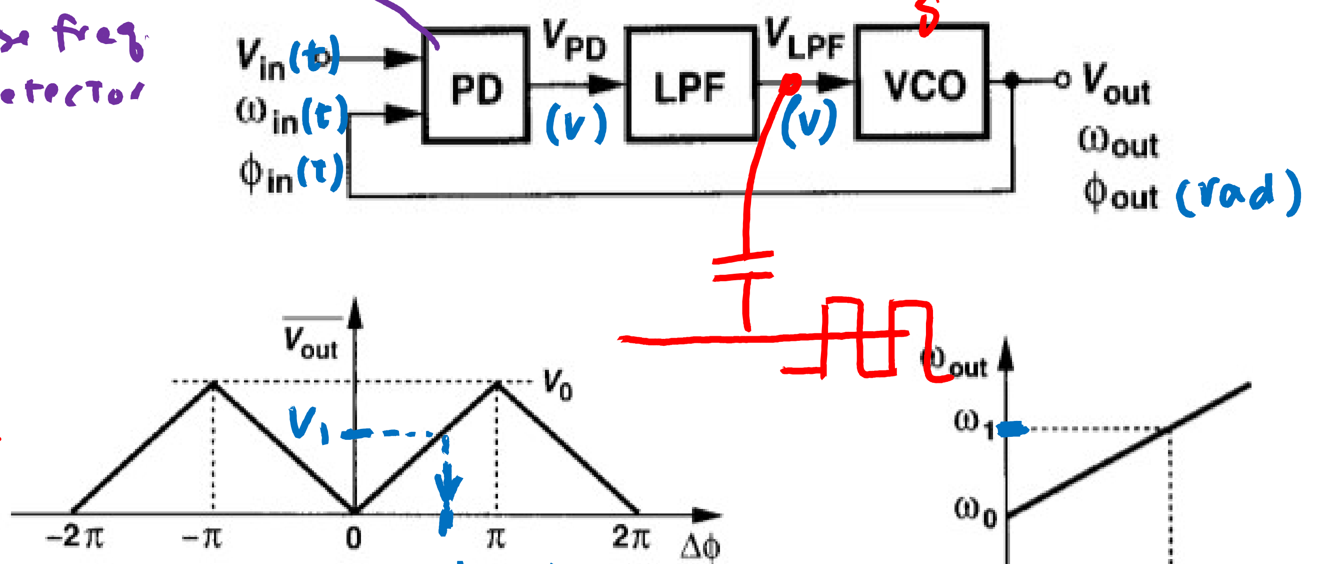
- **Transfer functions of each building block**

replaced by PFD

phase freq. detector

(rad)

$K_{PD} = \frac{V_{DD}}{\pi}$ $K_{LF} = 1$ @ LF $\frac{K_{VCO}}{s}$



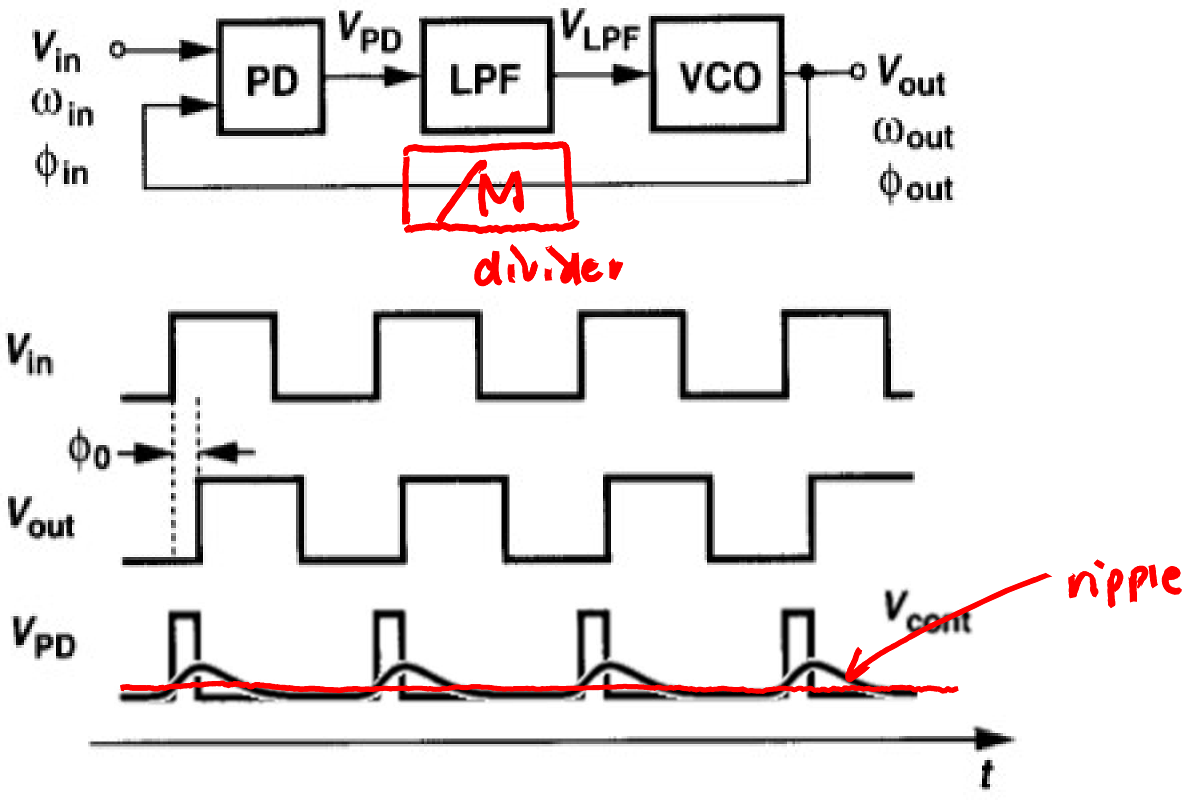
$\Delta\phi_{DC} \neq 0$

in order to run @ ω_1 $V_{ctrl} = V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}}$

so does $\overline{V_{PD}}$ (needs to settle to V_1) $\Rightarrow \frac{V_1}{\Delta\phi_{DC}} = K_{PD} \Rightarrow \Delta\phi_{DC} = \frac{V_1}{K_{PD}}$

$\Rightarrow \Delta\phi_{DC} = \frac{\omega_1 - \omega_0}{K_{VCO} \cdot K_{PD}}$

Phase-Locked Loops in Steady State (II)

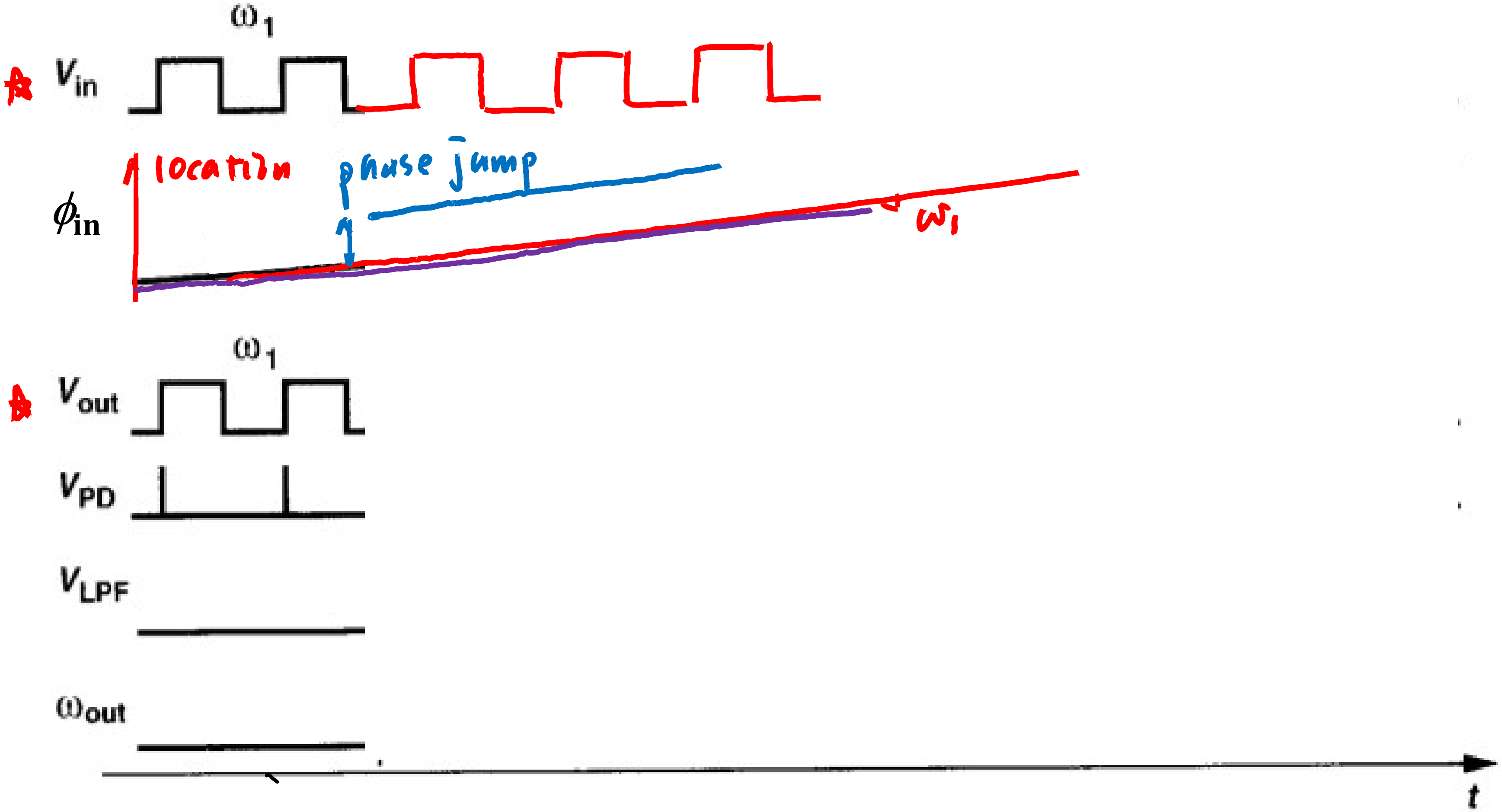


- The resulting phase error depends on the operating frequency
- To minimize phase error → $K_{PD}K_{VCO}$ needs to be maximized

- About operating frequency…

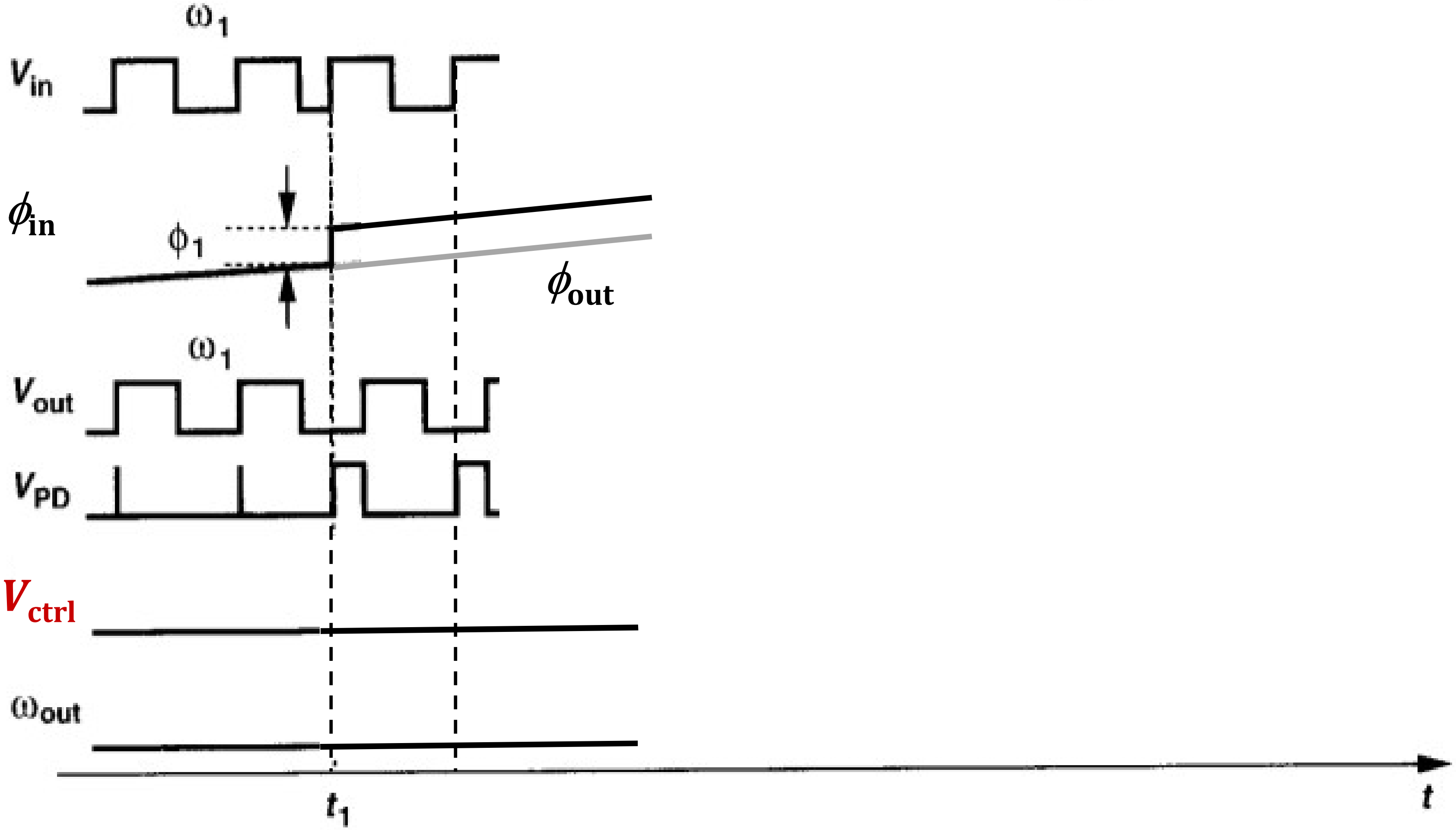
In Case with a Phase Jump

- How does it look like for a **phase** jump?



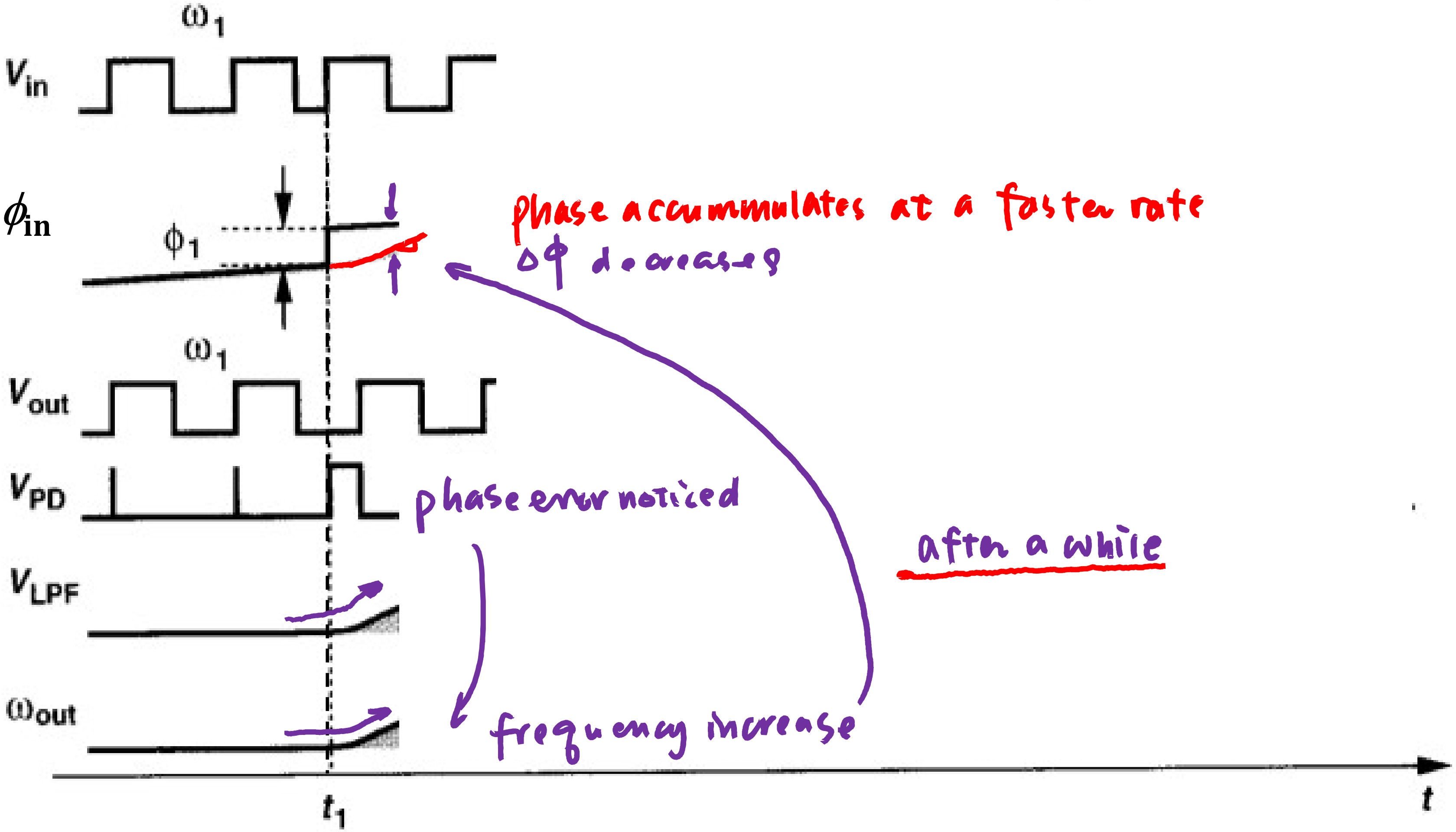
In Case with a Phase Jump

- **How does it look like for a phase jump?**
- **@ t_1 if open-loop**



In Case with a Phase Jump

- **How does it look like for a phase jump?**
- **@ t_1 with feedback loop**



phase accummulates at a faster rate

Δφ decreases

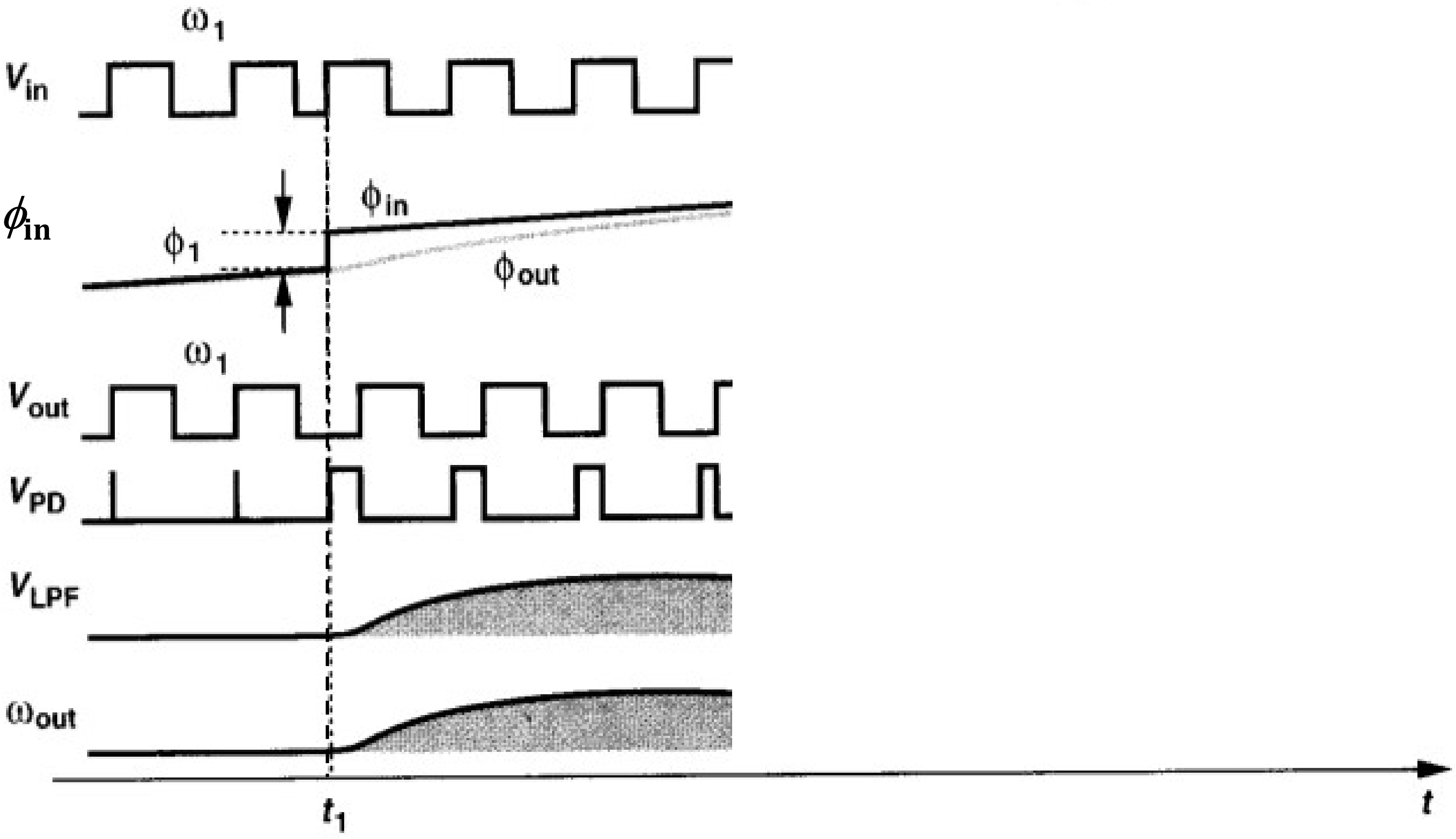
phase error noticed

frequency increase

after a while

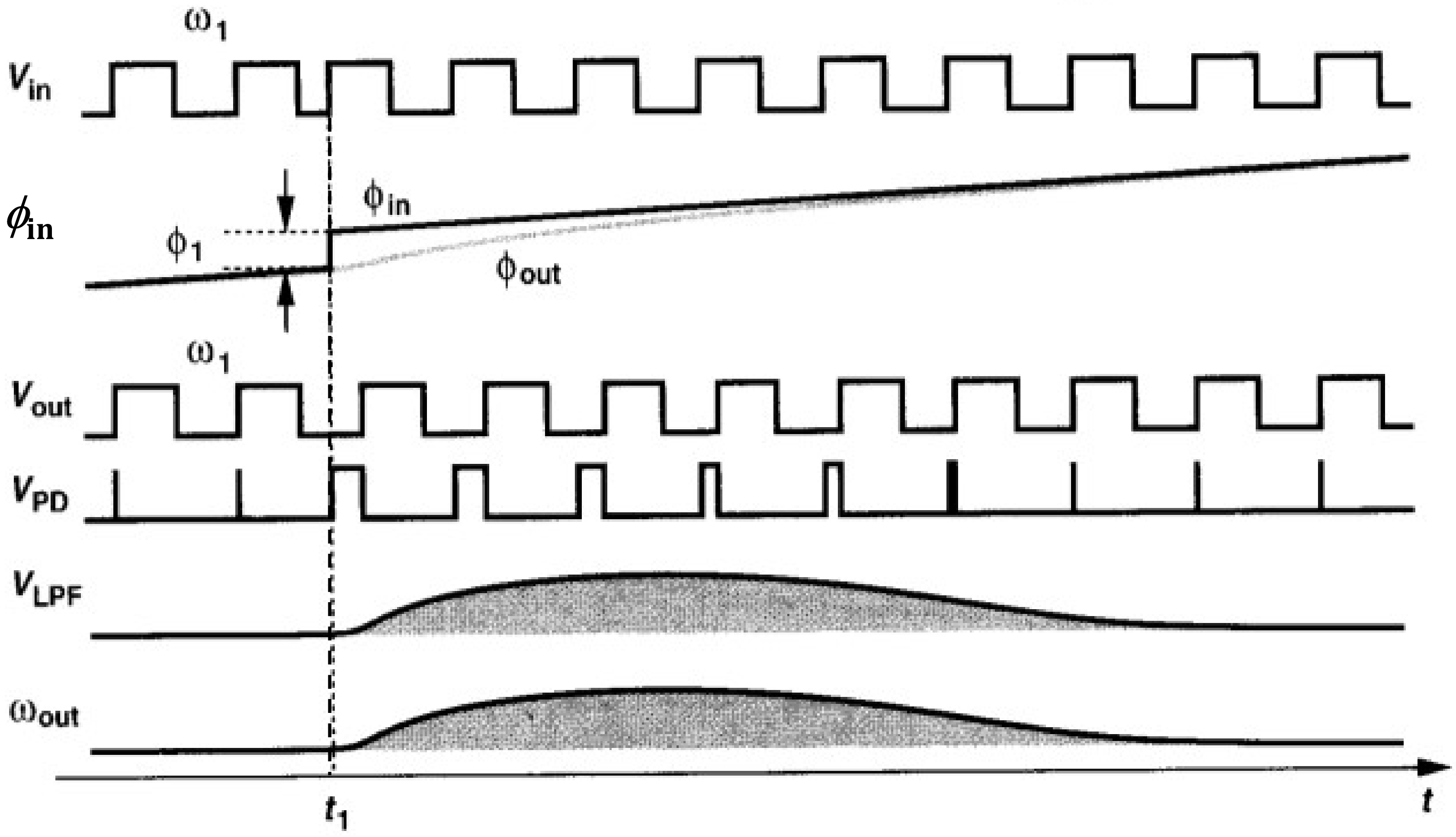
In Case with a Phase Jump

- **How does it look like for a phase jump?**
- **With feedback loop**



In Case with a Phase Jump

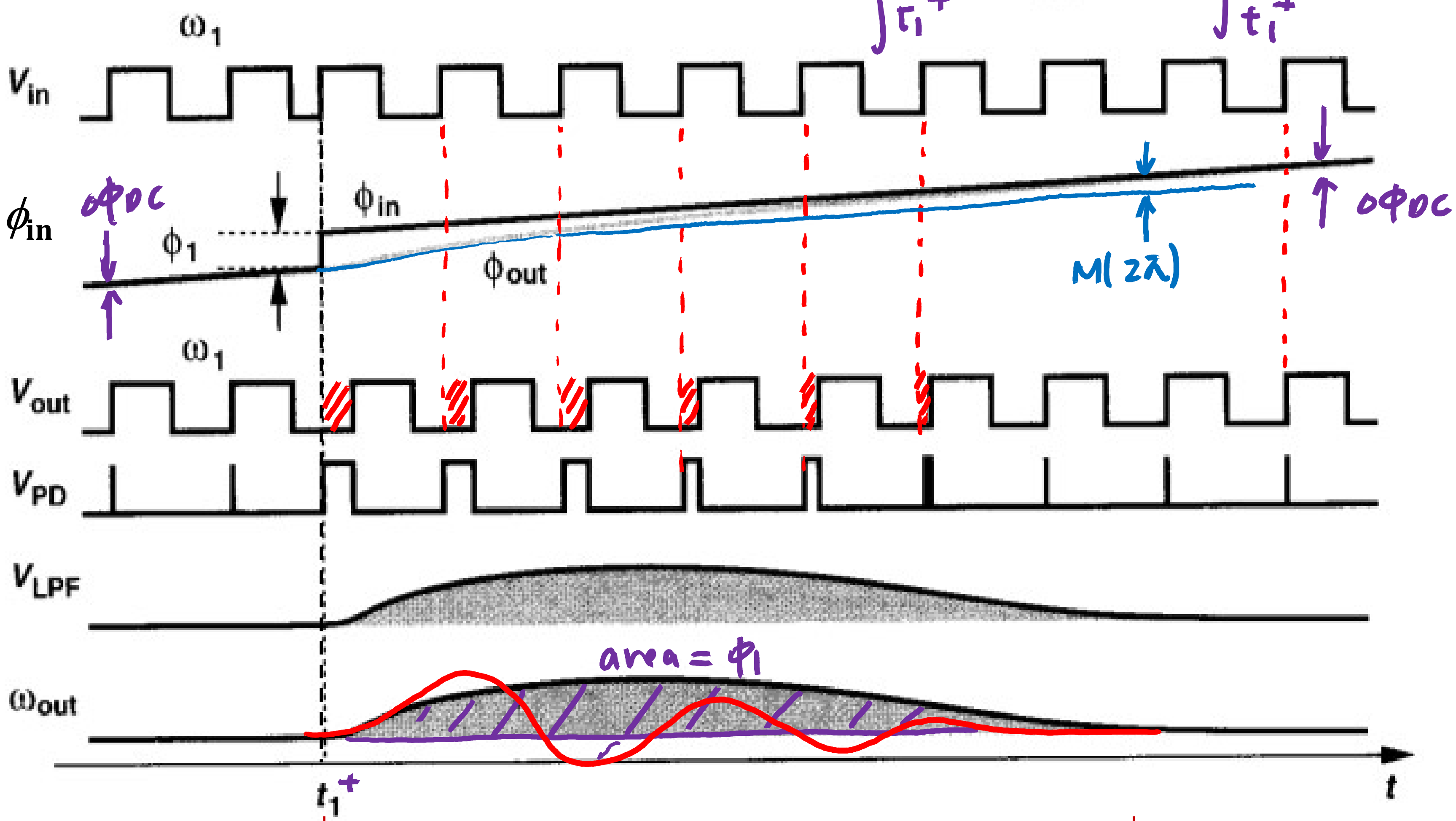
- **How does it look like for a phase jump?**
- **With feedback loop**



In Case with a Phase Jump

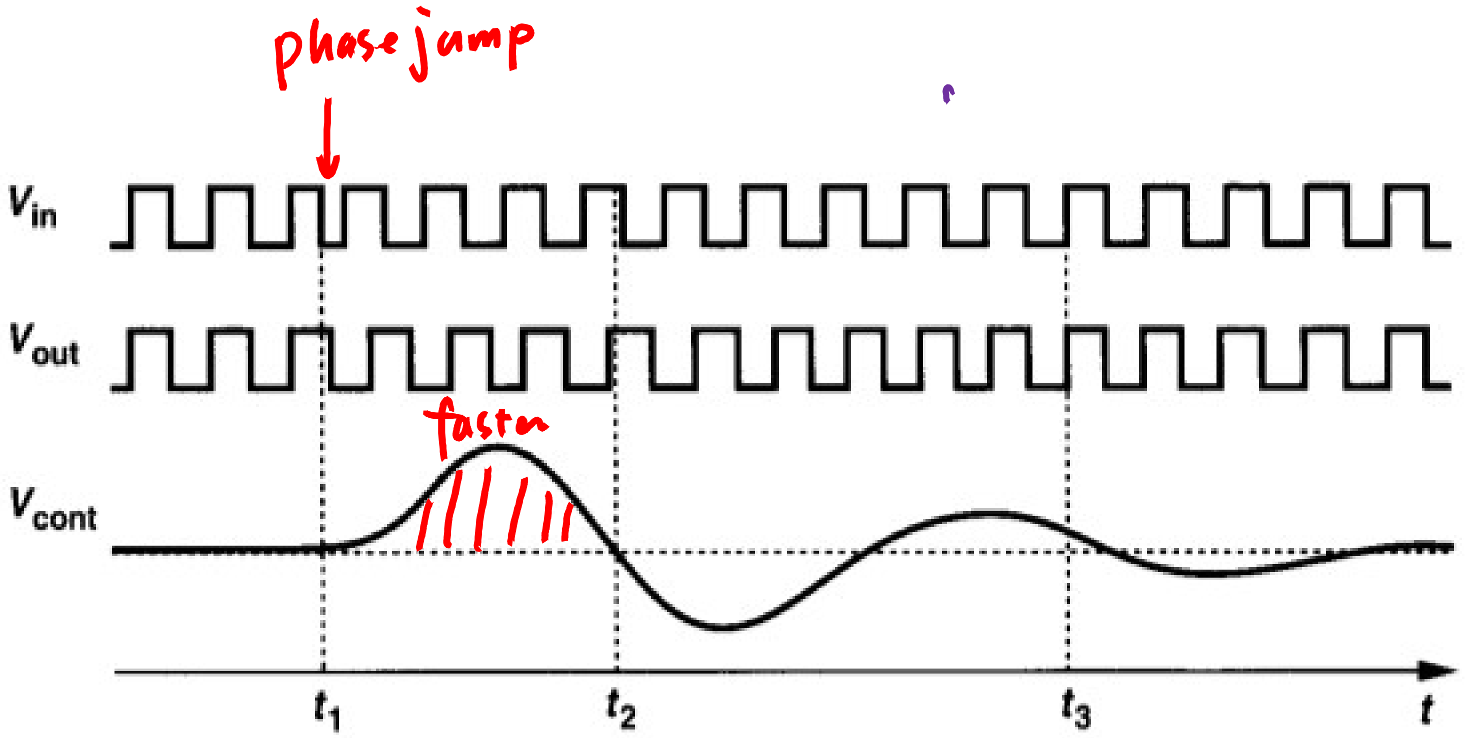
- How does it look like for a phase jump?
- With feedback loop

$$\int_{t_1^+}^{t} (\omega_{out}(\tau) - \omega_1) dt = \int_{t_1^+}^{t} \omega_{out}(\tau) dt - \int_{t_1^+}^{t} \omega_1 dt$$



steady state | transient | steady state

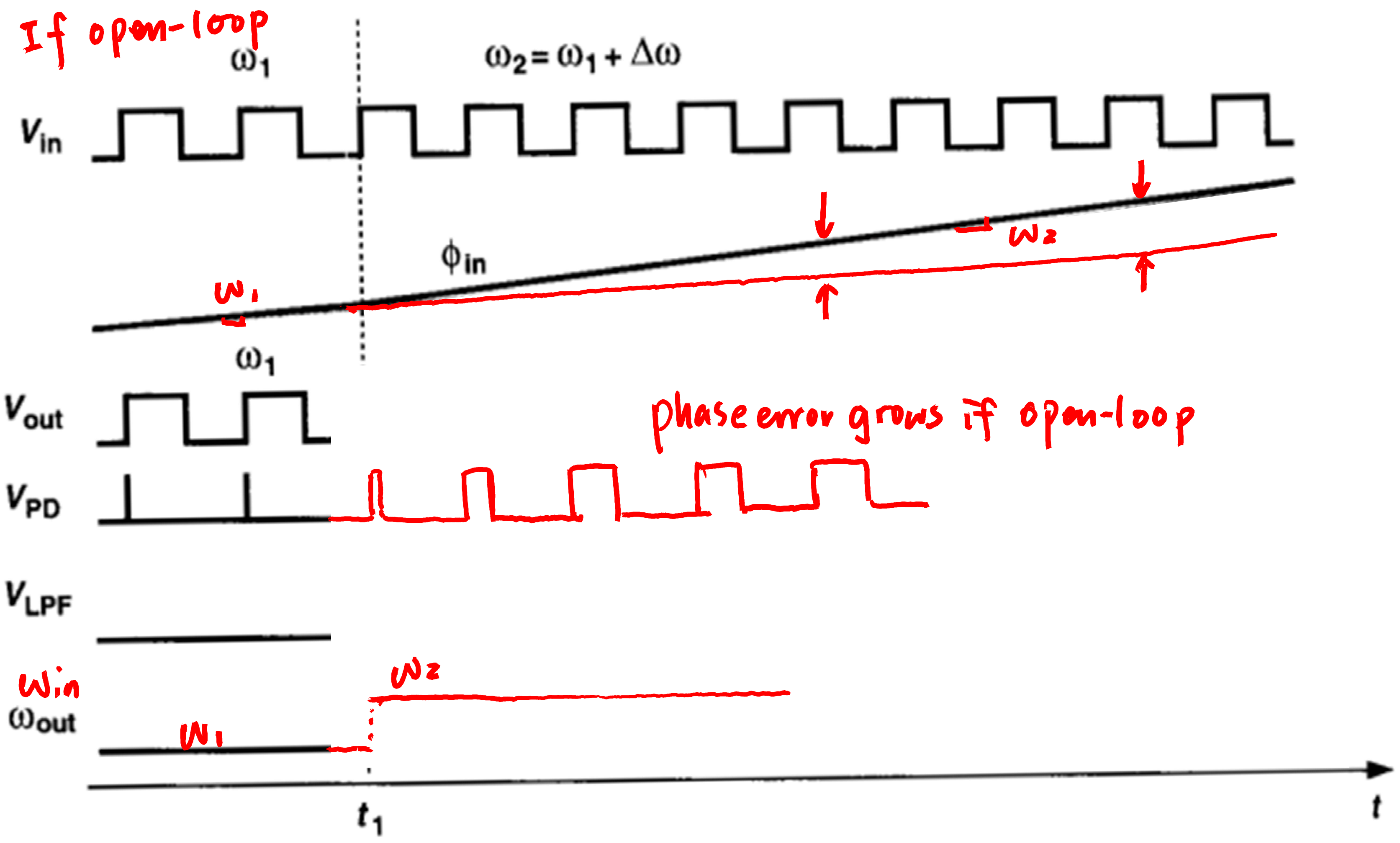
Underdamped Response to Phase Step



- @ t_1 the phase jump happens
- @ t_2 the frequencies are the same, but large phase error
- @ t_3 the phase is the same, but frequency is not

In Case with a Frequency Jump

- How does it look like for a frequency jump?



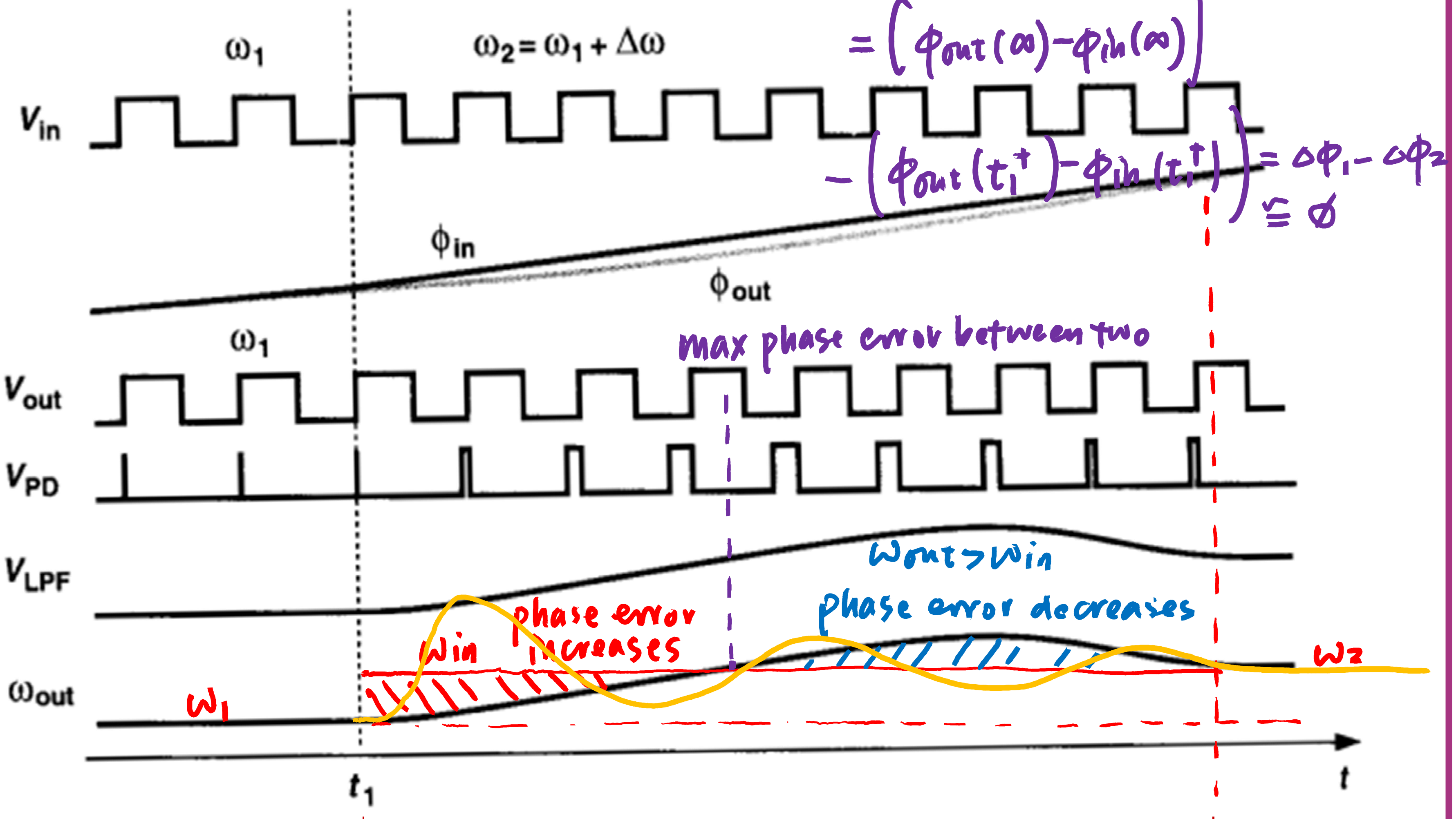
In Case with a Frequency Jump

- How does it look like for a **frequency** jump?

throughout the settling behavior

$$\int_{t_1^+}^{t\to\infty} \omega_{out}(t)-\omega_{in}(t)\,dt$$

$$= \left(\phi_{out}(\infty)-\phi_{in}(\infty)\right) - \left(\phi_{out}(t_1^+)-\phi_{in}(t_1^+)\right) = \Delta\phi_1-\Delta\phi_2 \cong 0$$



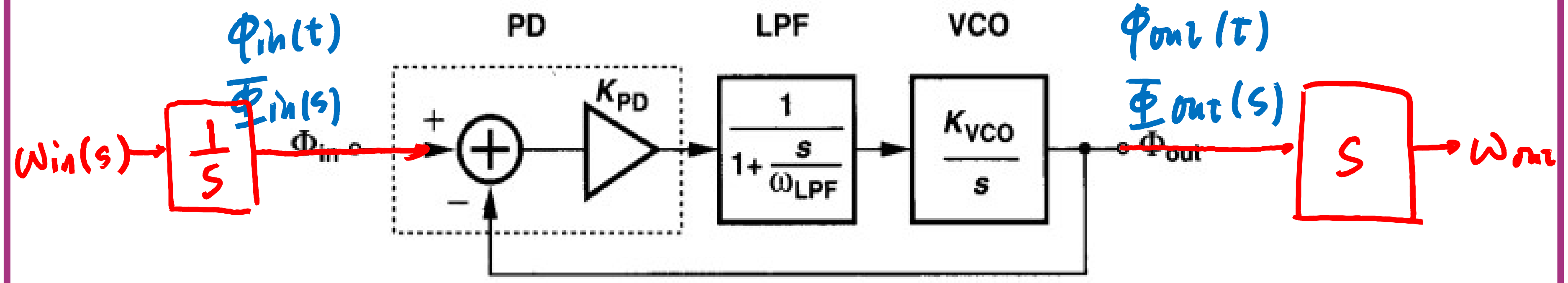
steady state | transient | steady state

Loop Dynamics (I)

- **From previous examples, how fast the loop responses depends on the design of the low-pass filter**

$\omega_{LPF} = \frac{1}{RC}$

- **Linear model of the PLL → to derive the response from $\phi_{ex,in}$ to $\phi_{ex,out}$**



- **Open-loop transfer function** (from phase → voltage → voltage → phase)

$$H(s)|_{open} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

2 poles $\left\{ \begin{array}{l} \text{one @ DC} \\ \text{one @ } \frac{1}{RC} \end{array} \right.$

- Low-frequency gain approaches infinity

$|H(s)|_{open} \to \infty$ as $s \to \cancel{\infty}\ 0$

Loop Dynamics (II)

- **Closed-loop transfer function**

$$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{H_{open}}{1+H_{open}} = \frac{\Phi_{out}(s)}{\Phi_{in}(s)}$$

- Low-frequency gain of unity 1

→ Output tracks the input phase well if input phase varies slowly

→ For input phase step, output phase eventually catches up

- **In fact** $\frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$ the same transfer function

- Low-frequency gain of unity 1

→ Output tracks the input frequency well if input frequency varies slowly

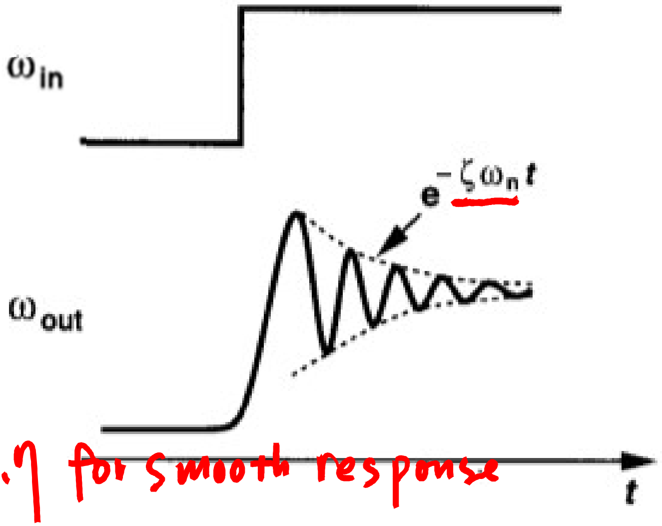
→ For input frequency step, output frequency eventually catches up

Loop Dynamics (III)

- **Second-order transfer function**

$$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\dfrac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\boxed{\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \quad \zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.}$$



we like to set ζ to 0.6~0.7 for smooth response

- If ζ>1, both poles are real → the system is over damped
- If ζ<1, both poles are complex → the step response can be written as

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$$

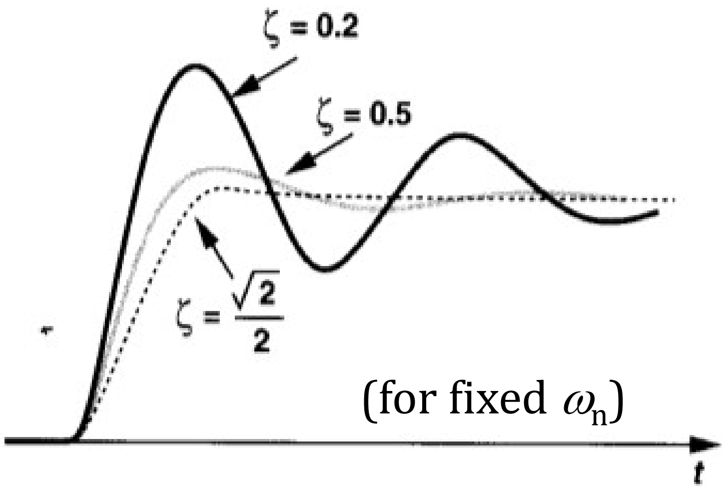
$$\omega_{out}(t) = [1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n\sqrt{1-\zeta^2}t + \theta)]\Delta\omega u(t)$$

(the same behavior for response to phase step)

- Settling speed → $\zeta\omega_n$ needs to be maximized

Loop Dynamics (IV)

- **Damping factor ζ**



(for fixed ω_n)

$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}}.$$

$$\zeta\omega_n = \frac{1}{2}\omega_{LPF}$$

- **For a preferred ζ → ω_n should be maximized for faster response**

→ ω_{LPF} and $K_{PD}K_{VCO}$ should be increased at the same time

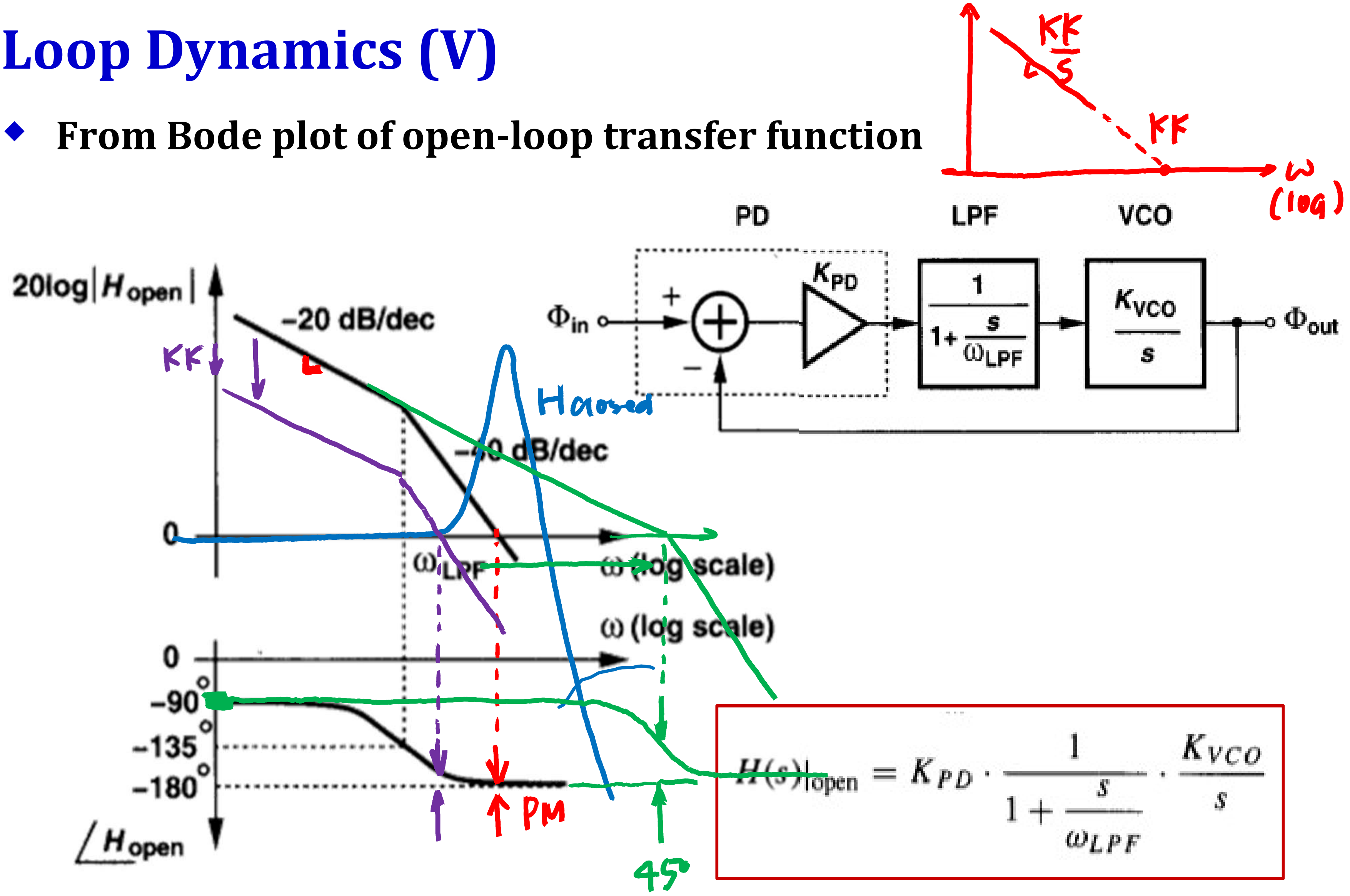
$\omega\uparrow$ $KK\uparrow$ @ V_{ctrl}

→ Strict trade-offs between response time, stability, steady-state ripple & jitter, and steady-state phase error

reference spur

Loop Dynamics (V)

- From Bode plot of open-loop transfer function



$$H(s)|_{open} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

- The loop becomes less stable if …