EE4280 Lecture 2: Mismatch

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Mismatch (I)

$W_0 = 1\mu m$ Even with one single device

$W_1, W_2, W_3, \ldots W_{1M}$

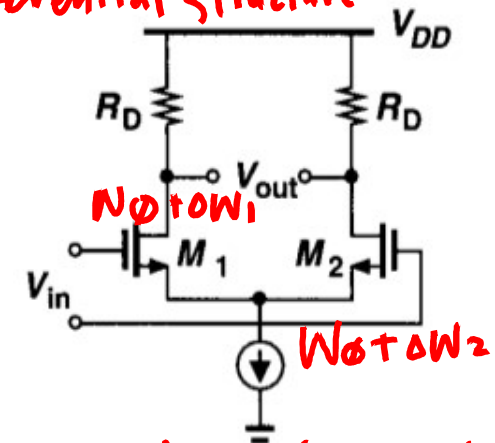
Due to uncertainties in each step of the manufacturing process

For identical devices, random and microscopic variations lead to

- Mismatches in physical dimension
- Mismatches in threshold voltages

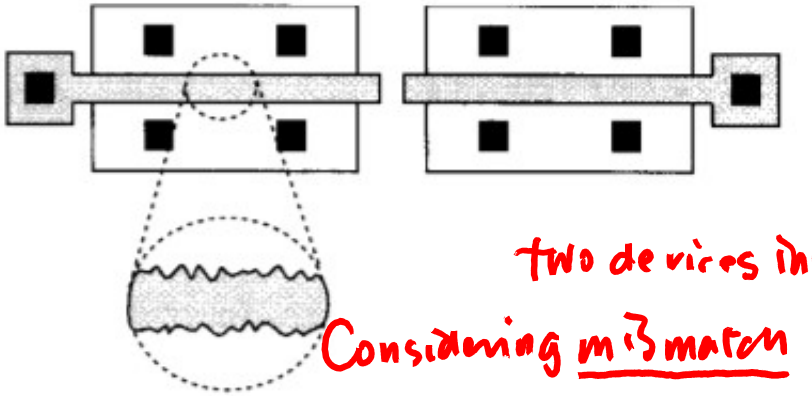
$W_0 + \Delta W_1$, $W_0 + \Delta W_2$ → ΔW_{rms}^2 over the entire sample space

differential structure



$W_0 + \Delta W_1$

$W_0 + \Delta W_2$



two devices involved

Considering mismatch ΔW_{12}

$\Delta W_{12} = (W_1 - W_2) = \Delta W_1 - \Delta W_2$

$\overline{\Delta W_{12}} = 0$

$\overline{\Delta W_{12}^2} = \overline{(\Delta W_1 - \Delta W_2)^2}$

To study mismatch of devices:

1. Identify and formulate the mechanisms leading to mismatches
2. Analyze the impact on circuit performance
   → Techniques to suppress the impact from mismatches

$= avg(\Delta W_1^2 - 2\Delta W_1 \Delta W_2 + \Delta W_2^2)$

$= 2 \cdot \Delta W_{rms}^2 - 2\,\overline{\Delta W_1 \Delta W_2}$

$$\sigma^2_{W_{12}rms} = 2\cdot\sigma^2_{Wrms} - 2\cdot\overline{\delta W_1\cdot\delta W_2}$$

for $\overline{\delta W_1\cdot\delta W_2}$: if M_1 and M_2 are totally uncorrelated

$$\overline{\delta W_1\cdot\delta W_2} = \emptyset$$

$$\sigma_{W_{12},rms} = \sqrt{2}\cdot\sigma_{Wrms}$$

What if we can increase the correlation between the two

So that $\overline{\delta W_1\cdot\delta W_2} \rightarrow \overline{\delta W^2}$

then $\sigma^2_{W_{12}rms} \rightarrow \emptyset$

Mismatch (II)

$\Delta L_B = \frac{\Delta L_1 + \Delta L_2}{2}$

$\overline{\Delta L_B^2} = \frac{1}{4}\left(\overline{\Delta L_1^2} + \overline{\Delta L_2^2} + 2\overline{\Delta L_1 \cdot \Delta L_2}\right)$

$\left(2\overline{\Delta L_1 \cdot \Delta L_2} \to 0\right)$

$\Delta L_{B,rms} = \frac{1}{\sqrt{2}} \Delta L_{A,rms}$

For a transistor operating in saturation region

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

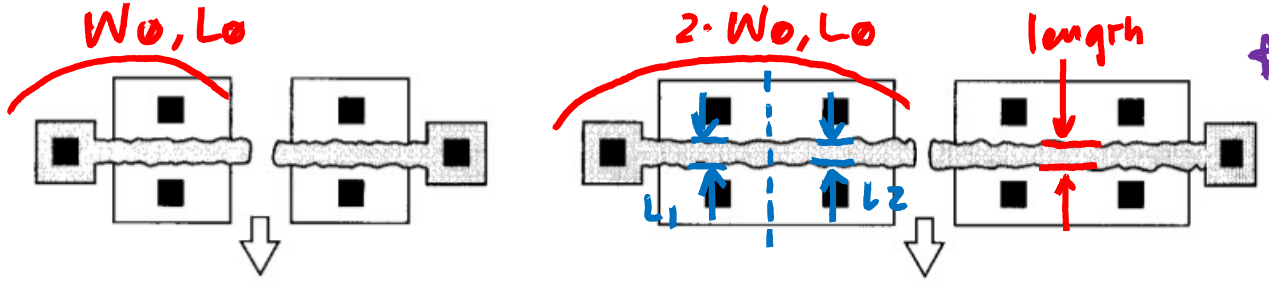
Device #A Device #B

All mismatches decreases as the area of the transistor *WL* increases

- **Random variations experience greater averaging**

★ if L_1 & L_2 uncorre.

★ if L_1 & L_2 highly corre. then $L_1 = L_2$ → $\Delta L_{B,rms} = \Delta L_{A,rms}$



$L_A = L_0 + \Delta L_A$

$L_B = L_0 + \Delta L_B$

$= \frac{L_1 + L_2}{2} = \frac{L_0 + \Delta L_1 + L_0 + \Delta L_2}{2}$

$= L_0 + \frac{\Delta L_1 + \Delta L_2}{2}$

ΔL_B, err of the wider tran.

Can be extended to other device parameters

depends on factory

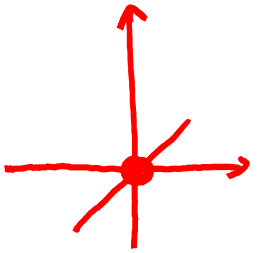
ΔV_{TH}

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \qquad \Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}$$

DC Offset

non-zero error

amplifier chain



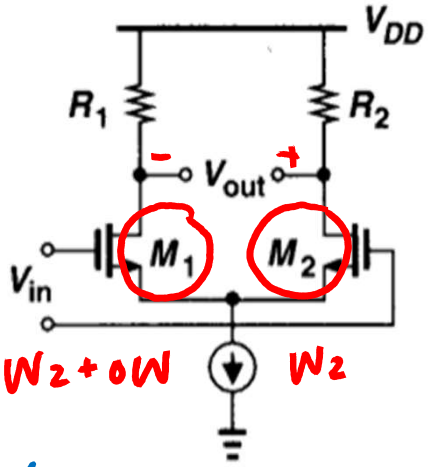
linearity

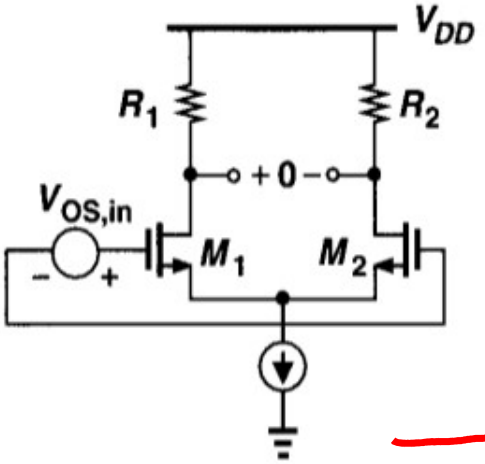
With perfect symmetry $V_{out} = 0$ when $V_{in} = 0$

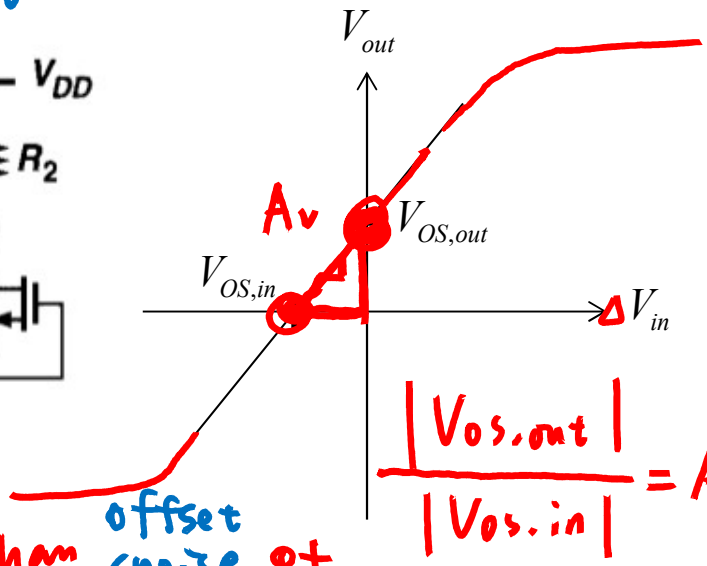
noise

With mismatches $V_{OS,out} \neq 0$ when $V_{in} = 0$

offset



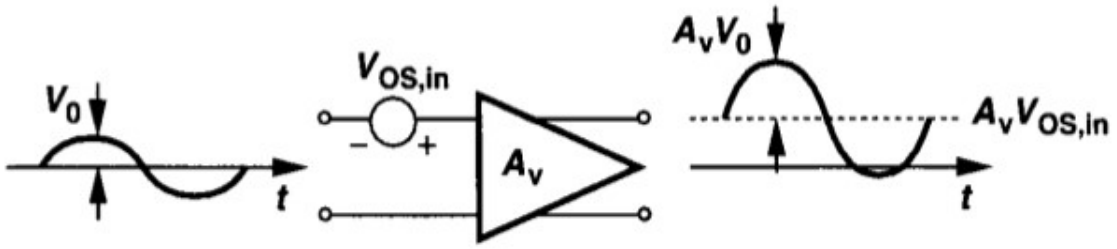




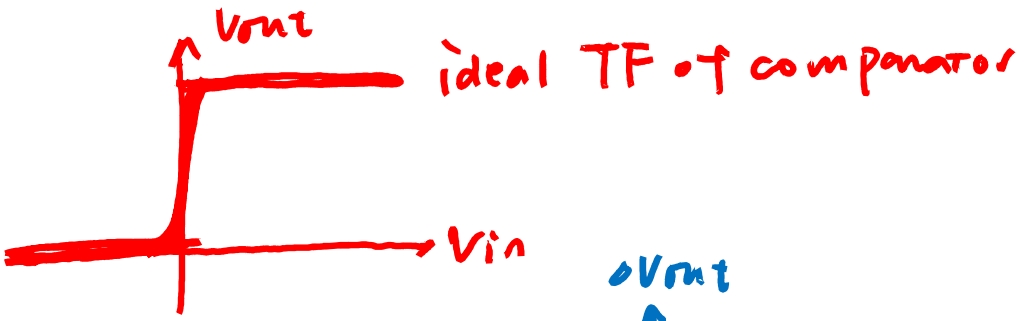
$$\frac{|V_{os,out}|}{|V_{os,in}|} = A_v$$

offset/noise in the first amp. is more critical than offset/noise of the following stages

- → May saturate the following stages
- → Degrade the precision with which signals can be measured



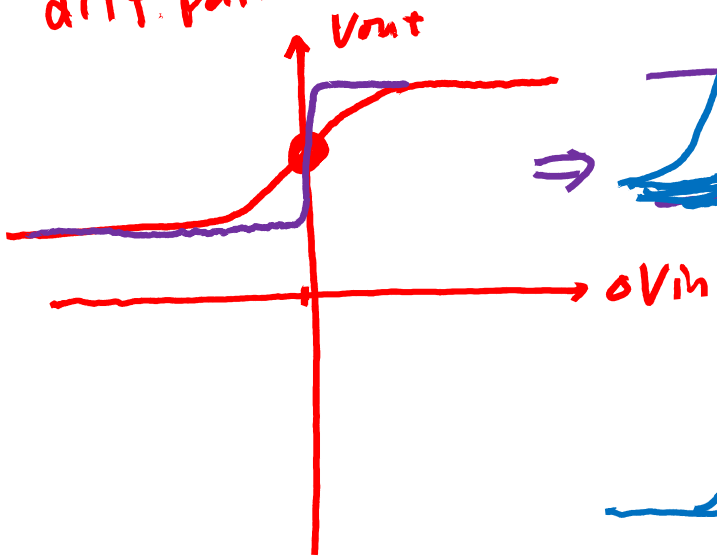
Comparator (ADC, mixed-signal ckt)



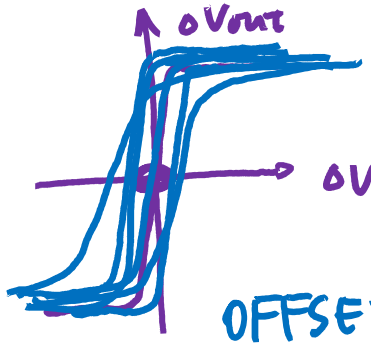
Vref = 0

high-gain amplifier

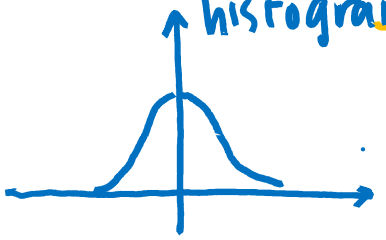
diff. pair



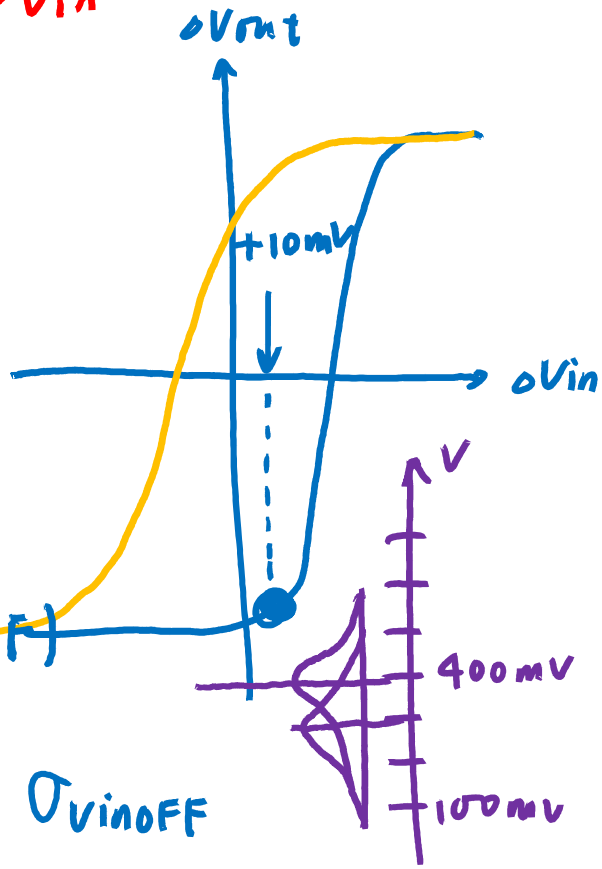
⇒



OFFSET

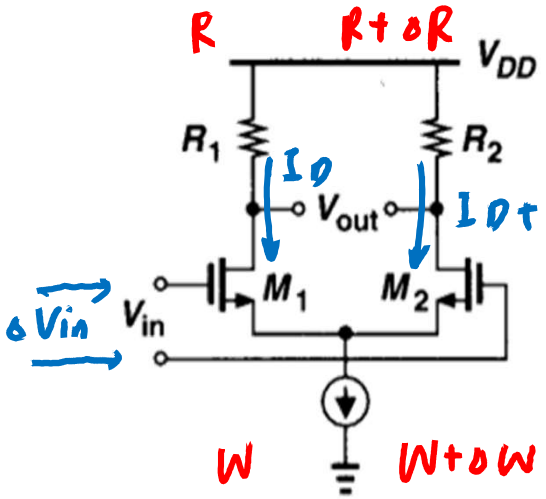


σ_{VinOFF}



DC Offset of a differential pair

- To calculate the input-referred offset



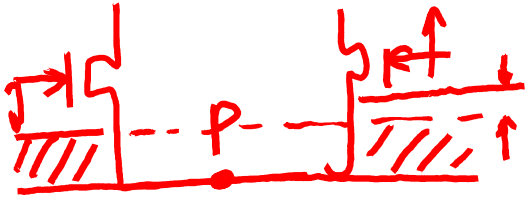
$V_{out}=0 \Rightarrow I_D R_D = (I_D+\Delta I_D)(R_D+\Delta R) = I_D R_D\left(1+\frac{\delta I}{I}\right)\left(1+\frac{\delta R}{R}\right)$

$\cong I_D R_D\left(1+\frac{\delta I}{I}+\frac{\delta R}{R}\right)$

$V_{OS,in} = V_{GS1} - V_{GS2}$

$= V_{TH}+V_{OV1}-(V_{TH2}+V_{OV2}) \Rightarrow \frac{\delta I}{I} = -\frac{\delta R}{R}$

$= -\delta V_{TH} + \sqrt{\frac{I_{D1}}{\mu C_{ox}\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{(I_D+\delta I)}{\mu C_{ox}\left(\frac{W}{L}+\delta\frac{W}{L}\right)}}$



$\cong -\delta V_{TH} + \sqrt{\frac{I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}\cdot\left(1-\left(1+0.5\frac{\delta I}{I}\right)\left(1-0.5\frac{\delta W}{W}\right)\right)$

$= -\delta V_{TH} + \sqrt{\frac{I_D}{\mu C_{ox}\left(\frac{W}{L}\right)}}\left(-0.5\frac{\delta I}{I}+0.5\frac{\delta W}{W}\right)$

$= -\delta V_{TH} + \frac{V_{OV}}{2}\left(\frac{\delta W}{W}-\frac{\delta I}{I}\right) \Rightarrow -\delta V_{TH} + \frac{V_{OV}}{2}\left(\frac{\delta W}{W}+\frac{\delta R}{R}\right)$

DC Offset of a differential pair

- **To calculate the input-referred offset**

$$\overline{V_{OS,in}^2} = \overline{\left(\frac{V_{GS}-V_{TH}}{2}\left[\frac{\Delta R_D}{R_D}+\frac{\Delta(W/L)}{(W/L)}\right]-\Delta V_{TH}\right)^2}$$

  - Depends on device mismatches and bias conditions
- **Offset can be viewed as low-frequency noise**
  - Similar to noise, larger g_{m1} suppresses input-referred offset voltage
- **Variance:**

$$V_{OS,in,rms} = \sqrt{\left(\frac{V_{OV}}{2}\right)^2\left(\frac{\Delta R_{rms}}{R_D}\right)^2+\left(\frac{V_{OV}}{2}\right)^2\left(\frac{\Delta W_{rms}}{W}\right)^2+\Delta V_{TH\,rms}^2}$$

Sample space

- **Consider only transistor mismatch, for I_{D1}=I_{D2}**

① ΔV_{TH} has a direct impact on $V_{OS,in}$

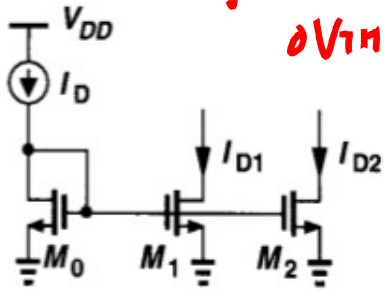
② We want $V_{OV}\downarrow$ $W/L\uparrow$ $g_m\uparrow$

Current mismatch in current mirror

- **Consider nominally identical transistors (M_1 and M_2) and neglect r_o**

Goal: Calculate $\frac{\Delta I}{I}$

as a result of ΔW, ΔV_{TH}



W $W+\Delta W$

V_{TH} $V_{TH}+\Delta V_{TH}$

I_D $I_D+\Delta I$

(REF)

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2$$

$$= f\left(\mu C_{ox}, \frac{W}{L}, V_{GS}, V_{th}\right)$$

total differential

$$\Delta y = \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \cdots$$

$$\Delta I_D = \frac{\partial I_D}{\partial (W/L)}\Delta\left(\frac{W}{L}\right) + \frac{\partial I_D}{\partial (V_{GS}-V_{TH})}\Delta(V_{GS}-V_{TH})$$

(gain) sensitivity of cur. to W.

- **From output current point of view** (2)
  - Smaller g_m required to suppress the mismatch
  - The same for noise current

$$\Delta I = \left(\frac{1}{2}\mu C_{ox} V_{ov}^2\right)\cdot\Delta\left(\frac{W}{L}\right) + \left(\mu C_{ox}\frac{W}{L}V_{ov}\right)\cdot\Delta V_{ov}$$

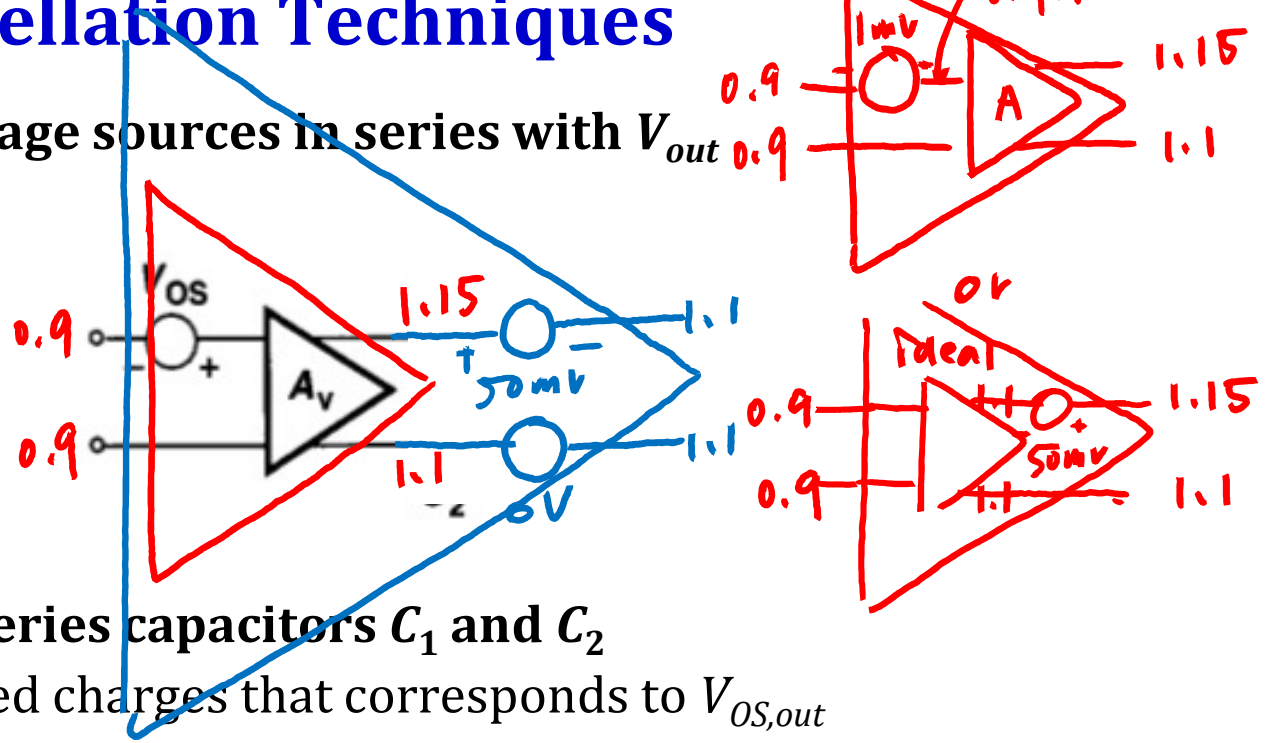
(1)

$$\Rightarrow \frac{\Delta I}{I} = \frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)} - 2\frac{\Delta V_{TH}}{V_{ov}}$$

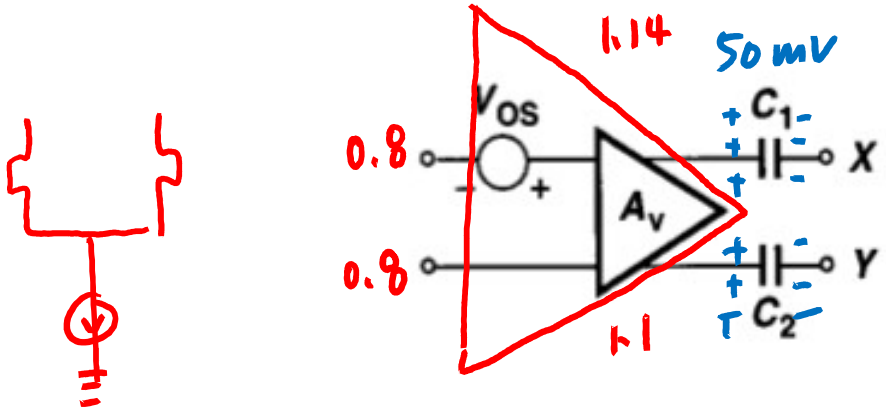
size err. impact directly on ΔI

Offset Cancellation Techniques

- **Add two voltage sources in series with V_{out}**

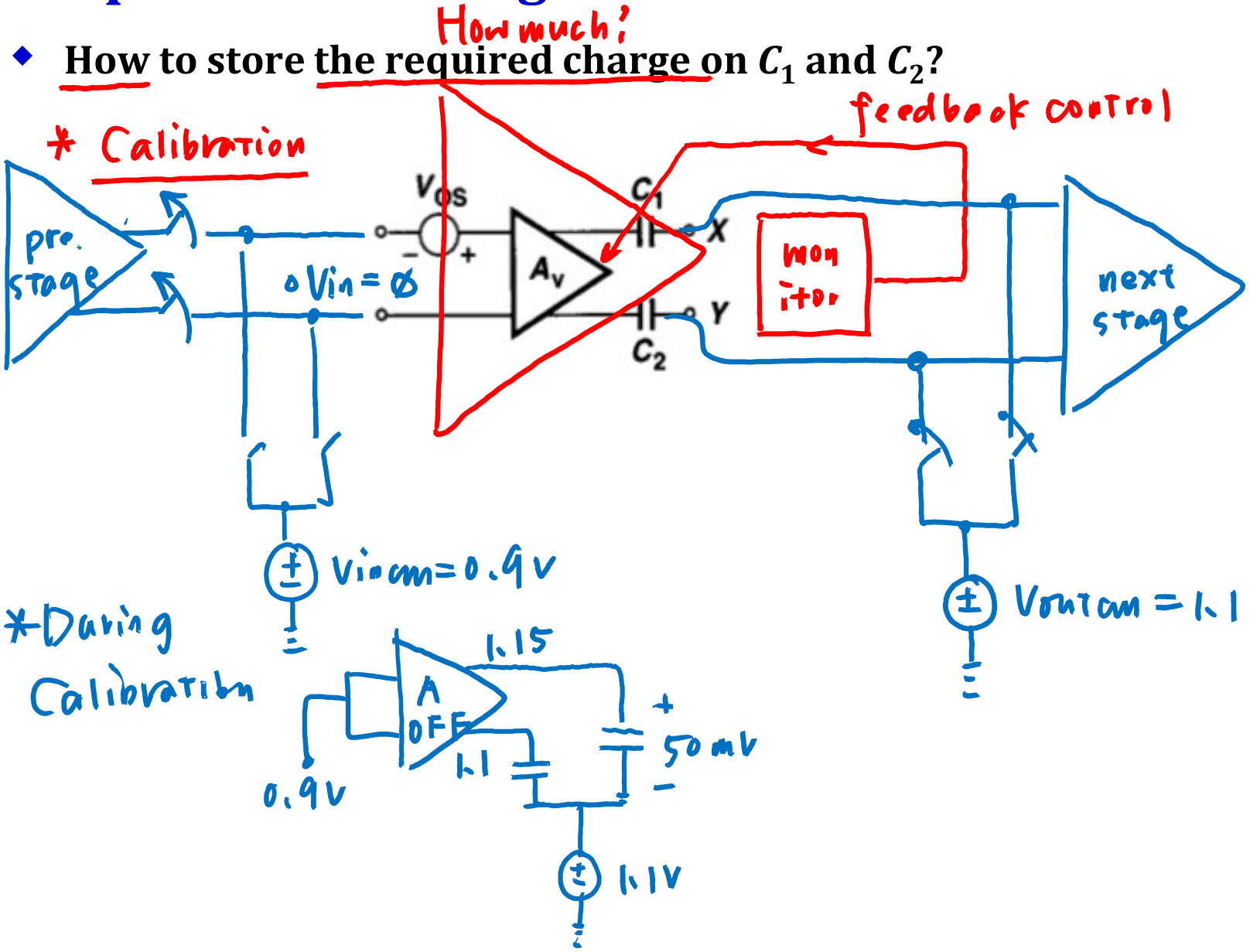


- **Use output series capacitors C_1 and C_2**
  - With stored charges that corresponds to $V_{OS,out}$



Output Offset Storage

- How to store the required charge on C_1 and C_2?



* During Normal Operation