EE4280 Lecture 8:
Charge-Pump Phase-Locked Loops

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Issues with Type-I Phase-Locked Loop

- **Strict trade-offs between response time, stability, steady-state ripple & jitter, and steady-state phase error**

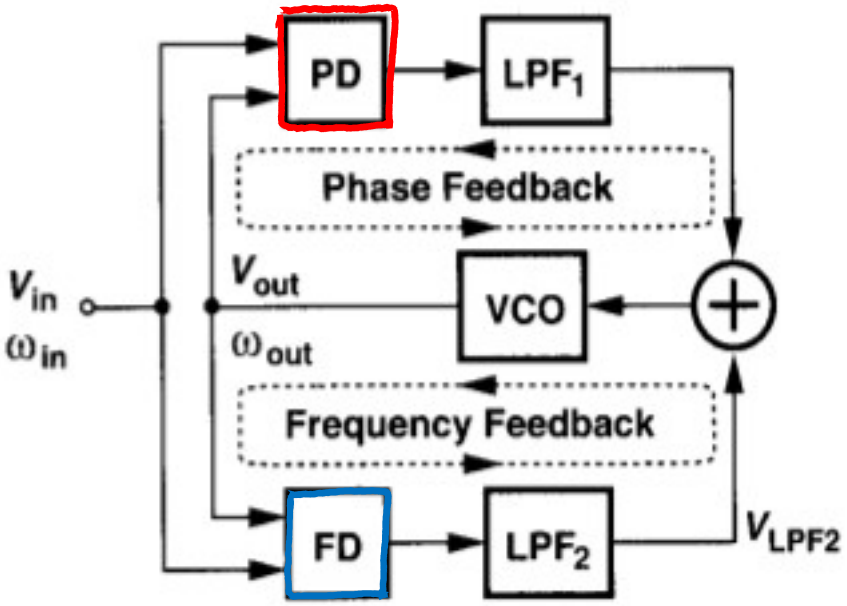
- **Limited acquisition range**
  - The initial frequency of VCO can be very far from the input frequency
  - The acquisition range is on the order of ω_{LPF}

→ Difference between win and ω_{out} has to be less than ω_{LPF}

→ Trade-offs further tightened

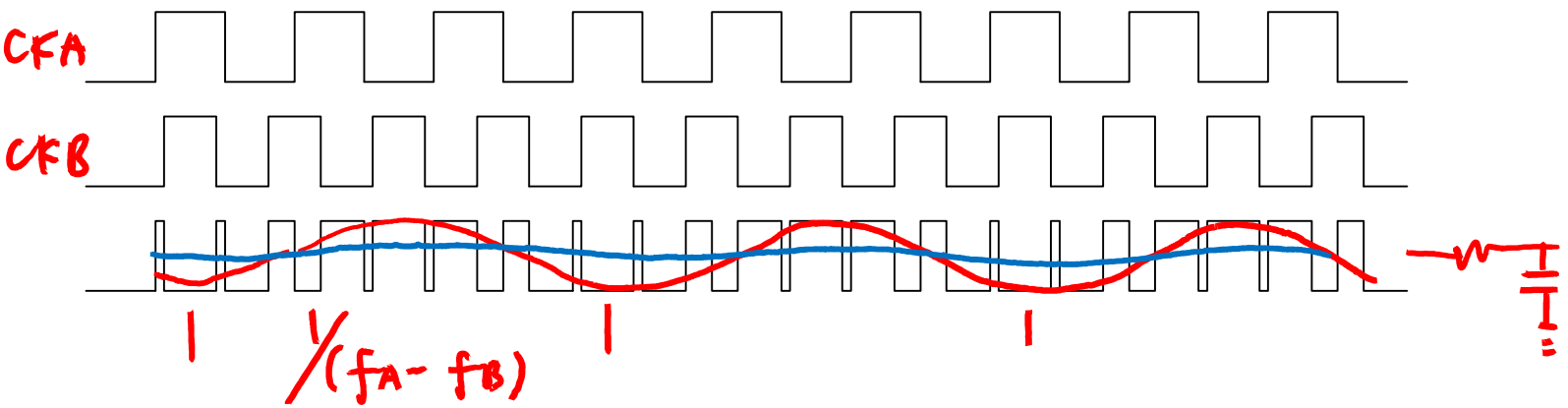
- Possible solution:

between steady state behavior and dynamic behavior



Two Inputs with Different Frequencies

- **An XOR cannot detect frequency error**



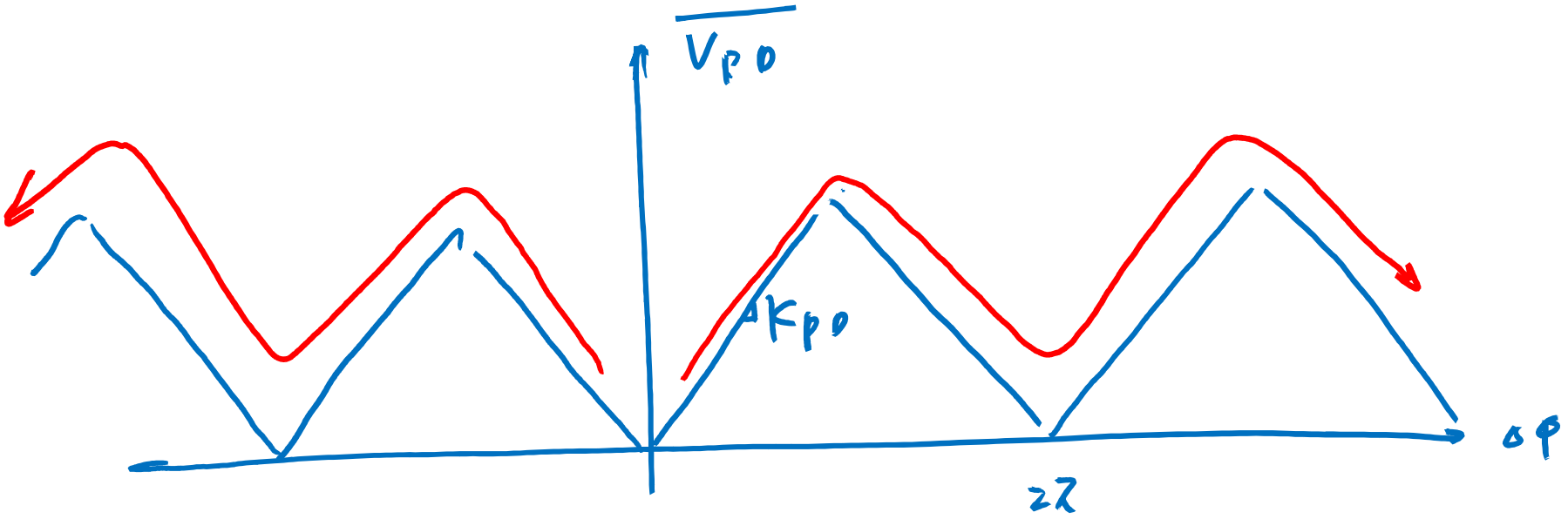
- **Output pulses varies periodically**
  - At beat frequency (the frequency difference of the two)

→ The larger the difference, the faster the output pulse width changes

→ The LPF output stays constant and does not change due to the change of phase difference

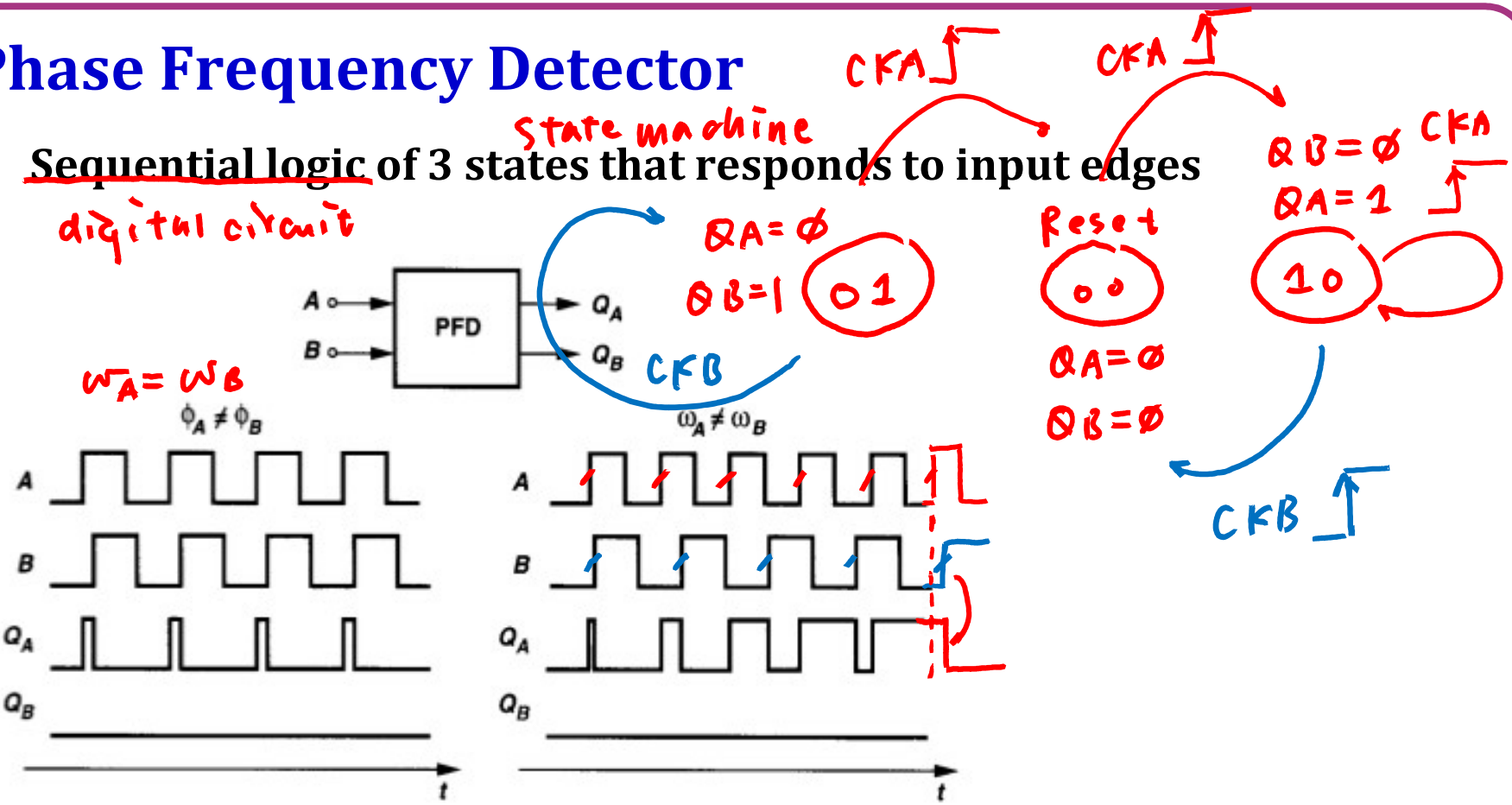
→ XOR (phase detector) does not detect frequency difference

Combinational nature of PD (XOR)



Phase Frequency Detector

- **Sequential logic of 3 states that responds to input edges**



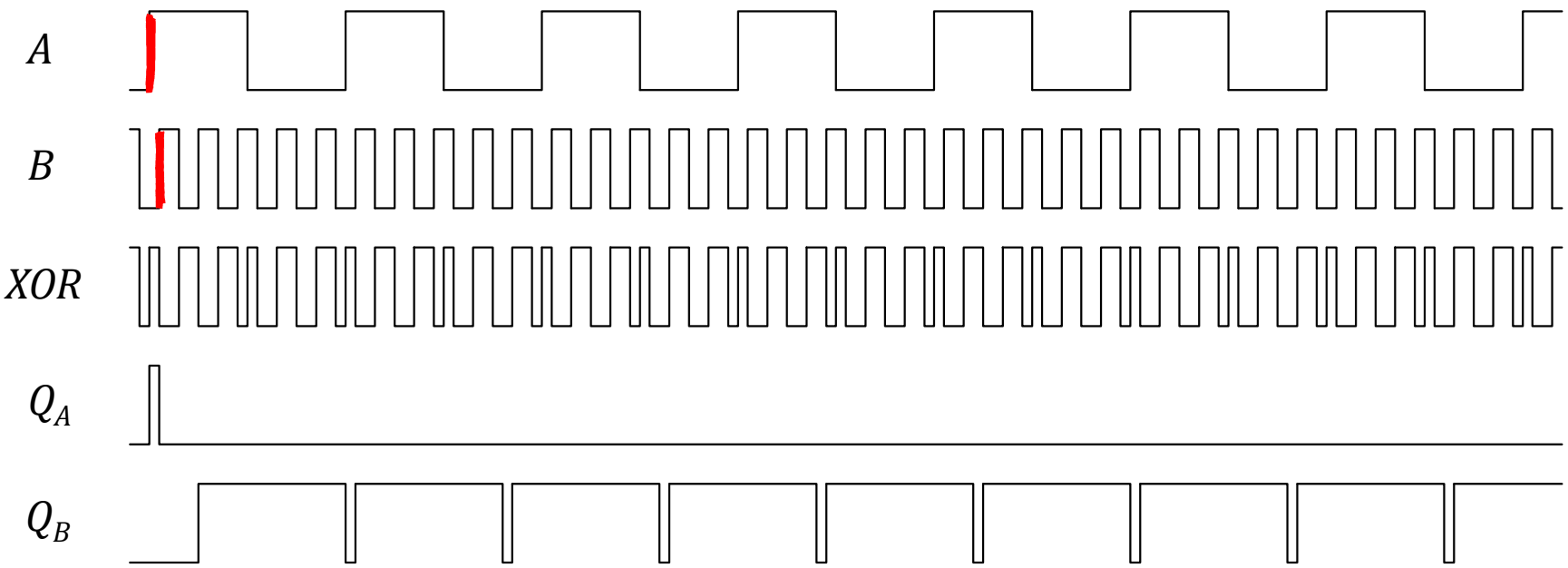
- Reset state: Q_A=Q_B=0 initially
- Q_A responds to rising edge of input A

→ does not reset until rising edge of input B

→ Two outputs indicate fast and slow in either phase or frequency

PFD – in Case with Large Frequency Difference

- **For larger frequency difference**



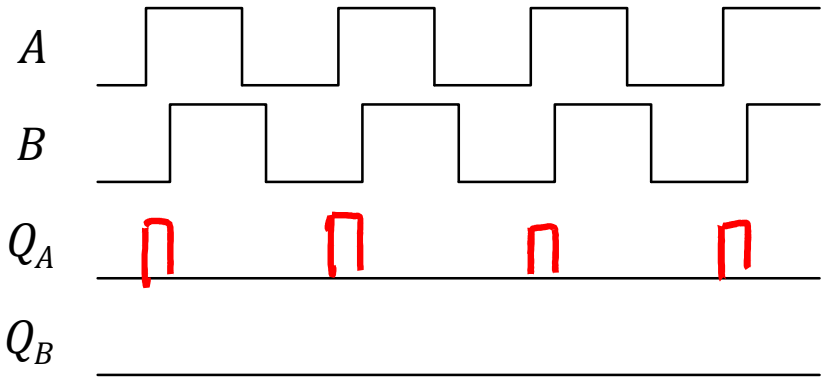
The Transfer Function of PFD

$\omega_1 = \omega_2$

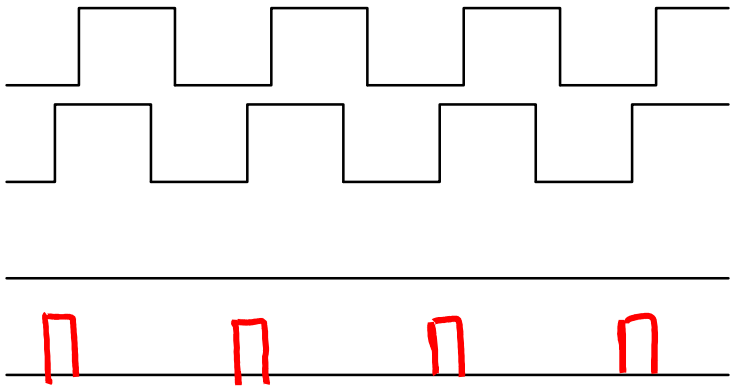
the module behaves like a PD

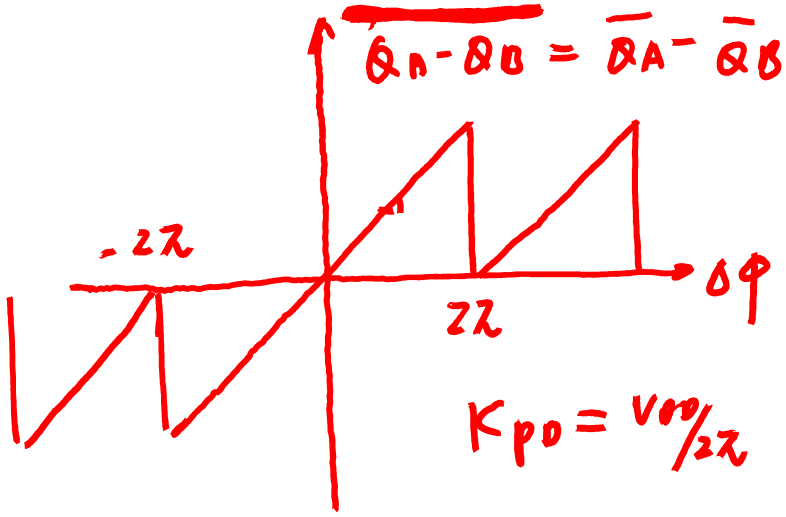
- Consider two outputs of the same frequency

in case where A leads B



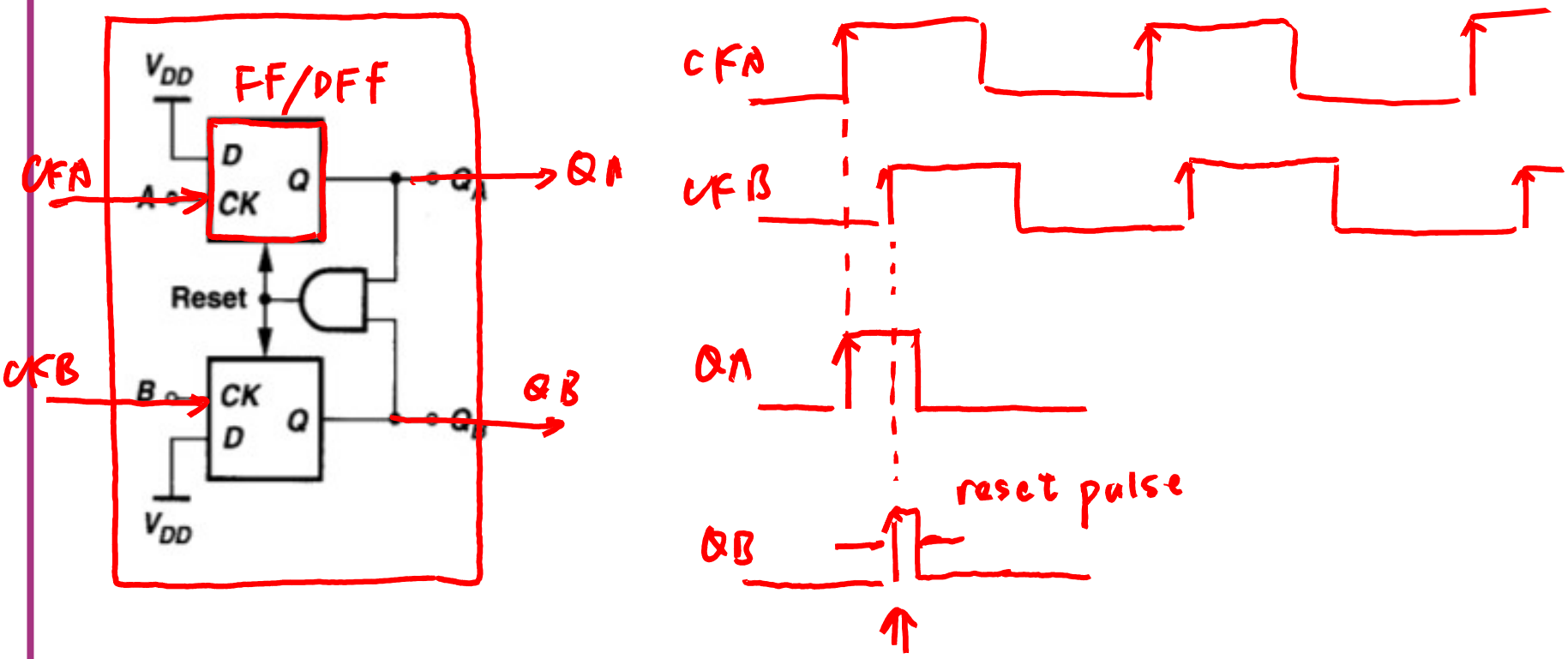
in case where B leads A





Implementation Example

- **Using resettable flip-flops**

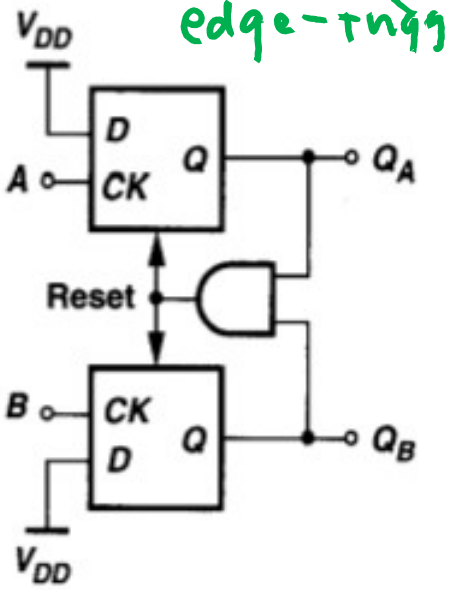


- **QA and QB are simultaneously high for a short period of time**

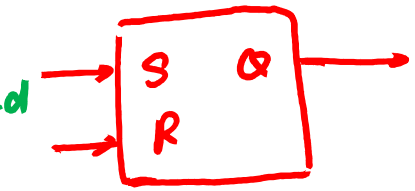
→ Reset pulse

Implementation Example

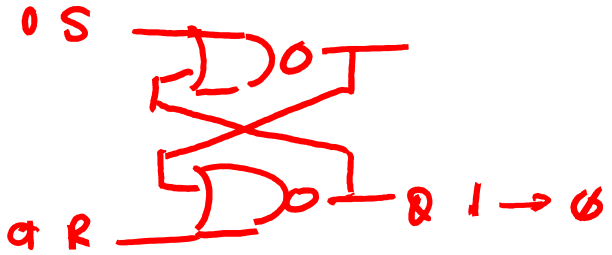
- Using resettable flip-flops → implemented using SR latch?

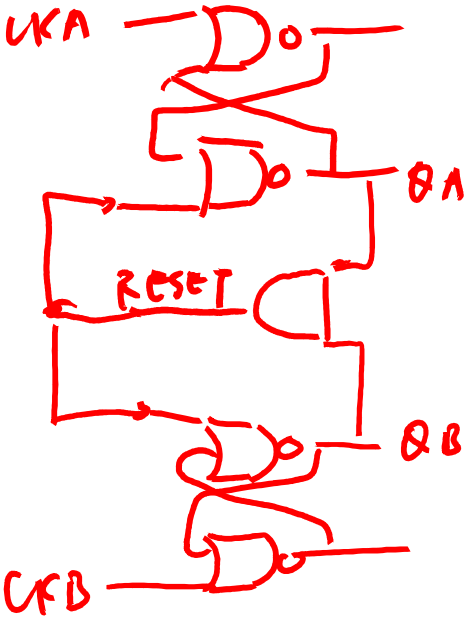


edge-triggered



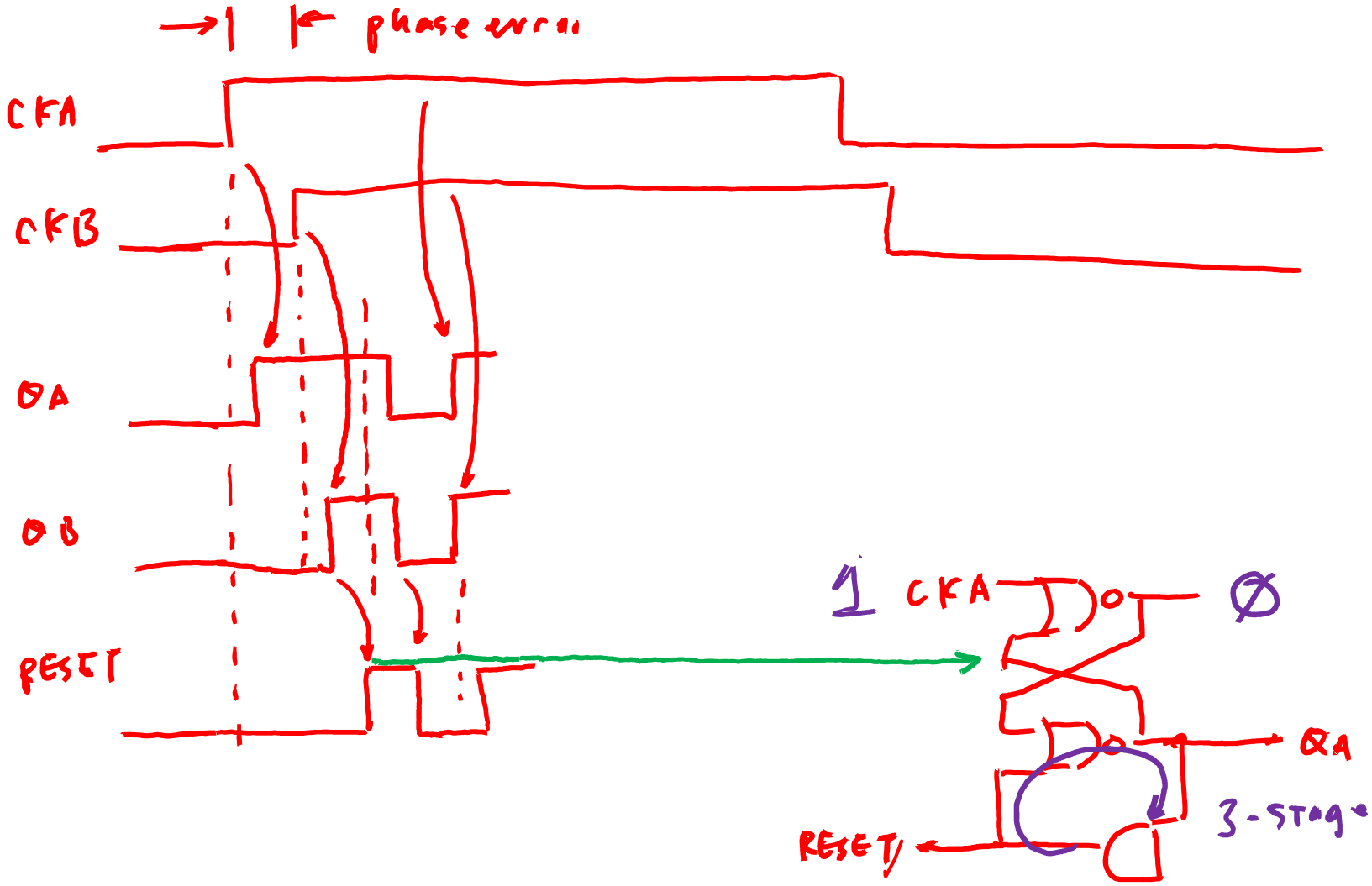
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

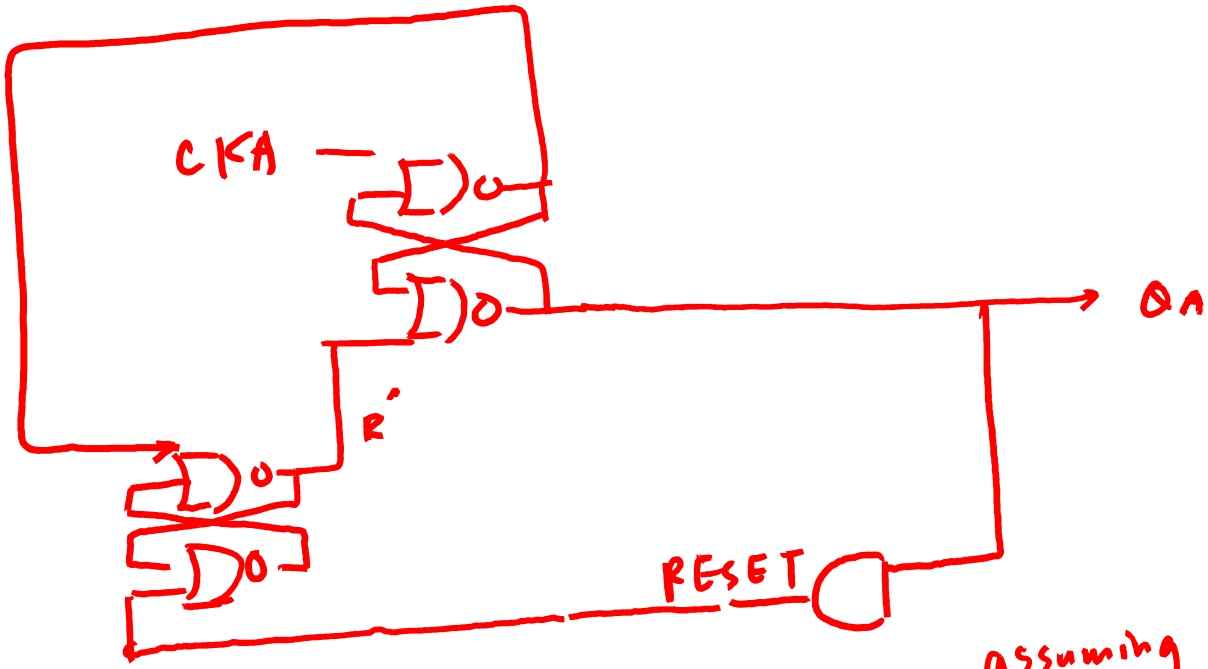




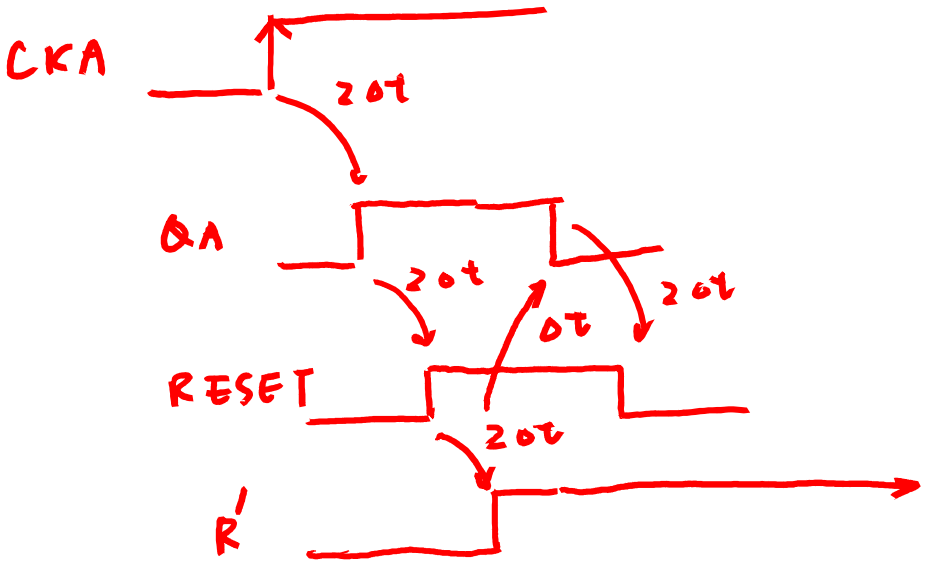
The Problem of Using SR Latch for Resettable FF

- For two clocks with close phases

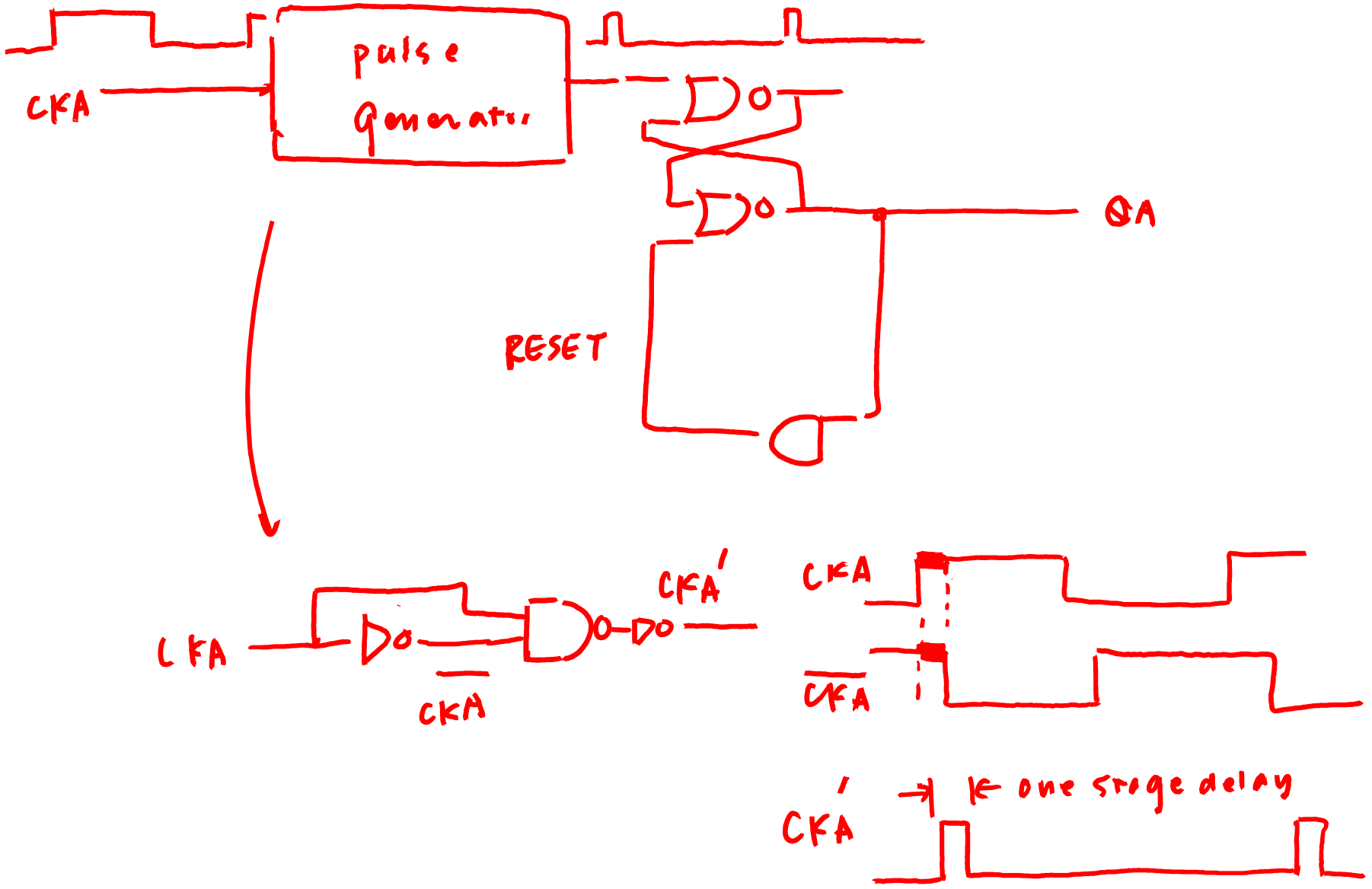




Assuming QB is high already



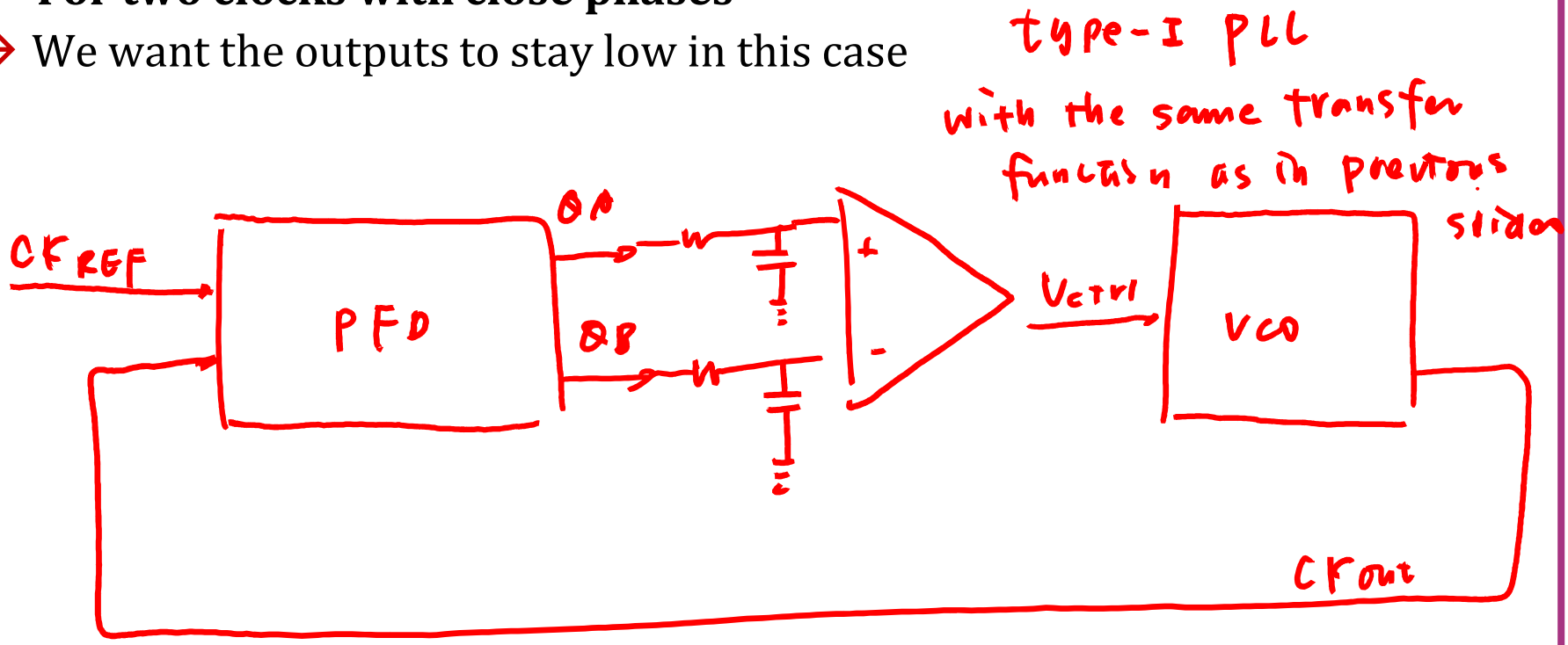
RESET pulse is 5ot


CKA
pulse
generator
D
Q
D
Q
QA
RESET
CKA
CKA'
D
Q
D
Q
CKA
CKA
CKA
CKA'
one stage delay

The Problem of Using SR Latch for Resettable FF

- **For two clocks with close phases**

→ We want the outputs to stay low in this case



- **How many numbers of stage delay is the reset pulse?**

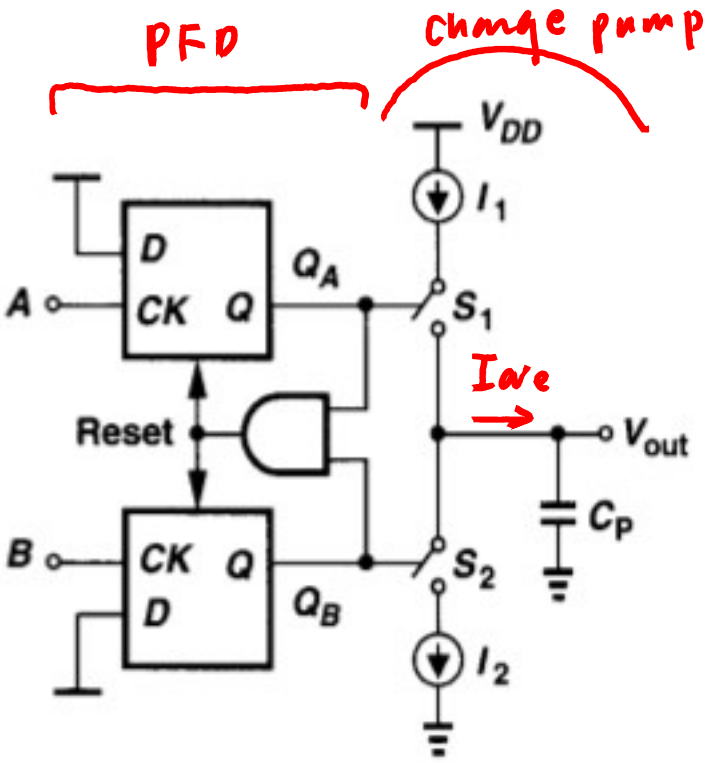
1

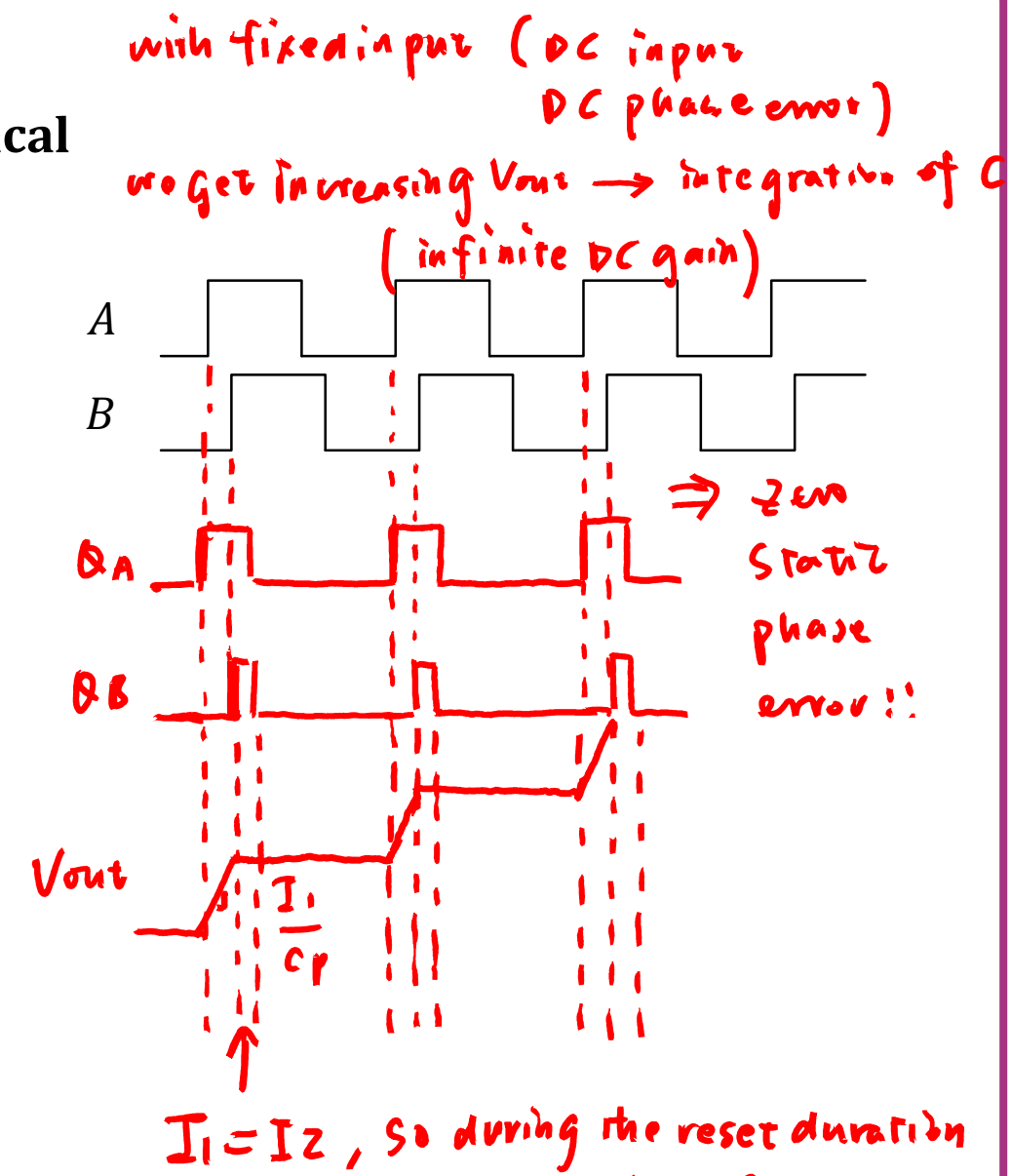
To Take the PFD's Outputs to VCO

- **A simple way**

Charge Pump

- I_1 and I_2 are nominally identical
- In case where A leads B

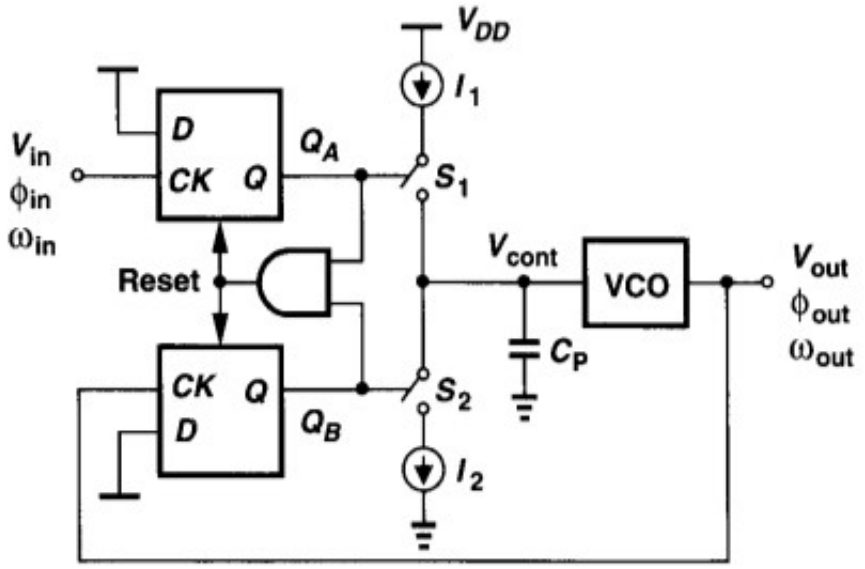


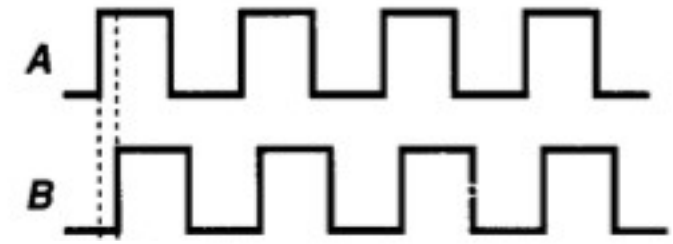


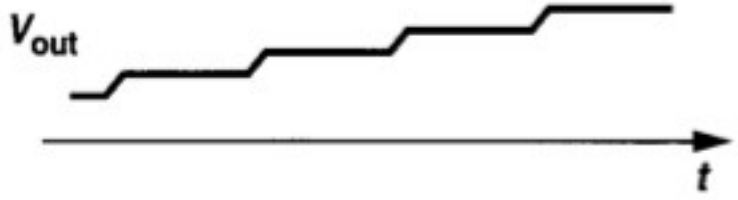
- The slope of V_{out}
- Effect of the reset pulses that appear in both Q_A and Q_B

Dynamics of Charge-Pump Phase-Locked Loops

- When the system is just turned on, ω_{out} and ω_{in} may be very different
- As ω_{out} approaches ω_{in}
- Transfer function of PFD+CP
  In case if $\Delta\phi_{in}$ doubles







Dynamics of Charge-Pump Phase-Locked Loops

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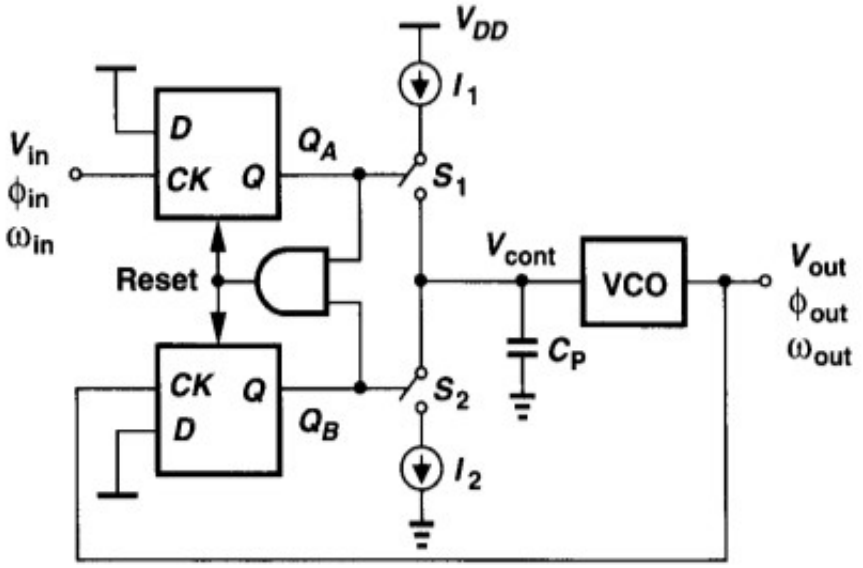
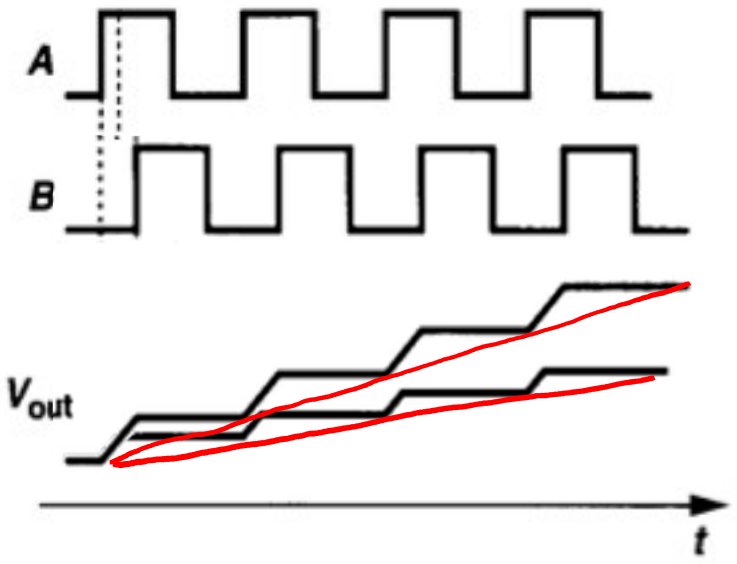
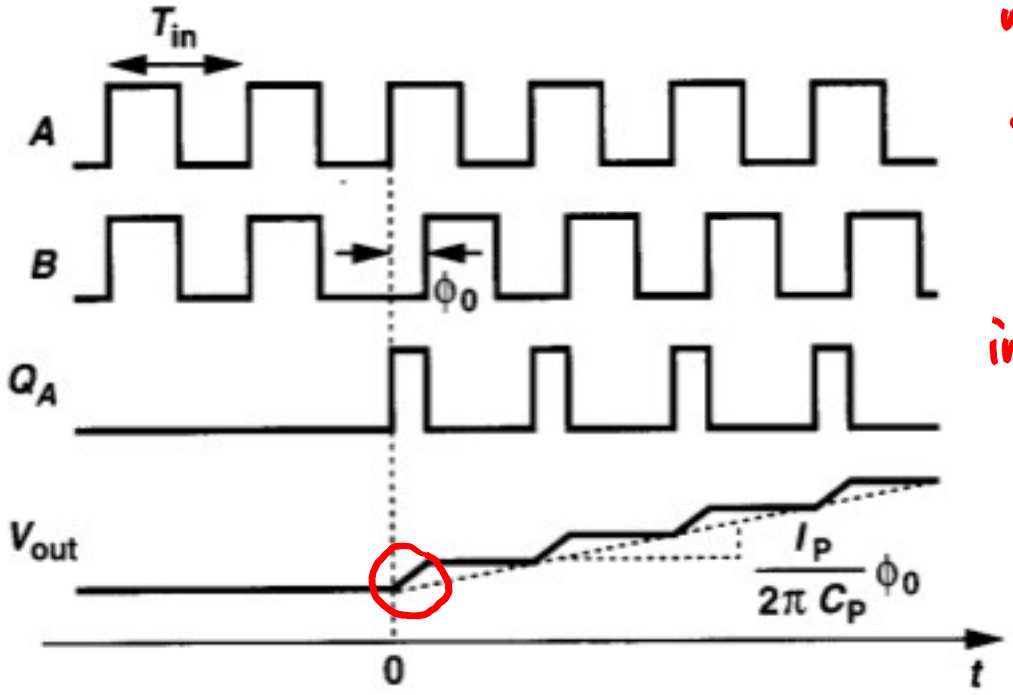




➔ Strictly speaking: not a linear system

Transfer Function of PFD+CP (I)

- With a phase step at input



with $\phi_{in}(t) = \phi_0 \cdot u(t)$

step response

$$V_{out}(t) = \frac{I}{C_P} \cdot \frac{\phi_0}{2\pi} \cdot t \cdot u(t)$$

impulse response

$$h(t) = \frac{I}{C_P} \frac{\phi_0}{2\pi} u(t)$$

$\Rightarrow$ transfer function

$$\frac{V_{out}}{\Phi_{in}}(s) = \frac{I}{C_P} \cdot \frac{1}{2\pi} \cdot \frac{1}{s}$$

$\frac{I_P}{C_P}$ for the duration of ϕ_0

average slope

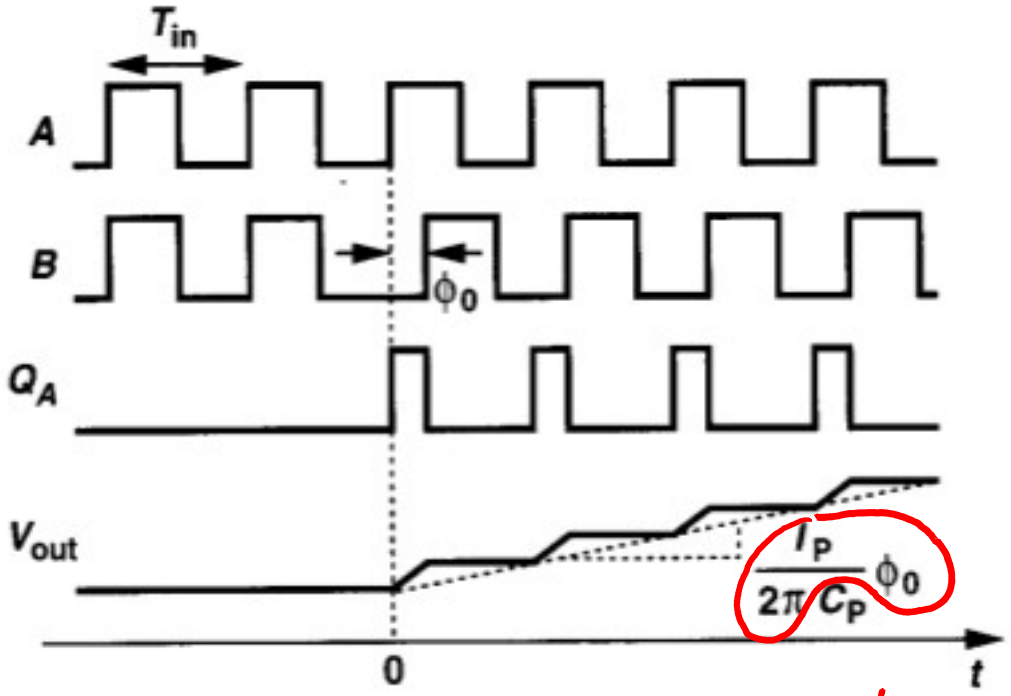
$$\frac{I}{C_P} \frac{\phi_0}{2\pi}$$

Transfer Function of PFD+CP (II)

- Average output current with $\Delta\phi_{in}$

I_{ave} → $\frac{1}{sC}$ → V_{out}

➔ The current flows into a capacitor, establishing V_{out}



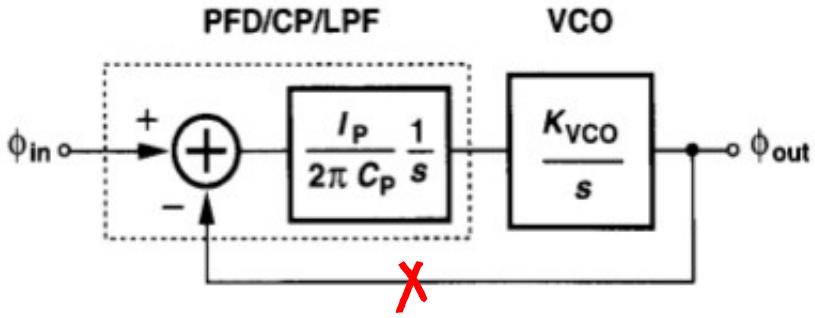
$$\frac{V_{out}}{\Phi_{in}}(s) = \frac{I}{2\pi}\frac{1}{sC}$$

$$I_{ave} = I\frac{\phi_0}{2\pi}$$

$$V_{out} = I_{ave}\frac{1}{sC} = I\frac{\phi_0}{2\pi}\frac{1}{sC}$$

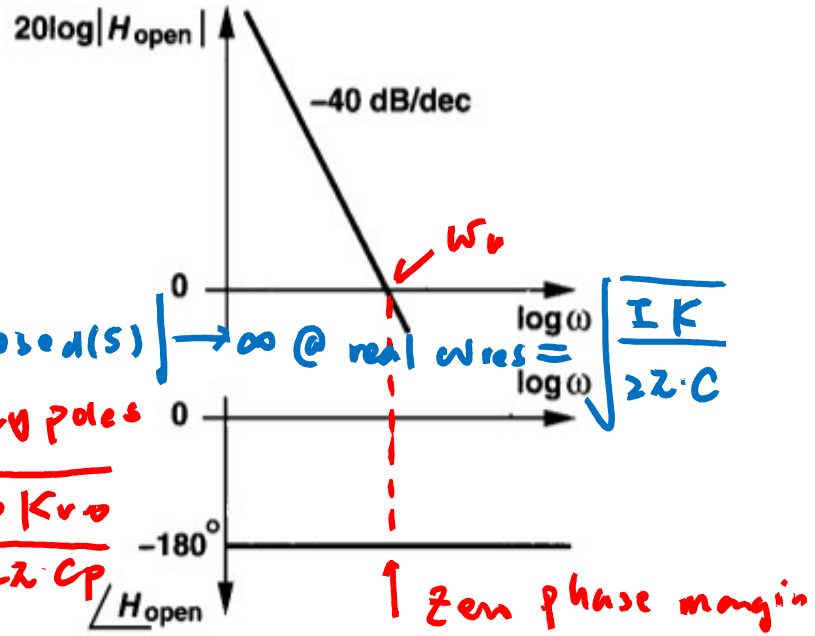
Loop Dynamics (I)

- **Linear model of the PLL → to derive the response from ϕ_{in} to ϕ_{out}**



- **Open-loop transfer function** (from phase → voltage → voltage → phase)

$$\frac{\Phi_{out}}{\Phi_{in}}(s)\Big|_{open} = \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{s^2}$$



- Two poles at origin → type-II PLL

- **Closed-loop transfer function**

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}}{s^2 + \frac{I_P K_{VCO}}{2\pi C_P}}$$

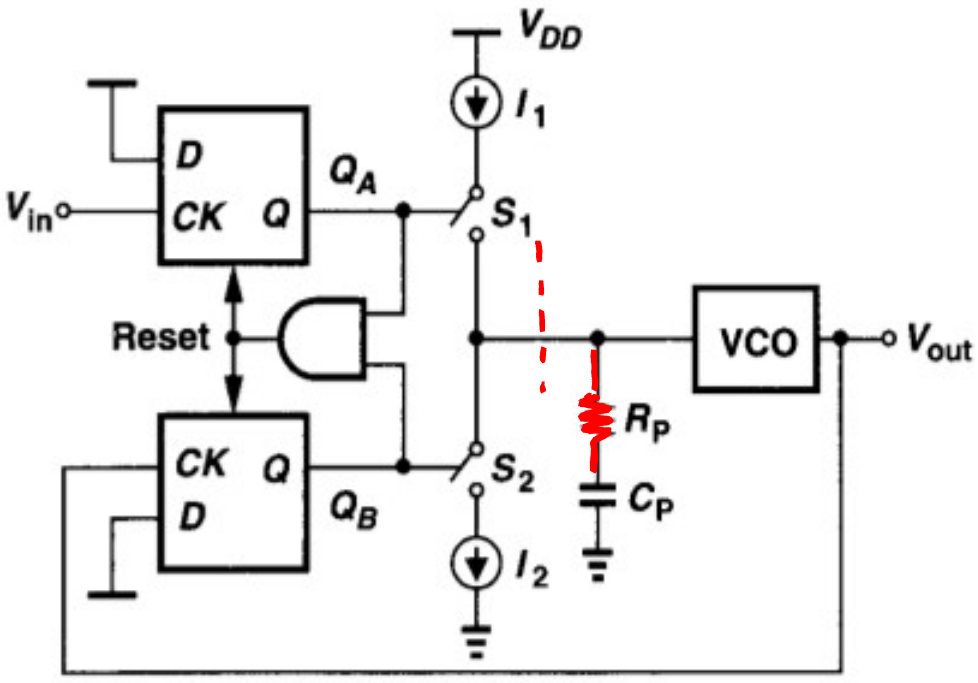
To Stabilize the Loop

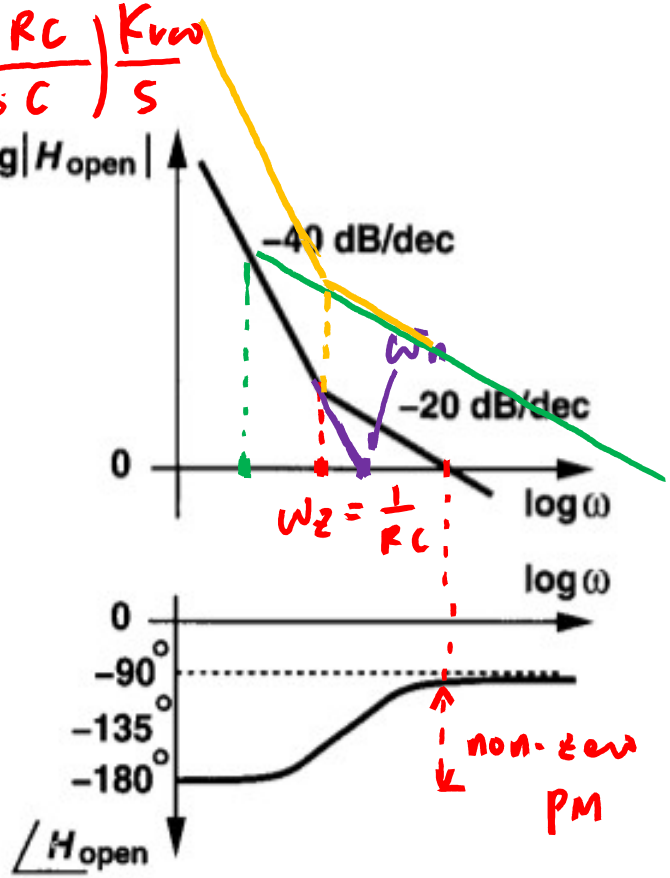
- **We need certain phase margin at ω_u**

→ A left-plane zero by inserting a resistor

→ The charge pump sees R in series with C

$$\frac{\Phi_{out}}{\Phi_{in}}(s)\Big|_{open} = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_P s}\right)\frac{K_{VCO}}{s} = \frac{I_P}{2\pi}\left(\frac{1+sRC}{sC}\right)\frac{K_{VCO}}{s}$$





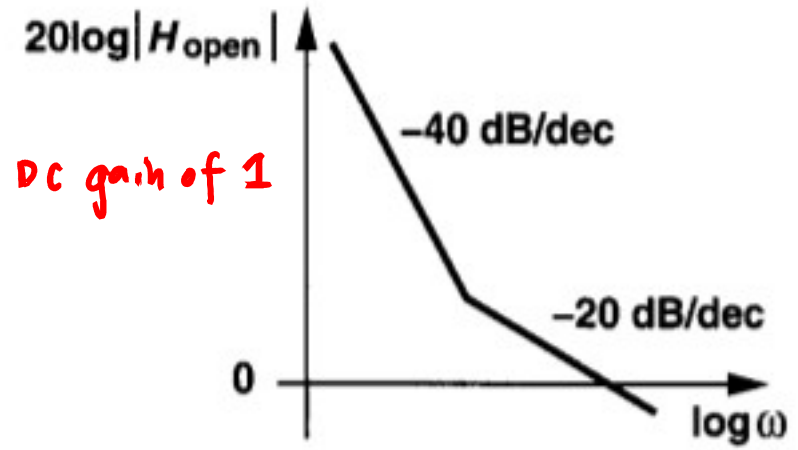
Loop Dynamics (II)

- **Closed-loop transfer function**

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_P s + \frac{I_P}{2\pi C_P} K_{VCO}}$$

DC gain of 1

$= \frac{\omega_{out}}{\omega_{in}}(s) = \frac{\phi_{out}}{\phi_{in}}(s)$



  - Low-frequency gain of unity

→ Output tracks the input phase well if input phase varies slowly

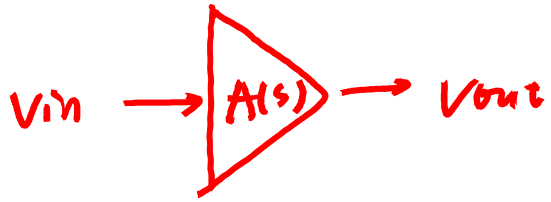
→ For input phase step, output phase eventually catches up

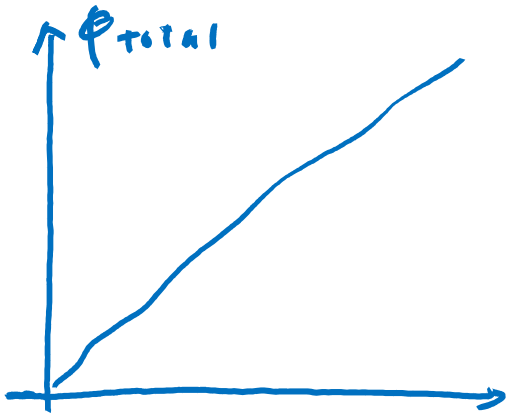
→ The same applies to frequency as well

- **Second-order system** $\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}}$ $\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} = \frac{RC}{2}\sqrt{\frac{I_{CP} K_{VCO}}{2\pi \cdot C_P}}$

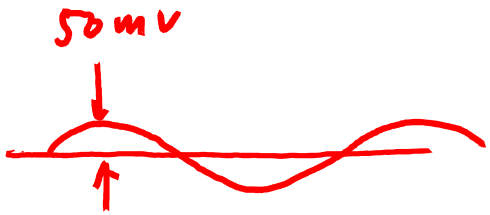
  - To stabilize the system by increasing the damping factor
  - To speed up the loop response (loop BW) 卡住 ζ 提高 ω_n (and ω_z)

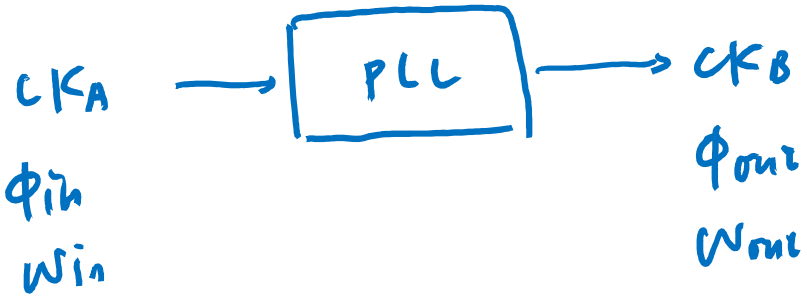
$= \frac{1}{2}\frac{\omega_n}{\omega_z}$





$$\frac{V_{out}}{V_{in}}(s) = A(s) = \frac{yyy}{s^2 + xxxs + yyy}$$

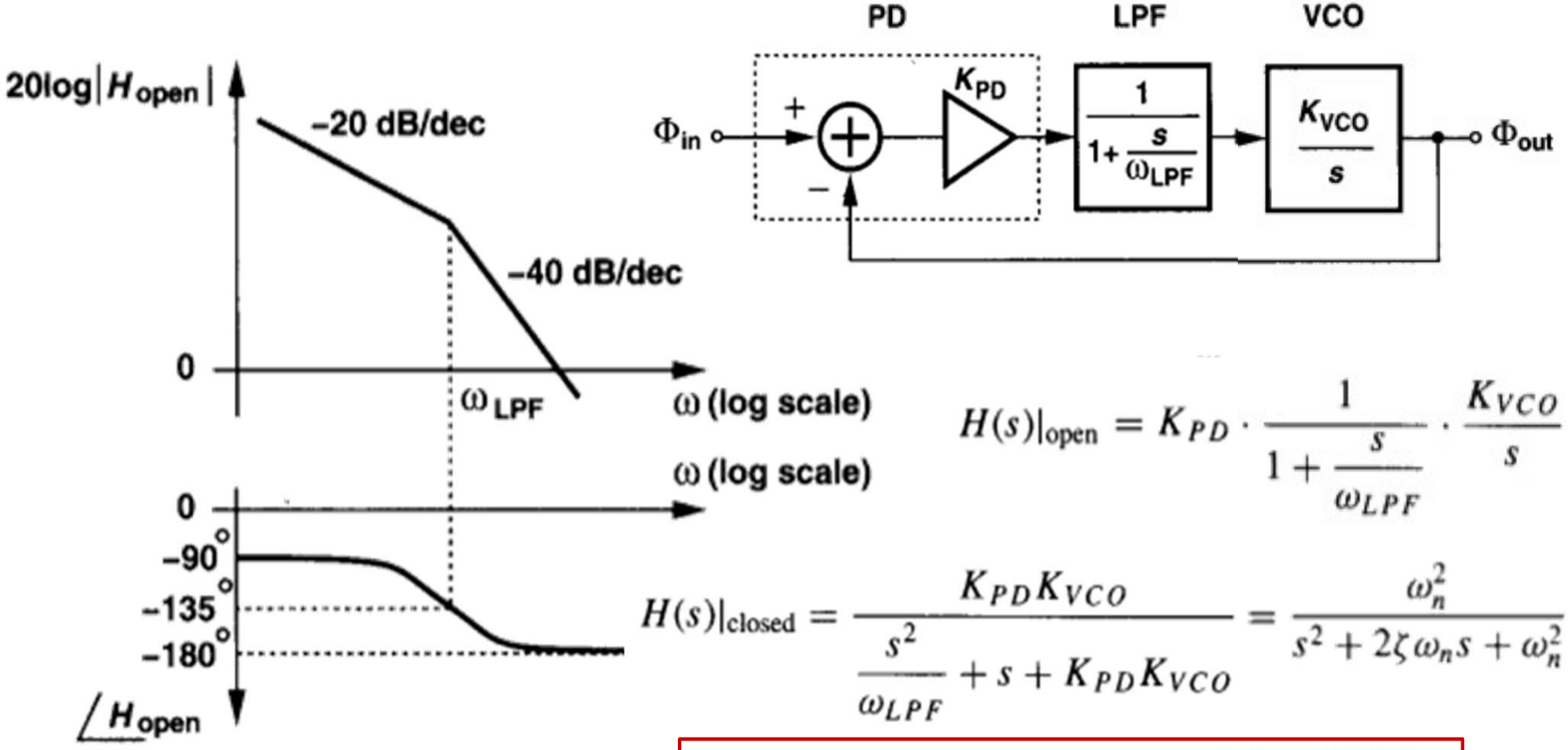




$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{yyy}{s^2 + xxxs + yyy}$$

Loop Dynamics of Basic PLL

- From Bode plot of open-loop transfer function



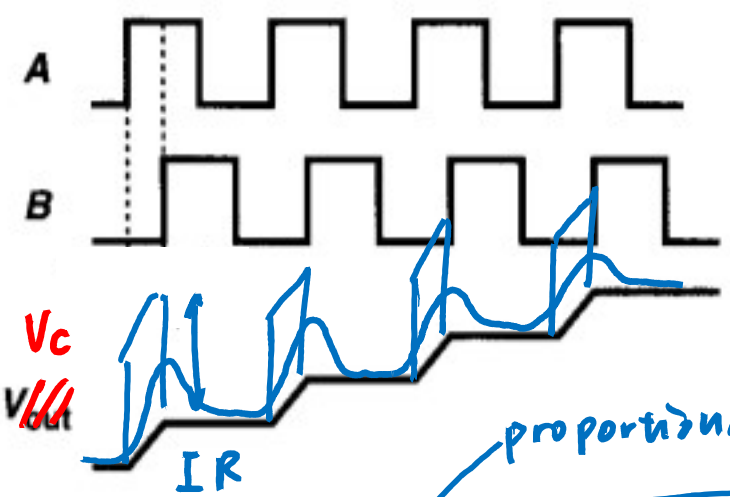
$$H(s)|_{open} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

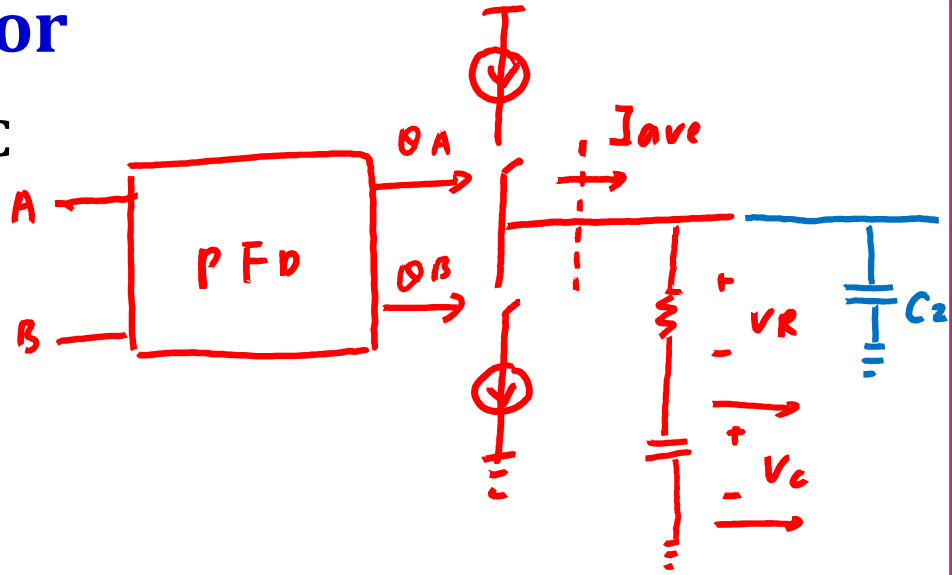
$$H(s)|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \qquad \zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.$$

The Third-Order Capacitor

- Transient in V_{ctrl} with series R+C





proportional control

integral control

$$Z_{LF} = \left(R + \frac{1}{sC_1}\right) \| \frac{1}{sC_2}$$

3-rd order capacitor

$$\frac{1}{R\frac{C_1C_2}{C_1+C_2}} \cong \frac{1}{RC_2}$$

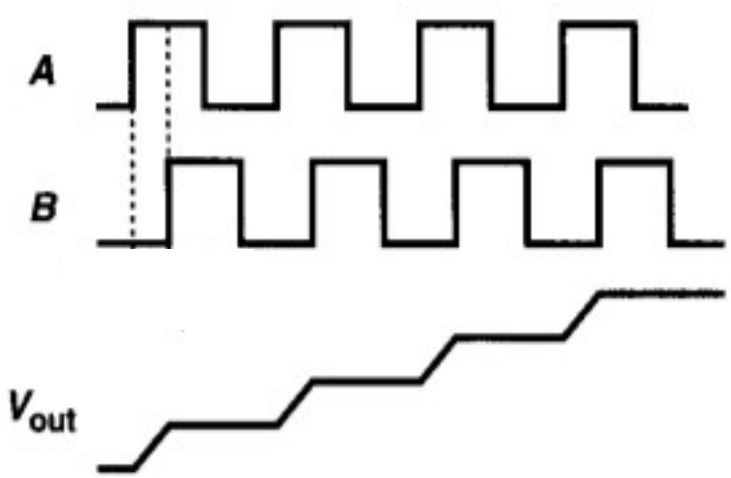
additional pole @

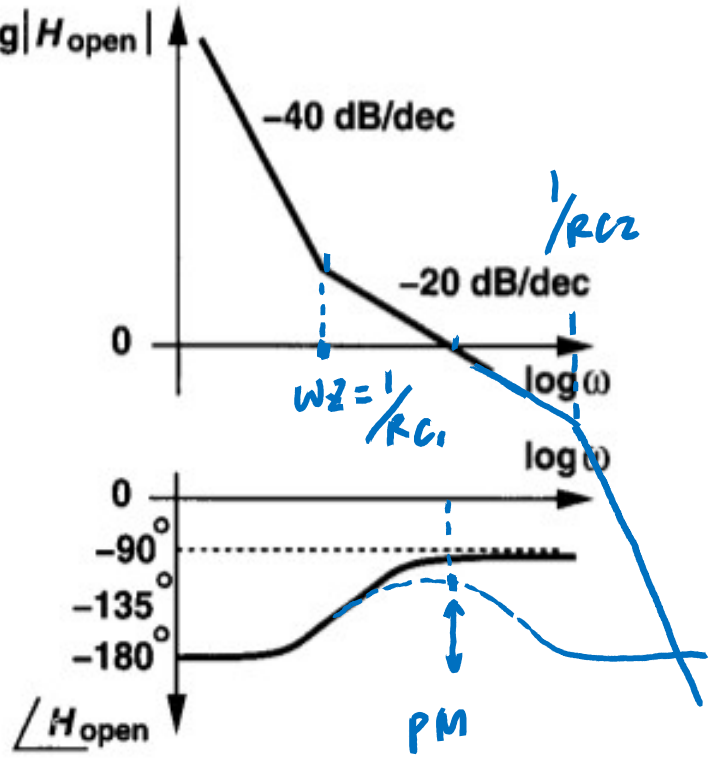
- Add a capacitor C_2 in parallel with R+C to smooth V_{ctrl}

$$H(s)|_{open} \cong \frac{I_{up}}{2\pi} \cdot \frac{K_{VCO}}{s} \cdot \frac{1+sRC_1}{sC_1} \cdot \frac{1}{1+sR\frac{C_1C_2}{C_1+C_2}}$$

The Third-Order Capacitor

- Transient in V_{ctrl} with series R+C





- Add a capacitor C_2 in parallel with R+C to smooth V_{ctrl}

$$H(s)|_{open}$$

Discrete-Time Nature of Phase-Locked Loops (I)

- **Continuous-time and linear approximation**
  - Yield reasonably accurate results when input frequency/phase varies slowly (compared to the reference frequency)
  - For example, with the operating frequency of 1 GHz and the input frequency varying with 1 MHz

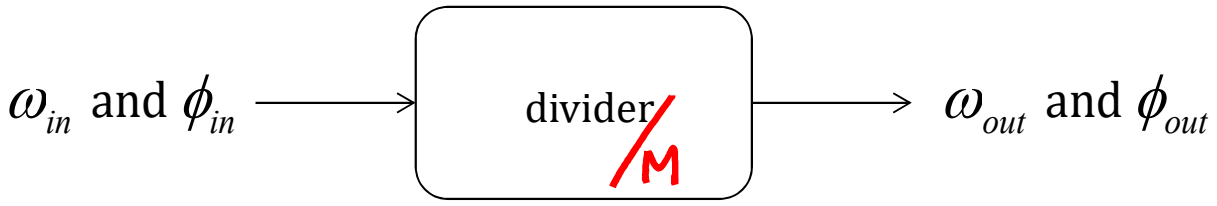
→ Very dense sampling → close to continuous-time operation

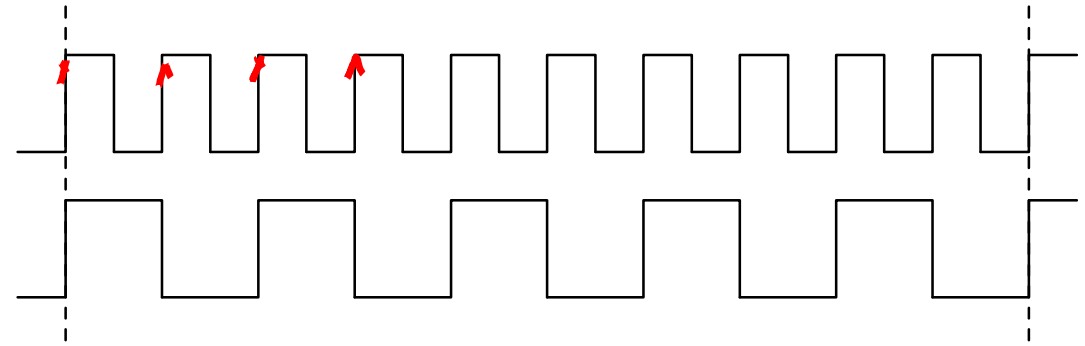
Discrete-Time Nature of Phase-Locked Loops (II)

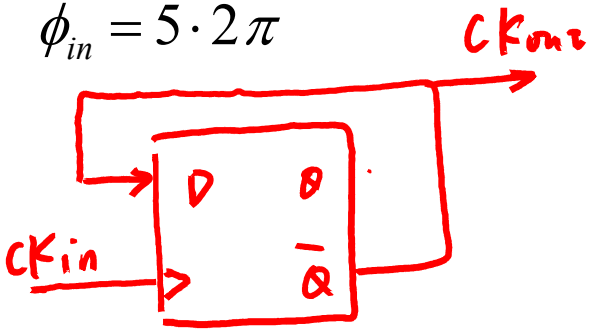
- **When the frequency (that the signal frequency/phase is varying at) becomes comparable to the reference frequency**
  - For example, if $\omega_m = 0.25\omega_{REF}$

- **Nonlinear operation**
- **Sampling delay results in additional phase shift → degrade stability**
- **Typically ω_n is kept to be 1/20~1/10 ω_{REF}**

Frequency Divider





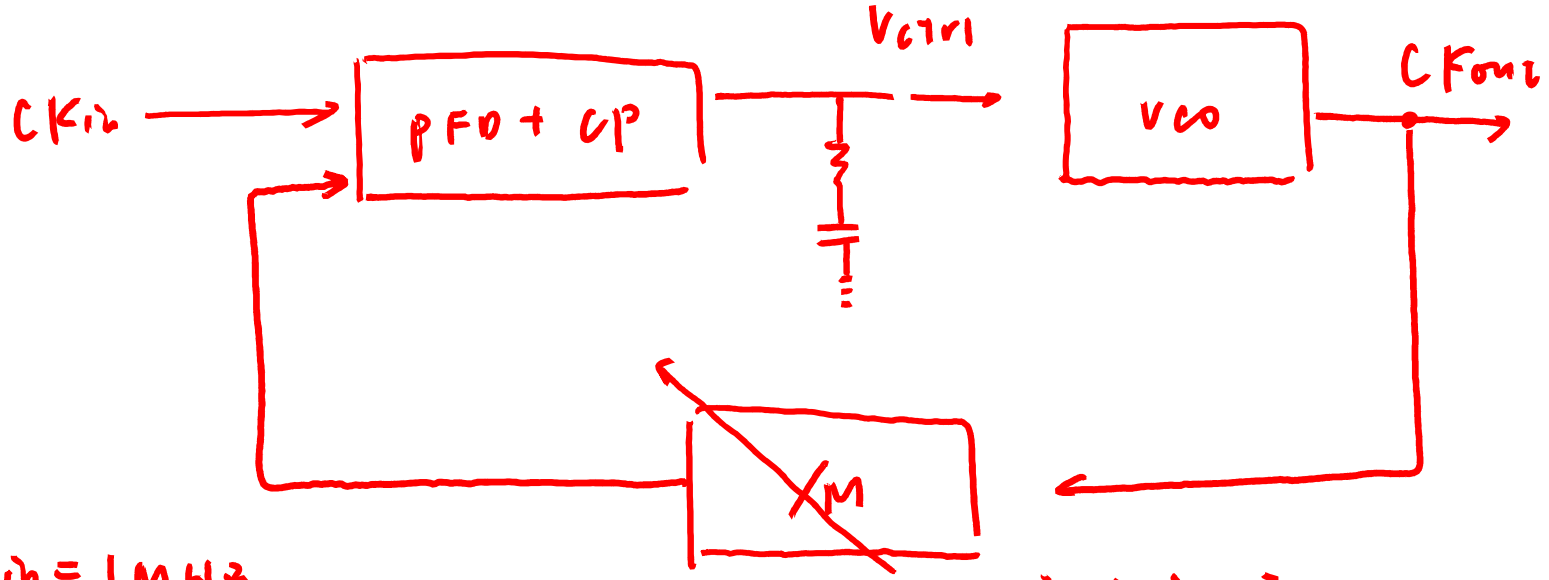


- Usually implemented using digital circuits
- Both frequency and phase are divided by N

With Frequency Divider in the Loop

- **Input frequency can be different from output frequency**

$$H_{loop}(s) = \frac{I_p}{2\pi}\left(R + \frac{1}{sC_1}\right)\frac{K_{VCO}}{s}\frac{1}{M}$$



$CK_{in} = 1\,MHz$

with $M = 1000 \rightarrow CK_{out} = 1\,GHz$

$M = 999 \rightarrow CK_{out} = 999\,MHz$

digital circuit with adjustable division ratio

output frequency can be adjusted with steps of f_{REF}

With Frequency Divider in the Loop

- **Input frequency can be different from output frequency**

- **The transfer function:**

$$\frac{\phi_{out}}{\phi_{in}} = \frac{\frac{I_{CP}}{2\pi}\left(R+\frac{1}{sC_P}\right)K_{VCO}}{1+\frac{I_{CP}}{2\pi}\left(R+\frac{1}{sC_P}\right)\frac{K_{VCO}}{M}} = \frac{\frac{I_{CP}K_{VCO}}{2\pi C_P}\left(1+sRC_P\right)}{s^2+\frac{I_{CP}K_{VCO}}{2\pi M}Rs+\frac{I_{CP}K_{VCO}}{2\pi C_P M}}$$

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi M C_P}} \text{ and } \zeta = \frac{R}{2}\sqrt{\frac{I_{CP}C_P K_{VCO}}{2\pi M}}$$

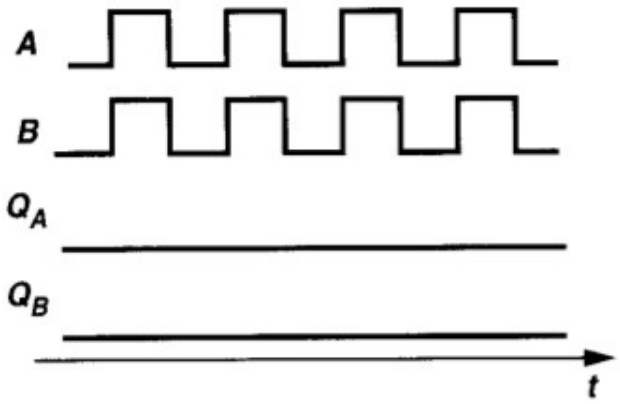
- **Can be used for frequency synthesis**

→ Frequency adjustment set by reference

Nonidealities in Phase-Locked Loops (I)

- **Design considerations of PFD+CP**

1) Reset pulse width: in case with no pulse or very narrow pulse



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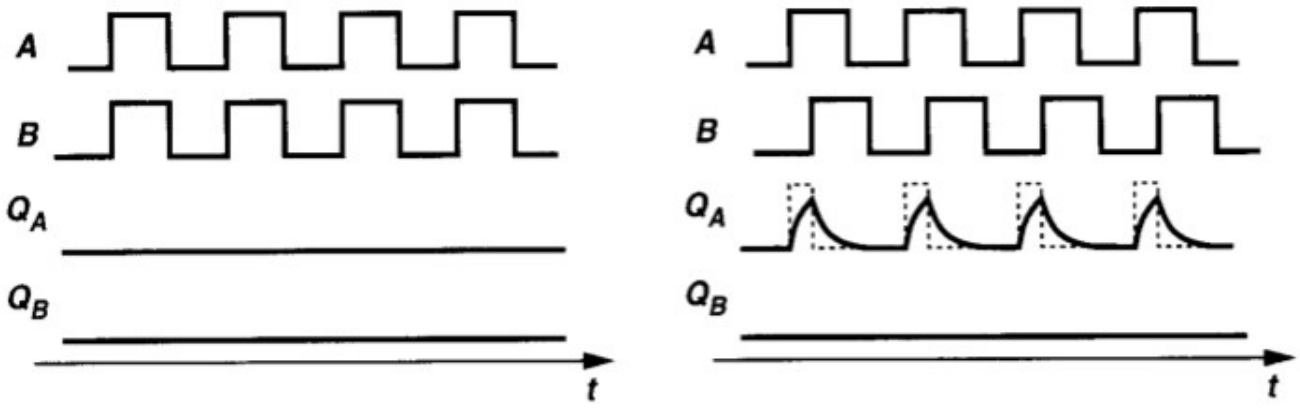
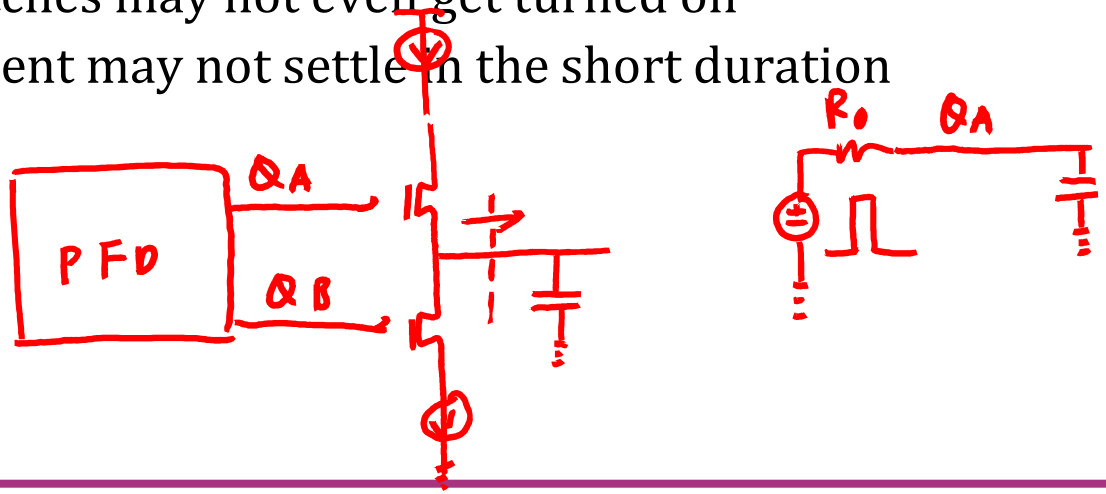


→ CP switches may not even get turned on

→ CP current may not settle in the short duration



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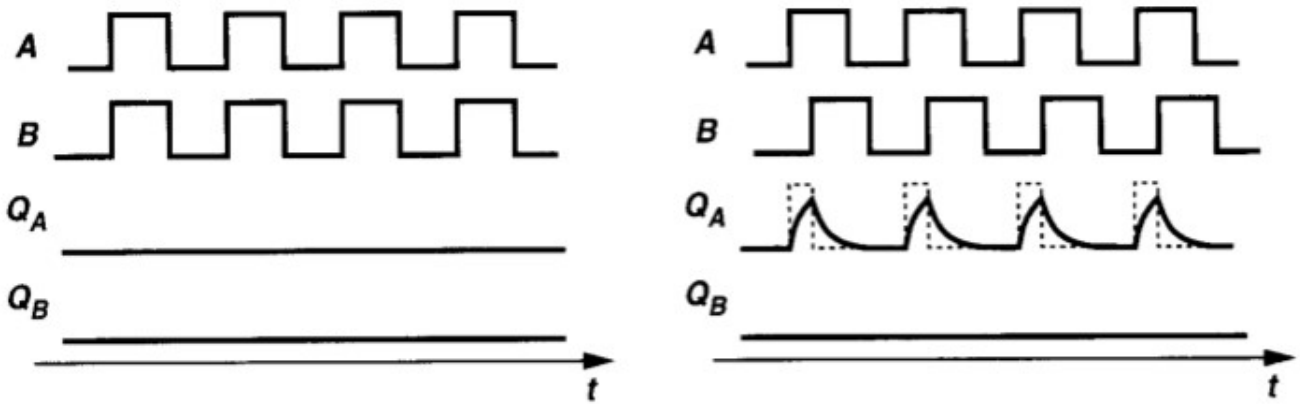
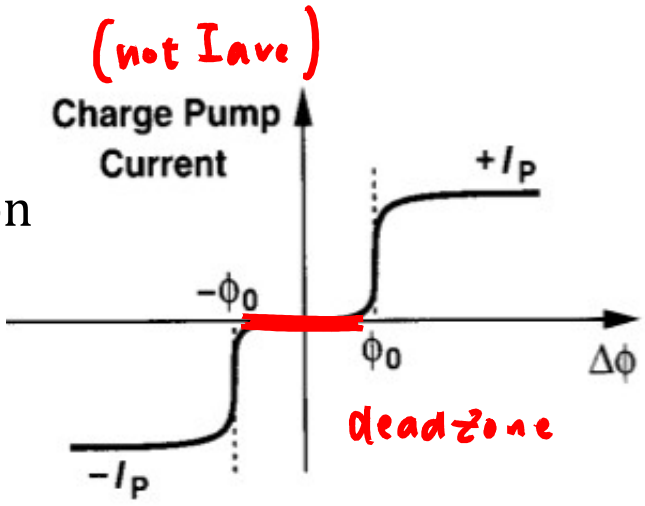


→ CP switches may not even get turned on

→ CP current may not settle in the short duration

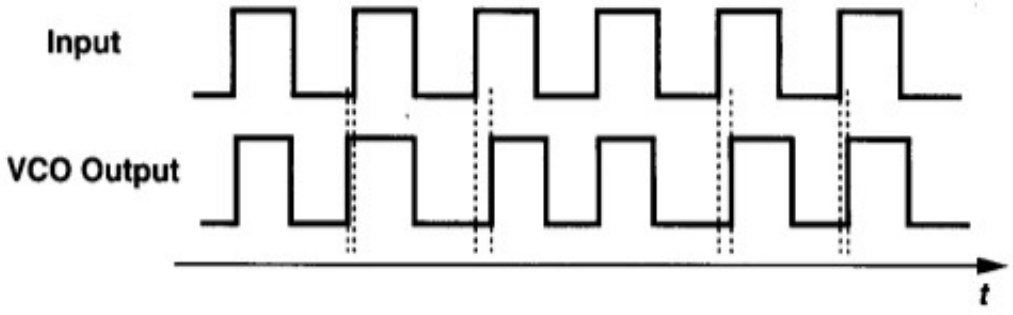
→ For very small phase error,
PFD+CP fail to produce proportional outputs



Nonidealities in Phase-Locked Loops (II)

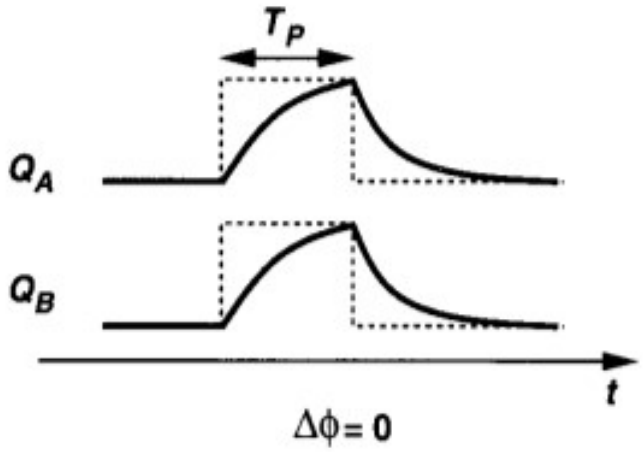
- **Effect of dead zone**

→ negative feedback is broken with small phase error



- **Sufficiently wide reset pulse allows PFD+CP to settle**

→ Ready for small phase error



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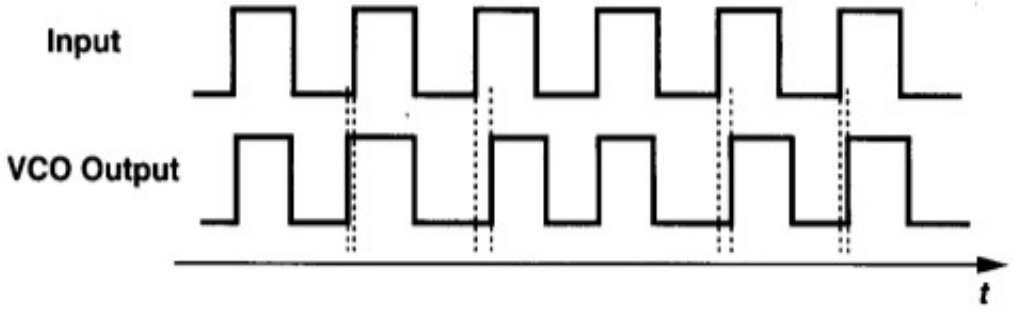

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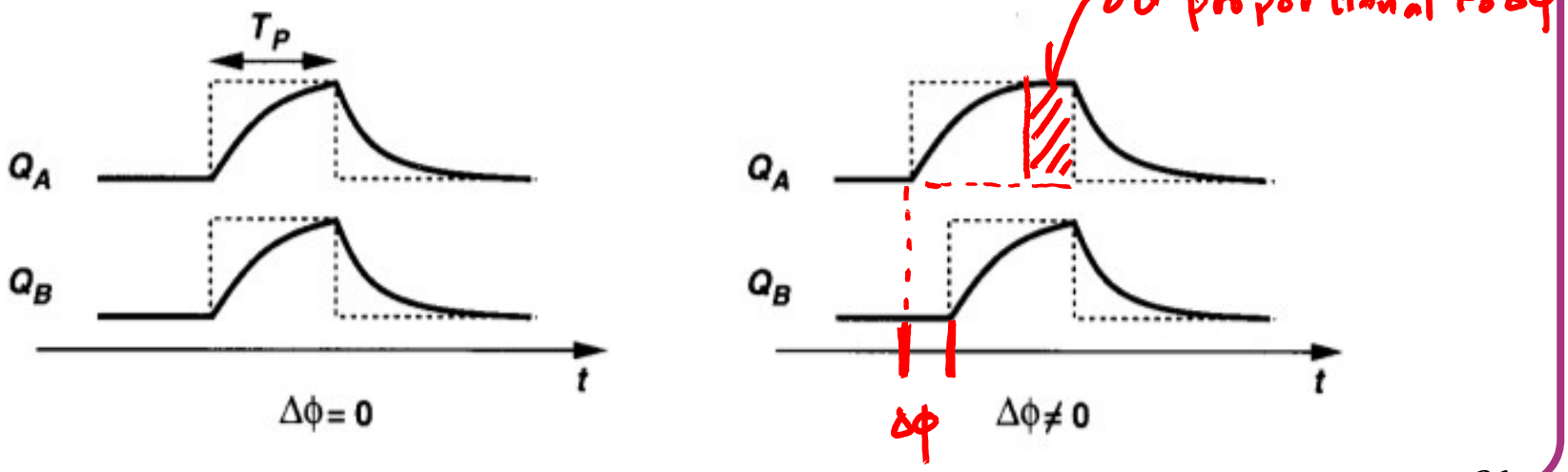
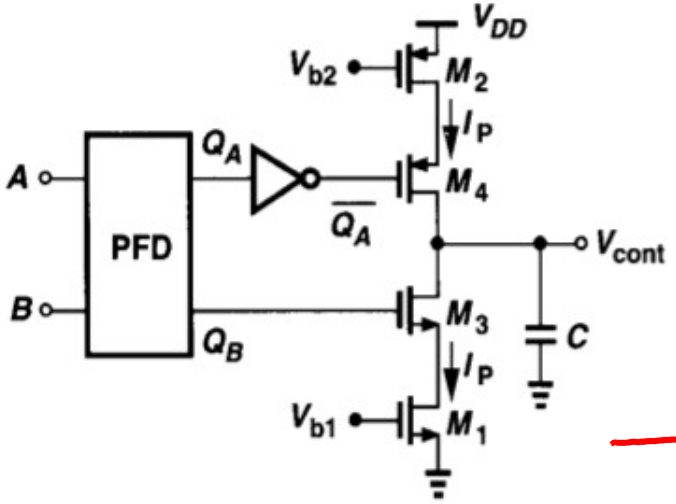


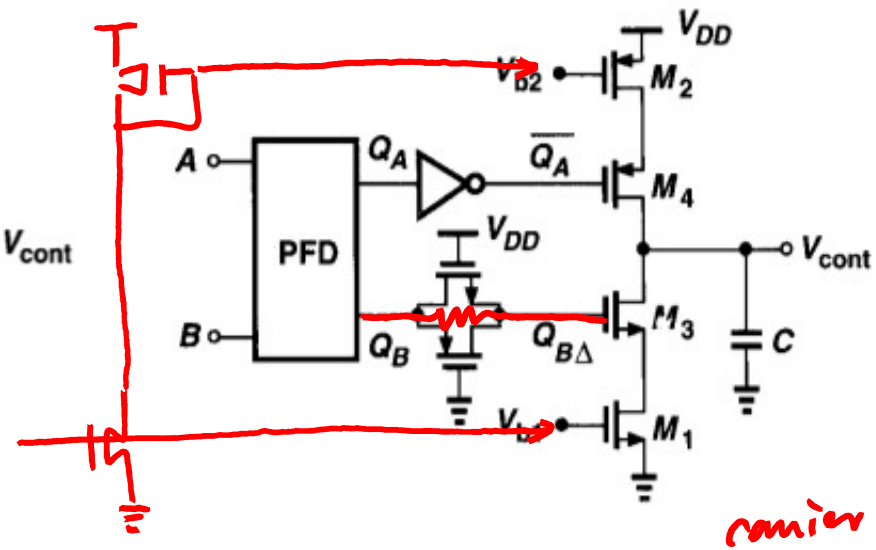
Nonidealities in Phase-Locked Loops (III)

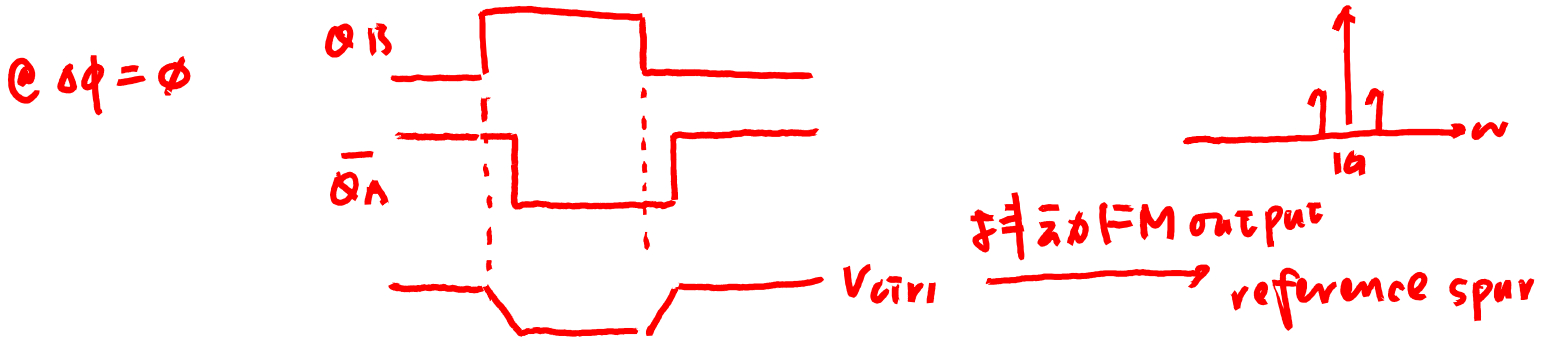
- **Design considerations of PFD+CP**

2) Skew in Q_A and Q_B pulses

- As the upper part of circuit is usually implemented using PMOS





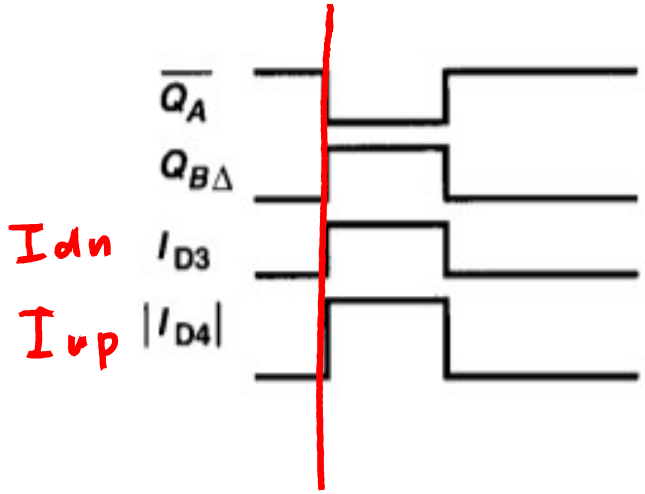


Nonidealities in Phase-Locked Loops (IV)

- **Design considerations of PFD+CP**

3) Mismatch between up and down currents

- Even with perfect pulse alignment, for example, if $I_{up}>I_{down}$



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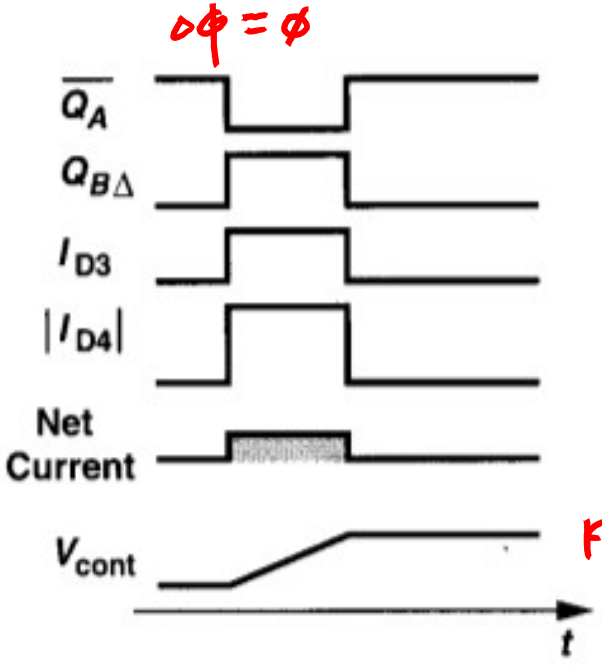

Loop dumping charge onto Cp even with zero phase error.

Nonidealities in Phase-Locked Loops (IV)

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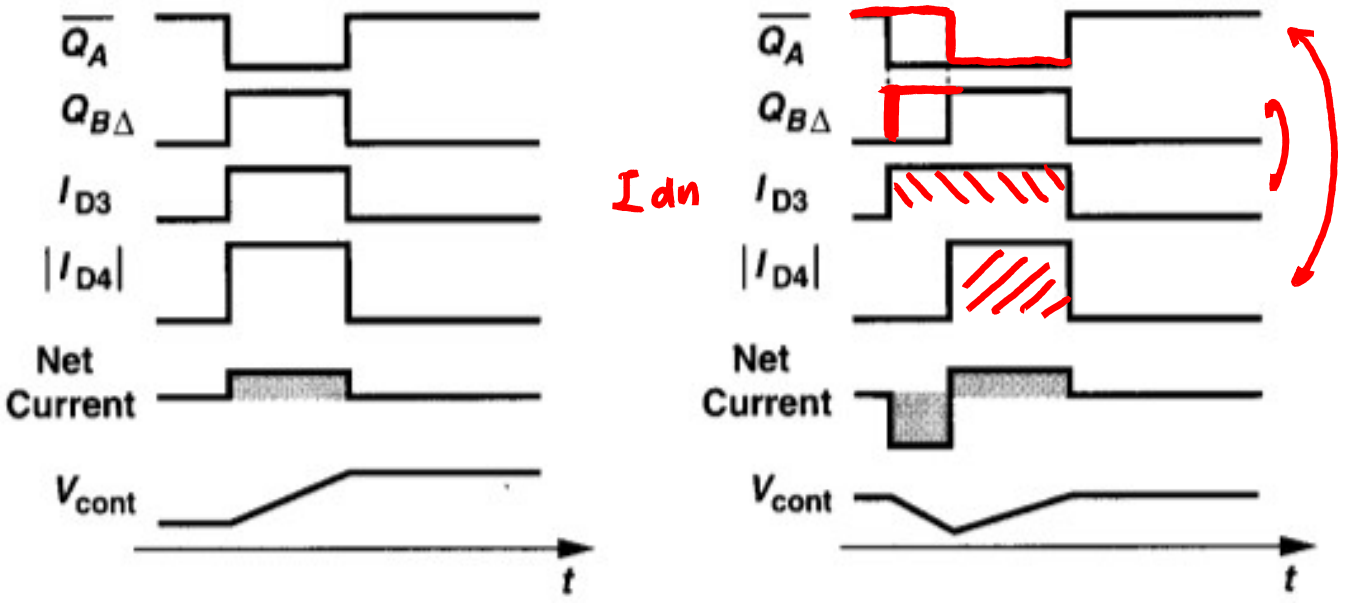
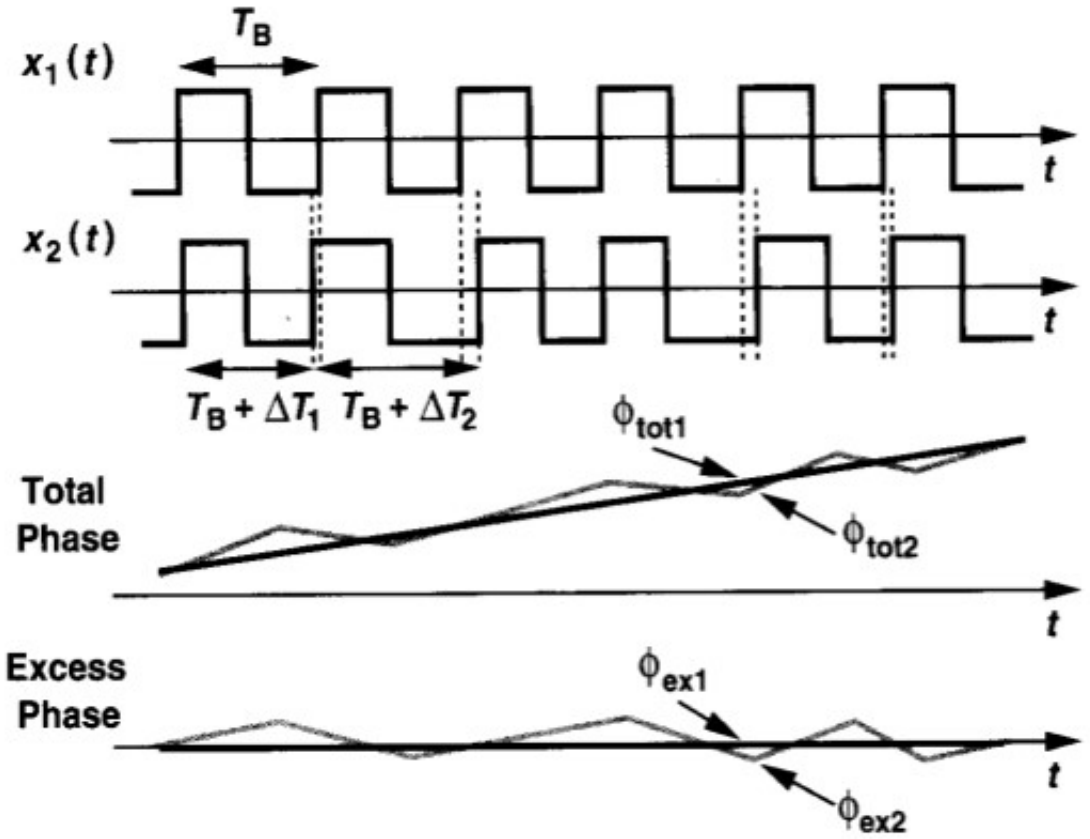


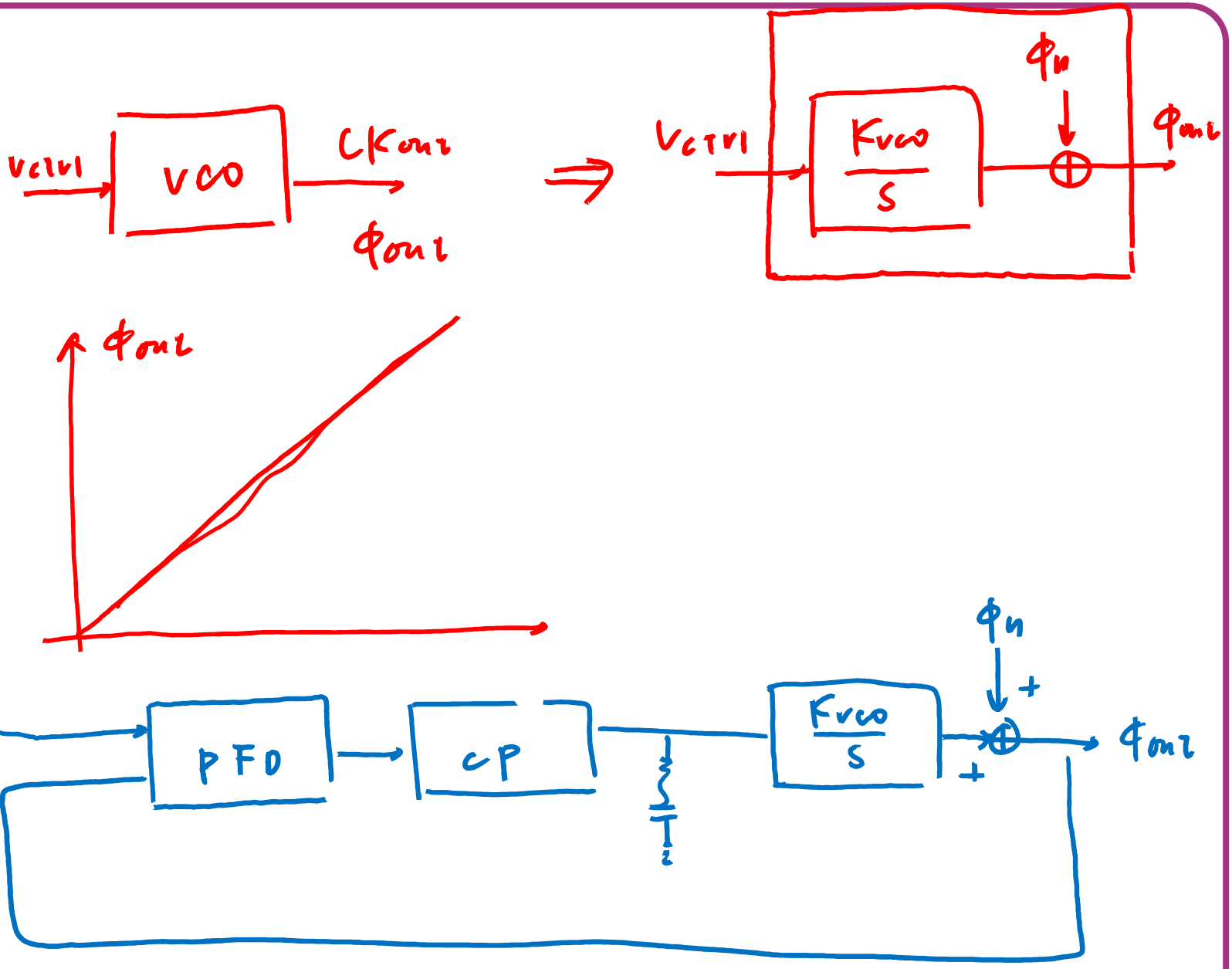
- Resulting in static phase error and V_{ctrl} ripple → reference spur
- Difficult to maintain perfect match between I_{up} and I_{down} due to r_o of transistors → worse for advanced technology

Phase Noise and Jitter in Phase-Locked Loops (I)

- **Total phase of a clean clock vs. a jittery clock**

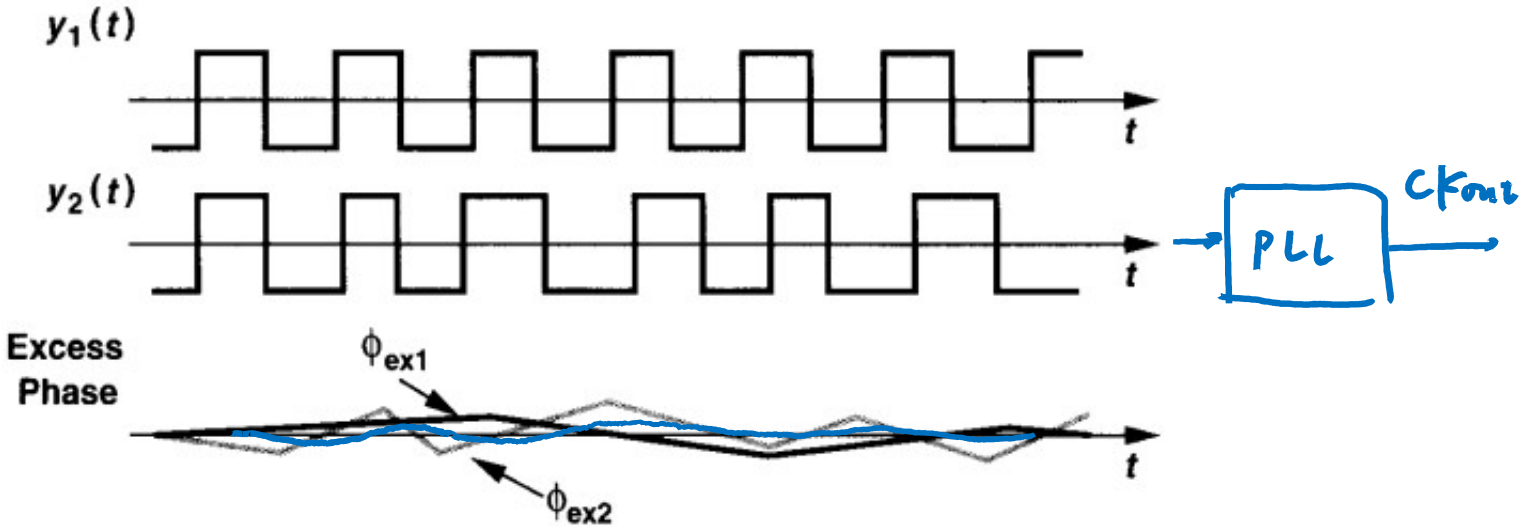


- **Different ways to characterize and quantify jitter**
  - Cycle jitter, cycle-to-cycle jitter, long-term or absolute jitter


VCTRL
VCO
CKout
φout
⇒
VCTRL
Kvco
s
φn
φout
φout
φin
PFD
CP
Kvco
s
φn
+
+
φout

Phase Noise and Jitter in Phase-Locked Loops (II)

- **The rate at which the phase varies**



- **Two sources of jitter that are of most interest**

  - Jitter of the reference input

$$\frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_P s + \frac{I_P}{2\pi C_P} K_{VCO}}$$

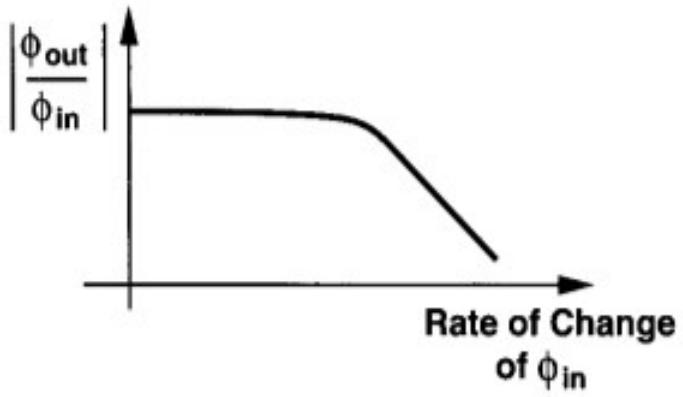
  - Jitter generated from the VCO

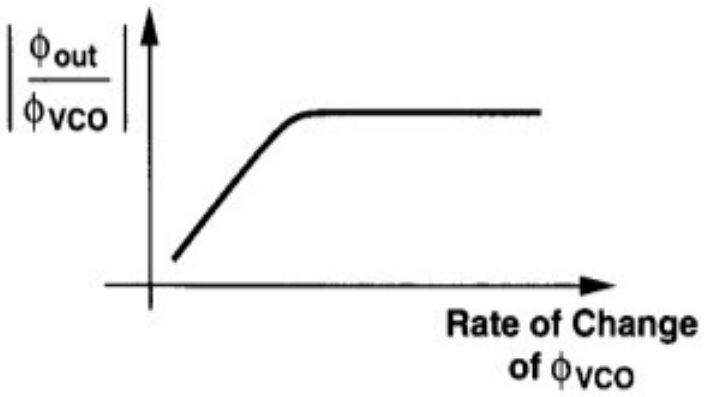
Phase Noise and Jitter in Phase-Locked Loops (III)

- **Jitter from VCO** $\frac{\Phi_{out}}{\Phi_{n,VCO}}(s) = \frac{1}{1 + H_{open}(s)}$

$$\frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_P s + \frac{I_P}{2\pi C_P} K_{VCO}}$$

$$\frac{\Phi_{out}}{\Phi_{VCO}}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$





- **Trade-off between noise contributions from different sources**