EE4280 Lecture 8:
Switched-Capacitor Circuits

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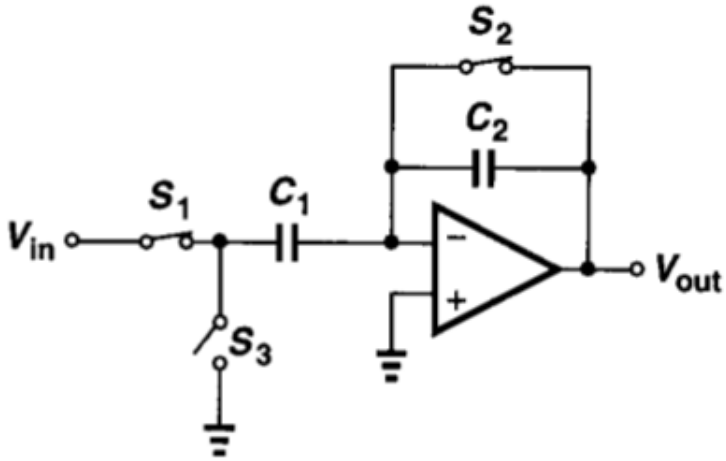
One Switched-Capacitor Circuit Example

- **Some capacitors**
- **Some switches**
  - Control signals needed
  - Typically 180° out-of-phase

→ Two-phase operation



- **An operational amplifier**
  - High voltage gain
  - Differential input
  - Single-ended output

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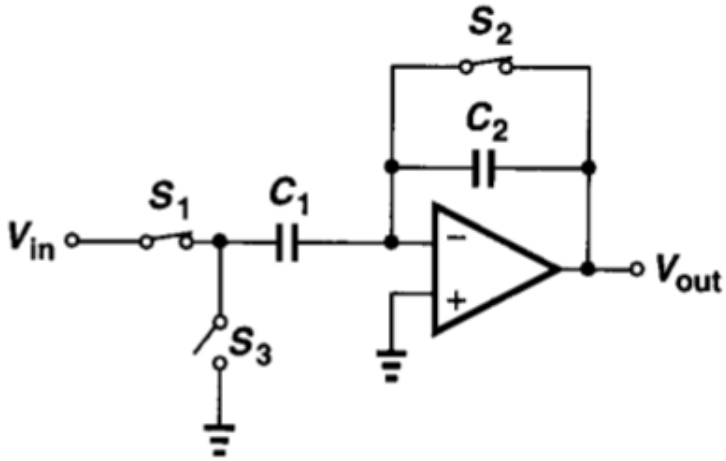

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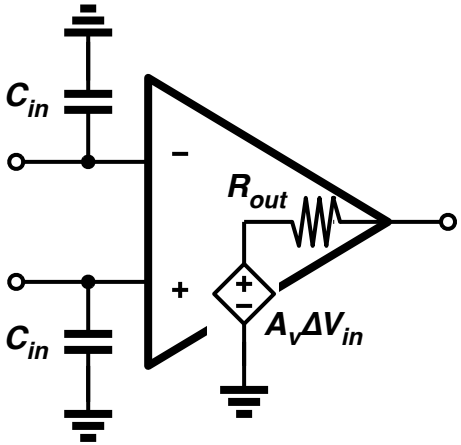
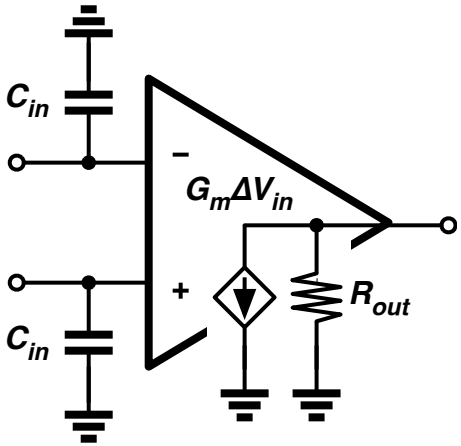
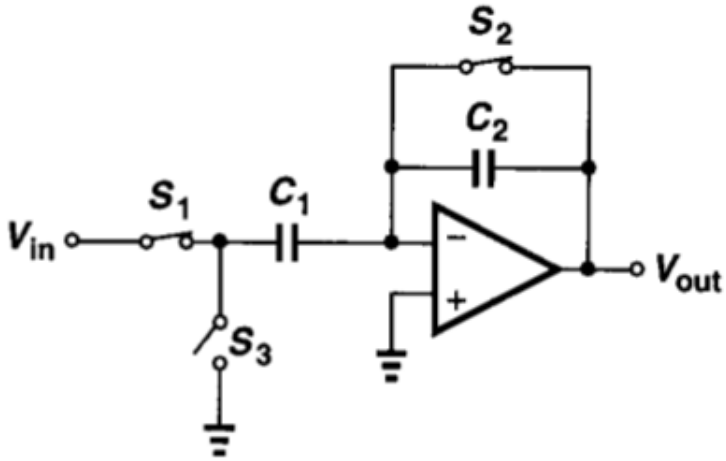




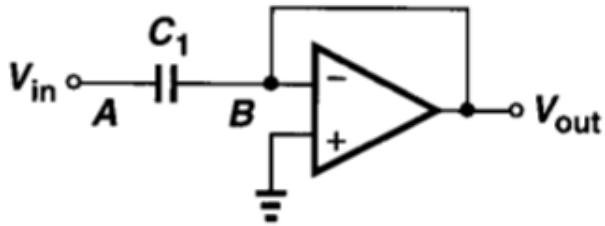
Operations – Phase #1

- S1 and S2 are ON



Operations – Phase #1

- **S1 and S2 are ON**
  - S2 provides a unity-gain feedback



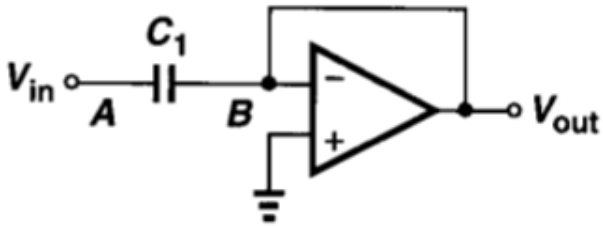
Operations – Phase #1

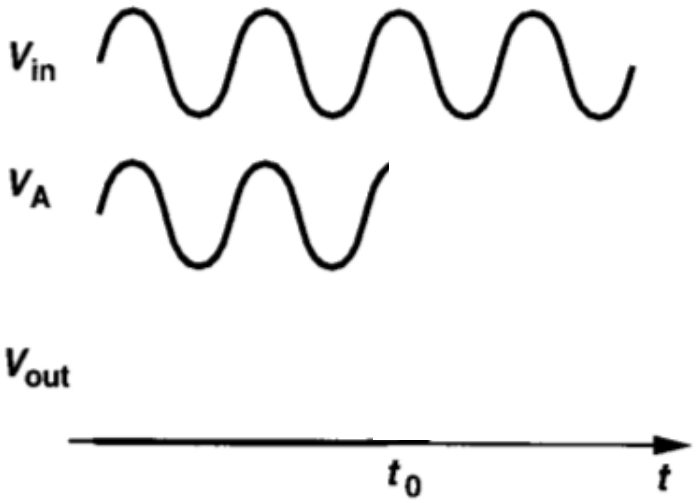
- **S1 and S2 are ON**
  - S2 provides a unity-gain feedback
  - The negative input port transient
  - Once reaching steady state
    - Virtual ground or virtual short
    - No current flowing into input
    - No voltage across C2

Operations – Phase #1

- **S1 and S2 are ON**
  - S1 connects C1 to Vin → sampling Vin across C1

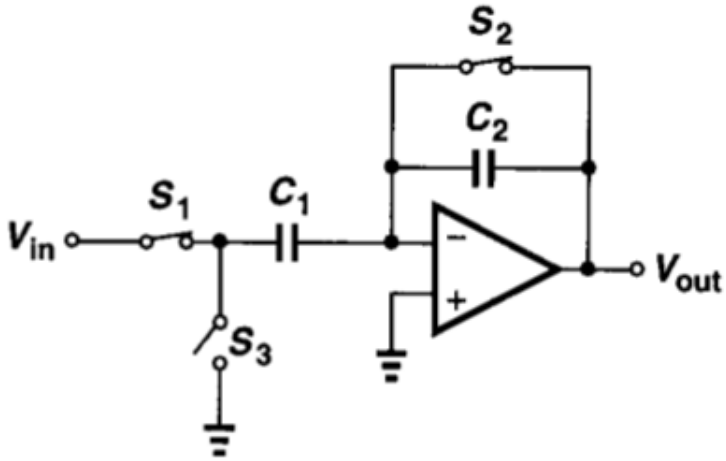
→ Sampling Phase





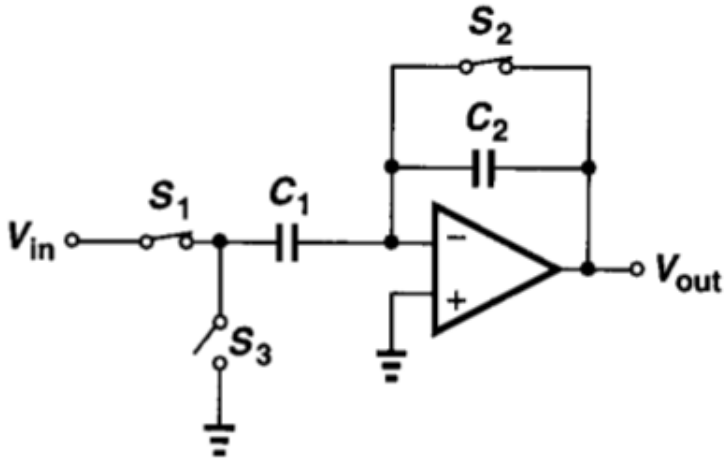
Operation – Phase #2

- S1 and S2 gets turned OFF
- S3 is then turned ON



Operation – Phase #2

- **S1 and S2 gets turned OFF**
  - Charges remain on capacitors
- **S3 is then turned ON**
  - Pull the left plate of C1 from Vin to ground

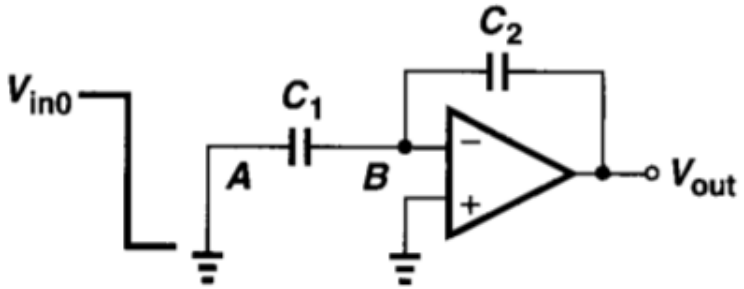


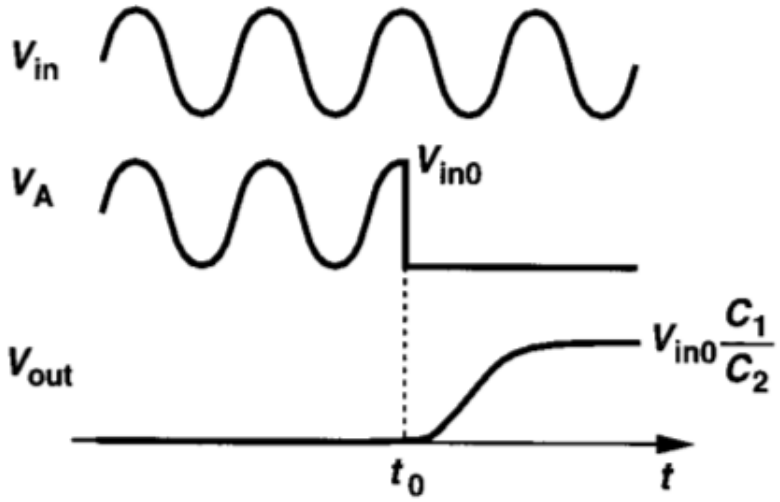
Operation – Phase #2

- **S1 and S2 gets turned OFF**
  - Charges remain on capacitors
- **S3 is then turned ON**
  - Pull the left plate of C1 from Vin to ground

→ Charge gets transferred

→ Amplification Phase

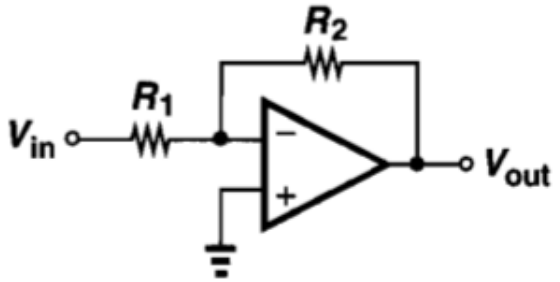




- **Non-inverting amplifier**
- **Sampling timing**
- **Stability considerations**

Continuous-Time Example

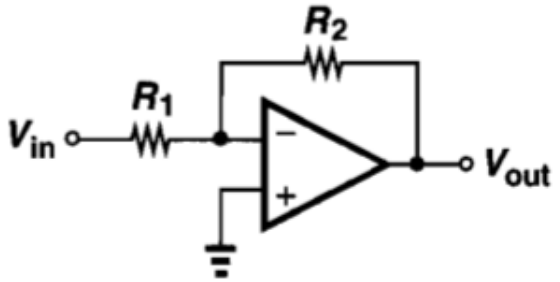
- **To amplify the input signal with resistive feedback**
  - Ideal voltage gain



Continuous-Time Example

- **To amplify the input signal with resistive feedback**
  - Ideal voltage gain

- **A few more details:**
  - Voltage sensing – current feedback
  - Loading effect on open-loop gain (when considering Rout of opamp)



Continuous-Time Example

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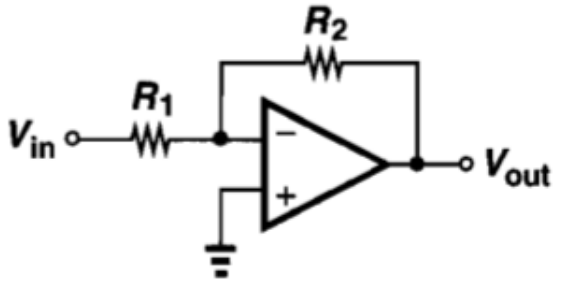
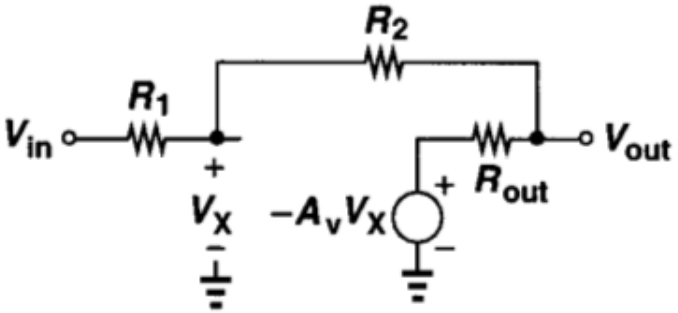


- **A few more details:**
  - Voltage sensing – current feedback
  - Loading effect on open-loop gain (when considering Rout of opamp)

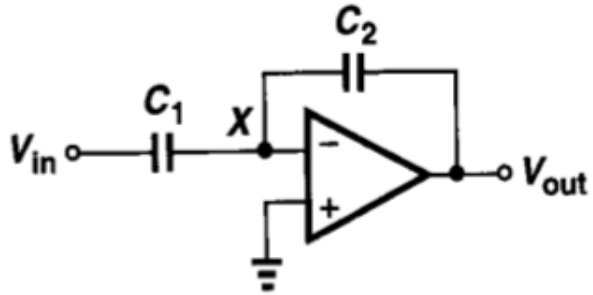
  - R2 flows current that comes from Rout

→ Degrading voltage gain from Vx to Vout



With Capacitive Feedback

- Loading effect can be avoid
- Need a mechanism to set the bias point of Vx

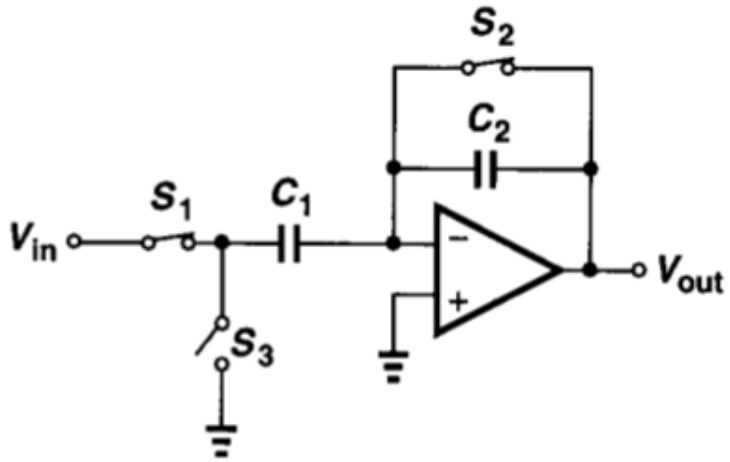


- Transfer function and Bode plot

- Accuracy

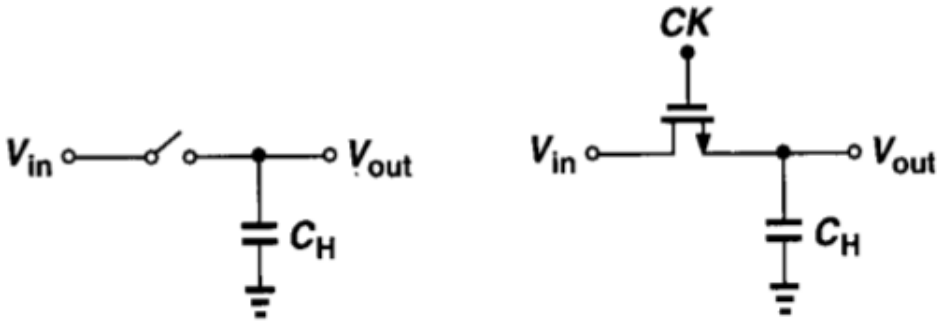
Switches

- **During the sampling phase**
  - Hoping VA to be exactly the same as Vin



Switches

- **During the sampling phase**

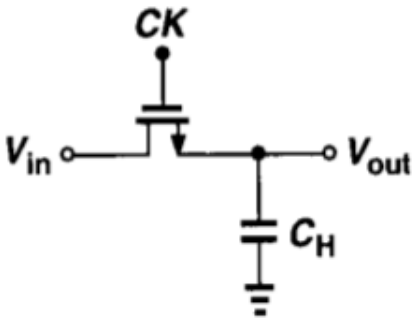


- With VCK of some high value, Vth of 0.3 V, and Vin of 0.3 V
- Once reaching steady state
  - Vout
  - The transistor current
  - The transistor operating in
- With VCK=0

Switches – A Few Cases (I)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

1. **Vin = 0 V while Vout = 1.0 V initially**

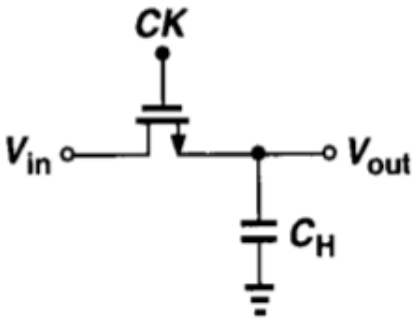


- Through the settling transient
  - The transistor current direction
  - The transistor operating region

Switches – A Few Cases (II)

- Vth of 0.3 V and VCK goes from 0 V to 1 V

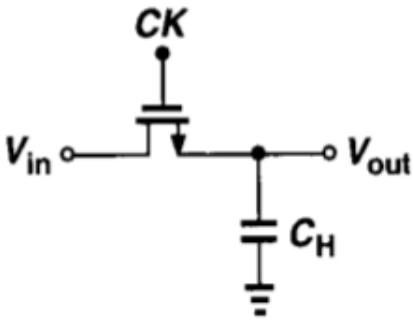
1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially



Switches – A Few Cases (III)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

1. **Vin = 0 V while Vout = 1.0 V initially**
2. **Vin = 0 V while Vout = 0.3 V initially**
3. **Vin = 0.3 V while Vout = 0 V initially**



- Through the settling transient
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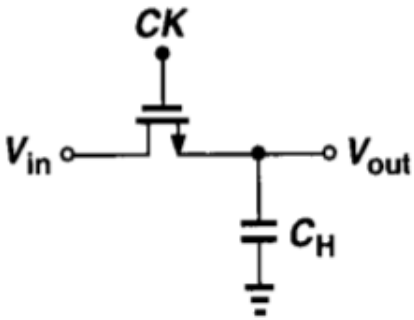
Switches – A Few Cases (IV)

- Vth of 0.3 V and VCK goes from 0 V to 1 V

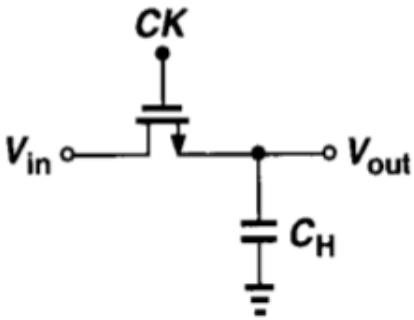
1. Vin = 0 V while Vout = 1.0 V initially
2. Vin = 0 V while Vout = 0.3 V initially
3. Vin = 0.3 V while Vout = 0 V initially
4. Vin = 1.0 V while Vout = 0 V initially



Switches – A Few Cases (IV)

- **Vth of 0.3 V and VCK goes from 0 V to 1 V**

4. Vin = 1.0 V while Vout = 0 V initially

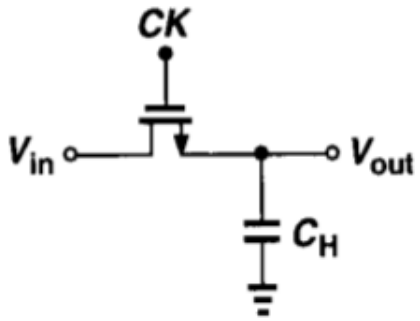


- Through the settling transient
  - The transistor current direction
  - The transistor operating region

On Resistance

- **Can be viewed as a resistor equal to**

$$R_{on} =$$

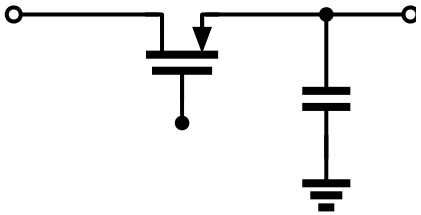


- On-resistance and speed depend on the input level

Using PMOS as Switch (I)

- VCK goes down to turn on the switch

1. Vin = 1.0 V while Vout = 0 V initially



Using PMOS as Switch (II)

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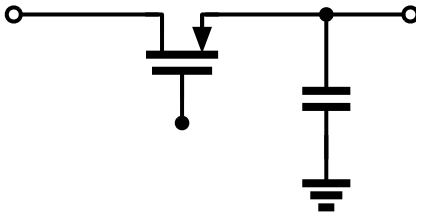
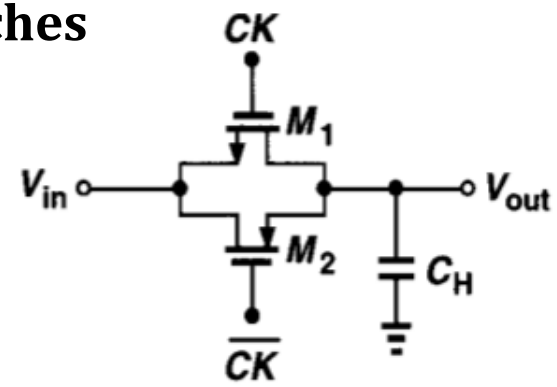


$R_{on,p}$ =

Pass Transistors

- **Transmission gates or Complementary switches**
  - Complementary clock signals needed

$$R_{on,eff} = R_{on,n} \parallel R_{on,p}$$



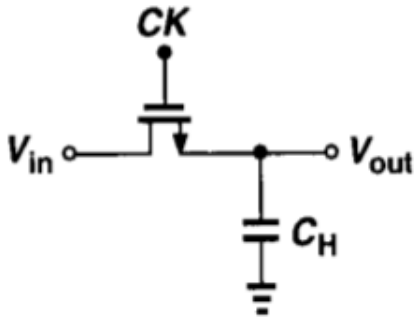
  - Can be sized so that the on-resistance is, to the first order, independent of the input level → Vthp and Vthn still vary due to body effect

Charge Injection

- **In order to reduce Ron and speed up the operation**

1) Rail-to-rail clock signals needed
2) Large transistors
3) Smaller holding capacitor

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$



- Charge in the channel when ON

Charge Injection

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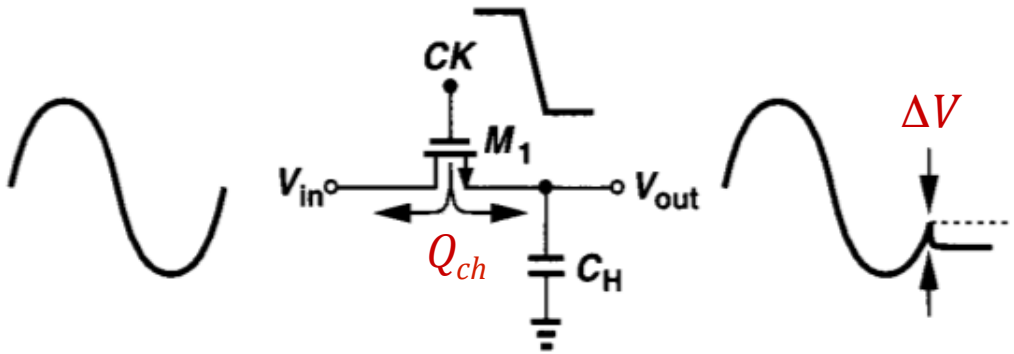

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}$$

- Charge in the channel when ON

→ Causing a pedestal at the output when turning OFF

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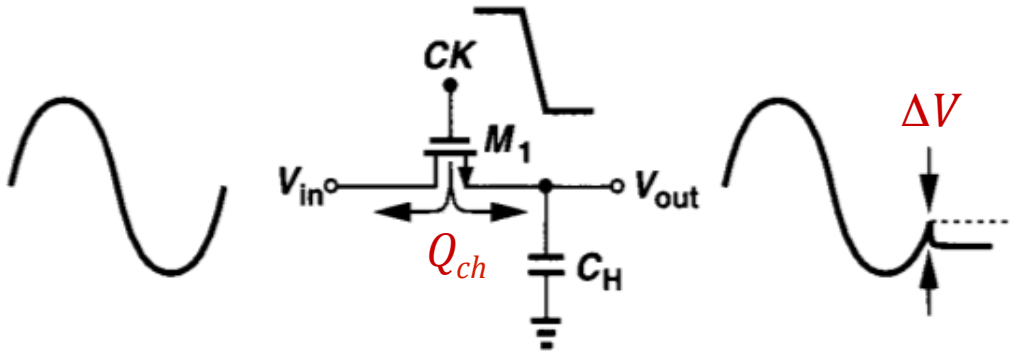

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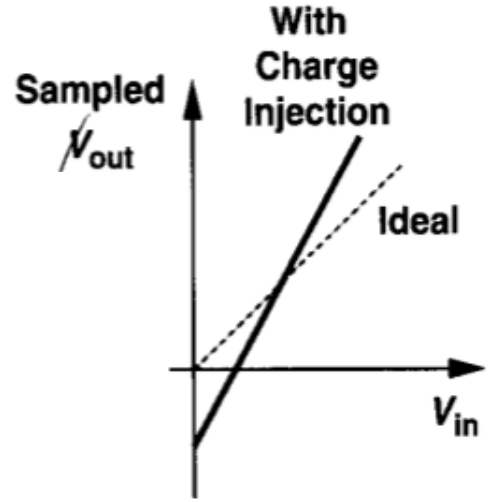
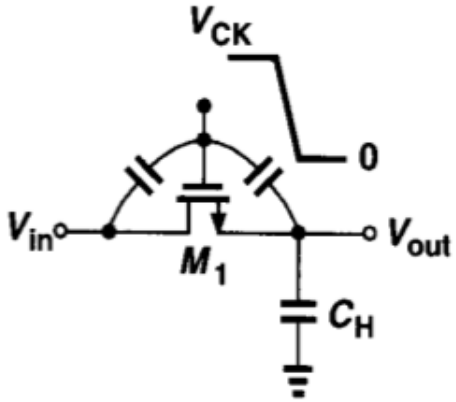


$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH})$$

→ Gain error and offset

Clock Feedthrough

- **Clock transitions get coupled to Vout through overlap capacitance**



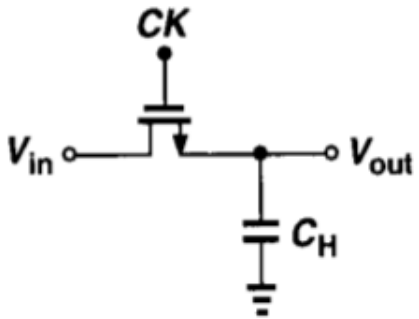
$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_H}$$

  - ΔV independent of Vin

- **Both charge injection and clock feedthrough trade-off with speed**

Charge Injection Cancellation (I)

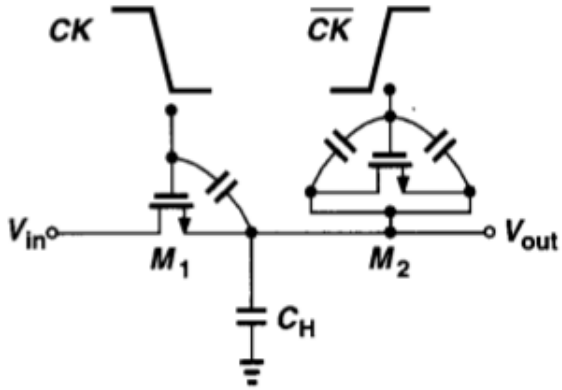
- **Dummy switch**
  - Injected charge can be removed by means of a second transistor



  - However, it is hard to know the fraction of charge going towards Vout

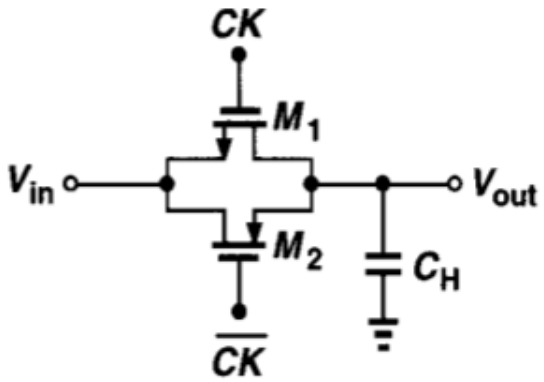
Dummy Switch on Clock Feedthrough

- **Also suppressed**



Charge Injection Cancellation (II)

- **Complementary switch**
  - Charges from NMOS cancel partially with charges from PMOS



  - Perfect cancellation for only one input level
  - Not perfect cancellation for clock feedthrough