EE4280 Lecture 6:
Phase-Locked Loops

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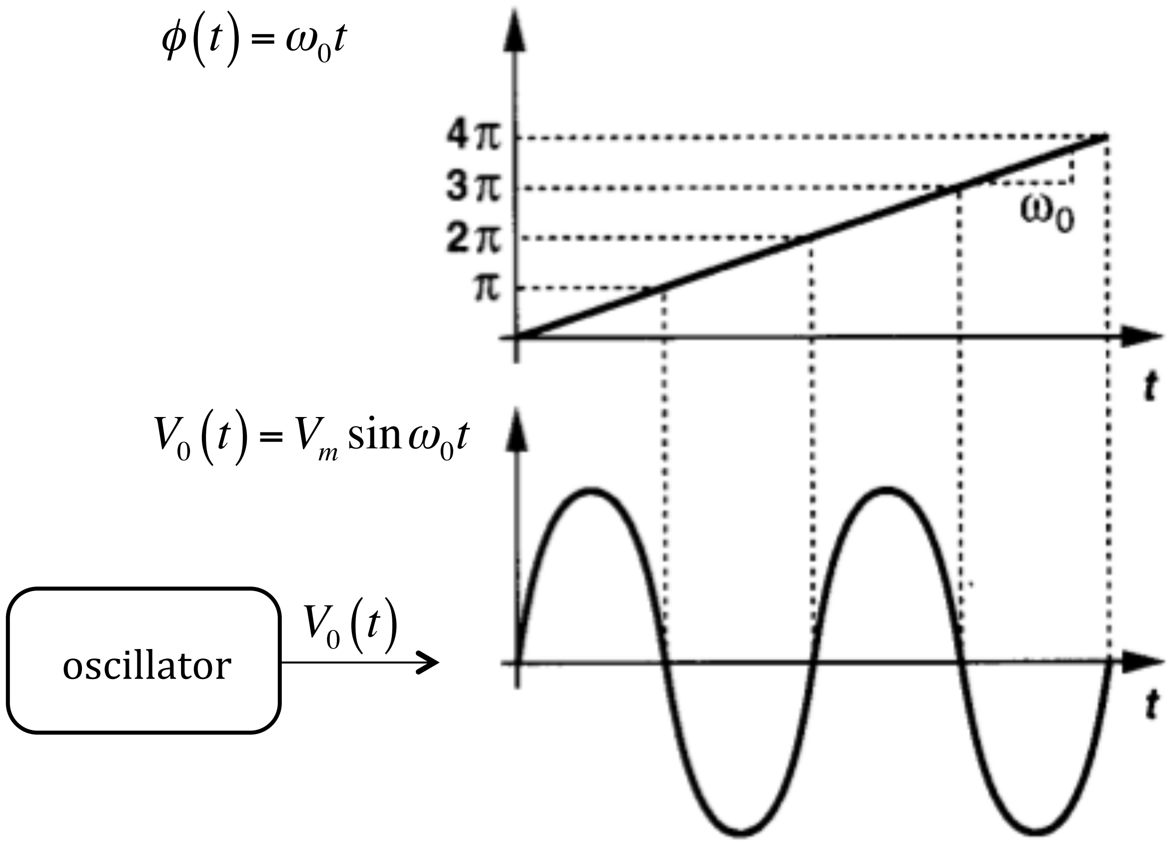
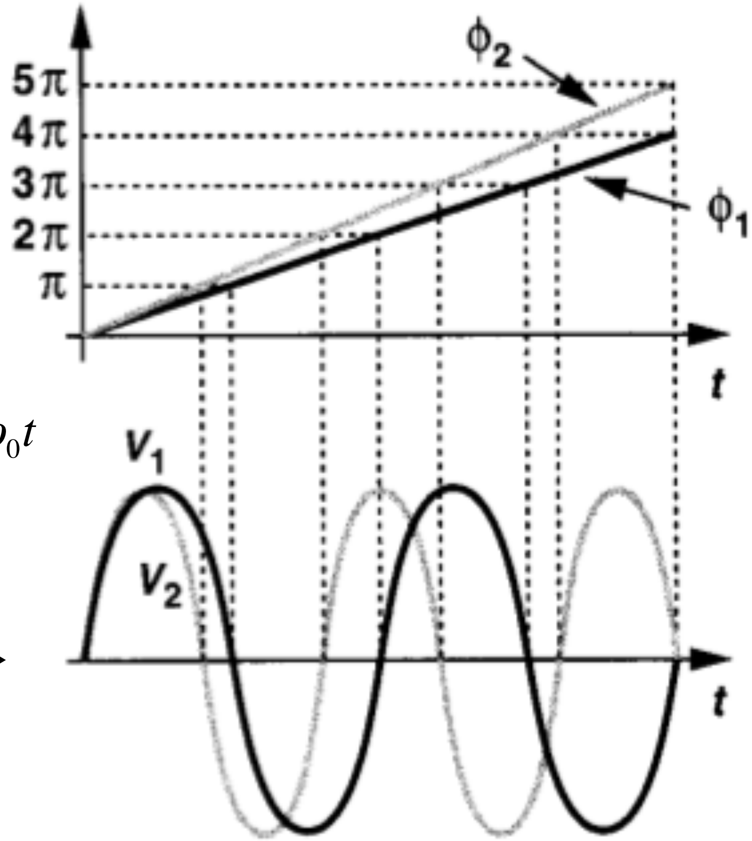
Mathematical Model of VCO



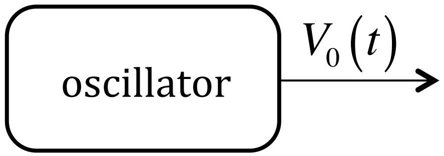
- **Oscillator's output phase is accumulated over time**

Mathematical Model of VCO

total phase $\phi(t) = \omega_0 t$



$V_0(t) = V_m \sin \omega_0 t$

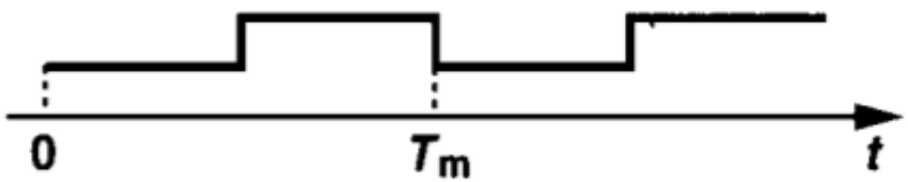


- **Oscillator's output phase is accumulated over time**
- **Faster frequency results in faster phase accumulation**

From V_{ctrl} to Output Frequency and Phase

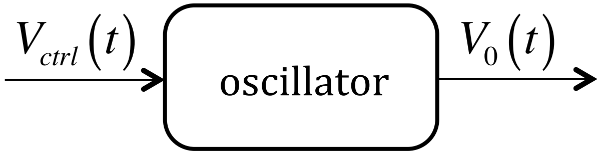
- **Usually a change in V_{ctrl} immediately results in a change in ω_{out}**

➔ Memoryless



- **If the frequency is a known function of time**

Excessive Phase and Transfer Function

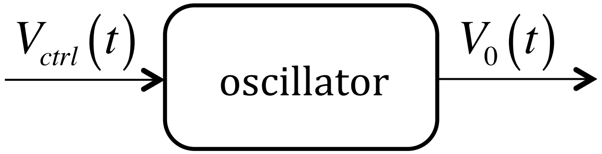


- **Often times, the excessive phase is of interest** $\phi_{ex}(t) = K_{VCO}\int V_{ctrl}(t)\,\mathrm{d}t$

➔ **Transfer function:**

Frequency Modulated Signal

- **With a small sinusoidal control voltage**

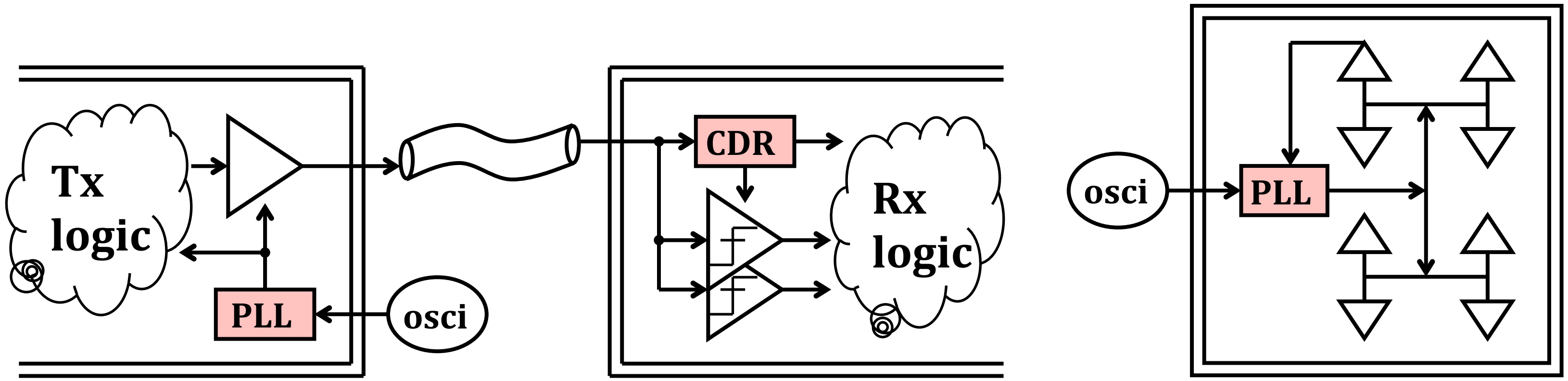


$$V_{cont} = V_m \cos \omega_m t \;\rightarrow\; V_{out}(t) = V_0 \cos\left(\omega_0 t + K_{VCO} \int V_{cont}\, dt\right)$$

- **Variation of V_{ctrl} causes unwanted components at output**

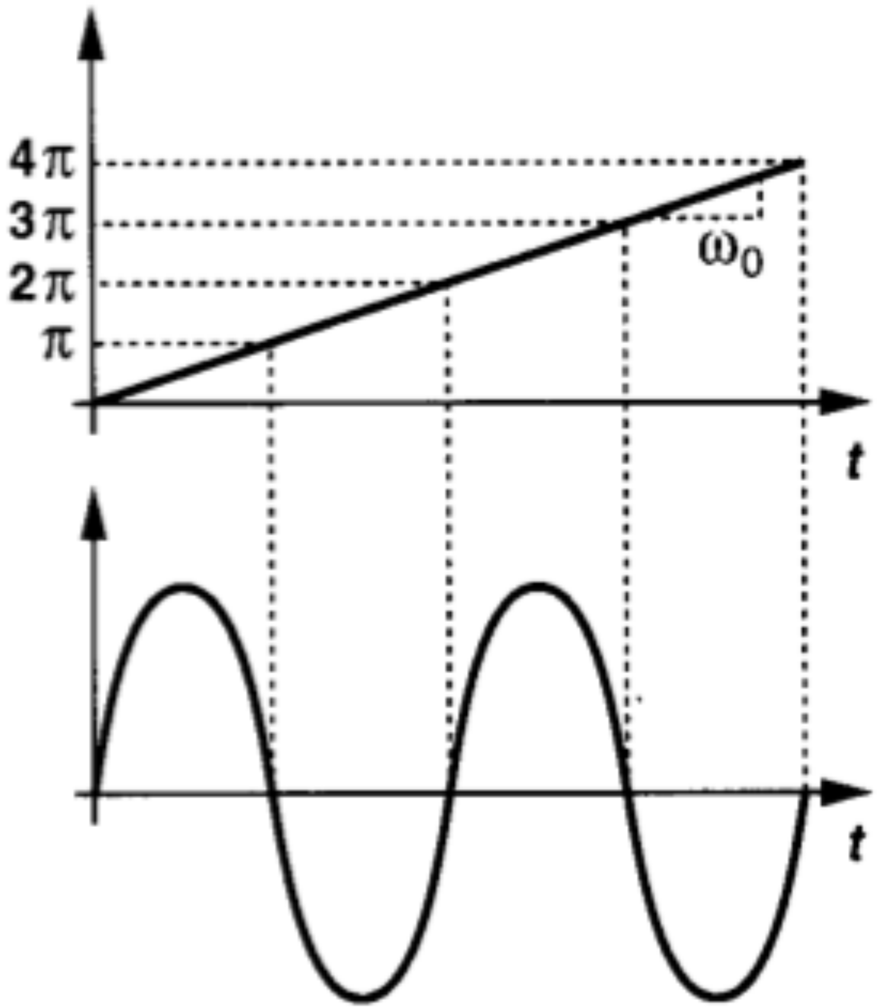
Phase-Locked Loops (I)

- **Phase-locked loops are used to generate a well-defined clock from a reference source**
- **Wide range of applications**
  - Clock generation and frequency synthesis
    - Generating a 10GHz clock from a 100MHz reference clock
    - Modulation/demodulation in wireless systems
  - Clock-and-data recovery
    - Extract clock frequency and optimum phase from incoming data stream
  - Skew cancellation
    - Phase aligning an internal clock to an I/O clock

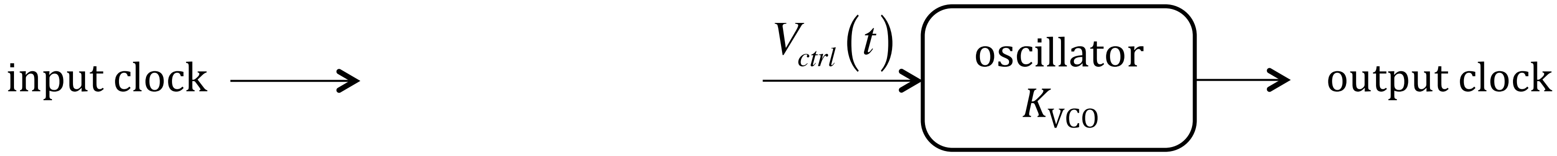


Phase-Locked Loops (II)

- A negative feedback system that compares and adjusts the output phase with the input phase



In Order to Achieve Phase Lock

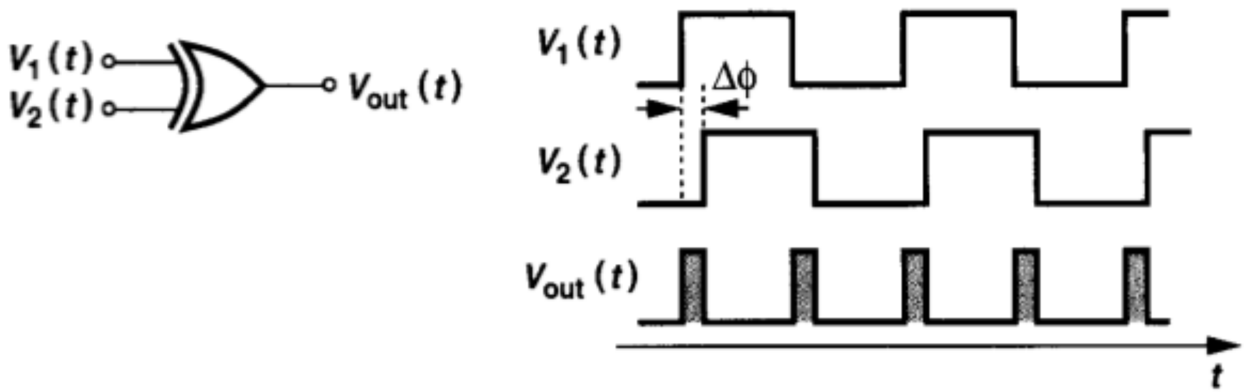


- **Need to measure the phase difference between the two clocks**

➔ **Phase detector**
A circuit whose average output is linearly proportional to the phase difference between the two inputs

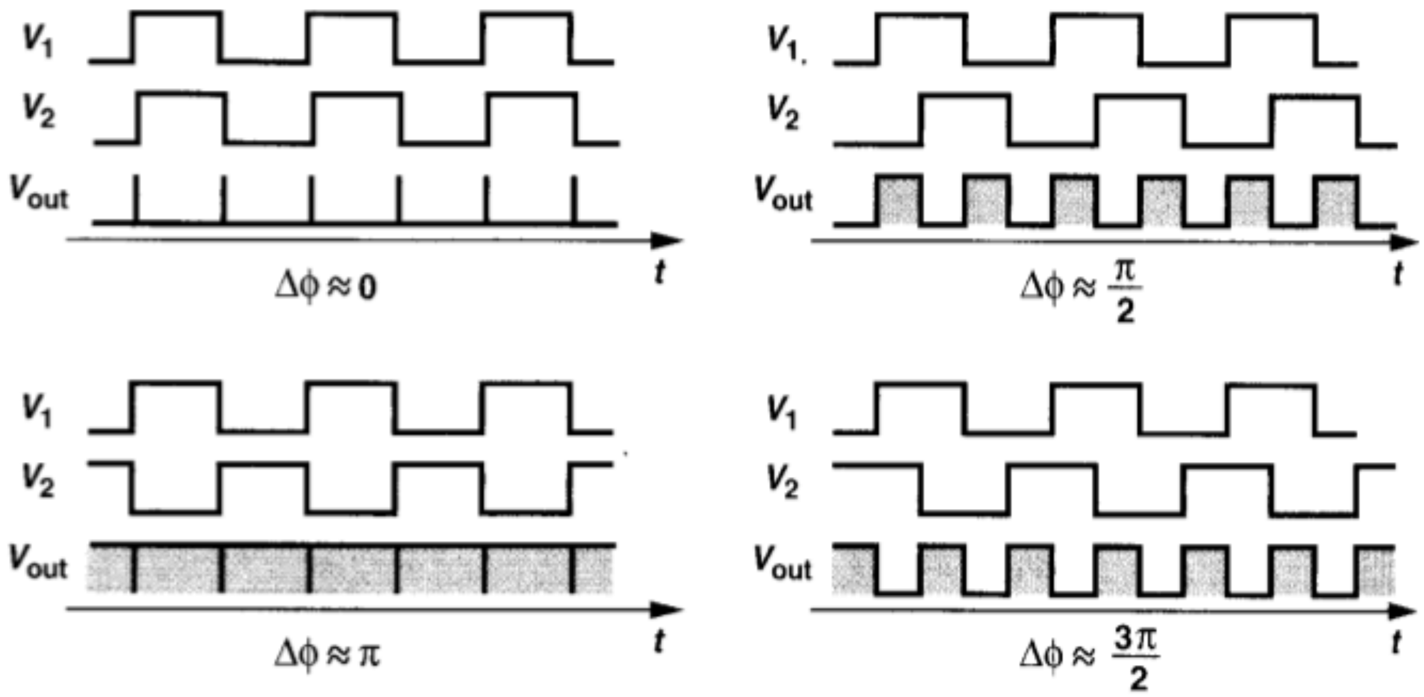
➔ **We must vary the frequency to adjust the phase through integration**

Phase Detector Example – XOR Gate (I)



- Respond to both (rising and falling) edges
- As the phase difference keeps increasing …

Phase Detector Example – XOR Gate (II)



- **The phase detector gain K_{PD} of**

Basic PLL Topology

- **A low-pass filter is used after the phase detector to extract the average PD output**

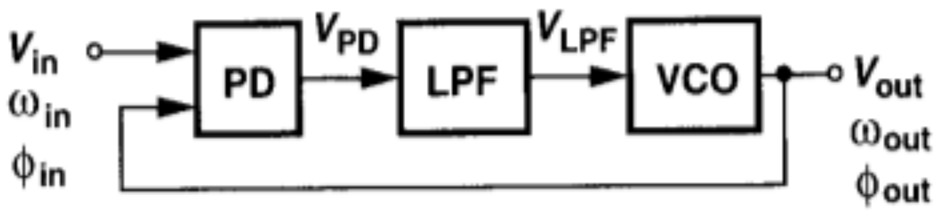
- **In steady state**

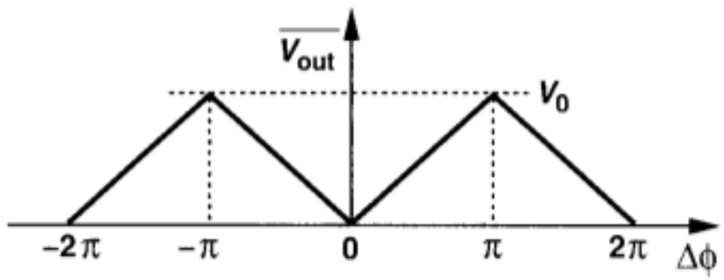
→ The phase difference settles to small value

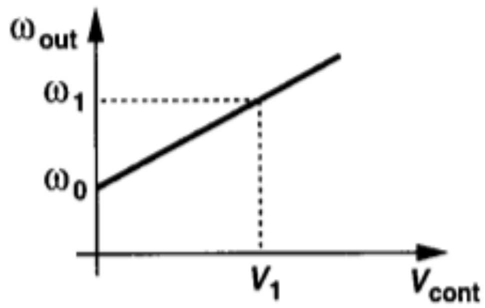
→ The two frequency becomes the same

Phase-Locked Loops in Steady State (I)

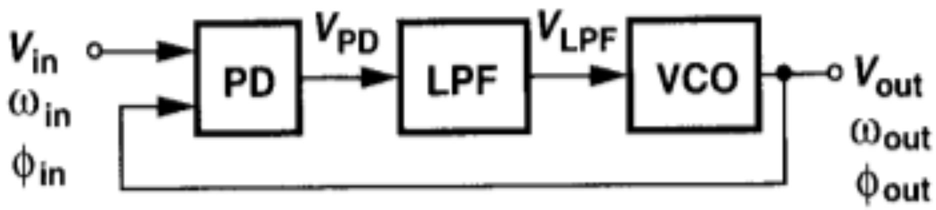
- **Transfer functions of each building block**

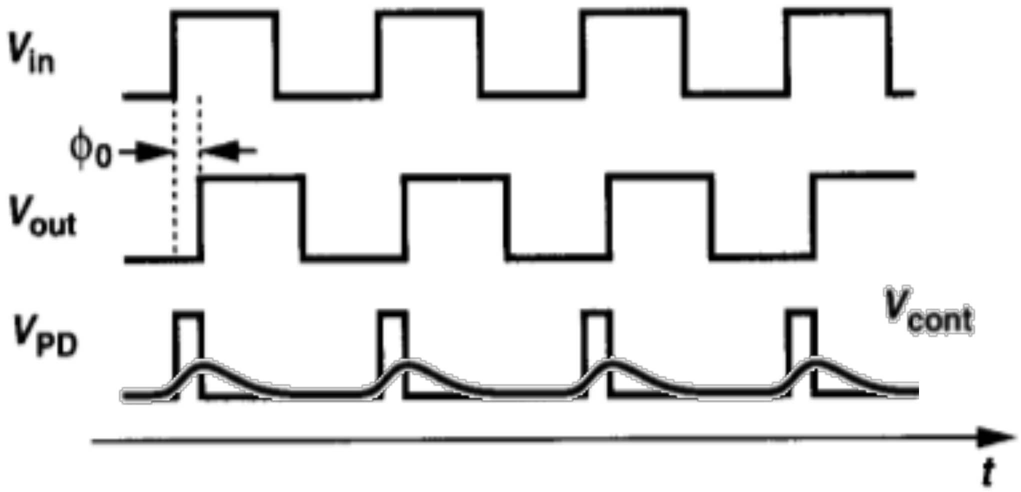






Phase-Locked Loops in Steady State (II)

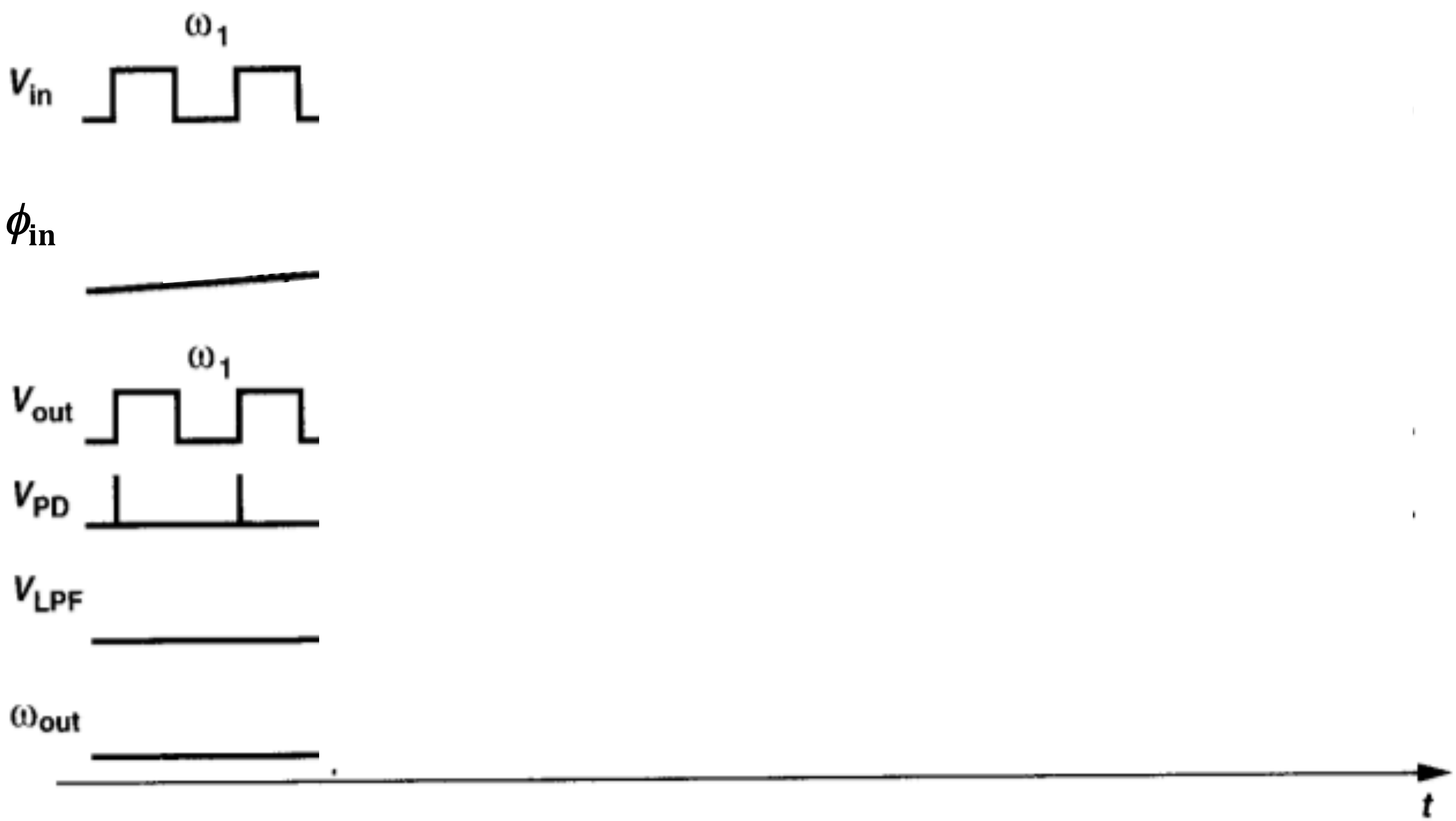




- **The resulting phase error depends on the operating frequency**
- **To minimize phase error → $K_{PD}K_{VCO}$ needs to be maximized**
- **About operating frequency…**

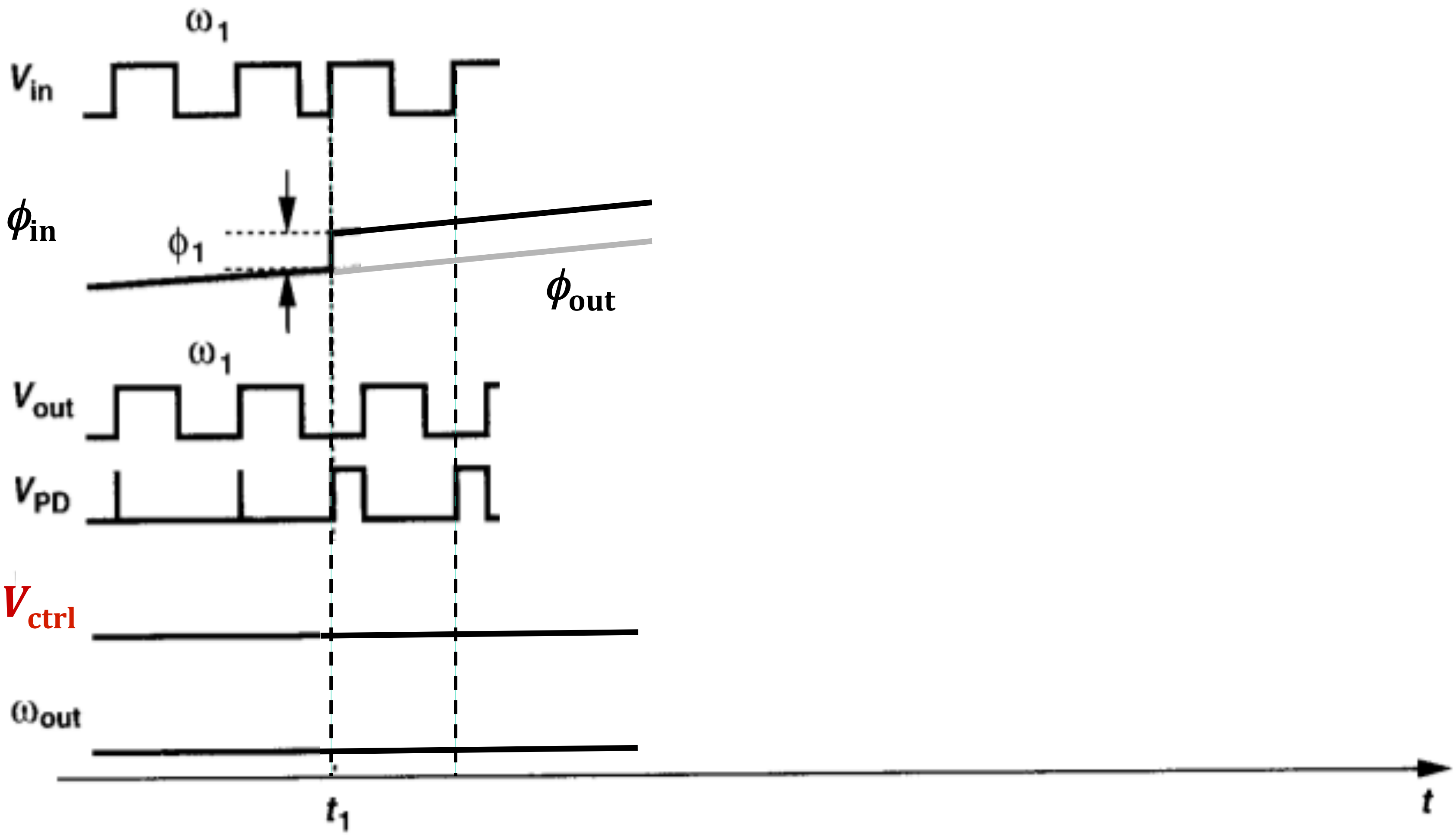
In Case with a Phase Jump

- **How does it look like for a phase jump?**



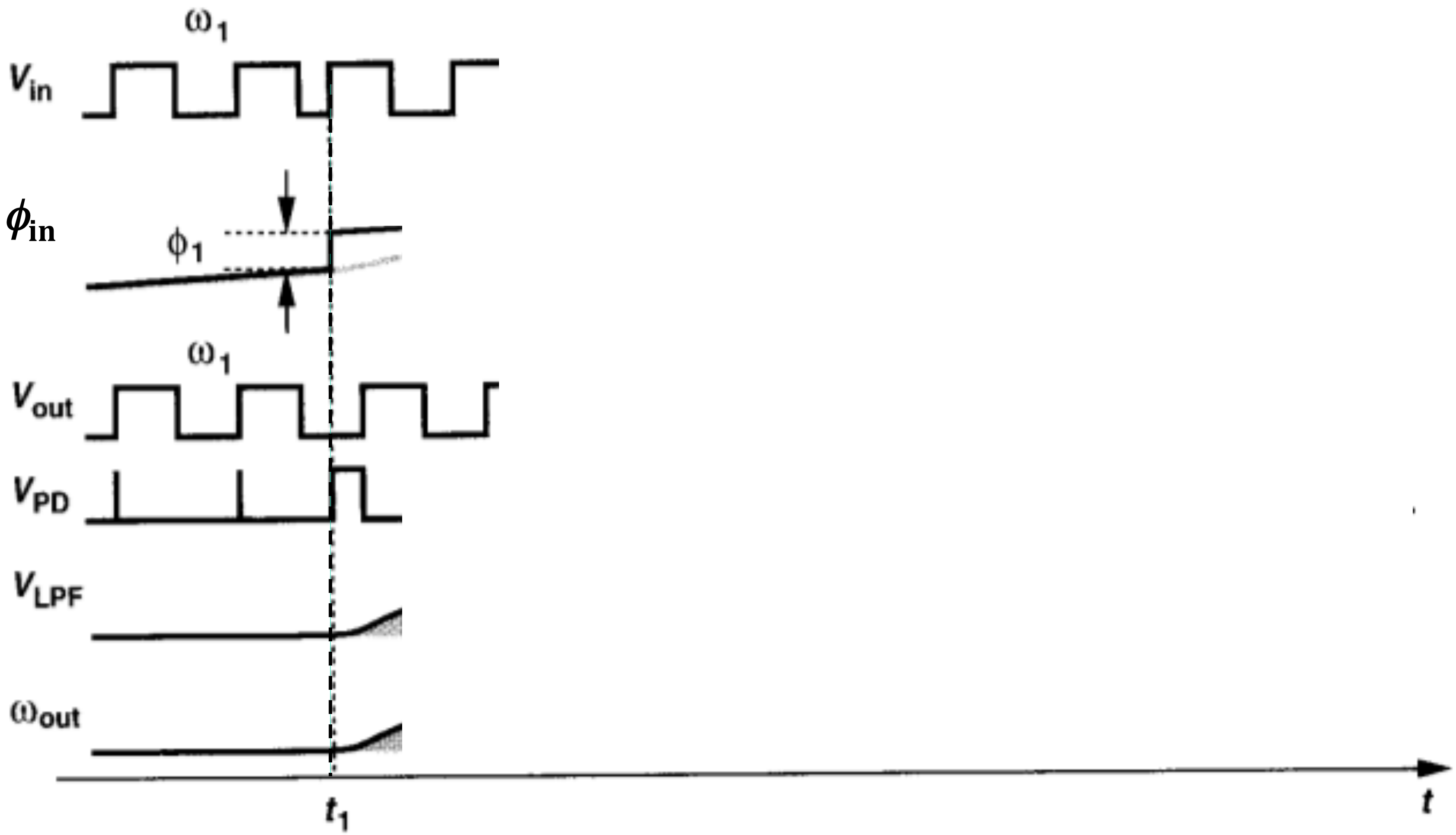
In Case with a Phase Jump

- **How does it look like for a phase jump?**
- **@ t_1 if open-loop**



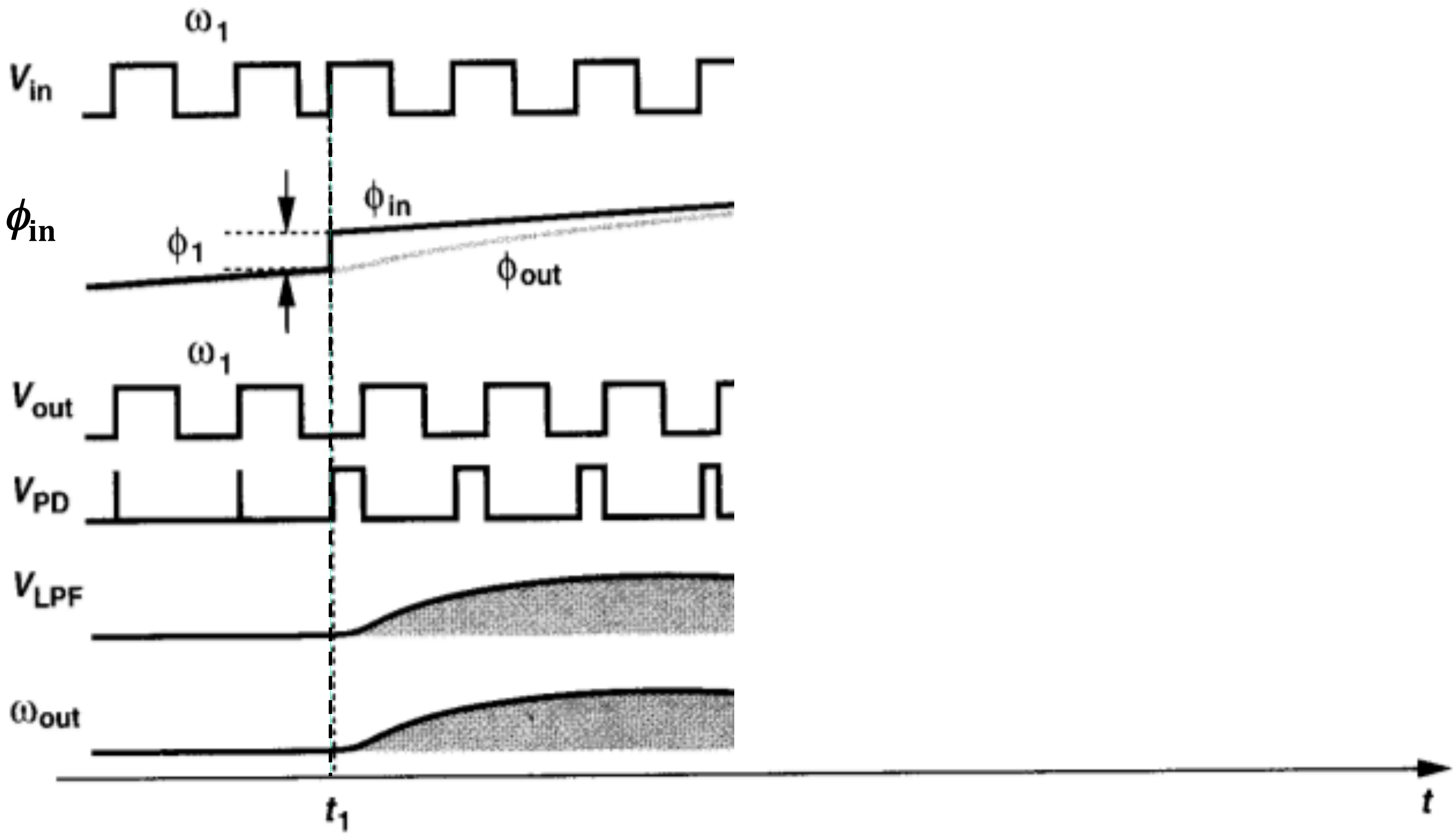
In Case with a Phase Jump

- How does it look like for a phase jump?
- @ t_1 with feedback loop



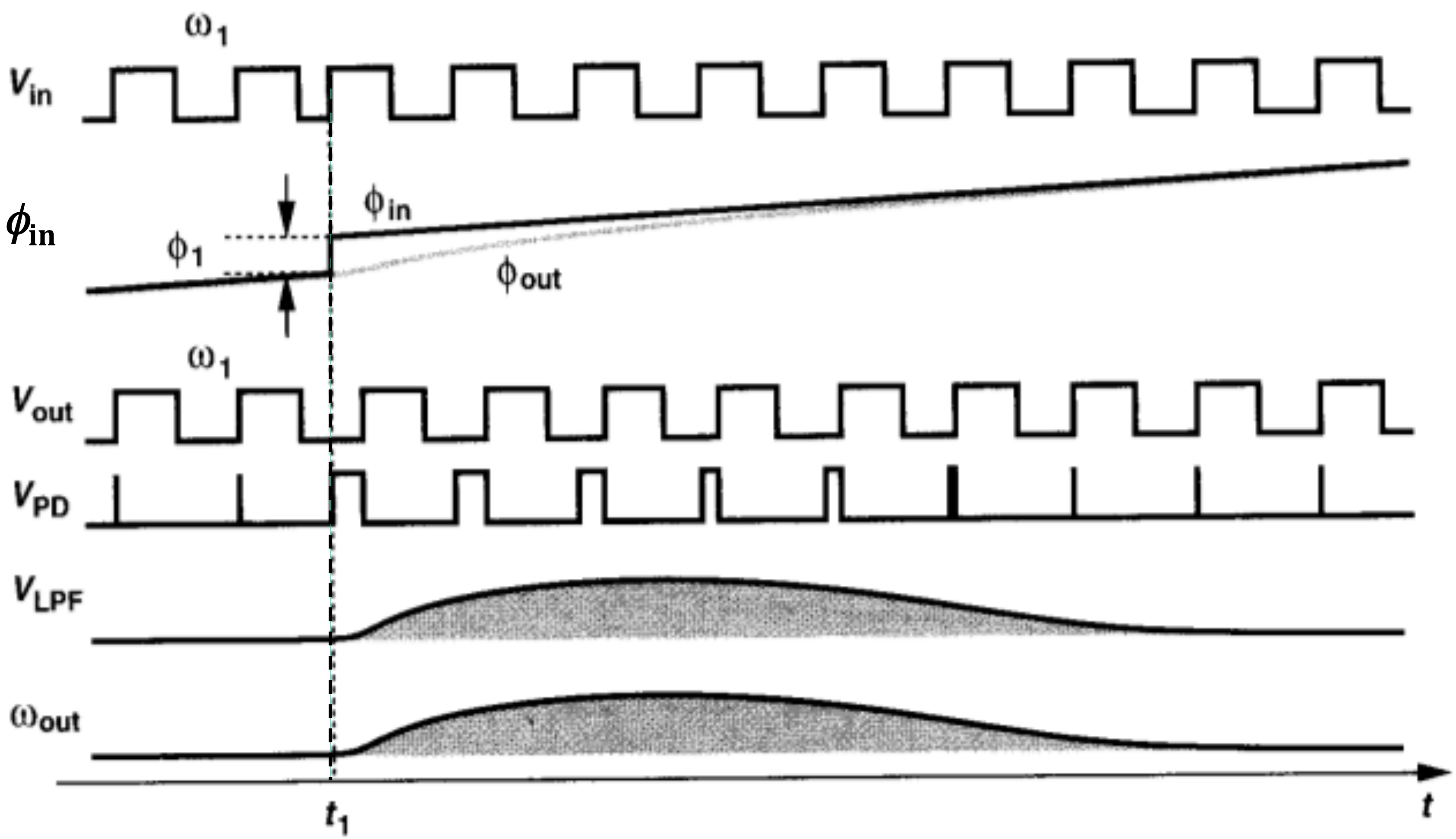
In Case with a Phase Jump

- How does it look like for a phase jump?
- With feedback loop



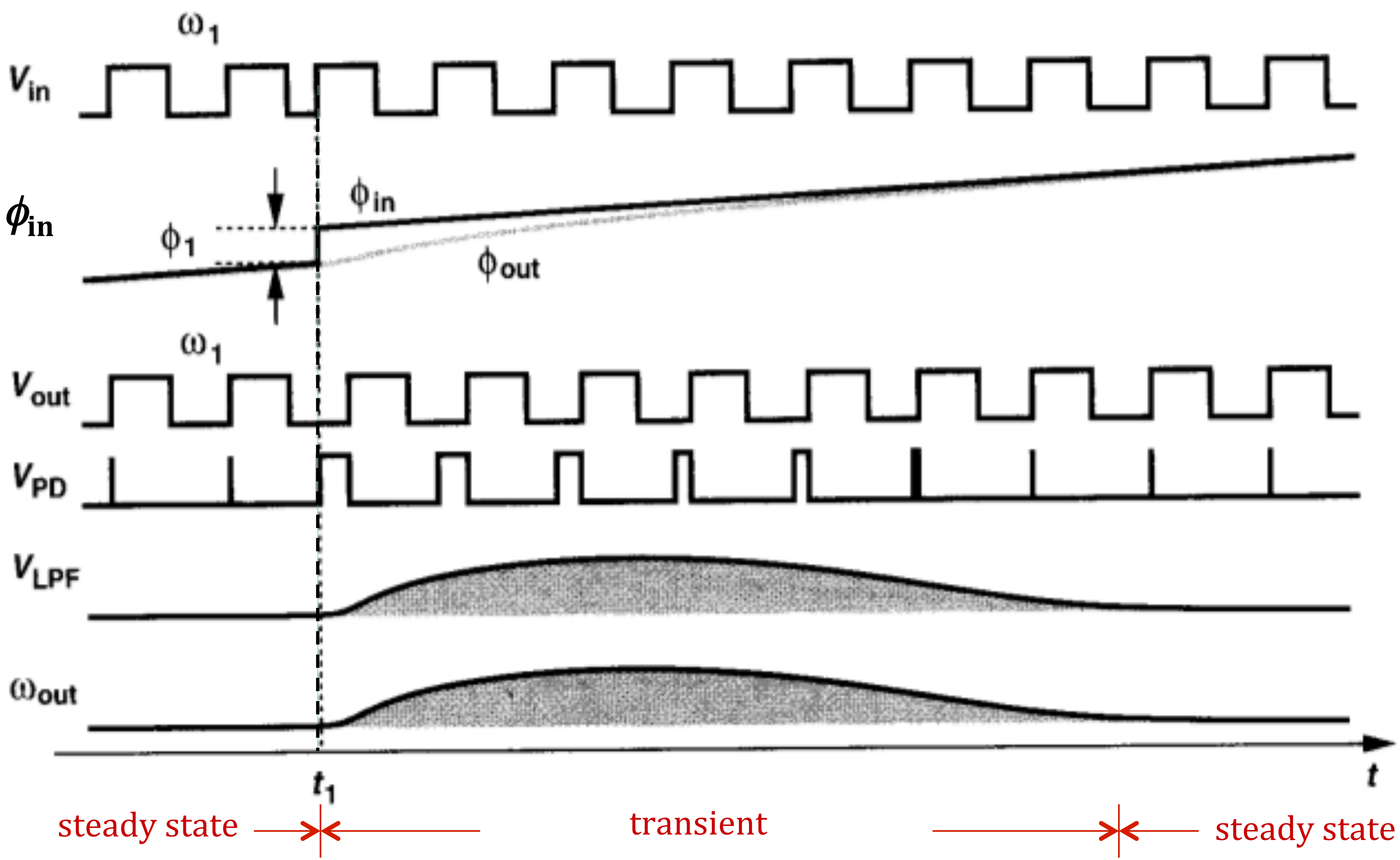
In Case with a Phase Jump

- How does it look like for a phase jump?
- With feedback loop

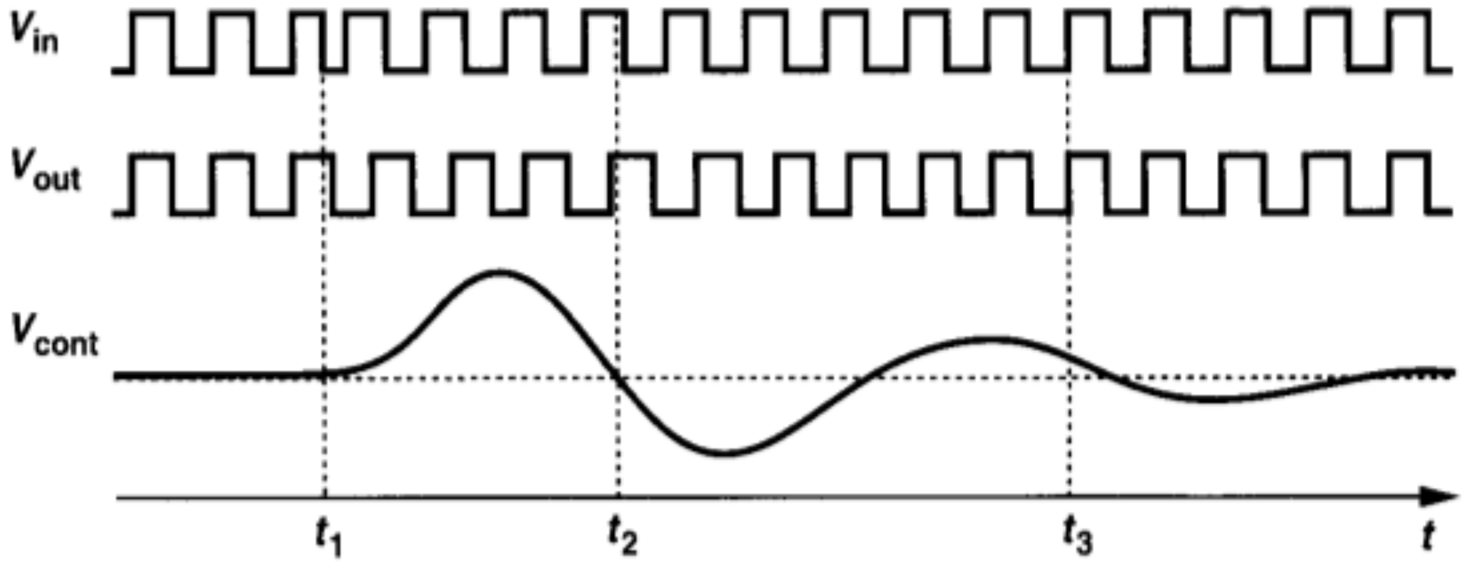


In Case with a Phase Jump

- How does it look like for a phase jump?
- With feedback loop



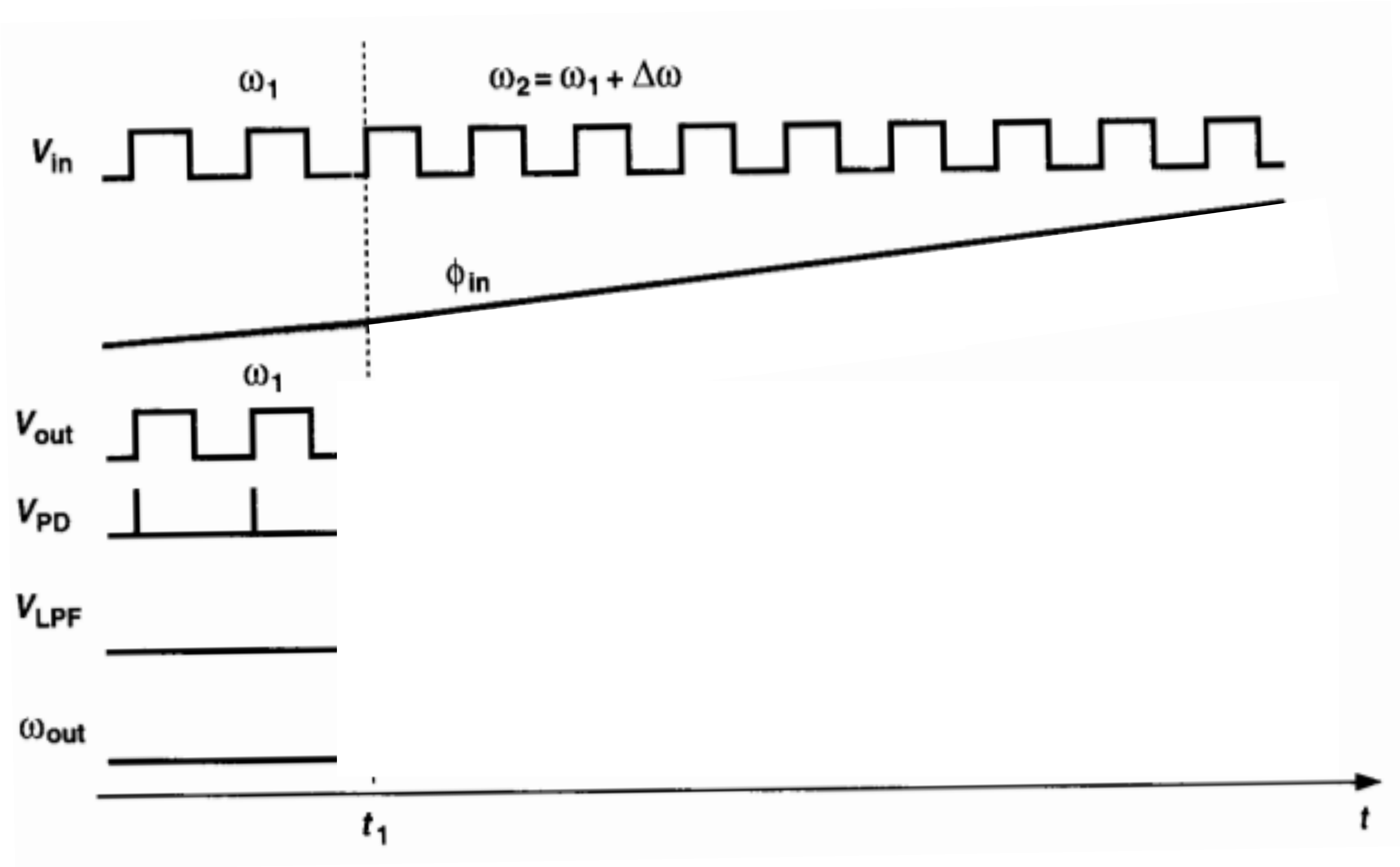
Underdamped Response to Phase Step



- @ t_1 the phase jump happens
- @ t_2 the frequencies are the same, but large phase error
- @ t_3 the phase is the same, but frequency is not

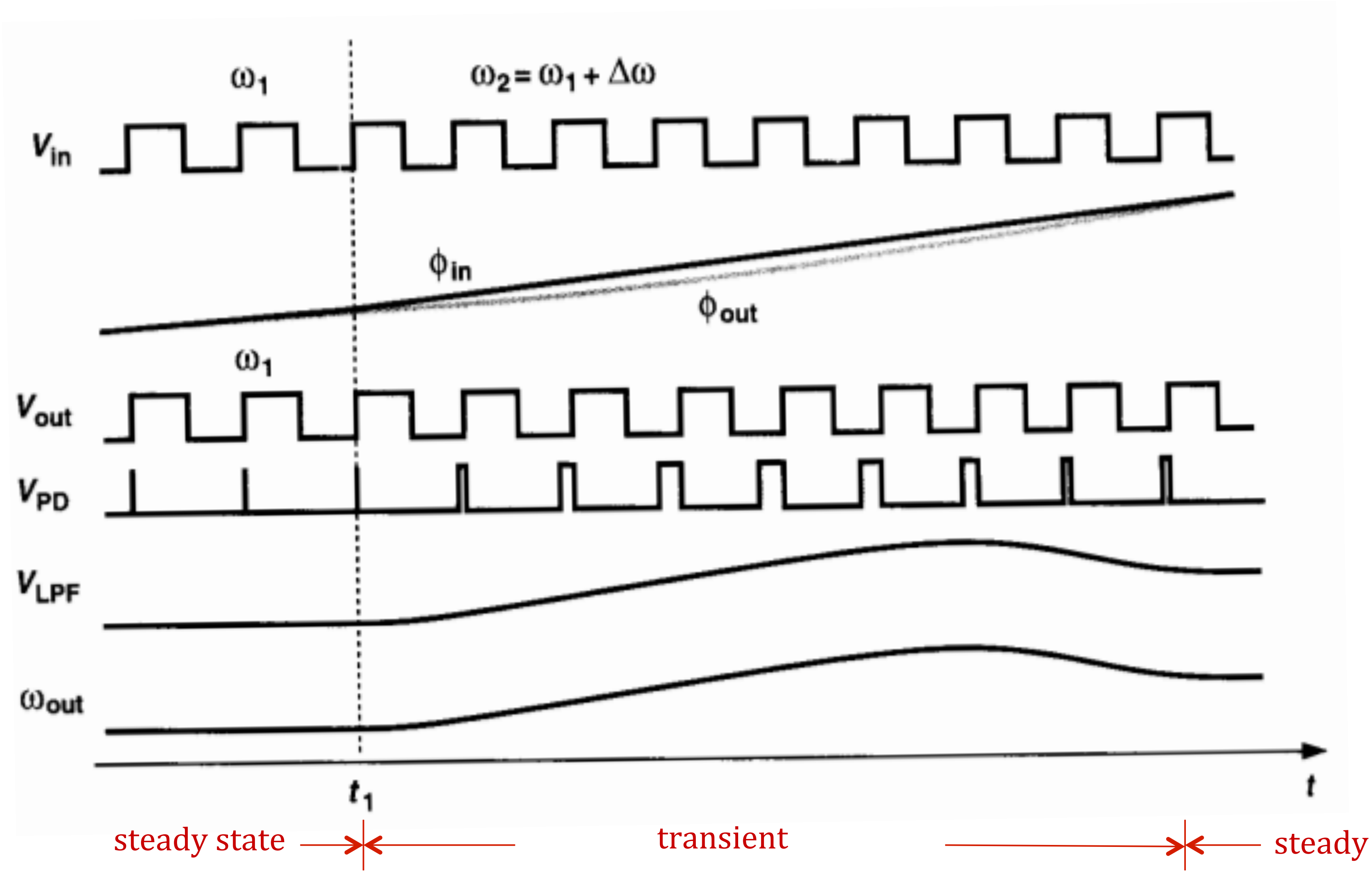
In Case with a Frequency Jump

- **How does it look like for a frequency jump?**



In Case with a Frequency Jump

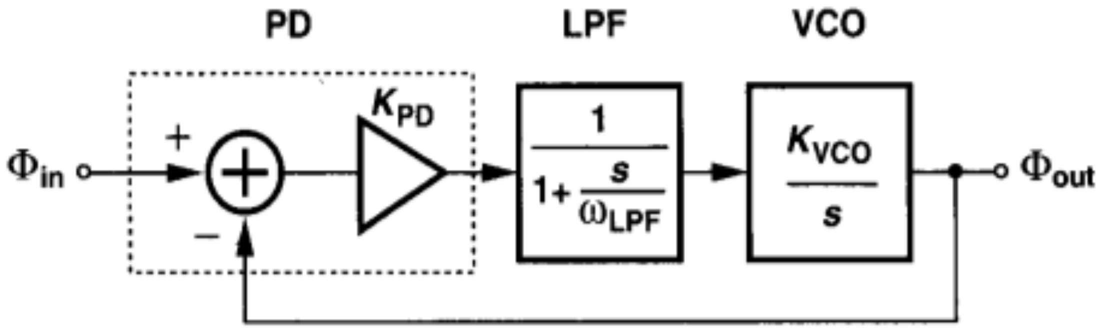
- **How does it look like for a frequency jump?**



Loop Dynamics (I)

- **From previous examples, how fast the loop responses depends on the design of the low-pass filter**

- **Linear model of the PLL → to derive the response from $\phi_{ex,in}$ to $\phi_{ex,out}$**



- **Open-loop transfer function** (from phase → voltage → voltage → phase)

$$H(s)|_{open} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

- Low-frequency gain approaches infinity

Loop Dynamics (II)

- **Closed-loop transfer function**

$$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

- Low-frequency gain of unity

→ Output tracks the input phase well if input phase varies slowly

→ For input phase step, output phase eventually catches up

- **In fact** $\frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$

- Low-frequency gain of unity

→ Output tracks the input frequency well if input frequency varies slowly

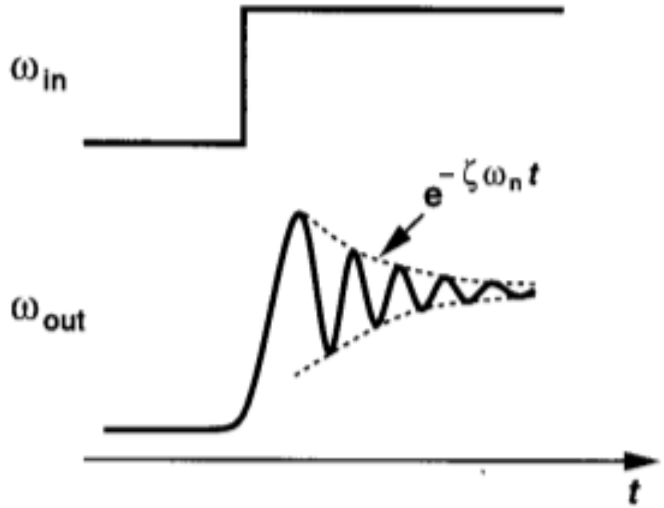
→ For input frequency step, output frequency eventually catches up

Loop Dynamics (III)

- **Second-order transfer function**

$$H(s)|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \qquad \zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}.$$



- If ζ >1, both poles are real → the system is over damped
- If ζ <1, both poles are complex → the step response can be written as

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$$

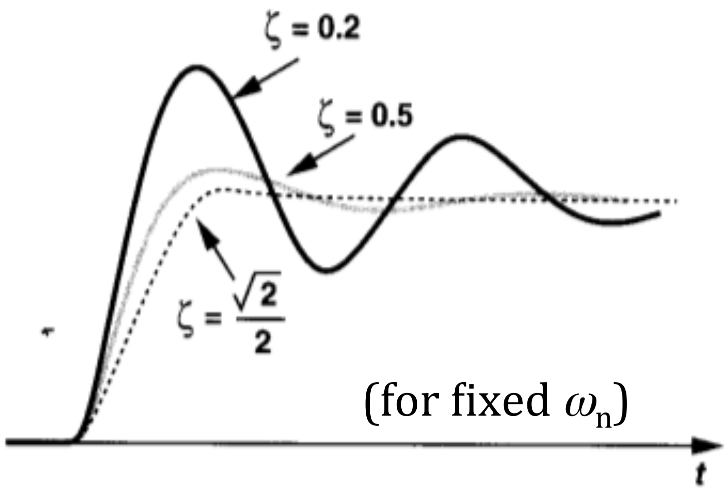
$$\omega_{out}(t) = [1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n\sqrt{1-\zeta^2}t + \theta)]\Delta\omega u(t)$$

(the same behavior for response to phase step)

- Settling speed → $\zeta\omega_n$ needs to be maximized

Loop Dynamics (IV)

- **Damping factor ζ**



$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}}.$$

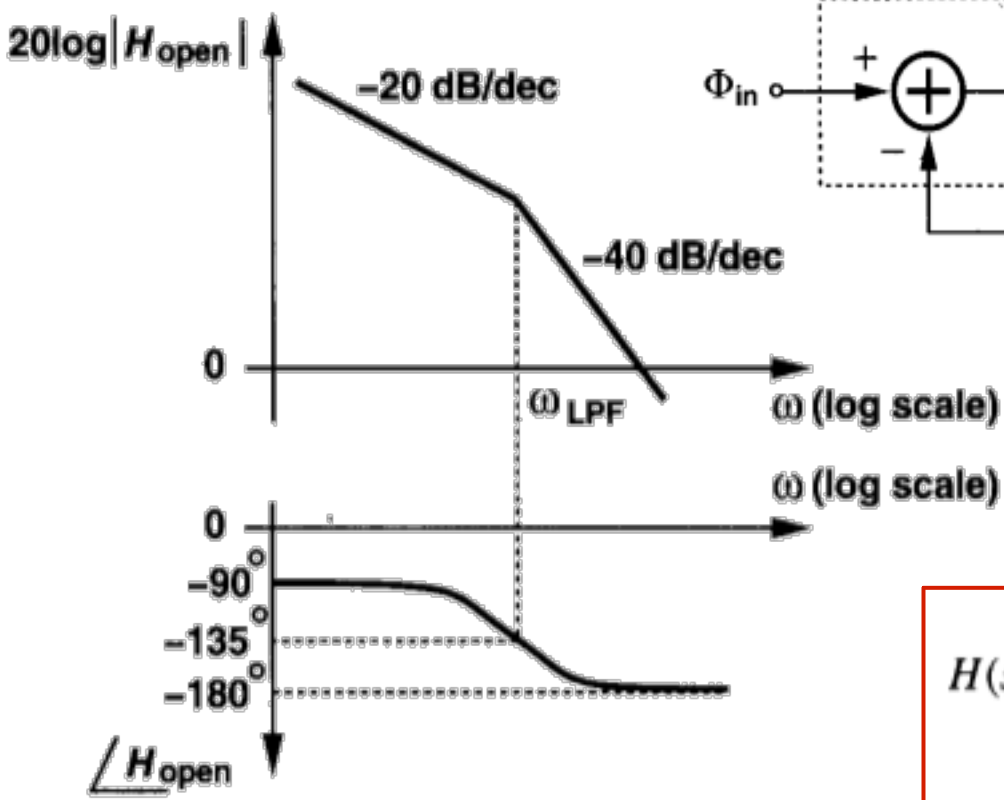
- **For a preferred $\zeta \rightarrow \omega_n$ should be maximized for faster response**

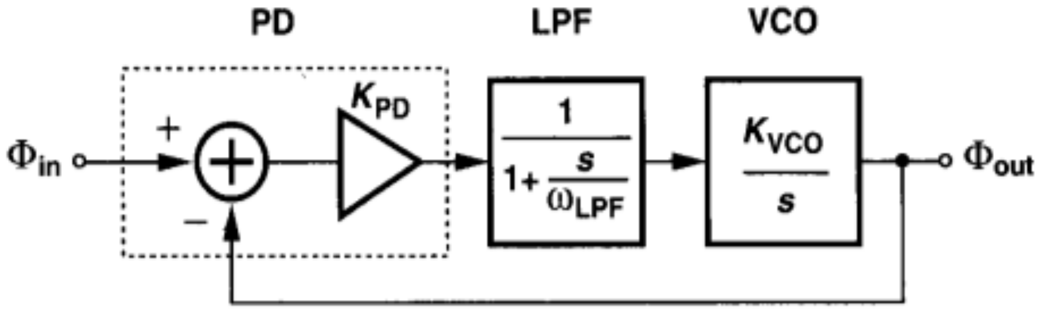
→ ω_{LPF} and $K_{PD}K_{VCO}$ should be increased at the same time

→ Strict trade-offs between response time, stability, steady-state ripple & jitter, and steady-state phase error

Loop Dynamics (V)

- **From Bode plot of open-loop transfer function**





$$H(s)|_{open} = K_{PD} \cdot \frac{1}{1 + \frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

- **The loop becomes less stable if …**