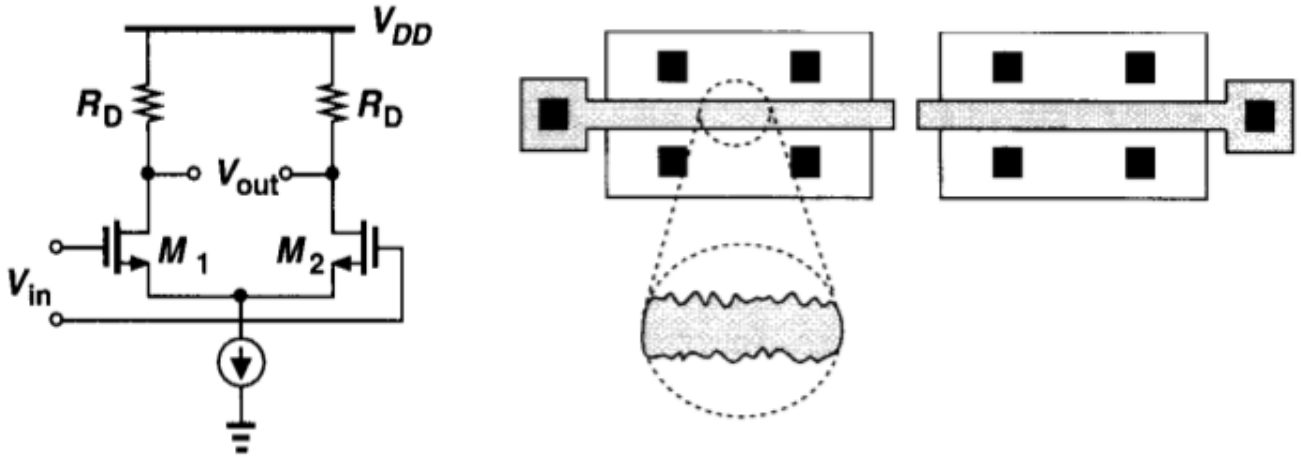
EE4280 Lecture 2: Mismatch

Ping-Hsuan Hsieh (謝秉璇)
Delta Building R908
EXT 42590
phsieh@ee.nthu.edu.tw

Mismatch (I)

Due to uncertainties in each step of the manufacturing process
For identical devices, random and microscopic variations lead to

- Mismatches in physical dimension
- Mismatches in threshold voltages



To study mismatch of devices:

1. Identify and formulate the mechanisms leading to mismatches
2. Analyze the impact on circuit performance

   → Techniques to suppress the impact from mismatches

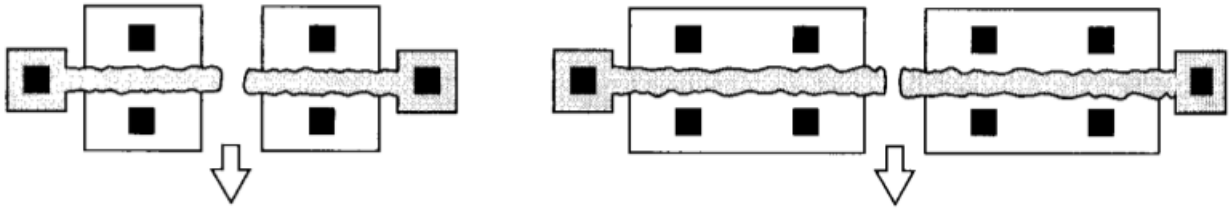
Mismatch (II)

For a transistor operating in saturation region

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2$$

All mismatches decreases as the area of the transistor *WL* increases

- **Random variations experience greater averaging**



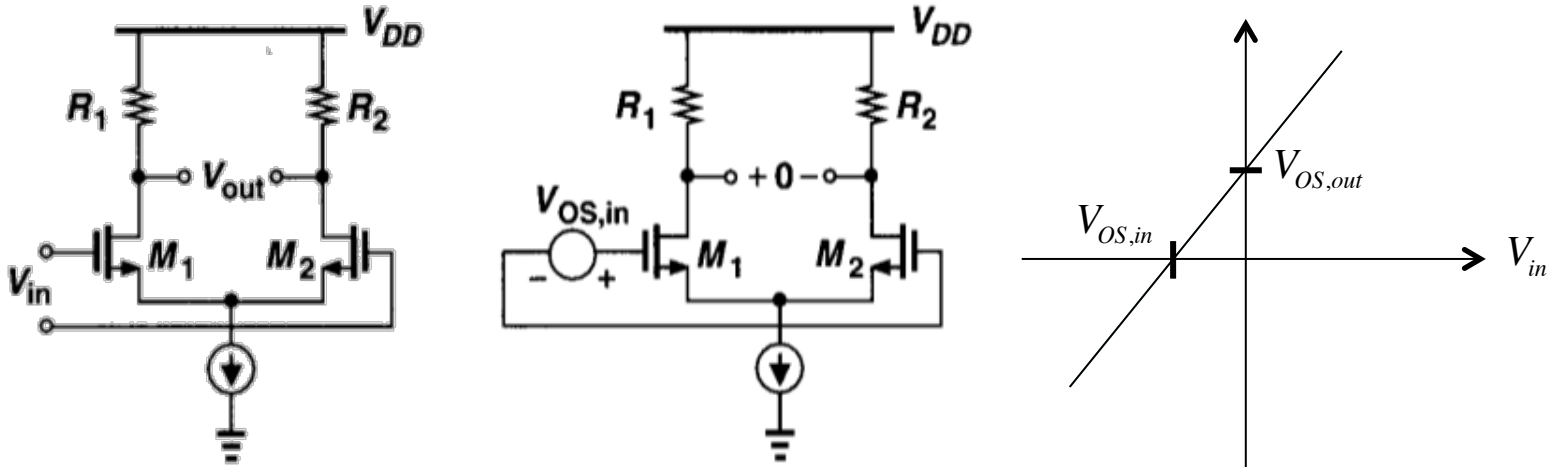
Can be extended to other device parameters

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \qquad \Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}$$

DC Offset

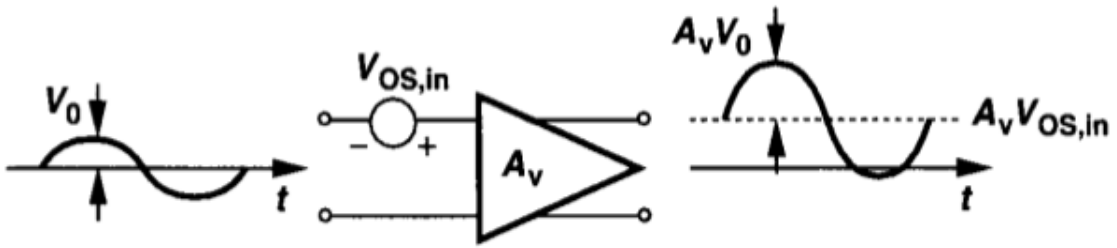
With perfect symmetry $V_{out} = 0$ when $V_{in} = 0$

With mismatches $V_{OS,out} \neq 0$ when $V_{in} = 0$



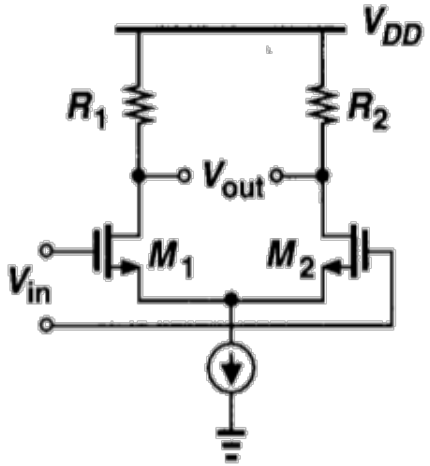
→ **May saturate the following stages**

→ **Degrade the precision with which signals can be measured**



DC Offset of a differential pair

- **To calculate the input-referred offset**



$$V_{out} = 0 \Rightarrow I_D R_D = (I_D + \Delta I_D)(R_D + \Delta R)$$

$$V_{OS,in} = V_{GS1} - V_{GS2}$$

DC Offset of a differential pair

- **To calculate the input-referred offset**

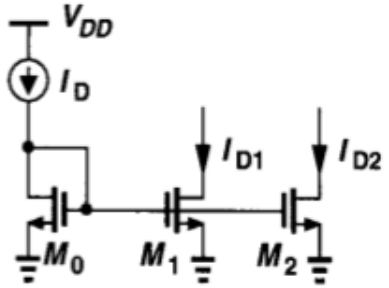
$$V_{OS,in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH}.$$

  - Depends on device mismatches and bias conditions
- **Offset can be viewed as low-frequency noise**
  - Similar to noise, larger g_{m1} suppresses input-referred offset voltage
- **Variance:**

- **Consider only transistor mismatch, for I_{D1}=I_{D2}**

Current mismatch in current mirror

- **Consider nominally identical transistors (M_1 and M_2) and neglect r_o**



$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2$$

$$= f\left(\mu C_{ox}, \frac{W}{L}, V_{GS}, V_{th}\right)$$

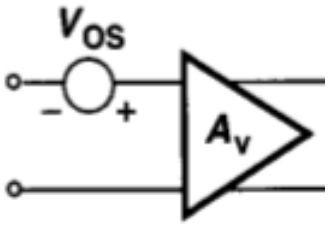
$$\Delta y = \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \cdots$$

$$\Delta I_D = \frac{\partial I_D}{\partial (W/L)}\Delta\left(\frac{W}{L}\right) + \frac{\partial I_D}{\partial (V_{GS}-V_{TH})}\Delta(V_{GS}-V_{TH})$$

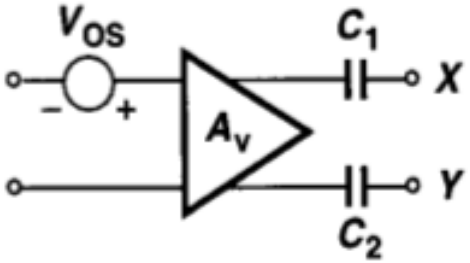
- **From output current point of view**
  - Smaller g_m required to suppress the mismatch
  - The same for noise current

Offset Cancellation Techniques

- **Add two voltage sources in series with V_{out}**

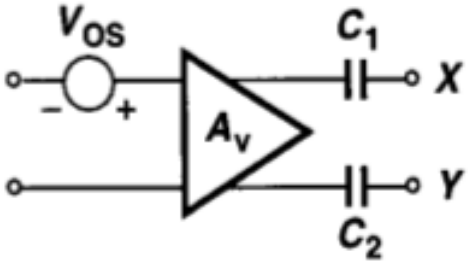


- **Use output series capacitors C_1 and C_2**
  - With stored charges that corresponds to $V_{OS,out}$



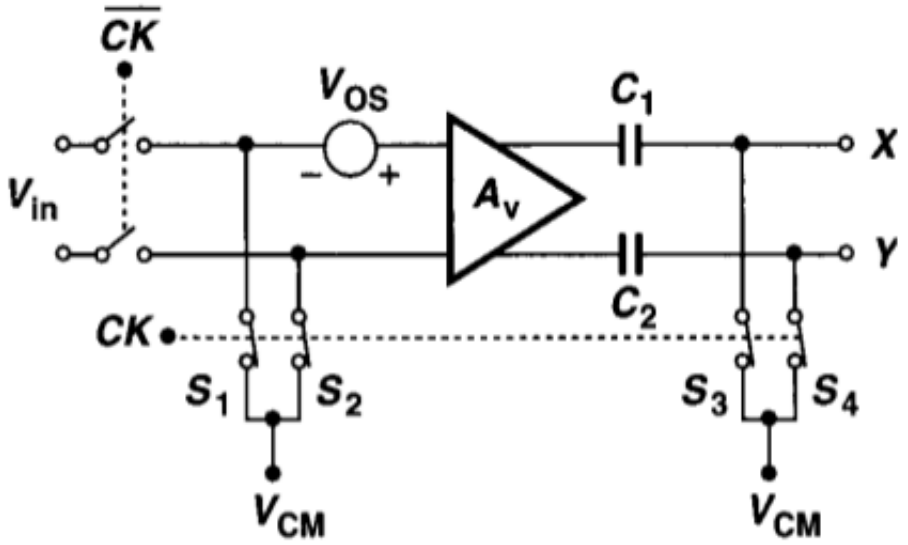
Output Offset Storage

- How to store the required charge on C_1 and C_2?



Output Offset Storage

- **A dedicated offset cancellation period required**
  - Controlled by signal *CK*
  - Design of switches → may cause additional mismatch



- $V_{OS,out}$ **may saturate the amplifier, degrading the voltage gain**

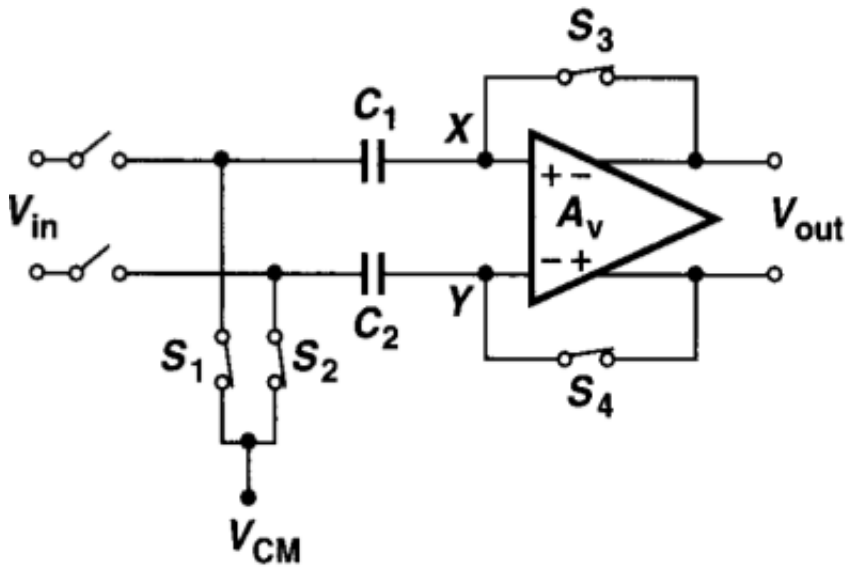
Input Offset Storage

- The concept of using series capacitors to store offset voltage can be applied to input (with smaller voltage value)

- How to store the required charge on C_1 and C_2?

Input Offset Storage

- How to store the required charge on C_1 and C_2?

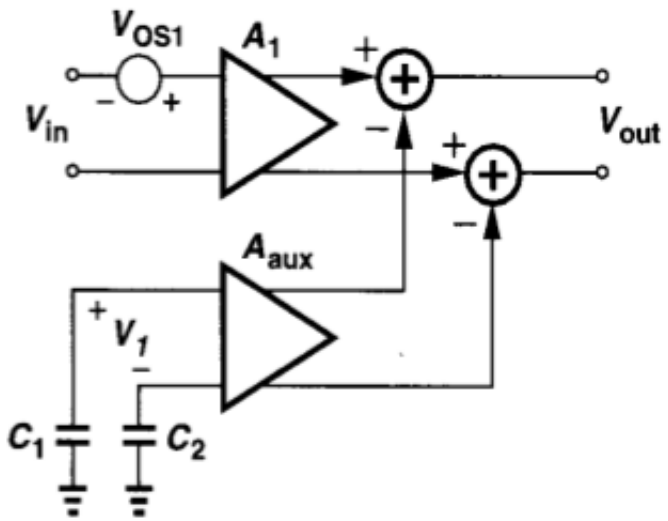


$V_{OS,\,in}$ =

- Allows larger A_V
- Still subject to switches mismatch
- Additional capacitors in the signal path

Offset Cancellation Techniques

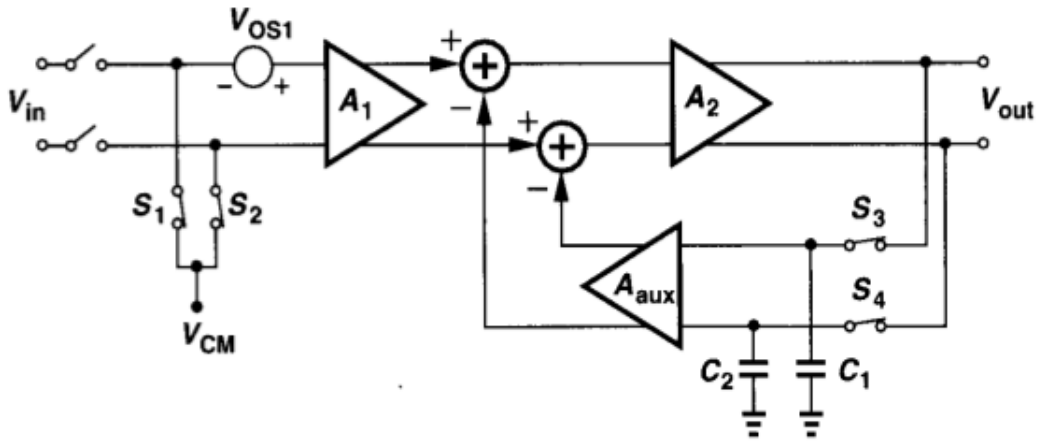
- To avoid capacitors in the signal path



- How to generate V_1 for offset cancellation?

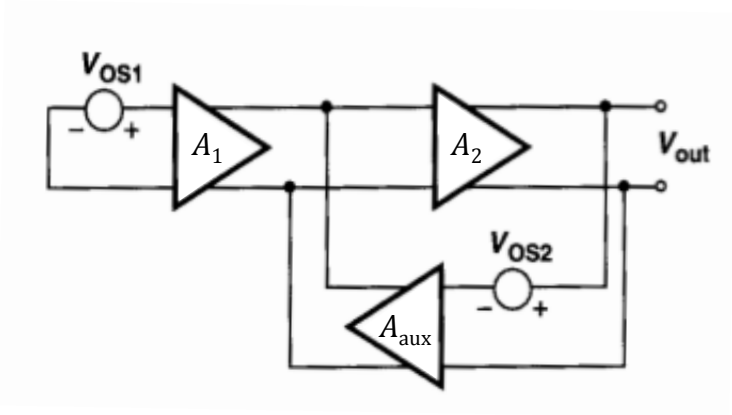
Offset Cancellation Techniques

- Add an additional stage A_2 and apply negative feedback



Offset Cancellation Techniques

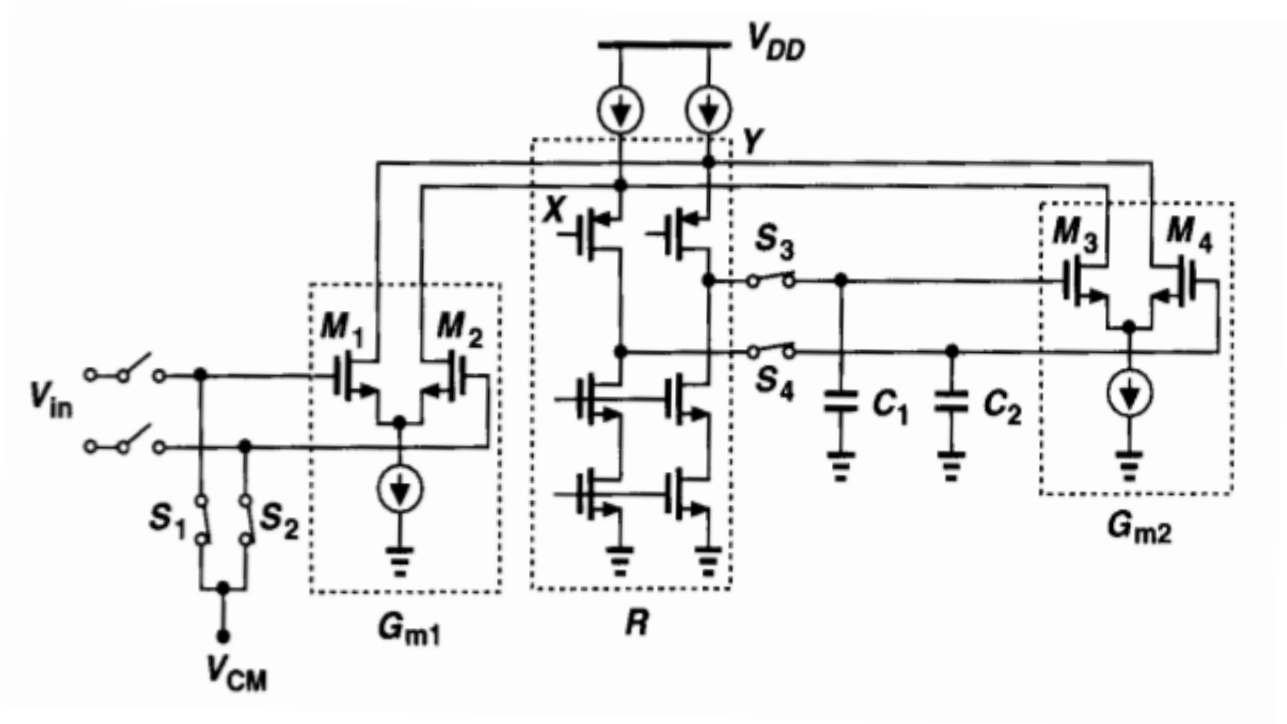
- If we further consider the offset in A_{aux}



- For mismatch in charge injection when turning S_3 and S_4 OFF

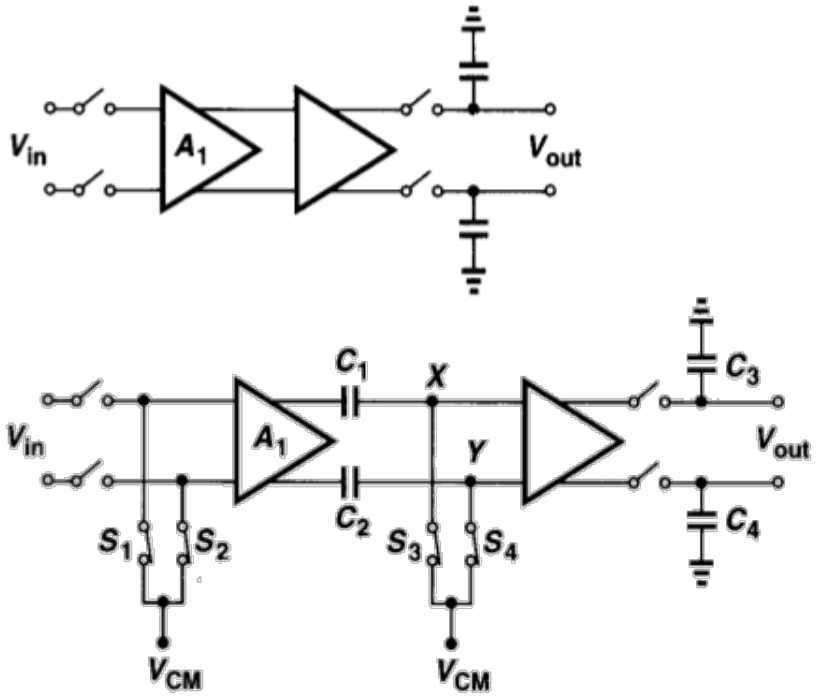
Offset Cancellation Techniques

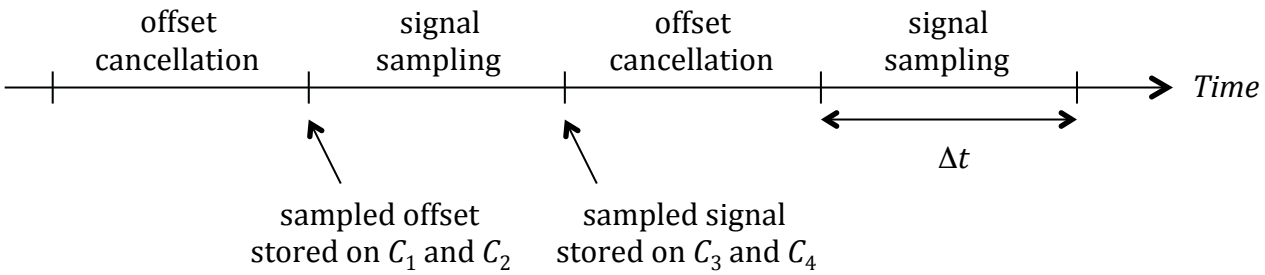
- The additional stage A_2 may not be allowed
- How to achieve "voltage addition"?



Reduction of Noise by Offset Cancellation

- **For a cascade of two amplifiers in the front-end of a sampling system**
  - Noise/offset of A_1 corrupts V_{in} directly





Reduction of Noise by Offset Cancellation

- **Assume** $\Delta t = 10$ ns

- **Consider two noise components at 1 MHz and 10 MHz respectively**
- **During the 10 ns**

- **Correlated double sampling (CDS)**
  - Two consecutive sampling operations with small Δt that low-frequency noise component cannot vary significantly