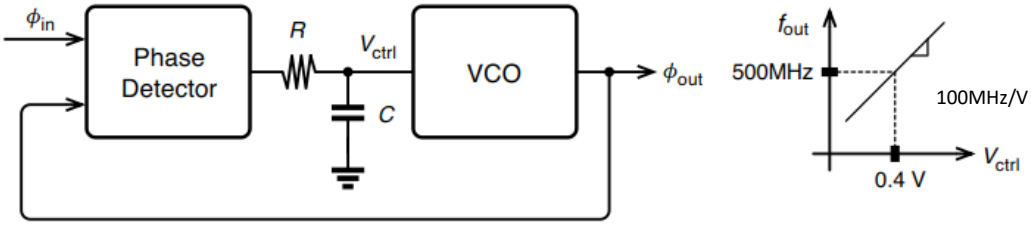
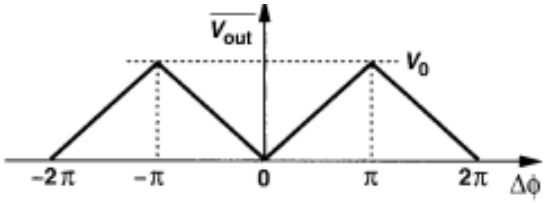
1. Consider the PLL shown in the following figure.



a) Use an XOR gate as the phase detector (with VDD of 1.8 V). The PLL is a second-order system. With the VCO transfer function shown in the figure, calculate the open-loop transfer function and the closed-loop transfer function of the system when the output frequency is 500MHz.
(Hint: Be careful on the difference between angular frequency and frequency.)

a. $\omega = 2\pi f, \phi(t) = \int \omega(t)dt,\ f_{out} = 460M + 100M \times V_{ctrl}$



V0 = 1.8V

$$\frac{\omega_{out}(s)}{\omega_{in}(s)}|_{open} = \frac{\Phi_{out}(s)}{\Phi_{in}(s)}|_{open} = K_{PD} \times \frac{1}{1+\frac{s}{\omega_{LPF}}} \times \frac{K_{VCO}}{s},$$

$$K_{VCO} = \frac{100MHz}{V} = \frac{200\pi M\left(\frac{rad}{s}\right)}{V}, \omega_{LPF} = \frac{1}{RC}, K_{PD} = \frac{1.8}{\pi}$$

$$\Rightarrow \frac{\Phi_{out}(s)}{\Phi_{in}(s)}|_{open} = \frac{(200\pi M)\times(1.8/\pi)}{s^2RC+s}, \frac{\Phi_{out}(s)}{\Phi_{in}(s)}|_{closed} = \frac{(200\pi M)\times(1.8/\pi)}{s^2RC+s+(200\pi M)\times(1.8/\pi)}$$

b) What corner frequency of the loop filter should be used so that the damping factor of the (second-order) system is 0.707?

b. $\omega_{corner} = \omega_{LPF} = \frac{1}{RC}, H(s)|_{closed} = \frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$

$$\rightarrow \zeta = \frac{1}{2}\sqrt{\frac{1}{RC\times(200\pi M)\times(1.8/\pi)}} = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \omega_{corner} = 2 \times (200\pi M) \times \left(\frac{1.8}{\pi}\right) = 720M\ rad/s$$

$$\Longrightarrow f_{corner} = \frac{\omega_{corner}}{2\pi} = 114.59M\ Hz$$

c) What is the phase margin in this case?

c. $H(s)|_{open} = \frac{K_{PD}K_{VCO}}{s^2RC+s} = \frac{K_{PD}K_{VCO}}{-\omega^2RC+j\omega} = \frac{K_{PD}K_{VCO}}{\omega^4R^2C^2+\omega^2}(-\omega^2RC - j\omega)$

$$\Rightarrow |H(s)|_{open}| = \frac{K_{PD}K_{VCO}}{\sqrt{\omega^4R^2C^2+\omega^2}} = 1\ @0dB \rightarrow \omega = 327.67\ rad/s$$

$$\Rightarrow \theta = \tan^{-1}(-\omega RC) = -24.47° \Rightarrow P.M. = (-90° + \theta) - 180° = 65.53°$$

d) When the loop is locked, what is the phase difference between the two inputs? (Who leads whom by how many degrees?)

d. $s\left(\frac{\Phi_{out}(s)}{\Phi_{in}(s)}|_{closed}\right)|_{s\to 0} = 0 \Rightarrow$ means that steady-state error is zero

$K_{PD} = \frac{1.8}{\pi} = \frac{V_{ctrl}}{\Delta\phi_{DC}}, V_{ctrl} = 0.4V \Rightarrow \Delta\phi_{DC} = 40°$

➔ The output phase leads the input phase by 40° when the loop is lock.

e) From b) If the filter corner frequency had been 5 times lower than calculated in previous question, what would have been the damping factor and the phase margin of the system?

e. $\zeta' = \text{new damping factor} = \zeta\sqrt{0.2} = \frac{1}{\sqrt{10}}$

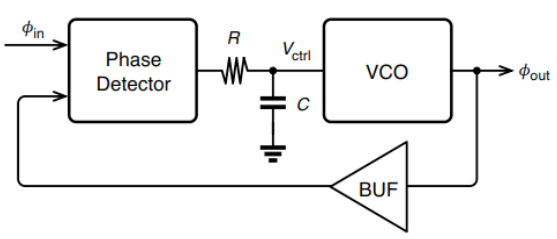
$\omega'_{corner} = 144M \text{ rad/s}, \theta' = -34.93° \Rightarrow P.M.' = 55.07°$

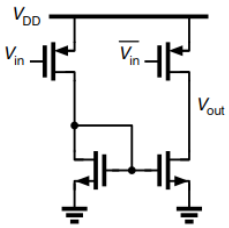
f) From b) What are the damping factor and the phase margin of the system when the output frequency is 505MHz? What is the phase difference between the two inputs in this case? (Who leads whom by how many degrees?)

f. When the output frequency becomes 505MHz, K_{VCO}, K_{PD}, and the transfer function aren't changed. Therefore, the damping factor and the phase margin of this system aren't changed.
However, the phase between the two inputs becomes 45 degree, which the output phase leads the input phase.

$K_{PD} = \frac{1.8}{\pi} = \frac{V_{ctrl}}{\Delta\phi'_{DC}}, V_{ctrl} = \frac{505M-460M}{100M} = 0.45V \Rightarrow \Delta\phi'_{DC} = 45°$

2. Use **HSpice** to design a PLL according to the following description.





In the simulations, set:
.option accurate=1
.option runlvl=6

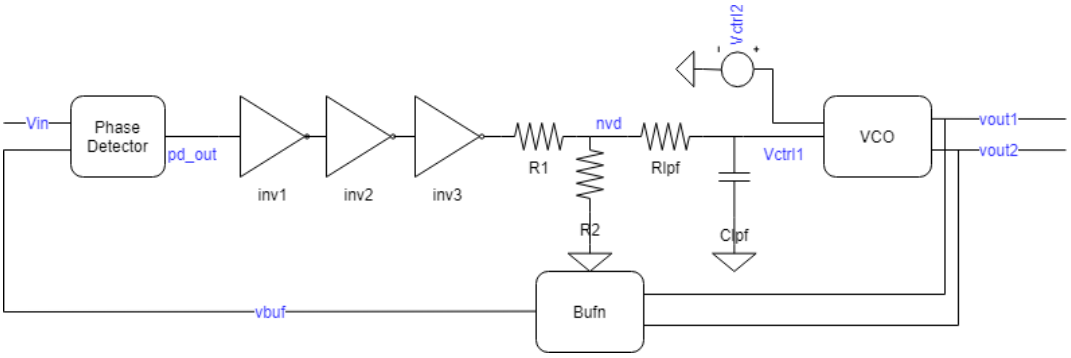
- Use an XOR gate as the phase detector. Use the VCO from HW3.
- Design the R and C values so that the damping factor of the (second-order) system is 0.707. Report the R and C value chosen.
- Put together the PLL. (You would need to first simulate each block to make sure they functions correctly.) Feed the input with a sinusoid of 500MHz whose common mode is 0.9 V and amplitude is also 0.9 V.
- You are allowed to add proper numbers of inverters (with proper size) after the phase detector to drive the loop filter.

- You may need to insert a buffer after the VCO to drive the phase detector. One example schematic is shown. You will need to design the buffer so that the buffer outputs are rail-to-rail with decent rise/fall time.
- Be careful with the initial conditions. You would need to set initial conditions for some of the oscillation nodes and the capacitor in the loop filter. Be careful with the phase of the input signal as well.
- Run transient simulations with long enough duration so that the loop reaches steady state.

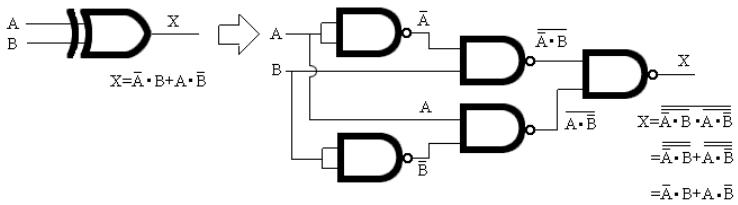
a) Report your schematic details (schematic and size), including any inverter or buffer you insert. Explain your design considerations.

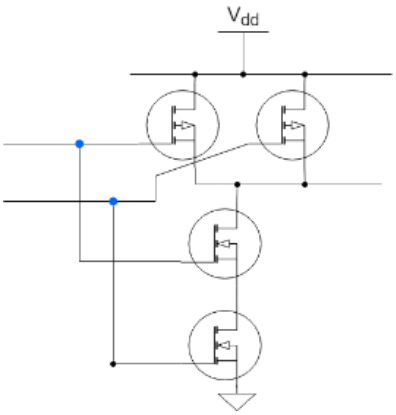
a.

- Overview



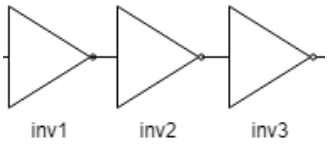
  - $R1 = 5k\Omega,\ R2 = 2k\Omega,\ Rlpf = 7k\Omega$, and $Clpf = 10fF$
- Phase Detector (Xor)





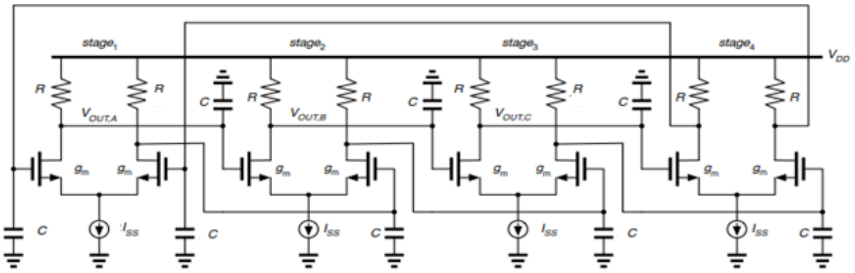
  - NAND size
    - NMOS: 6um/0.18um; PMOS: 8um/0.18um

- Three Inverters

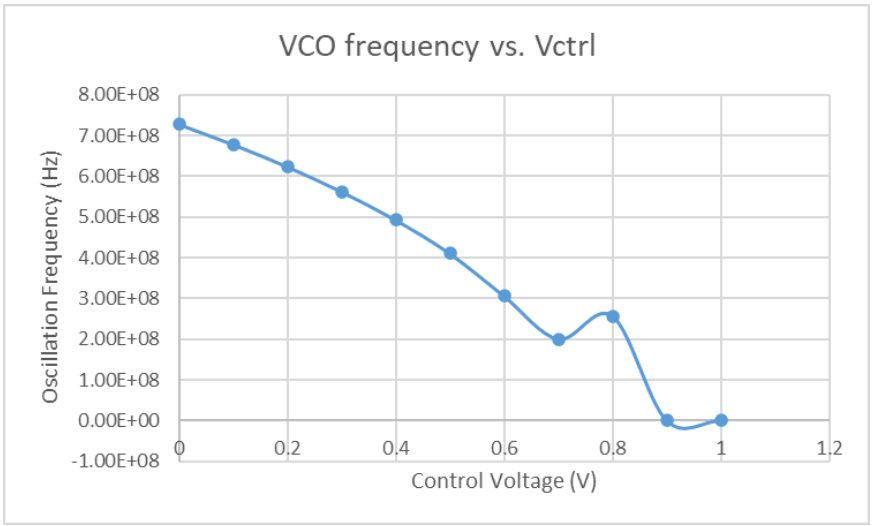


  - Purpose: 為了讓 PD 能夠推動後面的 LPF 和 VCO
  - 數量的選擇: 此電路需要接奇數個 inverter，因為我設計的 K_{VCO} 是負的，而一個 inverter 推不動，因此選擇用三個 inverter。

- VCO

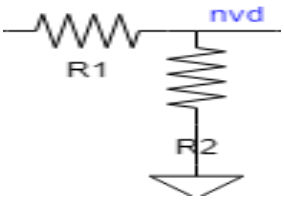


Element	Value
Stage NMOS (M11n, M12n)	$(50\mu m/0.18\mu m)$
Stage PMOS (M11p, M12p)	$(3.4\mu m/0.18\mu m)$
C	200 fF
I_{SS}	500 μA
Gain of each stage	8.15 (18.5dB)
Frequency of -3dB Gain	300 MHz
Input Common-mode	1.4 V
Output Common-mode	1.398 V



  - It shows that the value of K_{VCO} I designed is 950MHz/V
  - Implementation:
    此是將 stage1 & stage3 的 PMOS control 訊號連接至 LPF 後面，也就是接到 Vctrl1；stage2 & stage4 的 PMOS control 訊號連接至一個 0.4V 的定電壓。此做法的目的是為了降 K_{VCO}。

- Frequency divider

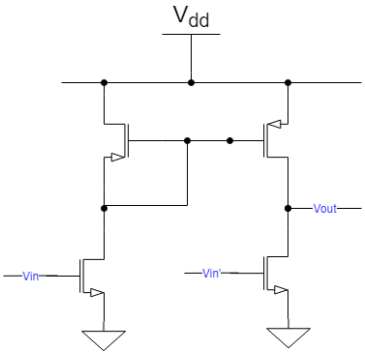


  - Purpose: To lower the value of K_{PD}
  - Result: $K_{PD} = \frac{1.8}{\pi} \times \frac{R2}{R1+R2} = \frac{0.51}{\pi}$

- For Low-pass-filter
  - $\omega_{corner} = \frac{1}{RC} = 311M \text{ rad/s for damping factor} = 0.707$

    ➔ I set the resister and capacitor in low-pass filter are $7k\Omega$ and 10fF respectively

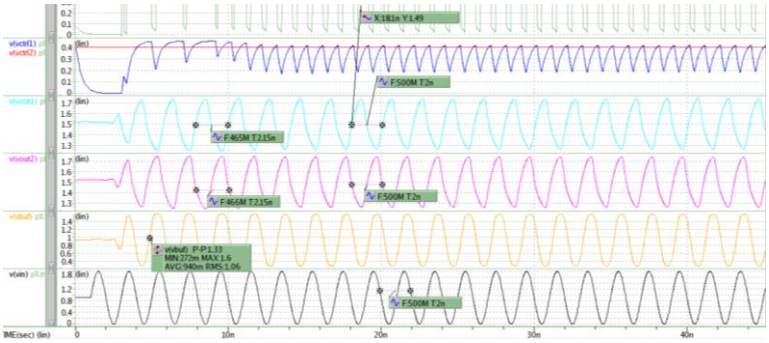
- For buffer stage (Bufn)



  - Purpose: 由於經由 VCO 後得的 output 只會在 1.2 ~ 1.8V 間震盪，因此加此 buffer 使得 vbuf 會變成在 0 ~ 1.8V 間震盪，因此選用 N-type 的 differential input single-ended output 的結構。
  - Result: 1.2 ~ 1.8V 間震盪的 vout1 和 vout2 經由 Bufn 得到的 output “vbuf”會在 0.27 ~ 1.6V 間震盪。

b) How long does it take for the loop to reach steady state? How do you measure it?

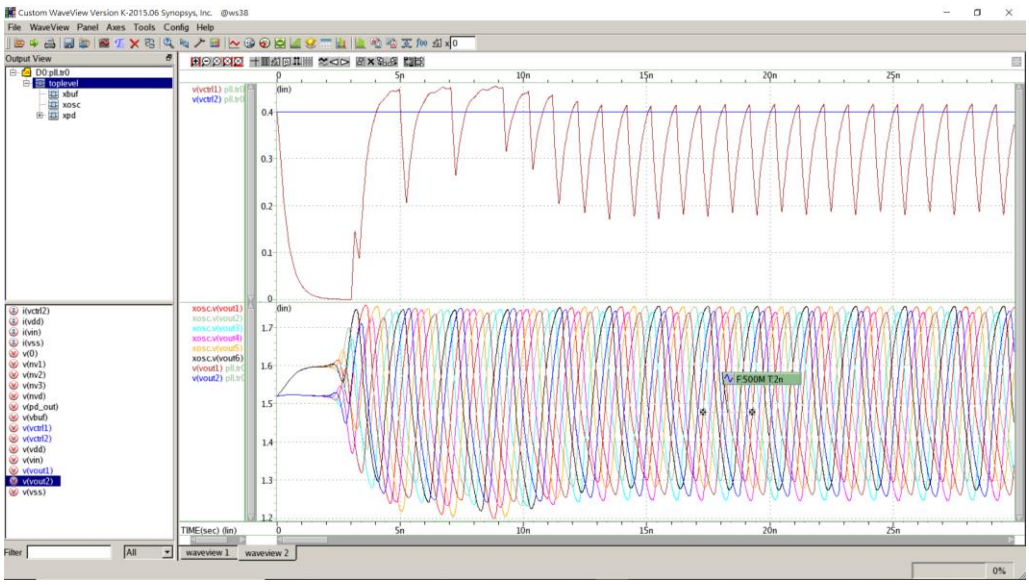
b.



  - It shows that the settling time is 18.1ns

c) Plot V_{ctrl} from *t*=0 to steady state. With the same scale in time, plot all 8 oscillation waveforms into one figure (on the same row). Mark important data points and explain.

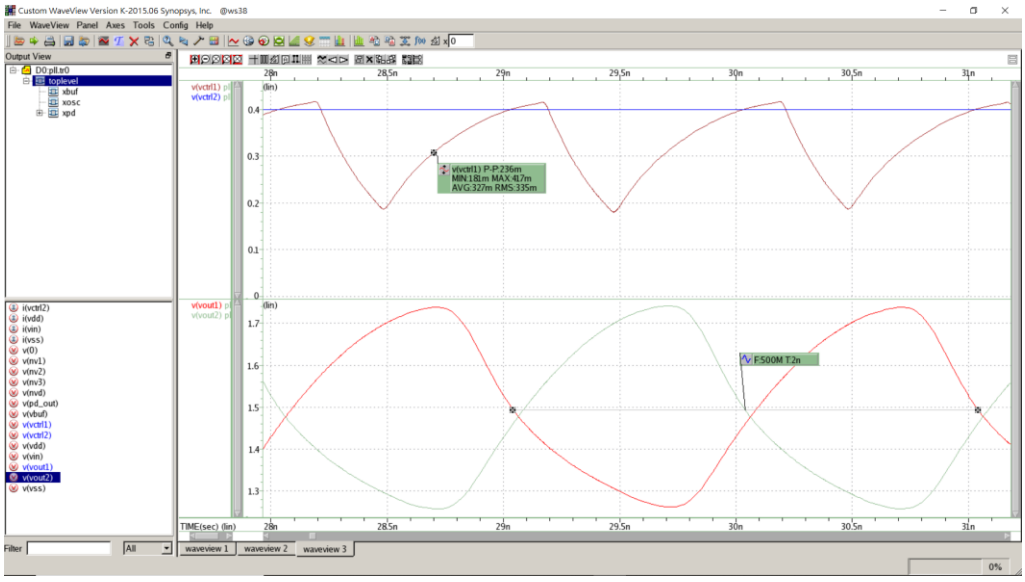
c.



- It shows that the settling time is 18.1ns and the frequency in the steady-state of all outputs in VCO are locked at 500MHz.

d) Plot the waveform of V_{ctrl} for 2 oscillation periods when the loop reaches the steady state. Comment on the waveform.

d.

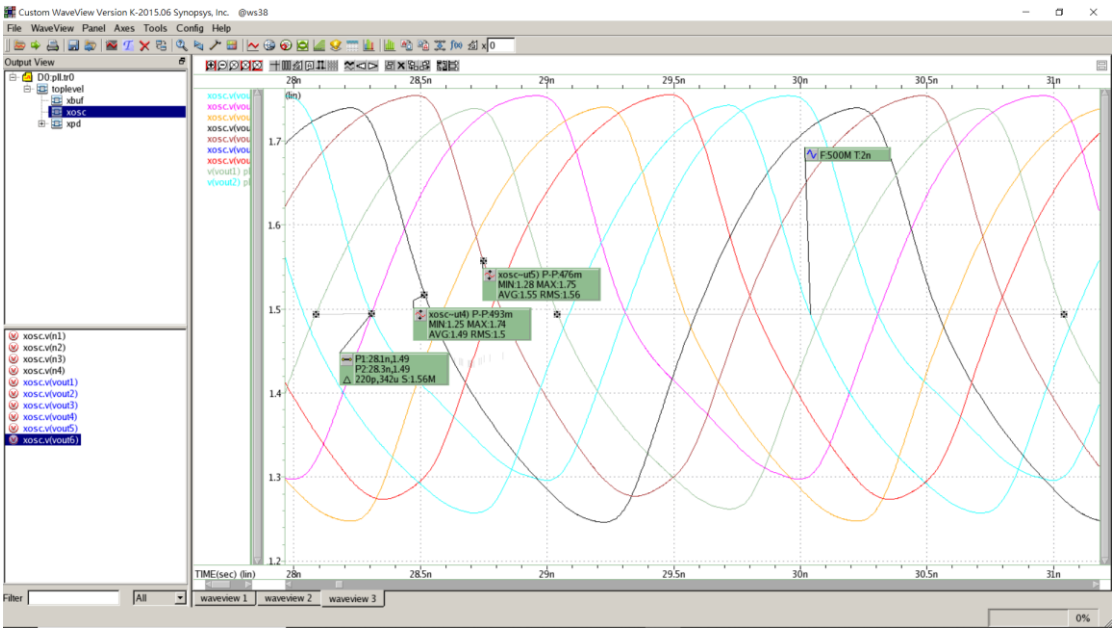


- It shows that V_{ctrl} oscillates between 0.181V to 0.417V in the steady state, and the average value of V_{ctrl} is 0.327V, which can make VCO oscillate at 500MHz.
- The error between 0.327V and 0.4V, which I designed in VCO, is due to the loading of the input of VCO increased.

e) Plot all 8 oscillation waveforms into one figure (on the same row) for 2 periods in steady state. How are the results different from VCO-only simulations and why?

Are all the oscillation amplitudes the same? Why or why not? Measure the phase difference and explain why (or why not) all 8 phases are evenly separated.

e.



- All the oscillation amplitudes are the same because gain in each stage are the same. However, the maximum value of the output in both stage2 and stage4 are lower than in both stage1 and stage3. This is because the average control voltage of stage2 and stage4 are much larger, which will increase $R_{ON,P}$.
- Phase difference $= \Delta t \times f \times 360° = 39.6°$, which is close to ideal phase difference $45°$. This is because the RC time constant and the oscillation frequency in each stage are the same.

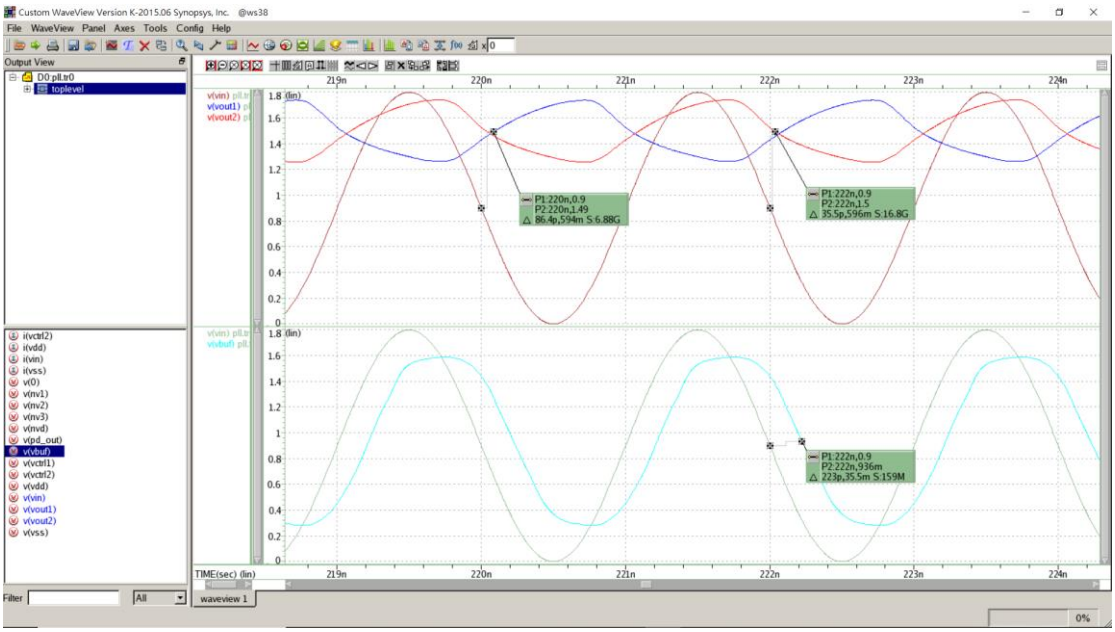
f) What is the expected static phase error between the two oscillation signals (from hand-calculation)?

f. By measurement, $K_{PD} = \frac{0.307}{0.75\pi} = 0.13$, $K_{VCO} = \frac{\omega_1 - \omega_0}{V_1 - V_0} = 456.7\text{M Hz/V}$

$$\Delta\phi_{DC} = \frac{\omega_1 - \omega_0}{K_{PD}K_{VCO}} = \frac{2\pi(478\text{M} - 295.32\text{M})}{0.13 \times 456.7\text{M}} = 19.33 = 27.7° \text{ (Vbuf leads Vin)}$$

g) Plot the waveforms for the oscillation node that goes into the buffer, and the two inputs that go into the phase detector for 2 oscillation periods after the loop reaches the steady state. Mark and measure the static phase error between 1) the reference input and that oscillation node, and 2) the two inputs that go into the phase detector. How are these two results different? Why? Which one corresponds to the static phase error from hand-calculation?

g.



- For the phase error between the reference input and the oscillation node (Vout1, Vout2)
  - Measurement:
    Phase difference (Vout1) $= \Delta t \times f \times 360° = 15.55°$
    Phase difference (Vout2) $= \Delta t \times f \times 360° = 6.39°$
- For the phase error between two inputs that go into the phase detector
  - Measurement:
    Phase difference $= \Delta t \times f \times 360° = 40.14°$
- The reason for the difference between the above two results is that there is a phase shift after the processing of buffer stage; therefore, the phase error between two inputs that go into the phase detector is much larger than the other.
- The signal after VCO stage processing is related to the static phase error, which I calculated above.