**EE4280 Analog Integrated Circuits Analysis and Design II** **2020 Spring**

**Homework IV –** due date: 06/17 (Wednesday) 10AM **(No late homework!!!)**

- Please submit your report with the correct file name (HW3_105061703.pdf or HW3_105061703.doc) to our course website (iLMS system) by the deadline. No hardcopy will be accepted this time.
- Please replace 105061703 with your own student ID.
- Use cic018.l for simulations. Do not change any of the model parameters.

**1)** Consider the PLL shown in the following figure.

**a)** Use an XOR gate as the phase detector (with VDD of 1.8 V). The PLL is a second-order system. With the VCO transfer function shown in the figure, calculate the open-loop transfer function and the closed-loop transfer function of the system when the output frequency is 500MHz.
(Hint: Be careful on the difference between angular frequency and frequency.)

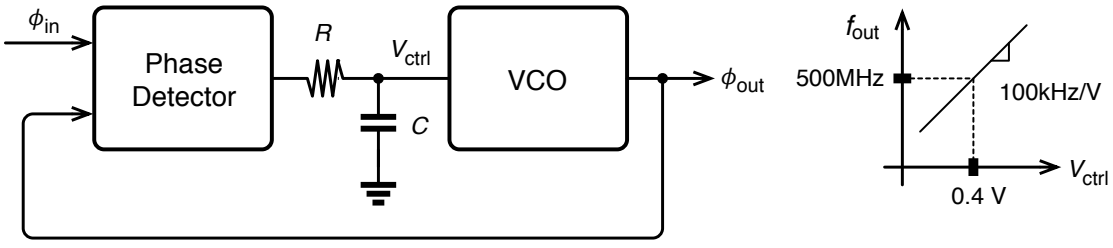
**b)** What corner frequency of the loop filter should be used so that the damping factor of the (second-order) system is 0.707?

**c)** What is the phase margin in this case?

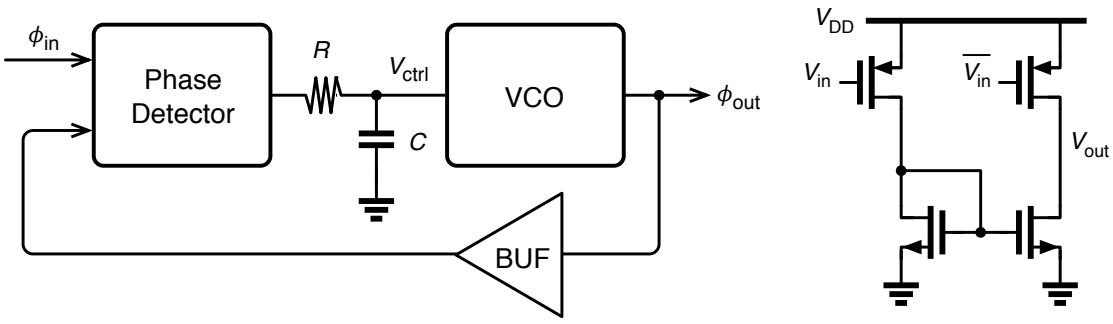
**d)** When the loop is locked, what is the phase difference between the two inputs? (Who leads whom by how many degrees?)

**e) From b)** If the filter corner frequency had been 5 times lower than calculated in previous question, what would have been the damping factor and the phase margin of the system?

**f) From b)** What are the damping factor and the phase margin of the system when the output frequency is 505MHz? What is the phase difference between the two inputs in this case? (Who leads whom by how many degrees?)



**2)** Use **HSpice** to design a PLL according to the following description.




In the simulations, set:
.option accurate=1
.option runlvl=6

- Use an XOR gate as the phase detector. Use the VCO from HW3.
- Design the R and C values so that the damping factor of the (second-order) system is 0.707. Report the R and C value chosen.

- Put together the PLL. (You would need to first simulate each block to make sure they functions correctly.) Feed the input with a sinusoid of 500MHz whose common mode is 0.9 V and amplitude is also 0.9 V.
- You are allowed to add proper numbers of inverters (with proper size) after the phase detector to drive the loop filter.
- You may need to insert a buffer after the VCO to drive the phase detector. One example schematic is shown. You will need to design the buffer so that the buffer outputs are rail-to-rail with decent rise/fall time.
- Be careful with the initial conditions. You would need to set initial conditions for some of the oscillation nodes and the capacitor in the loop filter. Be careful with the phase of the input signal as well.
- Run transient simulations with long enough duration so that the loop reaches steady state.

**a)** Report your schematic details (schematic and size), including any inverter or buffer you insert. Explain your design considerations.
**b)** How long does it take for the loop to reach steady state? How do you measure it?
**c)** Plot $V_{ctrl}$ from $t$=0 to steady state. With the same scale in time, plot all 8 oscillation waveforms into one figure (on the same row). Mark important data points and explain.
**d)** Plot the waveform of $V_{ctrl}$ for 2 oscillation periods when the loop reaches the steady state. Comment on the waveform.
**e)** Plot all 8 oscillation waveforms into one figure (on the same row) for 2 periods in steady state. How are the results different from VCO-only simulations and why?

Are all the oscillation amplitudes the same? Why or why not? Measure the phase difference and explain why (or why not) all 8 phases are evenly separated.

**f)** What is the expected static phase error between the two oscillation signals (from hand-calculation)?

**g)** Plot the waveforms for the oscillation node that goes into the buffer, and the two inputs that go into the phase detector for 2 oscillation periods after the loop reaches the steady state. Mark and measure the static phase error between 1) the reference input and that oscillation node, and 2) the two inputs that go into the phase detector. How are these two results different? Why? Which one corresponds to the static phase error from hand-calculation?