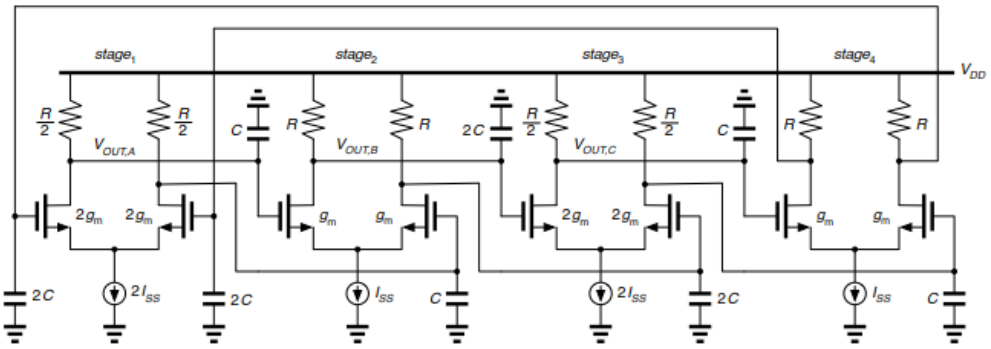
1.

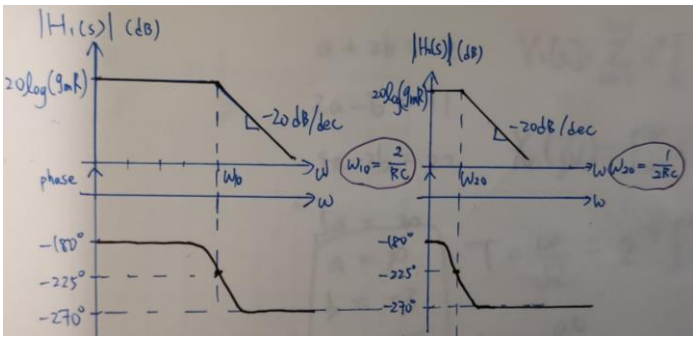
1) Neglect other capacitances. In the following circuit, stage$_1$ and stage$_3$ are twice "wider" than stage$_2$ and stage$_4$. Therefore, compared to stage$_{24}$, a) the differential pairs of stage$_{13}$ exhibit twice larger g_m, b) the load resistance is twice smaller, c) the input capacitance is twice larger (as shown in the figure), and d) the tail current is twice larger.



1a) Plot the small-signal transfer functions (Bode plot – both magnitude and phase) for stage$_1$ and stage$_2$. Indicate the low-frequency values (both magnitude and phase) and the locations of poles.

a. stage1: $H_1(s) = \frac{-(2g_m)(R/2)}{1+s(R/2)(C)} = \frac{-g_mR}{1+s/\omega_{10}}, \omega_{10} = \frac{2}{RC}$

stage2: $H_2(s) = \frac{-(g_m)(R)}{1+s(R)(2C)} = \frac{-g_mR}{1+s/\omega_{20}}, \omega_{20} = \frac{1}{2RC}$



1b) Determine the minimum required low-frequency gain per stage that guarante oscillation.

b. $H(s) = \left(\frac{-g_mR}{1+\frac{s}{0.5RC}}\right)\left(\frac{-g_mR}{1+\frac{s}{2RC}}\right)\left(\frac{-g_mR}{1+\frac{s}{0.5RC}}\right)\left(\frac{g_mR}{1+\frac{s}{2RC}}\right) = -(g_mR)^4\left(\frac{1}{1+\frac{s}{0.5RC}}\right)^2\left(\frac{1}{1+\frac{s}{2RC}}\right)^2$

$\angle H(\omega_{OSC})_{open} = -180° \times 5 - 2\,\text{atan}\left(\frac{RC}{2\omega_{OSC}}\right) - 2\,\text{atan}\left(\frac{2RC}{\omega_{OSC}}\right) = 0°$

$\Rightarrow \text{atan}\left(\frac{RC}{2\omega_{OSC}}\right) + \text{atan}\left(\frac{2RC}{\omega_{OSC}}\right) = 90° \Rightarrow \omega_{OSC} = \frac{1}{RC}$

$|H(\omega_{OSC})| = (g_mR)^4\left(\sqrt{1+2^2}\right)^{-2}\left(\sqrt{1+0.5^2}\right)^{-2} = \frac{4}{25}(g_mR)^4 = 1$

$\Rightarrow g_mR = 1.58$

1c) Calculate the oscillation frequency in terms of *R* and *C*. How much additional phase shift do stage$_1$ and stage$_2$ contribute at the oscillation frequency?

c. Oscillation frequency (ω_{OSC}) is $1/RC$.

Additional phase shift of stage1 is $\text{atan}\left(\frac{RC}{2\omega_{OSC}}\right) = 26.56°$

Additional phase shift of stage2 is $\text{atan}\left(\frac{2RC}{\omega_{OSC}}\right) = 63.44°$

1d) If the circuit is at the edge of oscillation (the swings are quite small), and the oscillation swing of $V_{OUT,A}$ is "A_0", what is the oscillation swing of $V_{OUT,B}$?

d. $V_{OUT,A} = A_0 \rightarrow V_{OUT,B} = A_0|H_2(\omega_{OSC})| = A_0\left(\frac{g_m R}{\sqrt{1+0.5^2}}\right) = 0.89A_0 g_m R$

2.

Following the previous question, use **HSpice** to design the ring oscillator with the following specifications and conduct the necessary simulations.
V_{DD}=1.8 V and common-mode of of 1.0 V for all the oscillation signals. Use ideal current sources of 500 μA for I_{SS}, (and 1 mA for 2×I_{SS}). Design the oscillator with an operating frequency of 2 GHz (by adding proper values of *C* and 2*C*).

2a) Design each stage with the low-frequency gain of 6 times the value calculated in **1b)**. Report the capacitance added and the transistor sizes used. Plot ac response (Bode plot – both magnitude and phase) for stage$_1$ and stage$_2$. Indicate the low-frequency values (both magnitude and phase) and the locations of poles.

a. We know that $I_{SS} = 500\mu A = 2I_{d2}$ and $V_{out,CM} = 1V$, then we can get

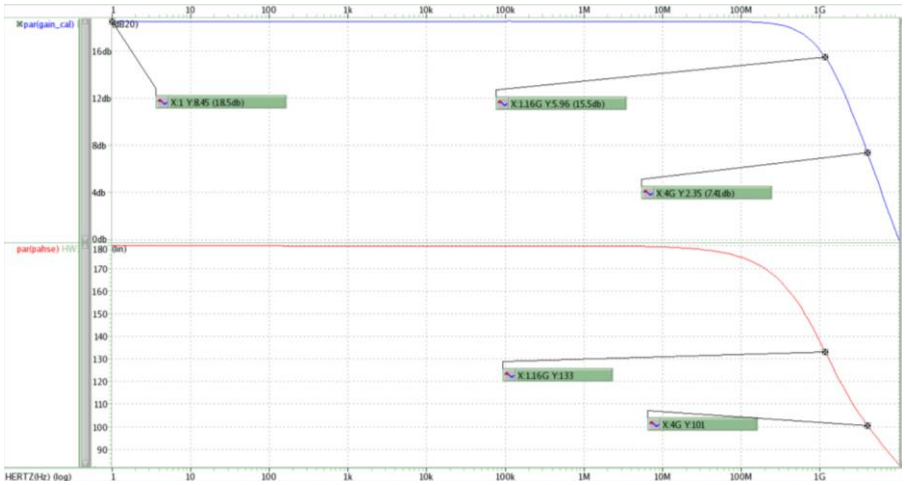
$R = \frac{V_{dd} - V_{out,CM}}{I_{d2}} = 3200\ \Omega$

Bandwidth = 2GHz, $RC = \frac{1}{2\pi f} = \frac{1}{2\pi(2G)} = 7.96 \times 10^{-11} \Rightarrow C = 24.9fF$

- Specification

Element	Value
Stage 1 (M11, M12, M31, M32)	$(80\mu m/0.18\mu m)$
Stage 2 (M21, M22, M41, M42)	$(40\mu m/0.18\mu m)$
R	3200 Ω
C	24.9 fF
I_{SS}	500 μA
Gain of each stage	8.45 (18.5dB)
Input Common-mode	1 V
V_{out}	1 V

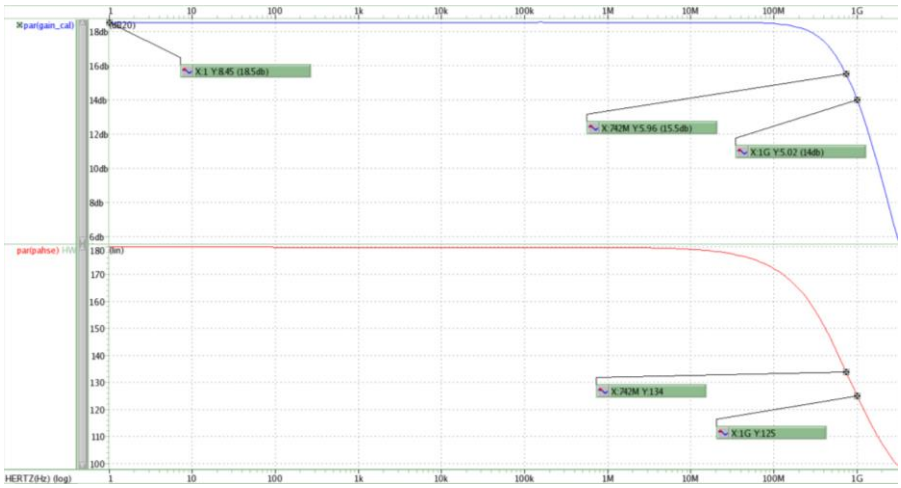
- Stage 1



poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-7.22929g	0.	-1.15058g	0.
-17.3299g	1.60159g	-2.75814g	254.902x
-17.3299g	-1.60159g	-2.75814g	-254.902x

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-14.7876g	0.	-2.35352g	0.
-19.3126g	0.	-3.07370g	0.
66.0360g	0.	10.5100g	0.

- Stage 2



poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-4.63966g	0.	-738.424x	0.
-4.85906g	0.	-773.344x	0.
-35.4780g	0.	-5.64649g	0.

zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-4.85297g	0.	-772.374x	0.
-32.1782g	0.	-5.12132g	0.
75.0592g	0.	11.9460g	0.

- It’s hard to get the 6 times value of minimum required low-frequency gain, so the gain per stage that we designed is 8.45 (5.35x gain).
- For Stage 1, we expect that the -3dB gain would locate at 4GHz, and it shows up at 1.16GHz in the simulation. For Stage 2, we expect that the -3dB gain would locate at 1GHz, and it shows up at 742MHz in the simulation.
  - This is because we ignore the parasitic capacitance and channel-length modulation in calculation.

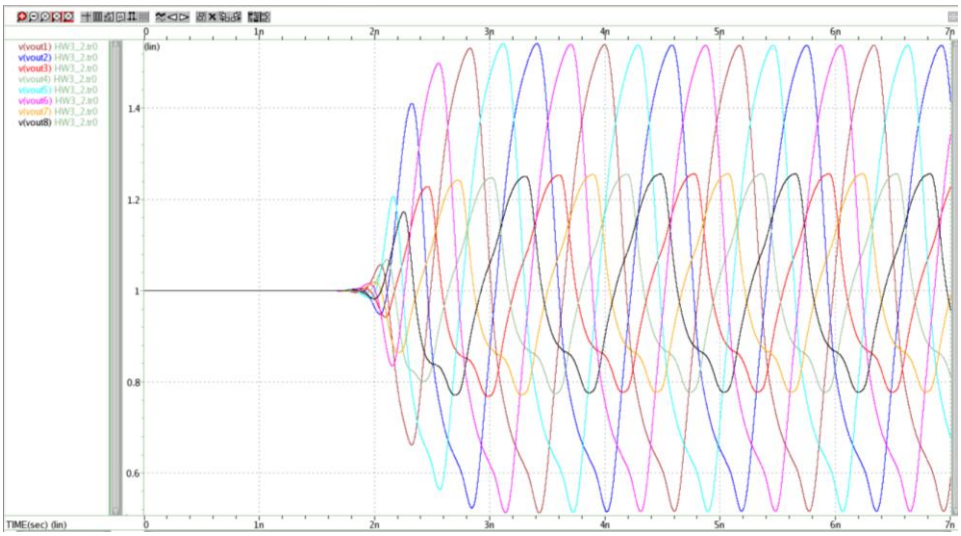
2b) Connect all four stages into a ring for oscillation. Perform transient simulations, and make sure that the waveforms settle. Use ".option accurate" in your simulation. Set the time step to less than 1 ps.

b. Use ".option DELMAX" to set the time step to less than 1 ps.

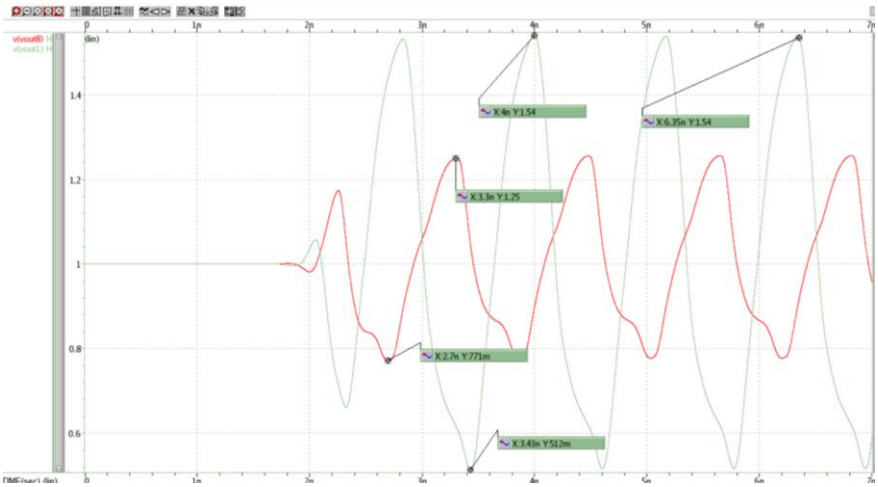
2c) Plot all 8 oscillation waveforms into one figure (on the same row) for at least 2 but no more than 3 periods in steady state. Mark the oscillation amplitudes of stage1 and stage2. Measure the additional phase shift stage1 and stage2 contribute.

c. Simulation

- All 8 oscillation waveforms



- Stage 1



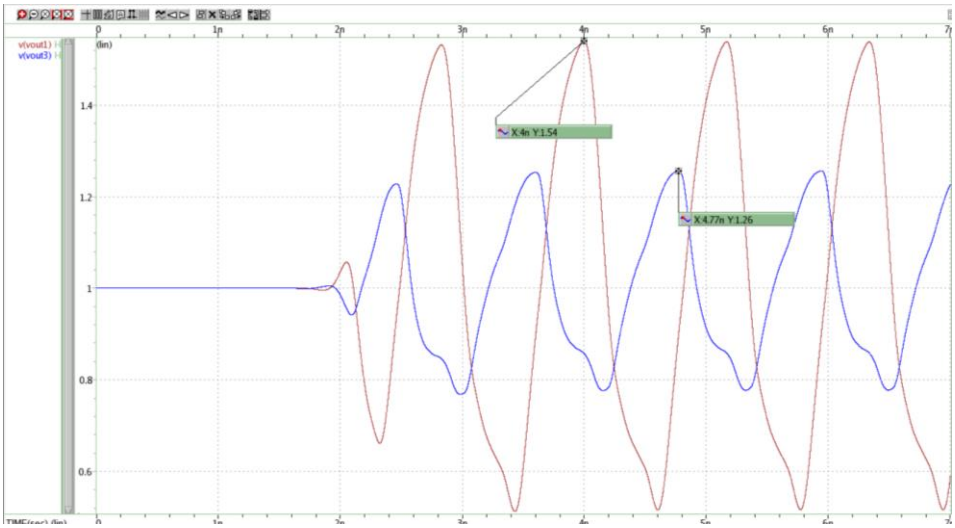
- Input: vout8, Output: vout1
- Amplitude of stage 1 (|vout1|): 540 mV
- Period of each signal = (6.35n – 4n)/2 = 1.175n

  total phase shift = $\frac{\Delta t}{T} \times 360° = \frac{4n-3.3n}{1.175n} \times 360° = 214.47°$

- Additional phase shift = 180° - total phase shift in one period

  Then, we can get the additional phase shift is $34.47°$.

- Stage 2



  - Input: vout1, Output: vout3
  - Amplitude of stage 2 (|vout3|): 255 mV
  - Period of each signal = 1.175n

    total phase shift = $\frac{\Delta t}{T} \times 360° = \frac{4.77n-4n}{1.175n} \times 360° = 235.91°$

  - Additional phase shift = 180° - total phase shift in one period

    Then, we can get the additional phase shift is $55.91°$.

2d) Comment (with concrete arguments) on any difference between the simulation results and the prediction from analysis (from previous questions).

d. Comment

- Hand-calculation

  Additional phase shift of stage1 is $26.56°$

  Additional phase shift of stage2 is $63.44°$
- Simulation

  Additional phase shift of stage1 is $34.47°$

  Additional phase shift of stage2 is $55.91°$
- Comment
  - The simulated values of -3dB gain both in stage 1 and stage 2 are lower than the expected values. This is because we ignore the parasitic capacitance and channel-length modulation in calculation.
  - Due to ignoring the parasitic capacitance and channel-length modulation in calculation, we got the larger values of additional phase shift in each stage in the simulation.

3.

3) Design a VCO based on the previous question. But this time, make all stages the same (instead of stage1 and stage3 twice "wider" than stage2 and stage4).

- Use the same size for all stages.
- Change the load resistors using PMOS transistors that operate in triode region.
- Use ideal current sources of 500 µA for I_{SS}.
- Design the oscillator so that with a control voltage of 0.6 V, the operating frequency is **300 MHz**, and the common mode is 1.4 V for all the oscillation signals. You may need to add additional capacitors for *C*.
- Size the NMOS transistors large enough so that the oscillation amplitude is large and the tail current steers fully when oscillating.

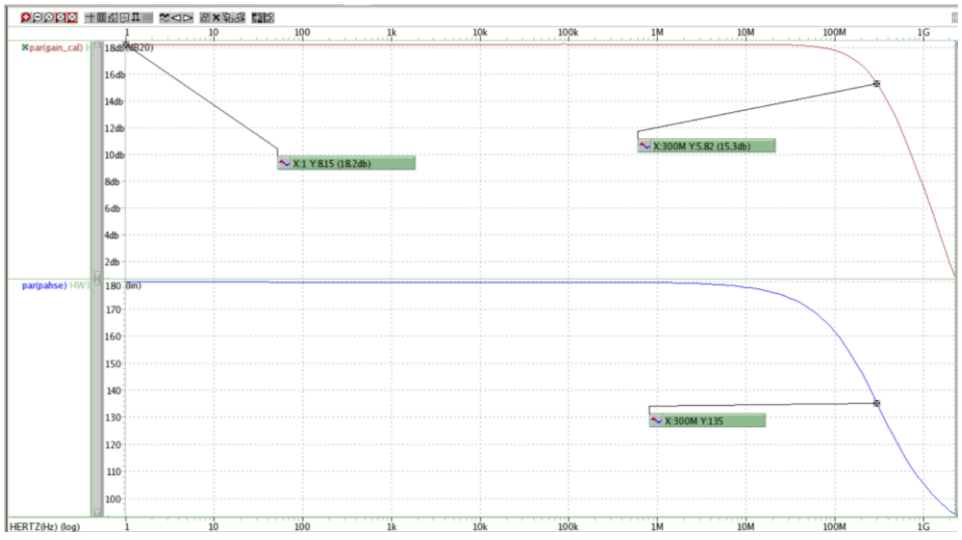
3a) Report the transistor sizes (both NMOS and PMOS) and the capacitor size.

a.

- Specification

Element	Value
Stage NMOS (M11n, M12n)	$(50\mu m/0.18\mu m)$
Stage PMOS (M11p, M12p)	$(3.4\mu m/0.18\mu m)$
C	200 fF
I_{SS}	500 µA
Gain of each stage	8.15 (18.5dB)
Frequency of -3dB Gain	300 MHz
Input Common-mode	1.4 V
Output Common-mode	1.398 V

- Waveview of each stage



- Pole-Zero

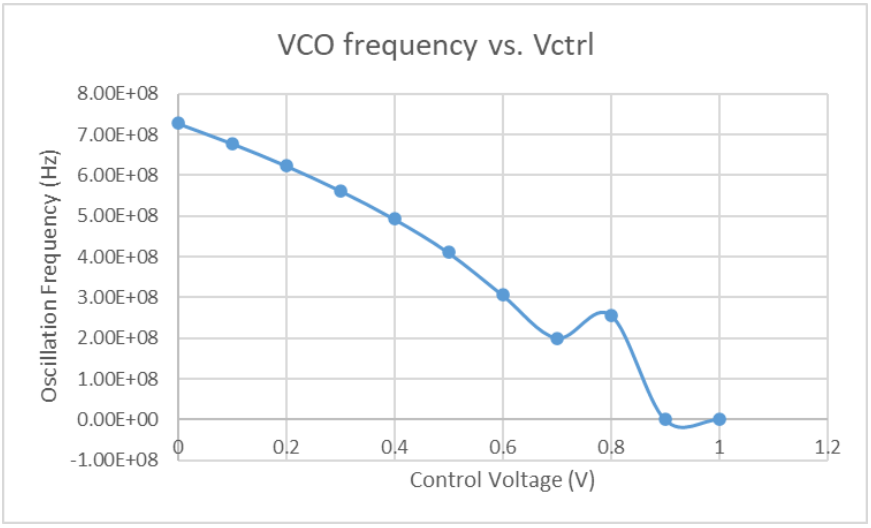
```
      poles (rad/sec)                poles ( hertz)
real              imag          real              imag
-1.54293g         0.            -245.564x         0.
-1.92607g         0.            -306.544x         0.
-37.4695g         0.            -5.96346g         0.

      zeros (rad/sec)                zeros ( hertz)
real              imag          real              imag
-1.54624g         0.            -246.091x         0.
-32.9394g         0.            -5.24247g         0.
70.4263g          0.            11.2087g          0.
```

3b) Plot VCO frequency vs. V_{ctrl} (for V_{ctrl} from 0 V to 1.0 V with step of 0.1 V). What is the V_{ctrl} value for 500 MHz? Estimate the VCO gain (K_{VCO}) at frequency of **500 MHz**.

b. VCO frequency vs. Vctrl

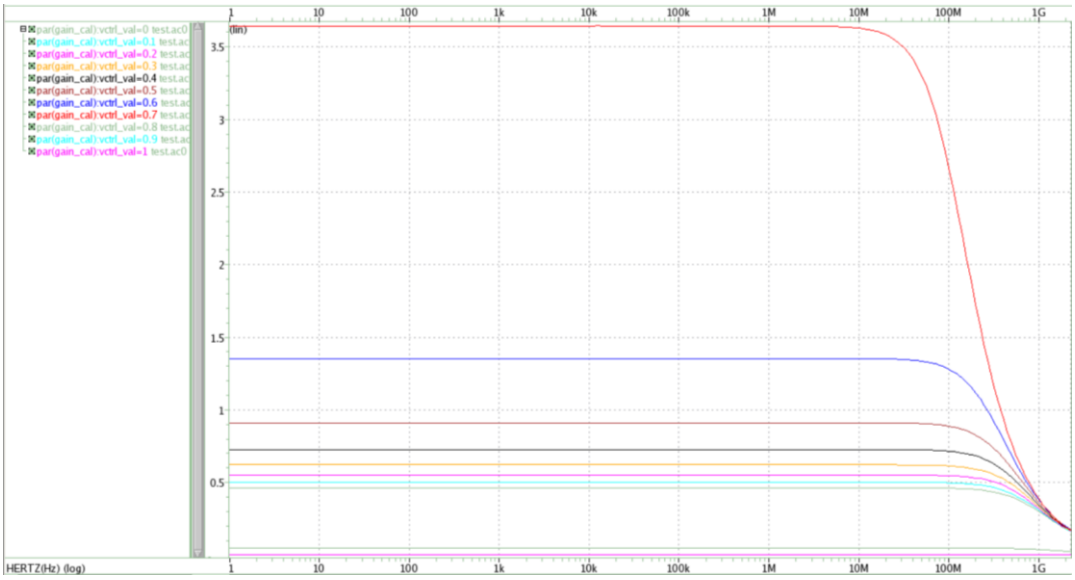
Vctrl_val	gain	gain (dB)	gain-3dB
0	3.4328	10.7131	7.28E+08
0.1	3.6819	11.3214	6.78E+08
0.2	4.0031	12.0479	6.24E+08
0.3	4.4367	12.9412	5.62E+08
0.4	5.0631	14.0884	4.93E+08
0.5	6.0764	15.673	4.10E+08
0.6	8.1461	18.219	3.06E+08
0.7	12.0564	21.6244	2.00E+08
0.8	6.78E-03	62.1989	2.57E+08
0.9	5.76E-03	231.7843	1.4125
1	6.35E-03	230.9334	1.4125

- VCO frequency vs. Vctrl



  - We can estimate the VCO gain at frequency 500 MHz is 0.37 V.

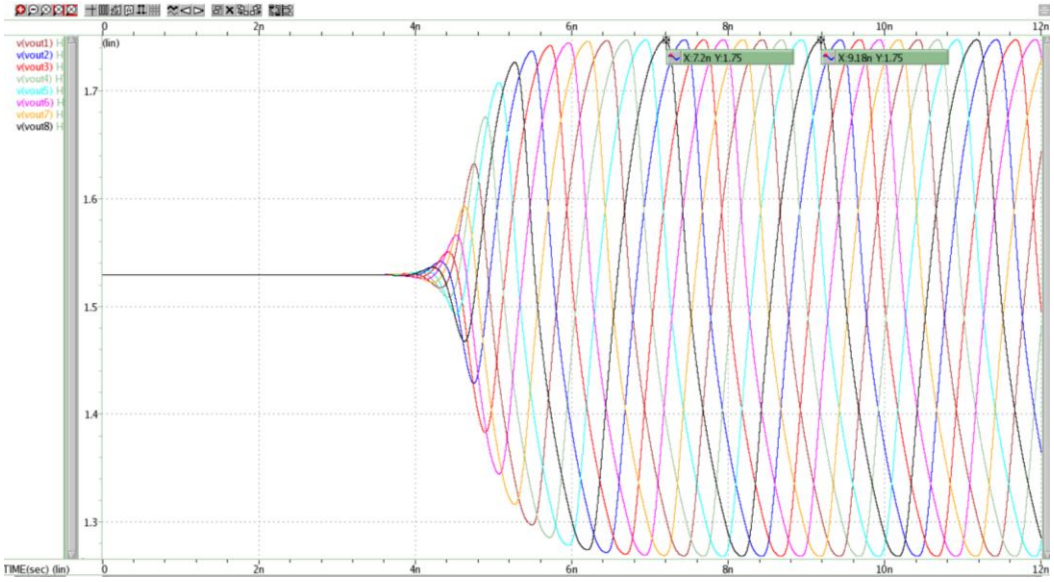
- AC response vs. Vctrl



3c) Plot all 8 oscillation waveforms (at 500 MHz) into one figure (on the same row) for at least 2 but no more than 3 periods in steady state. Measure the phase difference between stage4 and stage1, as well as between stage1 and stage2.

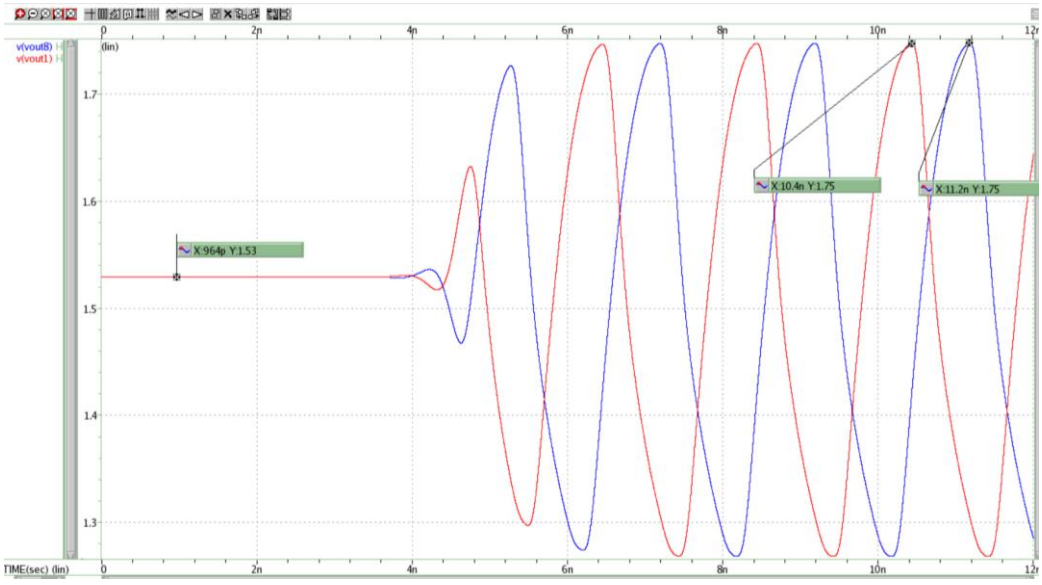
c. Simulation

- All 8 oscillation waveforms



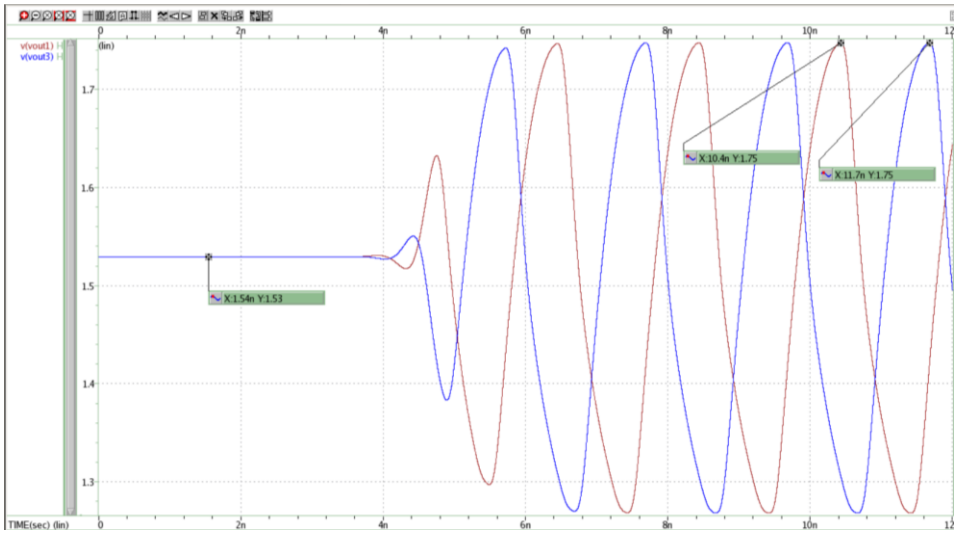
  - $V_{ctrl} = 0.37\ V$
  - Operating frequency = 1/(9.18n-7.2n) = 505 MHz

- Stage 4 (input) and Stage 1 (output)



  - Input: vout8, Output: vout1
  - Amplitude: 22 mV (1.75mV – 1.53mV)
  - Period of each signal = 505 MHz
    total phase shift = $\Delta t \times f \times 360° = 219.98°$
  - Additional phase shift = 180° - total phase shift in one period
    Then, we can get the additional phase shift is $39.98°$.

- Stage 1 (input) and Stage 2 (output)



  - Input: vout1, Output: vout3
  - Amplitude: 255 mV
  - Frequency of each signal = 505 MHz
    total phase shift = $\Delta t \times f \times 360° = 236.34°$
  - Additional phase shift = 180° - total phase shift in one period
    Then, we can get the additional phase shift is $56.34°$.
- Comment
  - Changing the value of Wn doesn't affect the value of output common mode.
  - This design doesn't work when control voltage (Vctrl) larger than 0.8 V.