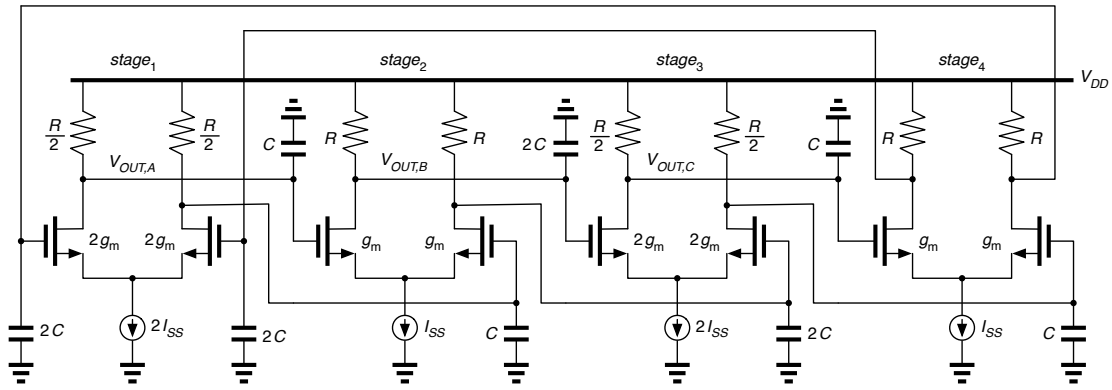
EE4280 Analog Integrated Circuits Analysis and Design II **2020 Spring**

Homework II – due date: 05/22 (Friday) 10AM **(No late homework!!!)**

- Please submit your report with the correct file name (HW3_105061703.pdf or HW3_105061703.doc) to our course website (iLMS system) by the deadline. No hardcopy will be accepted this time.
- Please replace 105061703 with your own student ID.
- Use cic018.l for simulations. Do not change any of the model parameters.

1) Neglect other capacitances. In the following circuit, stage_1 and stage_3 are twice "wider" than stage_2 and stage_4. Therefore, compared to stage_{24}, a) the differential pairs of stage_{13} exhibit twice larger g_m, b) the load resistance is twice smaller, c) the input capacitance is twice larger (as shown in the figure), and d) the tail current is twice larger.



1a) Plot the small-signal transfer functions (Bode plot – both magnitude and phase) for stage_1 and stage_2. Indicate the low-frequency values (both magnitude and phase) and the locations of poles.

1b) Determine the minimum required low-frequency gain per stage that guarantees oscillation.

1c) Calculate the oscillation frequency in terms of R and C. How much additional phase shift do stage_1 and stage_2 contribute at the oscillation frequency?

1d) If the circuit is at the edge of oscillation (the swings are quite small), and the oscillation swing of $V_{OUT,A}$ is "A_0", what is the oscillation swing of $V_{OUT,B}$?

2) Following the previous question, use **HSpice** to design the ring oscillator with the following specifications and conduct the necessary simulations.
V_{DD}=1.8 V and common-mode of of 1.0 V for all the oscillation signals. Use ideal current sources of 500 μA for I_{SS}, (and 1 mA for $2\times I_{SS}$). Design the oscillator with an operating frequency of **1 GHz** (by adding proper values of C and $2C$).

2a) Design each stage with the low-frequency gain of **5 times** the value calculated in **1b)**. Report the capacitance added and the transistor sizes used. Plot ac response (Bode plot – both magnitude and phase) for stage_1 and stage_2. Indicate the low-frequency values (both magnitude and phase) and the locations of poles.

2b) Connect all four stages into a ring for oscillation. Perform transient simulations, and make sure that the waveforms settle. Use ".option accurate" in your simulation. Set the time step to less than 1 ps.

2c) Plot all 8 oscillation waveforms into one figure (on the same row) for at least 2 but no more than 3 periods in steady state. Mark the oscillation amplitudes of stage_1 and stage_2. Measure the additional phase shift stage_1 and stage_2 contribute.

2d) Comment (with concrete arguments) on any difference between the simulation results and the prediction from analysis (from previous questions).

3) Design a VCO based on the previous question. But this time, make all stages the same (instead of stage_1 and stage_3 twice "wider" than stage_2 and stage_4).

- Use the same size for all stages.
- Change the load resistors using PMOS transistors that operate in triode region.
- Use ideal current sources of 500 μA for I_{SS}.
- Design the oscillator so that with a control voltage of 0.6 V, the operating frequency is **300 MHz**, and the common mode is 1.4 V for all the oscillation signals. You may need to add additional capacitors for *C*.
- Size the NMOS transistors large enough so that the oscillation amplitude is large and the tail current steers fully when oscillating.

3a) Report the transistor sizes (both NMOS and PMOS) and the capacitor size.

3b) Plot VCO frequency vs. V_{ctrl} (for V_{ctrl} from 0 V to 1.0 V with step of 0.1 V). What is the V_{ctrl} value for 500 MHz? Estimate the VCO gain (K_{VCO}) at frequency of **500 MHz**.

3c) Plot all 8 oscillation waveforms (at 500 MHz) into one figure (on the same row) for at least 2 but no more than 3 periods in steady state. Measure the phase difference between stage_4 and stage_1, as well as between stage_1 and stage_2.