

* + - Output noise voltage$ =36.6×10^{-18} (V^{2}/Hz)$
		- Input-referred noise voltage$ =5.23×10^{-18} (V^{2}/Hz)$
		- Total output noise voltage$ =36.6n V\_{rms}^{2}$
		- Total input-referred noise voltage$ =5.23n V\_{rms}^{2}$
	1. integ(abs('0|noise(outnoise)'),1k,1g)
	2. Change the size of 𝑀1 from the width in question 1)-g to 30μm with step size of 2μm. Repeat the previous simulations with a sinusoidal input amplitude of 25mV at frequency of 1MHz. Plot the ratio between the power of the second harmonic to that of the fundamental vs. transistor width.



* 1. How is the result compared to that in question 1)-d? Explain the possible reasons for this discrepancy and elaborate your arguments.

In question 1)-d, we concluded that the ratio of harmonic distortion would be increased with increasing the transistor width in the condition that M1 is operating in Saturation region.

In this plot, we can find that the ratio would be decreased when the transistor width is larger than 20μm. This is because M1 is operating in the linear region when the transistor width is larger than 16μm, and the relationship between$ A\_{HD2} $&$ A\_{F} $would be more complex than before.

* 1. What is the simulated output noise voltage and input-referred noise (both in terms of $V^{2}/Hz$) voltage at low frequencies? What is the total output noise voltage and total input-referred noise voltage (both in terms of $V\_{rms}$) if a noise bandwidth of 1GHz is assumed?



* + - Output noise voltage$ =36.6×10^{-18} (V^{2}/Hz)$
		- Input-referred noise voltage$ =5.23×10^{-18} (V^{2}/Hz)$
		- Total output noise voltage$ =\sqrt{V\_{n,out}^{2}×1G}=0.1913m V\_{rms}$
		- Total input-referred noise voltage$ =\sqrt{V\_{n,in}^{2}×1G}=72.32μ V\_{rms}$
	1. Change the size of 𝑀1 from the width in question 1)-g to 30μm with step size of 2μm. Repeat the noise simulations and plot the total output noise voltage and total input-referred noise voltage (both in terms of $V\_{rms}$) vs. transistor width.



* 1. How is the result compared to that in question 1)-e? Explain the possible reasons for this discrepancy and elaborate your arguments.

$S\_{v,in}=4kTg\_{m1}^{-1}, g\_{m1}=μ\_{n}C\_{ox}\left(W/L\right)V\_{ov}=2I\_{D}/V\_{ov}, S\_{v,out}=S\_{v,in}A\_{v}^{2}$

* When$ \left(W/L\right)=(8μm/0.18μm)$
	+ hand-calculation:$ S\_{v,in}=4.65×10^{-18} (V^{2}/Hz), S\_{v,out}=44.63×10^{-18} (V^{2}/Hz)$, with$ A\_{v}=g\_{m}R\_{L}=3.1$
	+ Simulation: $ S\_{v,in}=5.23×10^{-18} (V^{2}/Hz), S\_{v,out}=36.6×10^{-18} (V^{2}/Hz)$, with$ A\_{v}=2.64$
* We can find that the results of both hand-calculation and simulation are quite similar When$ \left(W/L\right)=(8μm/0.18μm).$
	+ - By the equation of$ S\_{v,in}$, we can find that$ S\_{v,in} $increase with increasing the transistor width (since power consumption is constant also means that drain current is constant). And the result of simulation also meets this analysis.
		- By the equation of$ S\_{v,out}$, we can find that$ S\_{v,out} $increase with decreasing the transistor width. And the result of simulation also meets this analysis.
	1. Based on the results of the previous two question sets, what is the optimal size for 𝑀1 that gives the minimum THD+N ratio? Notice that the noise power should be calculated at output node in this case.

$$THD+N=\frac{\sum\_{n=2}^{\infty }harmonic powers+noise power}{fundamental power}≈\frac{second harmonic powers+noise power}{fundamental power}$$



The optimal size of M1 is $\left(W/L\right)=(8μm/0.18μm)$.