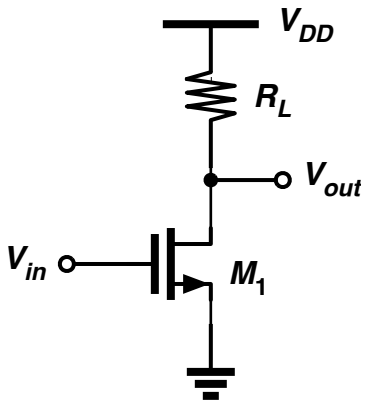
EE4280 Analog Integrated Circuits Analysis and Design II **2020 Spring**

Homework II – due date: 04/17 (Friday) 10AM **(No late homework!!!)**

- Please submit your report with the correct file name (HW2_105061703.pdf or HW2_105061703.doc) to our course website (iLMS system) by the deadline. No hardcopy will be accepted this time.
- Please replace 105061703 with your own student ID.
- Use cic018.l for simulations. Do not change any of the model parameters.

1) Consider a common-source amplifier like the following.



a. Assume the transistor operates in saturation. Express V_{out} as a function of V_{in}, and what is the small-signal voltage gain with $V_{in} = V_{in0}$?
b. What is the input-referred thermal noise voltage?
c. With a small input signal of $V_m \cos \omega t$, what are the amplitudes of the fundamental and the second harmonic at the output?
d. Keep the total power consumption the same, how does the harmonic distortion (which can be approximated as the ratio of the power of the second harmonic to that of the fundamental) change with the size of M_1?
e. Keep the total power consumption the same, how does the input-referred thermal noise voltage change with the size of M_1?

f. Use HSpice to design the common-source amplifier with the following specifications and conduct the necessary simulations.

$$V_{DD} = 1.8\ \text{V}, V_{in,DC} = 0.9\ \text{V}, V_{out,DC} = 0.9\ \text{V}, \text{and } I_{DC} = 1\ \text{mA}.$$

g. With minimum channel length, what are the size and the simulated overdrive voltage of M_1? What is the simulated small-signal voltage gain?
h. With dc analysis, plot the transfer function from V_{in} to V_{out} by changing V_{in} from 0 V to 1.8 V (with the step of 0.01 V).
i. What is the input voltage range that the small-signal voltage gain is within +/–10% of that at the operating point?

j. Why does the small-signal voltage gain decrease at the lower and upper bounds of this range?

k. Based on the analysis in question 1-c and the simulated over-drive voltage in question 1-g, at $V_{in,DC}$ of 0.9 V, if we feed the amplifier with a sinusoidal input signal of 25 mV, what is the expected ratio between the power of the second harmonic to that of the fundamental of output signal?

l. Feed the amplifier with a sinusoidal input signal. Set the amplitude to 25 mV and frequency to 1 MHz. With transient simulations for at least 500 periods, perform dft on the output waveform over a time period when the wave-form becomes steady (after at least 100 periods) and plot the result with y-axis in dB20 scale. Place markers at 1 MHz and 2 MHz.
Use ".option accurate" in your simulation. Set time step to less than 1 ns. Zoom in to [0 3] MHz for x-axis and [−150 0] dB for y-axis.

m. What is the simulated ratio between the power of the second harmonic to that of the fundamental?

n. How is this number compared to the prediction in question 1)-k? What are the possible reasons for this discrepancy?

o. Change the size of M_1 from the width in question 1)-g to 30 µm with step size of 2µm, Adjust $V_{in,DC}$ accordingly so that the power consumption stays constant. Repeat the previous simulations with a sinusoidal input amplitude of 25 mV at frequency of 1 MHz. Plot the ratio between the power of the second harmonic to that of the fundamental vs. transistor width.

p. How is the result compared to that in question 1)-d? Explain the possible reasons for this discrepancy and elaborate your arguments.

q. With the transistor size from question 1)-g, with noise analysis, what is the simulated output noise voltage and input-referred noise voltage (both in terms of V^2/Hz) at low frequencies? What is the total output noise voltage and total input-referred noise voltage (both in terms of V_{rms}) if a noise bandwidth of 1 GHz is assumed?

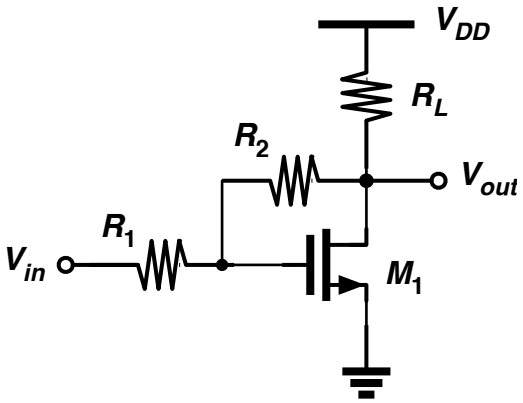
r. Change the size of M_1 from the size in question 1)-g to 30 µm with step size of 2µm, Adjust $V_{in,DC}$ accordingly so that the power consumption stays constant. Repeat the noise simulations and plot the total output noise voltage and total input-referred noise voltage (both in terms of V_{rms}) vs. transistor width.

s. How is the result compared to that in question 1)-e? Explain the possible reasons for this discrepancy and elaborate your arguments.

t. Based on the results of the previous two question sets, what is the optimal size for M_1 that gives the minimum THD+N ratio? Notice that the noise power should be calculated at output node in this case.

$$\text{THD} + \text{N} = \frac{\sum_{n=2}^{\infty} \text{harmonic powers} + \text{noise power}}{\text{fundamental power}} \approx \frac{\text{second harmonic power} + \text{noise power}}{\text{fundamental power}}$$

2) Consider a common-source amplifier placed in a negative feedback loop like the following.



a. With an input common-mode of of V_{in0} and feedback analysis, what are the "loop gain" and the "closed-loop gain" of the amplifier?
b. With a small input signal of $V_m \cos \omega t$, what are the amplitudes of the fundamental and the second harmonic at the output?
c. Compared to the results in question 1)-c (with the same input signal), how much improvement in linearity do we get from the negative feedback structure? What is the cost for this linearity improvement?

d. With loop gain $\gg 1$ and $R_2 = 10 \cdot R_1$, what is the small-signal closed-loop gain of the amplifier?

e. Use HSpice to simulate the circuit based on the same specifications as question 1)-f. Set R_1 and R_2 so that $R_2 = 10 \cdot R_1$ and $R_1 + R_2 > 10 \cdot R_L$.
f. With minimum channel length, what are the size and the simulated overdrive voltage of M_1? What are the values of R_1, R_2?
g. What is the simulated small-signal voltage gain? How is this number compared to that predicted in question 2-d? Explain the possible reasons for this discrepancy and elaborate your arguments.
h. Based on the simulated small-signal voltage gain of the CS amplifier with and without feedback (in question set 1), how much improvement in linearity (in terms of the ratio of the power of the second harmonic to that of the fundamental) would you expect if the same input signal is applied to the two amplifiers?

i. Feed the amplifier with a sinusoidal input signal. Set the amplitude to 25 mV and frequency to 1 MHz. With transient simulations for at least 500 periods, perform dft on the output waveform over a time period when the wave-

form becomes steady (after at least 100 periods) and plot the result with y-axis in dB20 scale. Place markers at 1 MHz and 2 MHz.
Use ".option accurate" in your simulation. Set time step to less than 1 ns. Zoom in to [0 3] MHz for x-axis and [−150 0] dB for y-axis.

j. What is the simulated ratio between the power of the second harmonic to that of the fundamental?
k. How is this result compared to that in question 2)-b? How is this improvement over a CS amplifier without feedback compared to that predicted in question 2)-h? What are the possible reasons for this discrepancy?