HSPICE® MOSFET Models Manual

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SYNOPSYS®

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HSPICE® MOSFET Models Manual, X-2005.09

Contents

About This Manual

This manual describes standard MOSFET models that you can use when simulating your circuit designs in HSPICE or HSPICE RF.

Inside This Manual

This manual contains the chapters described below. For descriptions of the other manuals in the HSPICE documentation set, see the next section, The HSPICE Documentation Set.

Chapter	Description
Chapter 1, Overview of MOSFET Models	Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.
Chapter 2, Technical Summary of MOSFET Models	Describes the technology used in all HSPICE MOSFET models.
Chapter 3, Common MOSFET Model Parameters	Lists and describes parameters that are common to several or all MOSFET model levels.
Chapter 4, Standard MOSFET Models: Level 1 to 40	Lists and describes standard MOSFET models (Levels 1 to 40).

Chapter	Description
Chapter 5, Standard MOSFET Models: Levels 50 to 64	Lists and describes standard MOSFET models (Levels 50 to 64).
Chapter 6, BSIM MOSFET Models: Levels 13 to 39	Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.
Chapter 7, BSIM MOSFET Models: Levels 47 to 65	Lists and describes seven of the newest BSIM-type MOSFET models supported by HSPICE.
Chapter 8, Customer Common Model Interface	Describes a Synopsys program interface you can use to add your own proprietary MOSFET models into the HSPICE or HSPICE RF simulator.
Appendix A, Finding Device Libraries	Describes how to use the HSPICE automatic model selector to find the proper model for each transistor size.
Appendix B, Comparing MOS Models	Compares and reviews the most commonly used MOSFET models.

The HSPICE Documentation Set

This manual is a part of the HSPICE documentation set, which includes the following manuals:

Manual	Description
HSPICE Simulation and Analysis User Guide	Describes how to use HSPICE to simulate and analyze your circuit designs. This is the main HSPICE user guide.
HSPICE Signal Integrity Guide	Describes how to use HSPICE to maintain signal integrity in your chip design.
HSPICE Applications Manual	Provides application examples and additional HSPICE user information.

Manual	Description
HSPICE Command Reference	Provides reference information for HSPICE commands.
HPSPICE Elements and Device Models Manual	Describes standard models you can use when simulating your circuit designs in HSPICE, including passive devices, diodes, JFET and MESFET devices, and BJT devices.
HPSPICE MOSFET Models Manual	Describes standard MOSFET models you can use when simulating your circuit designs in HSPICE.
HSPICE RF Manual	Describes a special set of analysis and design capabilities added to HSPICE to support RF and high-speed circuit design.
AvanWaves User Guide	Describes the AvanWaves tool, which you can use to display waveforms generated during HSPICE circuit design simulation.
HSPICE Quick Reference Guide	Provides key reference information for using HSPICE, including syntax and descriptions for commands, options, parameters, elements, and more.
HSPICE Device Models Quick Reference Guide	Provides key reference information for using HSPICE device models, including passive devices, diodes, JFET and MESFET devices, and BJT devices.

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Note: To use this feature, the HSPICE documentation files, the Index directory, and the index.pdx file must reside in the same directory. (This is the default installation for Synopsys documentation.) Also, Adobe Acrobat must be invoked as a standalone application rather than as a plug-in to your web browser.

Other Related Publications

For additional information about HSPICE, see:

- The HSPICE release notes, available on SolvNet (see Accessing SolvNet on page xvii)
- Documentation on the Web, which provides PDF documents and is available through SolvNet at http://solvnet.synopsys.com
- The Synopsys MediaDocs Shop, from which you can order printed copies of Synopsys documents, at http://mediadocs.synopsys.com

You might also want to refer to the documentation for the following related Synopsys products:

- CosmosScope
- Aurora
- Raphael
- VCS

Conventions

The following conventions are used in Synopsys documentation:

Convention	Description
`Courier`	Indicates command syntax.
`Italic`	Indicates a user-defined value, such as *`object_name`*.
`Bold`	Indicates user input—text you type verbatim—in syntax and examples.

Convention	Description
[ ]	Denotes optional parameters, such as `write_file [-f filename]`
`...`	Indicates that a parameter can be repeated as many times as necessary: `pin1 [pin2 ... pinN]`
|	Indicates a choice among alternatives, such as `low | medium | high`
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy.
Control-c	Indicates a keyboard combination, such as holding down the Control key and pressing c.

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Overview of MOSFET Models

Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.

A circuit netlist describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a netlist consists of a series of elements that define the individual components of the overall circuit. You can use your HSPICE-format netlist to help you verify, analyze, and debug your circuit design, before you turn that design into actual electronic circuitry.

Synopsys provides a series of standard models. Each model is like a template that defines various versions of each supported element type used in an HSPICE-format netlist. Individual elements in your netlist can refer to these standard models for their basic definitions. When you use these models, you can quickly and efficiently create a netlist and simulate your circuit design.

Referring to standard models in this way reduces the amount of time required to:

- Create the netlist.
- Simulate and debug your circuit design.
- Turn your circuit design into actual circuit hardware.

Within your netlist, each element that refers to a model is known as an *instance* of that model. When your netlist refers to predefined device models, you reduce

both the time required to create and simulate a netlist, and the risk of errors, compared to fully defining each element within your netlist.

One type of model that you can use as a template to define an element in your netlist is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. This manual describes the MOSFET models supplied for use with HSPICE.

A MOSFET device is defined by the MOSFET model and element parameters, and two submodels selected by the CAPOP and ACM model parameters.

- The CAPOP model parameter specifies the model for the MOSFET gate capacitances.
- The ACM (Area Calculation Method) parameter selects the type of diode model to use for the MOSFET bulk diodes.

Parameters in each submodel define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level, such as LEVEL 1 or LEVEL 50.

This manual describes:

- Design model and simulation aspects of MOSFET models.
- Parameters of each model level, and associated equations.
- Parameters and equations for MOSFET diode and MOSFET capacitor models.

Over the years, Synopsys has developed or adapted 64 different versions (or levels) of MOSFET models for use with HSPICE. Currently, Synopsys fully and officially supports 32 different MOSFET models.

The MOSFET models described in this manual are the most currently-developed and widely-used models. Synopsys has introduced LEVELs that are compatible with models developed by UC Berkeley, The University of Florida, Rensselaer Polytechnic Institute, and others.

This chapter describes:

Overview of MOSFET Model Types

Before you can select the appropriate MOSFET model type to use in analysis, you need to know the electrical parameters that are critical to your application. LEVEL 1 models are most often used to simulate large digital circuits in situations where detailed analog models are not needed. LEVEL 1 models offer low simulation time and a relatively high level of accuracy for timing calculations. If you need more precision (such as for analog data acquisition circuitry), use the more detailed models, such as the LEVEL 6 IDS model or one of the BSIM models (LEVEL 13, 28, 39, 47, 49, 53, 54, 57, 59, and 60).

For precision modeling of integrated circuits, the BSIM models consider the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

- Use the SOSFET model (LEVEL 27) to model silicon-on-sapphire MOS devices. You can include photocurrent effects at this level.
- Use LEVEL 5 and LEVEL 38 for depletion MOS devices.
- LEVEL 2 models consider bulk charge effects on current.
- LEVEL 3 models require less simulation time, provides as much accuracy as LEVEL 2, and have a greater tendency to converge.
- LEVEL 6 models are compatible with models originally developed using ASPEC. Use LEVEL 6 models to model ion-implanted devices.

Selecting Models

To describe a MOS transistor in your netlist, use both an element statement and a **.MODEL** statement.

The element statement defines the connectivity of the transistor and references the **.MODEL** statement. The **.MODEL** statement specifies either an n- or p-channel device, the level of the model, and several user-selectable model parameters.

Example

The following example specifies a PMOS MOSFET. PCH is a model reference name. The transistor is modeled using the LEVEL 13 BSIM model. Select the parameters from the MOSFET model parameter lists in this chapter.

```
M3 3 2 1 0 PCH <parameters>
   .MODEL PCH PMOS LEVEL=13 <parameters>
```

Selecting MOSFET Model LEVELs

MOSFET models consist of private client and public models that you select using the LEVEL parameter in the **.MODEL** statement. Synopsys frequently adds new models to the MOSFET device models.

Not all MOSFET models are available in the PC version. Table 1 shows what is available for PC users. The third column indicates models supported on all platforms, including PC. The last column lists models supported on all platforms except the PC.

Table 1 MOSFET Model Descriptions

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
1	Schichman-Hodges model	X	–
2	MOS2 Grove-Frohman model (SPICE 2G)	X	–
3	MOS3 empirical model (SPICE 2G)	X	–
4	Grove-Frohman: LEVEL 2 model derived from SPICE 2E.3	X	–
5	AMI-ASPEC depletion and enhancement (Taylor-Huang)	X	–
6	Lattin-Jenkins-Grove (ASPEC style parasitics)	X	–
7	Lattin-Jenkins-Grove (SPICE style parasitics)	X	–
8	advanced LEVEL 2 model	X	–

Table 1 MOSFET Model Descriptions (Continued)

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
9 **	AMD	–	X
10 **	AMD	–	X
11	Fluke-Mosaid model	–	X
12 **	CASMOS model (GTE style)	–	X
13	BSIM model	X	–
14 **	Siemens LEVEL=4	–	X
15	user-defined model based on LEVEL 3	–	X
16	not used	–	–
17	Cypress model	–	X
18 **	Sierra 1	–	X
19 ***	Dallas Semiconductor model	–	X
20 **	GE-CRD FRANZ	–	X
21 **	STC-ITT	–	X
22 **	CASMOS (GEC style)	–	X
23	Siliconix	–	X
24 **	GE-Intersil advanced	–	X
25 **	CASMOS (Rutherford)	–	X
26 **	Sierra 2	–	X
27	SOSFET	–	X
28	BSIM derivative; Synopsys proprietary model	X	–

Table 1 MOSFET Model Descriptions (Continued)

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
29 ***	not used	–	–
30 ***	VTI	–	X
31***	Motorola	–	X
32 ***	AMD	–	X
33 ***	National Semiconductor	–	X
34*	(EPFL) not used	–	X
35 **	Siemens	–	X
36 ***	Sharp	–	X
37 ***	TI	–	X
38	IDS: Cypress depletion model	–	X
39	BSIM2	X	–
41	TI Analog	X	–
46 ***	SGS-Thomson MOS LEVEL 3	–	X
47	BSIM3 Version 2.0	–	X
49	BSIM3 Version 3 (Enhanced)	X	–
50	Philips MOS9	X	–
53	BSIM3 Version 3 (Berkeley)	X	–
54	UC Berkeley BSIM4 Model	X	–
55	EPFL-EKV Model Ver 2.6, R 11	X	–
57	UC Berkeley BSIM3-SOI MOSFET Model Ver 2.0.1	X	–

Table 1 MOSFET Model Descriptions (Continued)

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
58	University of Florida SOI Model Ver 4.5 (Beta-98.4)	X	–
59	UC Berkeley BSIM3-501 FD Model	X	–
61	RPI a-Si TFT Model	X	–
62	RPI Poli-Si TFT Model	X	–
63	Philips MOS11 Model	X	–
64	STARC HiSIM Model	X	–

* not officially released
** equations are proprietary – documentation not provided
*** requires a license and equations are proprietary – documentation not provided

Selecting MOSFET Capacitors

CAPOP is the MOSFET capacitance model parameter. This parameter determines which capacitor models to use when modeling the MOS gate capacitance; that is, the gate-to-drain capacitance, the gate-to-source capacitance, and the gate-to-bulk capacitance. CAPOP selects a specific version of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Modified Meyer gate-capacitance model with parameters (general default)

Parameter	Description
CAPOP=3	Modified Meyer gate-capacitance model with parameters and Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model specialized (LEVEL 2)
CAPOP=12	Ward-Dutton model specialized (LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (Default for Levels 13, 28, and 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance Model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model (from among CAPOP=11, 12, or 13) for the specified DC model.

Table 2 CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12
13, 28, 39	13	13
others	2	11

LEVELs 49 and 53 use the Berkeley CAPMOD capacitance-model parameter. Proprietary models, and LEVELs 5, 17, 21, 22, 25, 27, 31, 33, 49, 53, 55, and 58, use built-in capacitance routines.

Selecting MOS Diodes

The ACM (Area Calculation Method) model parameter controls the geometry of the source and drain diffusions, and selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

Parameter	Description
ACM=0	SPICE model. Element areas determine the parameters.
ACM=1	ASPEC model. The element width determines the parameters.
ACM=2	Synopsys model, combination of ACM=0,1 with provisions for lightly-doped drain technology.
ACM=3	Extension of ACM=2 model that deals with stacked devices (shared source/drains) and source/drain periphery capacitance along the gate edge.

For more about ACM, see MOSFET Diode Models on page 39.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs that have width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length. These model parameters help the simulator to select the appropriate model for the specified width and length.

The automatic model selection program searches a data file for a MOSFET model where the width and length are within the range specified in the MOSFET element statement. Simulation then uses this model statement.

To search a data file for MOSFET models within a specified range of width and length:

1. Provide a root extension for the model reference name (in the **.MODEL** statement).
2. Use the model geometric range parameters (LMIN, LMAX, WMIN, and WMAX).

These model parameters define the range of physical length and width dimensions to which the MOSFET model applies.

Example 1

If the model reference name in the element statement is NCH, the model selection program examines the models with the same root model reference name (NCH), such as NCH.1, NCH.2 or NCH.A.

The model selection program selects the first MOSFET model statement whose geometric range parameters include the width and length specified in the associated MOSFET element statement.

Example 2

The following example shows how to call the MOSFET model selection program from a data file. The model selector program examines the **.MODEL** statements where the model reference names have the root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50.

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/selector.sp`

Setting MOSFET Control Options

Specific control options (set in the **.OPTION** statement) used for MOSFET models include the following. For flag options, 0 is unset (off) and 1 is set (on).

Option	Description
ASPEC	This option uses ASPEC MOSFET model defaults and set units. Default=0.
BYPASS	This option avoids recomputing nonlinear functions that do not change with iterations. Default=1.
MBYPAS	BYPASS tolerance multiplier (BYTOL = MBYPASSxVNTOL). Default=1 if DVDT=0, 1, 2, or as 3. Default=2 if DVDT=4.
DEFAD	Default drain diode area. Default=0.
DEFAS	Default source diode area. Default=0.
DEFL	Default channel length. Default=1e-4m.

Option	Description
DEFNRD	Default number of squares for drain resistor. Default=0.
DEFNRS	Default number of squares for source resistor. Default=0.
DEFPD	Default drain diode perimeter. Default=0.
DEFPS	Default source diode perimeter. Default=0.
DEFW	Default channel width. Default=1e-4m.
GMIN	Pn junction parallel transient conductance. Default=1e-12mho.
GMINDC	Pn junction parallel DC conductance. Default=1e-12mho.
SCALE	Element scaling factor. Default=1.
SCALM	Model scaling factor. Default=1.
WL	Reverses order in VSIZE MOS element from the default order (length-width) to width-length. Default=0.

- The AD element statement overrides the DEFAD default.
- The AS element statement overrides the DEFAS default.
- The L element statement overrides the DEFL default.
- The NRD element statement overrides the DEFNRD default.
- The NRS element statement overrides the DEFNRS default.
- The PD element statement overrides the DEFPD default.
- The PS element statement overrides the DEFPS default.
- The W element statement overrides the DEFW default.

Scaling Units

The SCALE and SCALM options control the units.

- SCALE scales element statement parameters.
- SCALM scales model statement parameters. It also affects the MOSFET gate capacitance and diode model parameters.

In this chapter, scaling applies only to parameters that you specify as scaled. If you specify SCALM as a parameter in a **.MODEL** statement, it overrides the SCALM option. In this way, you can use models with different SCALM values in the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

Table 3 Model Parameter Scaling

Parameter Units	Parameter Value
meter	multiplied by SCALM
$meter^2$	multiplied by $SCALM^2$
$meter^{-1}$	divided by SCALM
$meter^{-2}$	divided by $SCALM^2$

To override global model size scaling for individual MOSFET, diode, and BJT models that use the **.OPTION** SCALM=<*val*> statement, include SCALM=<*val*> in the **.MODEL** statement. **.OPTION** SCALM=<*val*> applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models. You cannot override SCALM in the model.

Scaling for LEVEL 25 and 33

When using the proprietary LEVEL 25 (Rutherford CASMOS) or LEVEL 33 (National) models, the SCALE and SCALM options are automatically set to 1e-6. However, if you use these models with other scalable models, you must explicitly set the SCALE=1e-6 and SCALM=1e-6 options.

Bypassing Latent Devices

Use the BYPASS (latency) option to decrease simulation time in large designs. To speed simulation time, this option does not recalculate currents, capacitances, and conductances, if the voltages at the terminal device nodes have not changed. The BYPASS option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use **.OPTION** BYPASS to set BYPASS.

BYPASS might reduce simulation accuracy for tightly-coupled circuits such as op-amps, high gain ring oscillators, and so on. Use **.OPTION** MBYPAS to set MBYPAS to a smaller value for more-accurate results.

General MOSFET Model Statement

You can use the **.MODEL** statement to include a MOSFET model in your HSPICE netlist. For a general description of the **.MODEL** statement, see the *HSPICE Command Reference*.

The following syntax is for all MOSFET model specifications. All related parameter levels are described in their respective sections.

Syntax

.MODEL *mname* [PMOS | NMOS] <ENCMODE=0 | 1>
+ (<LEVEL=*val*> <*keyname1*=*val1*> <*keyname2*=*val2*>…)
+ <VERSION=*version_number*>

or

.MODEL *mname* NMOS <ENCMODE=0 | 1>
+ (<LEVEL = *val*> <*keyname1*=*val1*> <*keyname2*=*val2*>…)
+ <VERSION=*version_number*> …)

Parameter	Description
mname	Model name. Elements refer to the model by this name.
PMOS	Identifies a p-channel MOSFET model.
NMOS	Identifies an n-channel MOSFET model.
ENCMODE	Applicable to BSIM4 (level 54) and BSIM3v3 (level 49 and 53), use to suppress warning messages originating in CMI code while inside encrypted code. Default is 0 (off). Set to off if this parameter is not present. This parameter cannot be overwritten through the instance line.
LEVEL	Use the LEVEL parameter to select from several MOSFET model types. Default=1.0.
VERSION	Specifies the version number of the model for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the **.MODEL** statement description for information about the effects of this parameter.

Example

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
   .MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
   .MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
   + VERSION=95.1
```

MOSFET Output Templates

Several MOSFET models produce an output template, consisting of a set of parameters that specify the output of state variables, stored charges, capacitances, parasitic diode current, and capacitor currents. Different MOSFET model levels support different subsets of these output parameters. Table 4 on page 14 lists all parameters in the MOSFET output templates, and indicates which model levels support each parameter.

Table 4 Parameters in MOSFET Output Templates

Name	Alias	Description	MOSFET Level
L	LV1	Channel Length (L) This is also the *effective* channel length for all MOSFET models except Level 54.	All
W	LV2	Channel Width (W) This is also the *effective* channel width for all MOSFET models except Level 54.	All
AD	LV3	Area of the drain diode (AD)	All
AS	LV4	Area of the source diode (AS)	All
ICVDS	LV5	Initial condition for the drain-source voltage (VDS)	All
ICVGS	LV6	Initial condition for the gate-source voltage (VGS)	All
ICVBS	LV7	Initial condition for the bulk-source voltage (VBS)	All except 57, 58, 59
ICVES	LV7	Initial condition for the substrate-source voltage (VES)	57, 58, 59

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
–	LV8	Device polarity: • 1 = forward • -1 = reverse (not used after HSPICE release 95.3).	All
VTH	LV9	Threshold voltage (bias dependent)	All
VDSAT	LV10	Saturation voltage (VDSAT)	All
PD	LV11	Drain diode periphery (PD)	All
PS	LV12	Source diode periphery (PS)	All
RDS	LV13	Drain resistance (squares) (RDS)	All
RSS	LV14	Source resistance (squares) (RSS)	All
XQC	LV15	Charge-sharing coefficient (XQC).	All
GDEFF	LV16	Effective drain conductance (1/RDeff), rgeoMod is not 0	All
GSEFF	LV17	Effective source conductance (1/RSeff), rgeoMod is not 0	All
CDSAT	LV18	Drain-bulk saturation current, at -1 volt bias.	All
CSSAT	LV19	Source-bulk saturation current, at -1 volt bias.	All
VDBEFF	LV20	Effective drain bulk voltage.	All
BETAEFF	LV21	BETA effective	All
GAMMAEFF	LV22	GAMMA effective	All
DELTAL	LV23	ΔL (MOS6 amount of channel length modulation)	1, 2, 3, 6
UBEFF	LV24	UB effective	1, 2, 3, 6

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
VG	LV25	VG drive	1, 2, 3, 6
VFBEFF	LV26	VFB effective.	All
–	LV31	Drain current tolerance (not used in HSPICE releases after 95.3).	All
IDSTOL	LV32	Source-diode current tolerance.	All
IDDTOL	LV33	Drain-diode current tolerance.	All
COVLGS	LV36	Gate-source overlap and fringing capacitances	All
COVLGD	LV37	Gate-drain overlap and fringing capacitances	All
COVLGB	LV38	Gate-bulk overlap capacitances	All except 57 and 59
COVLGE	LV38	Gate-substrate overlap capacitances	57, 59
VBS	LX1	Bulk-source voltage (VBS)	All except 57 and 59
VES	LX1	Substrate-source voltage (VES)	57, 59
VGS	LX2	Gate-source voltage (VGS)	All
VDS	LX3	Drain-source voltage (VDS)	All
CDO	LX4	Channel current (IDS)	All
CBSO	LX5	DC source-bulk diode current (CBSO)	All
CBDO	LX6	DC drain-bulk diode current (CBDO)	All
GMO	LX7	DC gate transconductance (GMO)	All
GDSO	LX8	DC drain-source conductance (GDSO)	All

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
GMBSO	LX9	DC substrate transconductance (GMBSO)	All except 57, 58, 59
GMESO	LX9	DC substrate transconductance (GMBSO/GMESO)	57, 58, 59
GBDO	LX10	Conductance of the drain diode (GBDO)	All
GBSO	LX11	Conductance of the source diode (GBSO)	All
QB	LX12	Total bulk (body) charge (QB)—Meyer and Charge Conservation	All
CQB	LX13	Bulk (body) charge current (CQB)—Meyer and Charge Conservation	All
QG	LX14	Total Gate charge (QG)—Meyer and Charge Conservation	All
CQG	LX15	Gate charge current (CQG)—Meyer and Charge Conservation	All
QD	LX16	Total Drain charge (QD)	49, 53
QD	LX16	Channel charge (QD)—Meyer and Charge Conservation	All except 49 and 53
CQD	LX17	Drain charge current (CQD)	49, 53
CQD	LX17	Channel charge current (CQD)—Meyer and Charge Conservation	All except 49 and 53
CGGBO	LX18	CGGBO = dQg/dVg = CGS + CGD + CGB - Meyer and Charge Conservation	All except 54, 57, 59, 60
CGGBO	LX18	Intrinsic gate capacitance	54, 57, 59, 60
CGDBO	LX19	CGDBO = -dQg/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60
CGDBO	LX19	Intrinsic gate-to-drain capacitance	54, 57, 59, 60

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CGSBO	LX20	CGSBO = -dQg/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60
CGSBO	LX20	Intrinsic gate-to-source capacitance	54, 57, 59, 60
CBGBO	LX21	CBGBO = -dQb/dVg - Meyer and Charge Conservation	All except 54, 57, 59, 60
CBGBO	LX21	Intrinsic bulk-to-gate capacitance	54
CBGBO	LX21	Intrinsic floating body-to-gate capacitance	57, 59, 60
CBDBO	LX22	CBDBO = -dQb/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60
CBDBO	LX22	Intrinsic bulk-to-drain capacitance	54
CBDBO	LX22	Intrinsic floating body-to-drain capacitance	57, 59, 60
CBSBO	LX23	CBSBO = -dQb/dVs - Meyer and Charge Conservation	All except 54, 57, 59, 60
CBSBO	LX23	Intrinsic bulk-to-source capacitance	54
CBSBO	LX23	Intrinsic floating body-to-source capacitance	57, 59, 60
QBD	LX24	Drain-bulk charge (QBD)	All
–	LX25	Drain-bulk charge current (CQBD), (not used in HSPICE releases after 95.3).	All
QBS	LX26	Source-bulk charge (QBS)	All
–	LX27	Source-bulk charge current (CQBS), (not used after HSPICE release 95.3).	All
CAP_BS	LX28	Bias dependent bulk-source capacitance	All except 57, 58

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CAP_BS	LX28	Extrinsic drain to substrate Capacitances—Meyer and Charge Conservation. `CAP_BS=csbox+csesw` • csbox is the substrate-to-source bottom capacitance • csesw is the substrate-to-source sidewall capacitance	57, 58
CAP_BD	LX29	Bias dependent bulk-drain capacitance	All except 57, 58
CAP_BD	LX29	Extrinsic source to substrate Capacitances—Meyer and Charge Conservation. `CAP_BD=cdbox+cdesw` • cdbox is the substrate-to-drain bottom capacitance • cdesw is the substrate-to-drain sidewall capacitance	57, 58
CQS	LX31	Channel-charge current (CQS).	All
CDGBO	LX32	CDGBO = -dQd/dVg - Meyer and Charge Conservation	All except 54, 57, 59, 60
CDGBO	LX32	Intrinsic drain-to-gate capacitance	54, 57, 59, 60
CDDBO	LX33	CDDBO = dQd/dVd - Meyer and Charge Conservation	All except 54, 57, 59, 60
CDDBO	LX33	Intrinsic drain capacitance	54, 57, 59, 60
CDSBO	LX34	CDSBO = -dQd/dVs Drain-to-source capacitance - Meyer and Charge Conservation	All

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
QE	LX35	Substrate charge (QE)—Meyer and Charge Conservation	57, 58, 59
CQE	LX36	Substrate charge current (CQE)—Meyer and Charge Conservation	57, 58, 59
CDEBO	LX37	CDEBO = -dQd/dVe intrinsic drain-to-substrate capacitance	57, 59
igso	LX38	Gate-to-Source Current	54
CBEBO	LX38	CBEBO = -dQb/dVe intrinsic floating body-to-substrate capacitance	57, 59
igdo	LX39	Gate-to-Drain Current	54
CEEBO	LX39	CEEBO = dQe/dVe intrinsic substrate capacitance	57, 59
CEGBO	LX40	CEGBO = -dQe/dVg intrinsic substrate-to-gate capacitance	57, 59
CEDBO	LX41	CEDBO = -dQe/dVd intrinsic substrate-to-drain capacitance	57, 59
CESBO	LX42	CESBO = -dQe/dVs intrinsic substrate-to-source capacitance	57, 59
VBSI	LX43	Body-source voltage (VBS)—Meyer and Charge Conservation	57, 58, 59
ICH	LX44	Channel current—Meyer and Charge Conservation	57, 58, 59
IBJT	LX45	Parasitic BJT collector current—Meyer and Charge Conservation	57, 58, 59
III	LX46	Impact ionization current—Meyer and Charge Conservation	57, 58, 59

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
IGIDL	LX47	GIDL current—Meyer and Charge Conservation	57, 58, 59
ITUN	LX48	Tunneling current—Meyer and Charge Conservation	57, 58, 59
Qbacko	LX49	Internal body charge	57, 59
Ibp	LX50	Body contact current	57, 59
Sft	LX51	Value of the temperature node with shmod=1	57, 59
VBFLOAT	LX52	Internal body node voltage, if you do not specify the terminal	57, 59
Rbp	LX53	Combination of rbody and rhalo	57, 59
IGB	LX54	Gate tunneling current	57, 59
QSRCO	LX55	Total Source charge (Charge Conservation: QS=-(QG+QD+QB))	49, 53, 57, 59
CQs	LX56	Source charge current	57, 59
CGEBO	LX57	CGEBO = -dQg/dVe intrinsic gate-to-substrate capacitance	57, 59
CSSBO	LX58	CSSBO = dQs/dVs intrinsic source capacitance	57, 59
CSGBO	LX59	CSGBO = -dQs/dVg intrinsic source-to-gate capacitance	57, 59
CSDBO	LX60	CSDBO = -dQs/dVd intrinsic source-to-drain capacitance	57, 59
CSEBO	LX61	CSEBO = -dQs/dVe intrinsic source-to-substrate capacitance	57, 59
weff	LX62	Effective channel width	54

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
leff	LX63	Effective channel length	54
weffcv	LX64	Effective channel width for CV	54
leffcv	LX65	Effective channel length for CV	54
igbo	LX66	Gate-to-Substrate Current (Igb = Igbacc + Igbinv)	54
igcso	LX67	Source Partition of Igc	54
igcdo	LX68	Drain Partition of Igc	54
iimi	LX69	Impact ionization current	54
igidlo	LX70	Gate-induced drain leakage current	54
igdt	LX71	Gate Dielectric Tunneling Current (Ig = Igs + Igd + Igcs + Igcd + Igb)	54
igc	LX72	Gate-to-Channel Current at zero Vds	54
igbacc	LX73	Determined by ECB (Electron tunneling from the Conduction Band); significant in the accumulation	54
igbinv	LX74	Determined by EVB (Electron tunneling from the Valence Band); significant in the inversion	54
vfbsd	LX75	Flat-band Voltage between the Gate and S/D diffusions	54
vgse	LX76	Effective Gate-to-Source Voltage	54
vox	LX77	Voltage Across Oxide	54
rdv	LX78	Asymmetric and Bias-Dependent Source Resistance, (rdsMod = 1)	54

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
rsv	LX79	Asymmetric and Bias-Dependent Drain Resistance, (rdsMod = 1)	54
cap_bsz	LX80	Zero voltage bias bulk-source capacitance	54
cap_bdz	LX81	Zero voltage bias bulk-drain capacitance	54
CGGBM	LX82	Total gate capacitance (including intrinsic), and all overlap and fringing components	54, 57, 59, 60
CGDBM	LX83	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60
CGSBM	LX84	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60
CDDBM	LX85	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance	54, 57, 59, 60
CDSBM	LX86	Total drain-to-source capacitance	54, 57, 60
CDGBM	LX87	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60
CBGBM	LX88	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components	54, 57, 59, 60
CBDBM	LX89	Total bulk-to-drain capacitance (including intrinsic), and junction capacitance	54
CBDBM	LX89	Total floating body-to-drain capacitance (including intrinsic), and junction capacitance.	57, 59, 60

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CBSBM	LX90	Total bulk-to-source capacitance (including intrinsic), and junction capacitance	54
CBSBM	LX90	Total floating body-to-source capacitance (including intrinsi)c, and junction capacitance.	57, 59, 60
CAPFG	LX91	Fringing capacitance	54
CDEBM	LX92	Total drain-to-substrate capacitance (including intrinsi)c, and junction capacitance.	57, 59, 60
CSGBM	LX93	Total source-to-gate capacitance (including intrinsic), and overlap and fringing components.	57, 59, 60
CSSBM	LX94	Total source capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60
CSEBM	LX95	Total source-to-substrate capacitance (including intrinsic), and junction capacitance.	57, 59, 60
CEEBM	LX96	Total substrate capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60
QGI	LX97	Intrinsic Gate charge	49, 53
QSI	LX98	Intrinsic Source charge	49, 53
QDI	LX99	Intrinsic Drain charge	49, 53
QBI	LX100	Intrinsic Bulk charge (Charge Conservation: QBI= -(QGI+ QSI+ QDI))	49, 53
CDDBI	LX101	Intrinsic drain capacitance	49, 53

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CBDBI	LX102	Intrinsic bulk-to-drain capacitance	49, 53
CBSBI	LX103	Intrinsic bulk-to-source capacitance	49, 53
VBDI	LX109	Body-drain voltage(VBD)—Meyer and Charge Conservation	57, 58, 59
IGISLO	LX110	Gate-induced source leakage current	54
GRII	LX118	Intrinsic channel reflected gate conductance	54
GRGELTD	LX119	Gate electrode conductance	54

2

Technical Summary of MOSFET Models

Describes the technology used in all HSPICE MOSFET models.

Nonplanar and Planar Technologies

Two MOSFET fabrication technologies have dominated integrated circuit design: nonplanar and planar technologies.

Nonplanar techonology.

Nonplanar technology uses metal gates. The simplicity of the process generally provides acceptable yields.

The primary problem with metal gates is metal breakage across the field oxide steps. Field oxide grows when oxidizing the silicon surface. When the surface is cut, it forms a sharp edge. Because metal is affixed to these edges to contact the diffusion or make a gate, thicker metal must be applied to compensate for the sharp edges. This metal tends to gather in the cuts, making etching difficult.

The inability to accurately control the metal width necessitates very conservative design rules and results in low transistor gains.

Planar techonology:

In planar technology, the oxide edges are smooth with a minimal variance in metal thickness. Shifting to nitride is accomplished using polysilicon gates.

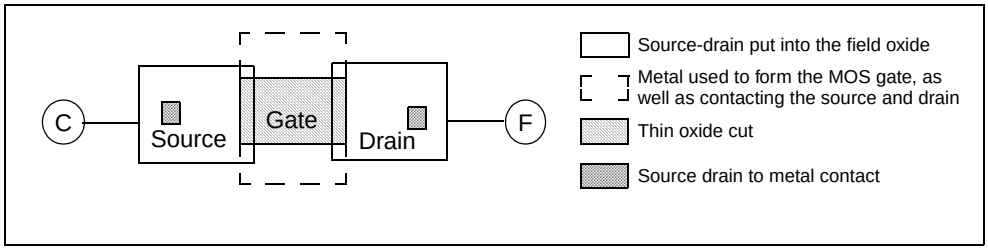
Adding a chemical reactor to the MOS fabrication process enables depositing silicon nitride, silicon oxide, and polysilicon. The ion implanter is the key element in this processing by using implanters with beam currents greater than 10 milliamperes.

Because implanters define threshold voltages, diffusions, and field thresholds, processes require a minimum number of high temperature oven steps. This enables low temperature processing and maskless pattern generation. The new wave processes are more similar to the older nonplanar metal gate technologies.

Field Effect Transistors

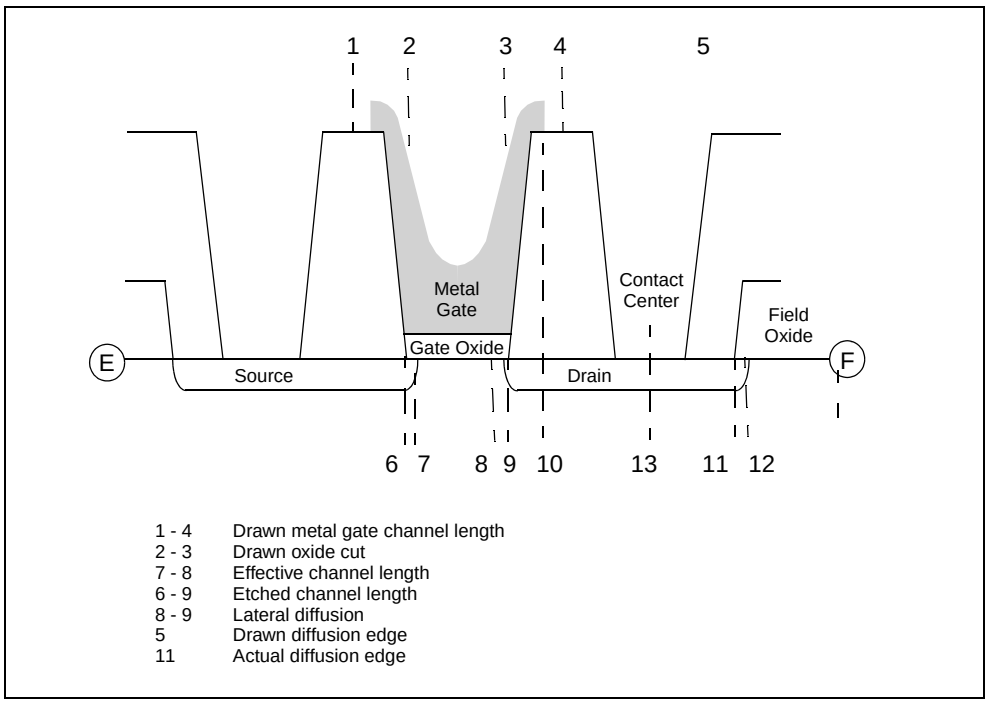
The metal gate MOSFET is nonisoplanar as shown in Figure 1 and Figure 2 on page 29.

Figure 1 Field Effect Transistor



Looking at the actual geometry, from source-to-drain, Figure 2 shows a perspective of the nonisoplanar MOSFET.

Figure 2 Field Effect Transistor Geometry



To visualize the construction of a silicon gate MOSFET, observe how a source or drain to field cuts (Figure 3.) Cut A-B shows a drain contact (Figure 4).

Figure 3 Isoplanar Silicon Gate Transistor

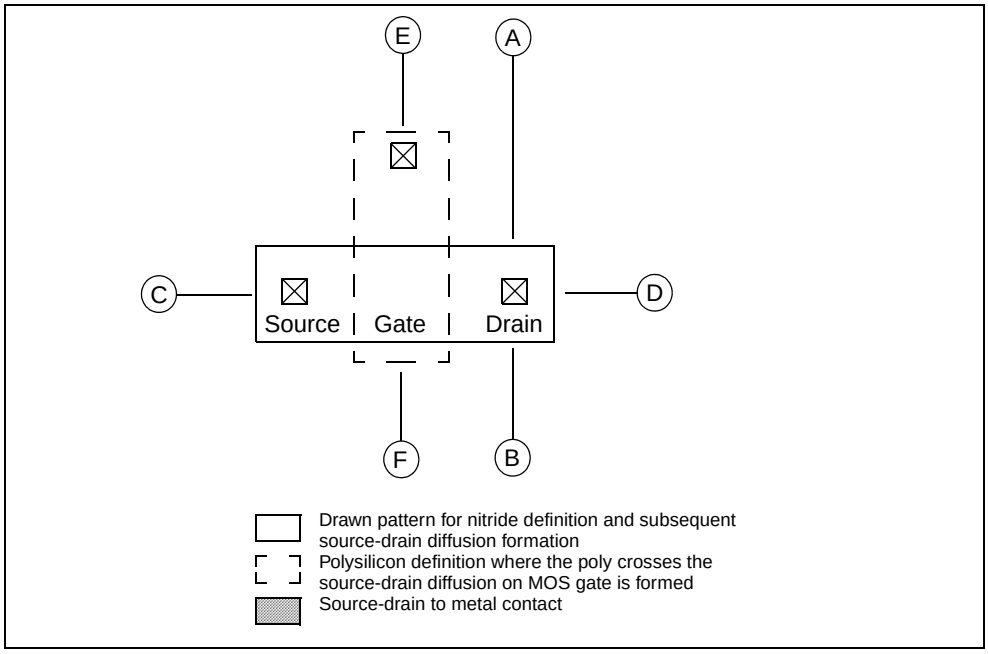
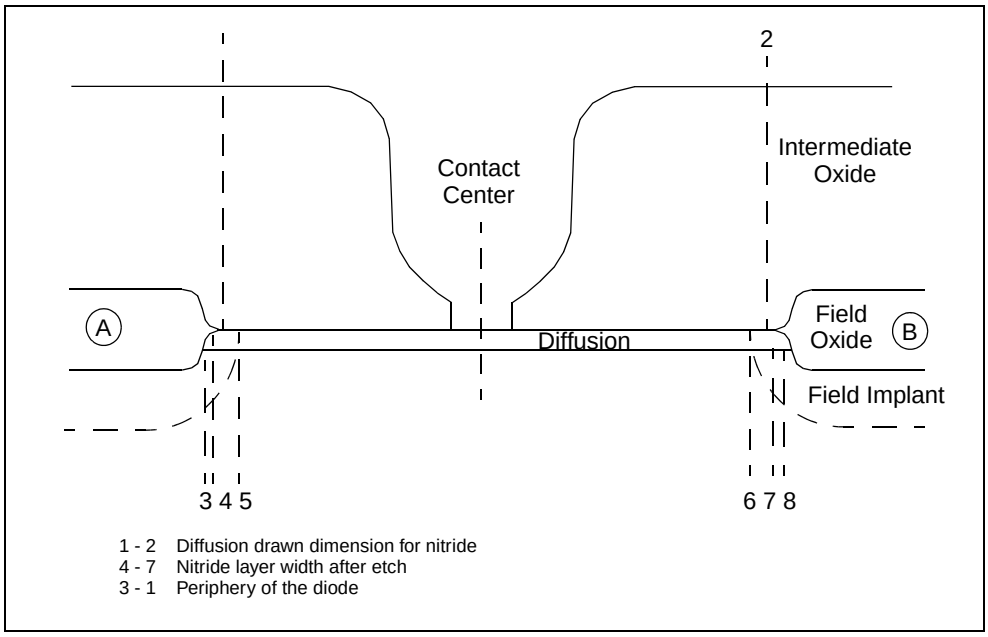
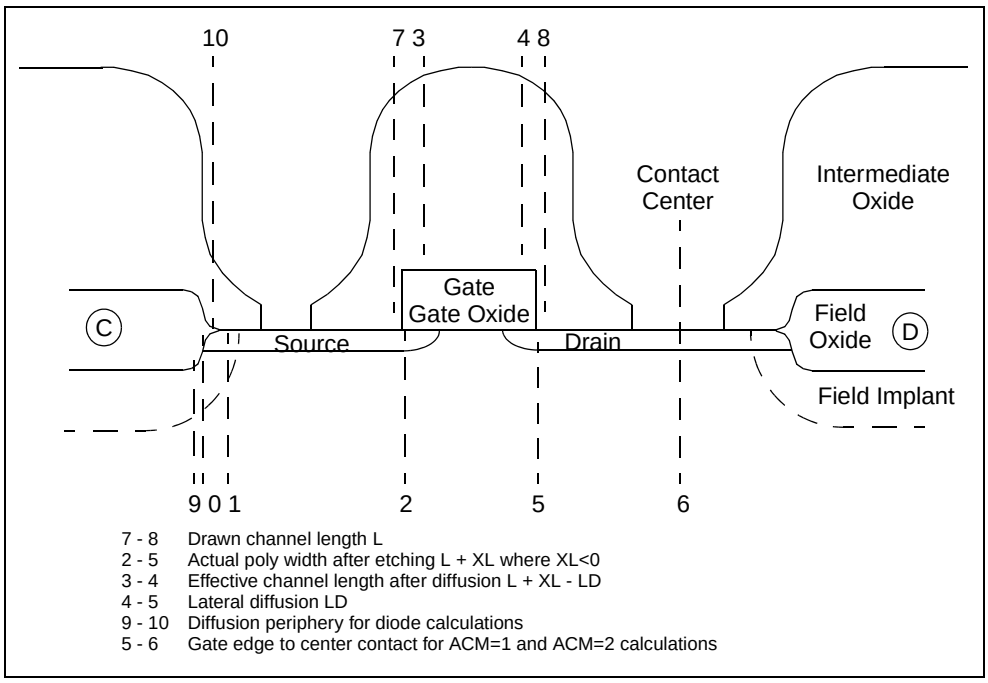


Figure 4 Isoplanar MOSFET Construction, Part A



CD represents the cut from the source to the drain (Figure 5 on page 31), and includes the contacts.

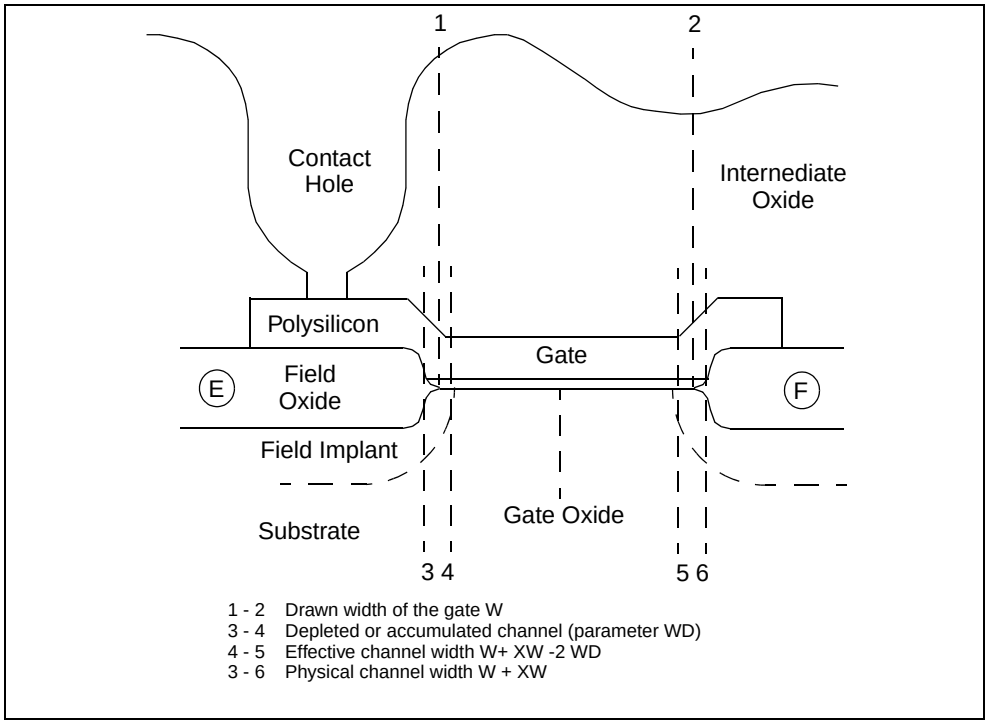
Figure 5 Isoplanar MOSFET Construction, Part B



The planar process produces parasitic capacitances at the poly to field edges of the device. The cut along the width of the device demonstrates the importance of these parasitics (Figure 6 on page 32).

The encroachment of the field implant into the channel narrows the channel width, and increases the gate to bulk parasitic capacitance.

Figure 6 Isoplanar MOSFET, Width Cut



MOSFET Equivalent Circuits

Equation Variables

This section lists the equation variables and constants.

Table 5 Equation Variables and Constants

Variable/ Quantity	Definition
cbd	Bulk-to-drain capacitance
cbs	Bulk-to-source capacitance
cbg	Gate-to-bulk capacitance
cgd	Gate-to-drain capacitance
cgs	Gate-to-source capacitance

Table 5 Equation Variables and Constants (Continued)

Variable/ Quantity	Definition
f	Frequency
gbd	Bulk-to-drain dynamic conductance
gbs	Bulk-to-source dynamic conductance
gds	Drain-to-source dynamic conductance (controlled by vds)
gdb	Drain-to-bulk impact ionization conductance
gm	Drain-to-source dynamic transconductance (controlled by vgs)
gmbs	Drain-to-source dynamic bulk transconductance (controlled by vsb)
ibd	Bulk-to-drain DC current
ibs	Bulk-to-source DC current
ids	Drain-to-source DC current
idb	Drain-to-bulk impact ionization current
ind	Drain-to-source equivalent noise circuit
inrd	Drain resistor equivalent noise circuit
inrs	Source resistor equivalent noise circuit
rd	Drain resistance
rs	Source resistance
vsb	Source-to-bulk voltage
vds	Drain-to-source voltage
vgs	Gate-to-source voltage
Δt	t-tnom
εsi	1.0359e-10F/m dielectric constant of silicon

Table 5 Equation Variables and Constants (Continued)

Variable/ Quantity	Definition
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	New temperature of model or element in °K
tnom	tnom = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C).
vt	k · t/q
vt(tnom)	k · tnom/q

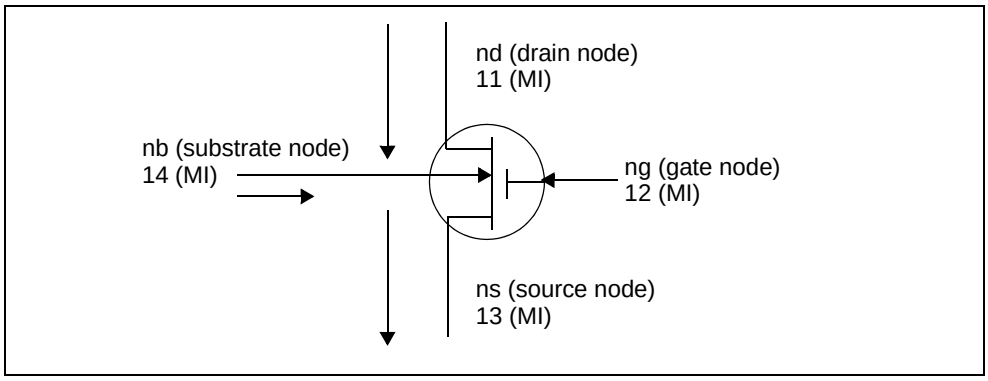
Using the MOSFET Current Convention

Figure 7 on page 34 shows the assumed direction of current flow through a MOS transistor. To print the drain current, use either I(M1) or I1(M1) syntax.

- I2 produces the gate current.
- I3 produces the source current.
- I4 produces the substrate current.

References to bulk are the same as references to the substrate.

Figure 7 MOSFET Current Convention, N-channel



Using MOSFET Equivalent Circuits

Simulators use three equivalent circuits to analyze MOSFETs:

- DC
- Transient
- AC and noise-equivalent circuits

The components of these circuits form the basis for all element and model equations. The equivalent circuit for DC sweep is the same as the one used for transient analysis, but excludes capacitances. Figure 8 through Figure 10 display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (ids). Noise and AC analyses do not use the actual ids current. Instead, the model uses the partial derivatives of ids with respect to the vgs, vds, and vbs terminal voltages.

The names for these partial derivatives are as follows.

Transconductance

$$gm = \frac{\partial(ids)}{\partial(vgs)}$$

Conductance

$$gds = \frac{\partial(ids)}{\partial(vds)}$$

Bulk Transconductance

$$gmbs = \frac{\partial(ids)}{\partial(vbs)}$$

The ids equation describes the basic DC effects of the MOSFET. Simulation considers the effects of gate capacitance, and of source and drain diodes, separately from the DC ids equations. Simulation also evaluates the impact ionization equations separately from the DC ids equation, even though the ionization effects are added to ids.

Figure 8 Equivalent Circuit, MOSFET Transient Analysis

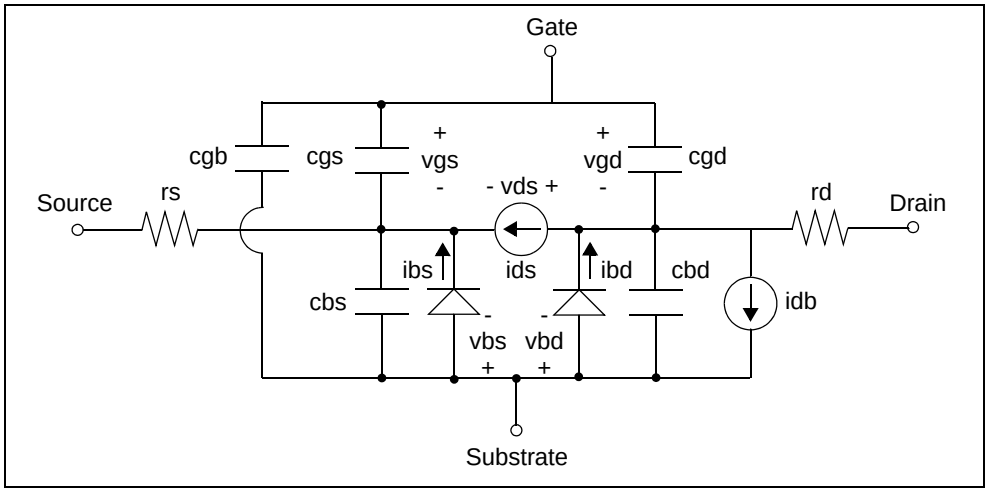


Figure 9 Equivalent Circuit, MOSFET AC Analysis

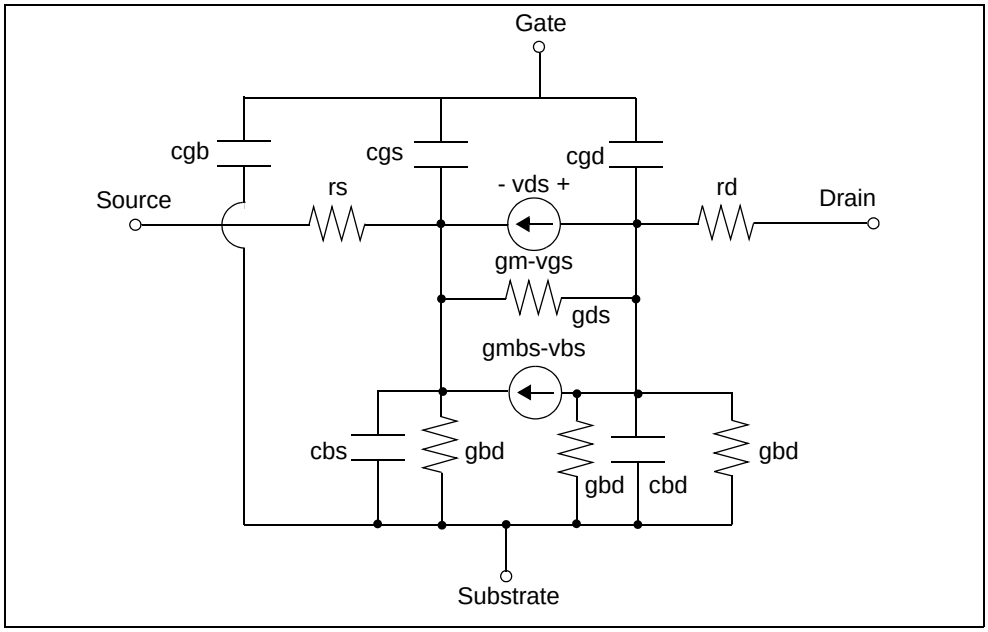


Figure 10 Equivalent Circuit, MOSFET AC Noise Analysis

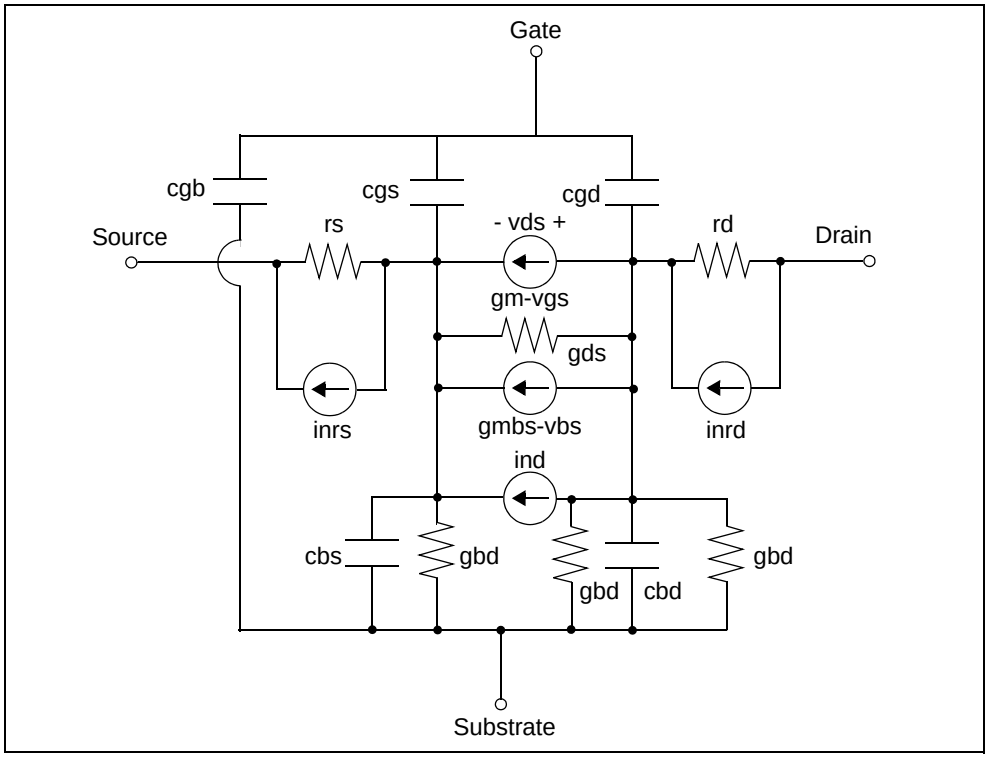


Table 6 MOSFET DC Operating Point Output

Quantities	Definitions
id	drain current
ibs	B-S bulk-to-source current
ibd	B-D bulk-to-drain current
vgs	G-S gate-source voltage
vds	D-S drain-source voltage
vbs	B-S bulk-source voltage
vth	threshold voltage
vdsat	saturation voltage

Table 6 MOSFET DC Operating Point Output (Continued)

Quantities	Definitions
beta	beta value
gam eff	gamma effective
gm	DC gate transconductance
gds	D-S drain-source conductance
gmb	B-S bulk-source conductance
cdtot	total drain capacitance
cgtot	total gate capacitance
cstot	total source capacitance
cbtot	total bulk capacitance (total floating body capacitance for SOI MOSFET)
cgs	total gat- to-source capacitance
cgd	total gat- to-drain capacitance

MOSFET Diode Models

You can use the Area Calculation Method (ACM) parameter to precisely control bulk-to-source and bulk-to-drain diodes within MOSFET models. Use the ACM model parameter to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

Selecting MOSFET Diode Models

To select a MOSFET diode model, set the ACM parameter within the MOSFET model statements.

- If ACM=0, the pn bulk junctions of the MOSFET are modeled in the SPICE style.
- The ACM=1 diode model is the original ASPEC model.
- The ACM=2 model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model.
- The ACM=3 diode model is a further improvement that deals with capacitances of shared sources and drains, and gate edge source/drain-to-bulk periphery capacitance.
- If you do not set the ACM model parameter, the diode model defaults to the ACM=0 model.
- If ACM=0 and ACM=1 models, you cannot specify HDIF. In the ACM=0 model, you cannot specify LDIF. The ACM=1 model does not use the AD, AS, PD, and PS geometric element parameters.

Enhancing Convergence

- The GMIN option creates a parallel conductance across the bulk diodes and drain-source for transient analysis.
- The GMINDC option creates a parallel conductance across the bulk diodes and drain-source for DC analysis.

These options enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the RSH, RS, and RD parameters to prevent over-driving the diode in either a DC or transient forward

bias condition. These parameters also enhance the convergence properties of the diode model.

MOSFET Diode Model Parameters

Table 7 DC Model Parameters

Name (Alias)	Units	Default	Description
ACM		0	Area calculation method
JS	amp/m^2	0	Bulk junction saturation current: JSscaled=JS/SCALM2 – for ACM=1 unit is amp/m and JSscaled=JS/SCALM.
JSW	amp/m	0	Sidewall bulk junction saturation current: JSWscaled=JSW/SCALM.
IS	amp	1e-14	Bulk junction saturation current. For the ASPEC=1 option, default=0.
N		1	Emission coefficient.
NDS		1	Reverse bias slope coefficient.
VNDS	V	-1	Reverse diode current transition point.

Table 8 Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CBD	F	0	Zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0.
CBS	F	0	Zero bias bulk-source junction capacitance. Use only when CJ and CJSW are 0.

Table 8 Capacitance Model Parameters (Continued)

Name (Alias)	Units	Default	Description
CJSW (CJP)	F/m	0	Zero-bias sidewall bulk junction capacitance. CJSWscaled = CJSW/ SCALM. Default = 0.
CJ (CDB, CSB, CJA)	F/m^2	579.11 $\mu F/m^2$	Zero-bias bulk junction capacitance: • CJscaled = CJ/SCALM2 —for ACM=1 the unit is F/m. • CJscaled = CJ/SCALM. Default for the ASPEC=0 option is: $CJ = \left(\frac{\varepsilon si \cdot q \cdot NSUB}{2 \cdot PB}\right)^{1/2}$
CJGATE	F/m	CSJW	Zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only). CJGATEscaled=CJGATE/SCALM • Default = CJSW for Hspice releases later than H9007D. • Default = 0 for HSPICE releases H9007D and earlier, or if you do not specify CJSW.
FC		0.5	Forward-bias depletion capacitance coefficient (not used).
MJ (EXA, EXJ, EXS, EXD)		0.5	Bulk junction grading coefficient.
MJSW (EXP)		0.33	Bulk sidewall junction grading coefficient.
NSUB (DNB, NB)	$1/cm^3$	1.0e15	Substrate doping.
PB (PHA, PHS, PHD)	V	0.8	Bulk junction contact potential.
PHP	V	PB	Bulk sidewall junction contact potential.
TT	s	0	Transit time

Table 9 Drain and Source Resistance Model Parameters

Name (Alias)	Units	Default	Description
RD	ohm/sq	0.0	Drain ohmic resistance. This parameter is usually the sheet resistance of a lightly- doped region for ACM≥1.
RDC	ohm	0.0	Additional drain resistance due to contact resistance.
LRD	ohm/m	0	Drain resistance length sensitivity. Use this parameter with automatic model selection, WRD, and PRD to factor a model for the device size.
WRD	ohm/m	0	Drain resistance width sensitivity (used with LRD).
PRD	ohm/m^2	0	Drain resistance product (area) sensitivity (used with LRD).
RS	ohm/sq	0.0	Source ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for ACM≥1.
LRS	ohm/m	0	Source resistance length sensitivity. Use this parameter with automatic model selection, WRS, and PRS to factor a model for the device size.
WRS	ohm/m	0	Source resistance width sensitivity (used with LRS).
PRS	ohm/m^2	0	Source resistance product (area) sensitivity (used with LRS).
RSC	ohm	0.0	Source resistance due to contact resistance.
RSH (RL)	ohm/sq	0.0	Drain and source diffusion sheet resistance.

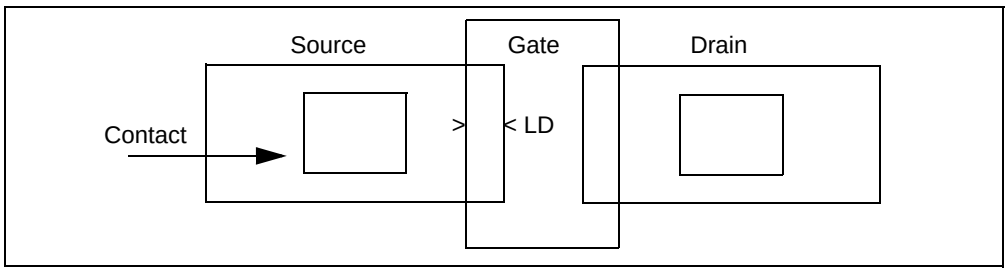
Table 10 Using MOS Geometry Model Parameters

Name (Alias)	Units	Default	Description
HDIF	m	0	Length of heavily-doped diffusion, from contact to lightly-doped region (ACM=2, 3 only): HDIFwscaled = HDIF · SCALM
LD (DLAT,LATD)	m		Lateral diffusion into the channel from the source and drain diffusion. • If you do not specify LD and XJ, LD default=0.0. • If you specify LD, but you do not specify XJ, then simulation calculates LD from XJ. Default=0.75 · XJ. • For LEVEL 4 only, lateral diffusion is derived from LD · XJ. LDscaled = LD · SCALM
LDIF	m	0	Length of lightly-doped diffusion adjacent to the gate (ACM=1, 2): LDIFscaled = LDIF · SCALM
WMLT		1	Width diffusion layer shrink reduction factor.
XJ	m	0	Metallurgical junction depth: XJscaled = XJ · SCALM
XW (WDEL, DW)	m	0	Accounts for masking and etching effects: XWscaled = XW · SCALM

Using an ACM=0 MOS Diode

Figure 11 shows the parameter value settings for a MOSFET diode, designed with a MOSFET that has a channel length of 3 μm and a channel width of 10 μm.

Figure 11 ACM=0 MOS Diode



Example

A transistor might include:

```
LD=.5mm    W=10mm    L=3mm
```

Parameter	Description
AD	area of drain (about 80 pm^2)
AS	area of source (about 80 pm^2)
CJ	4e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-8 A/m^2
JSW	1e-13 A/m
NRD	number of squares for drain resistance
NRS	number of squares for source resistance
PD	sidewall of drain (about 36 μm)
PS	sidewall of source (about 36 μm)

Calculating Effective Areas and Peripheries

For ACM=0, simulation calculates the effective areas and peripheries as follows:

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$

$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

Calculating Effective Saturation Current

For ACM=0, simulation calculates the MOS diode effective saturation currents as follows:

Source Diode Saturation Current

Define:

$$val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0, then $isbs = val$

Otherwise, $isbd = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=0, simulation calculates the effective drain and source resistances as follows:

Source Resistance

Define: $val = NRS \cdot RSH$

If val > 0, then $RSeff = \frac{val + RSC}{M}$

Otherwise, $RSeff = \frac{RS + RSC}{M}$

Drain Resistance

Define: $val = NRD \cdot RSH$

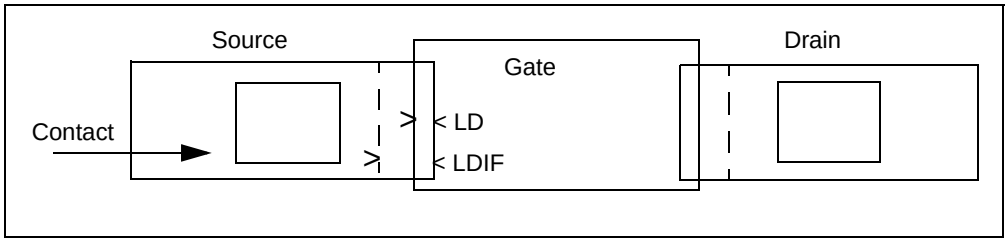
If val > 0, then $RDeff = \frac{val + RDC}{M}$

Otherwise, $RDeff = \frac{RD + RDC}{M}$

Using an ACM=1 MOS Diode

If you specify the ACM=1 model parameter, simulation uses ASPEC-style diodes, and does not use the AD, PD, AS, and PS parameters. The JS and CJ units differ from SPICE-style diodes (ACM=0).

Figure 12 ACM=1 MOS Diode



Example

Table 11 lists parameter value settings for a transistor with the following parameter values:

- LD=0.5 μm
- W=10 μm
- L=3 μm
- LDIF=0.5 μm

Table 11 ACM=0 MOS Diode Parameters

Parameter	Description
CJ	1e-10 F/m of gate width Note the change from F/m^2 (in ACM=0) to F/m.
CJSW	2e-10 F/m of gate width
JS	1e-14 A/m of gate width Note the change from A/m^2 (in ACM=0) to A/m
JSW	1e-13 A/m of gate width
NRD	number of squares for drain resistance
NRS	number of squares for source resistance

Calculating Effective Areas and Peripheries

For ACM=1, simulation calculates the effective areas and peripheries as follows:

$$ADeff = Weff \cdot WMLT$$

$$ASeff = Weff \cdot WMLT$$

$$PDff = Weff$$

$$PSeff = Weff$$

The following equation calculates the *Weff* value used in the preceding equations:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

Note: The Weff value is not the same as the weff value in the LEVEL 1, 2, 3, 6, and 13 models. The $2 \cdot WDscaled$ term is not subtracted.

Calculating Effective Saturation Current

For ACM=1, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=1, simulation calculates the effective drain and source resistances as follows.

Source Resistance

For UPDATE=0:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1, LDIF=0, and you specify the ASPEC option, then:

$$RSeff = \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE ≥ 1, LDIF=0, and you specify the ASPEC option, then:

$$RDeff = \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

See LEVEL 6/LEVEL 7 IDS: MOSFET Model on page 155 and LEVEL 7 IDS Model on page 181 for more possibilities.

Using an ACM=2 MOS Diode

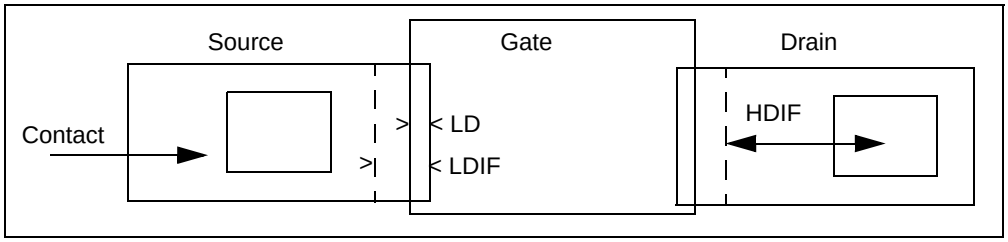
If you set the ACM=2 model parameter, simulation uses HSPICE-style MOS diodes. You can use a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly-doped and heavily-doped diffusions (the LD, LDIF, and HDIF parameters set the diffusion type). This model preserves the JS, JSW, CJ, and CJSW units (used in SPICE) for full compatibility.

ACM=2 automatically generates more-reasonable diode parameter values than those for ACM=1. You can generate the ACM=2 geometry in either of two ways:

- AD, AS, PD, and PS element parameters in the element statement generate parasitics. These parameters do not have default option values.
- To suppress the diode, set IS=0, AD=0, and AS=0.

If you set AS=0 in the element and IS=0 in the model, simulation suppresses the source diode. Use this setting for shared contacts.

Figure 13 ACM=2 MOS Diode



Example

For a transistor with LD=0.07µm, W=10 µm, L=2 µm, LDIF=1 µm, and HDIF= 4 µm. Table 12 shows typical MOSFET diode parameter values.

Table 12 ACM=2 MOS Diode Parameters

Parameter	Description
AD	Area of drain. Default option value for AD is not applicable.
AS	Area of source. Default option value for AS is not applicable.
CJ	1e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-4 A/m^2
JSW	1e-10 A/m
HDIF	Length of heavily-doped diffusion contact-to-gate (about 2 μm). HDIFeff=HDIF · WMLT · SCALM
LDIF+LD	Length of lightly-doped diffusion (about 0.4μm).
NRD	Number of squares drain resistance. Default value for NRD does not apply.
NRS	Number of squares source resistance. Default for NRS does not apply.
PD	Periphery of drain, including gate width for ACM=2. No default.
PS	Periphery of source, including gate width for ACM=2. No default.
RD	Resistance (ohm/square) of lightly-doped drain diffusion (about 2000).
RS	Resistance (ohm/square) of lightly-doped source diffusion (about 2000).
RSH	Diffusion sheet resistance (about 35).

Calculating Effective Areas and Peripheries

For ACM=2, simulation calculates the effective areas and peripheries as follows:

- If you do not specify AD then $ADeff = 2 \cdot HDIFeff \cdot Weff$

  Otherwise, $ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$

- If you do not specify AS, then $ASeff = 2 \cdot HDIFscaled \cdot Weff$

  Otherwise, $ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$

- If you do not specify PD, then $PDeff = M \cdot (4 \cdot HDIFeff + 2 \cdot Weff)$

  Otherwise, $PDeff = M \cdot PD \cdot WMLT \cdot SCALE$

- If you do not specify PS, then $PSeff = M \cdot (4 \cdot HDIFeff + 2 \cdot Weff)$

  Otherwise, $PSeff = M \cdot PS \cdot WMLT \cdot SCALE$

The following equations calculate values used in the preceding equation:

$$Weff = Wscaled \cdot WMLT + XWscaled$$

$$HDIFeff = HDIFscaled$$

$$HDIFscaled = HDIF \cdot SCALM \cdot WMLT$$

The Weff value is not the same as the Weff value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WDscaled$ term is not subtracted.

Calculating Effective Saturation Currents

For ACM=2, simulation calculates the MOS diode effective saturation currents as follows.

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0, then $isbs = val$.

Otherwise, $isbs = M \cdot IS$.

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$.

If val > 0, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=2, simulation calculates the effective drain and source resistances as follows.

Source Resistance

If you specify NRS, then:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M}\right)$$

Otherwise:

$$RSeff = \frac{RSC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RS}{Weff}$$

Drain Resistance

If you specify NRD, then:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M}\right)$$

Otherwise:

$$RDeff = \frac{RDC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RD}{Weff}$$

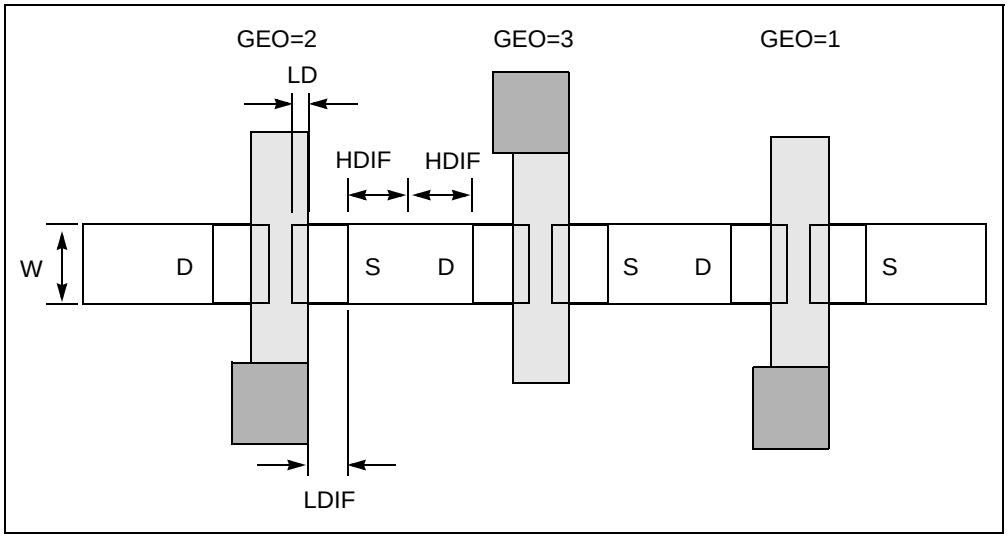
Using an ACM=3 MOS Diode

Use ACM=3 to properly model MOS diodes of stacked devices. You can also use the CJGATE parameter to model the drain and source periphery capacitances separately, along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. CJGATE defaults to the CJSW value, which in turn defaults to 0.

The AD, AS, PD, and PS calculations depend on the device layout as determined by the value of the GEO element parameter. You can specify the following GEO values in the MOS element description:

- GEO=0: other devices do not share the drain and source of the device (default).
- GEO=1: another device shares the drain.
- GEO=2: another device shares the source.
- GEO=3: another device shares the drain and source.

Figure 14 Stacked Devices and Corresponding GEO Values



Calculating Effective Areas and Peripheries

ACM=3 calculates the effective areas and peripheries based on the GEO value.

If you do not specify AD, then:

- *For GEO=0 or 2,* $ADeff = 2 \cdot HDIFeff \cdot Weff$
- For GEO=1 or 3, $ADeff = HDIFeff \cdot Weff$
- Otherwise, $ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$

If you do not specify AS, then:

- For GEO=0 or 1, $ASeff = 2 \cdot HDIFeff \cdot Weff$
- For GEO=2 or 3, $ASeff = HDIFeff \cdot Weff$
- Otherwise, $ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$

If you do not specify PD, then:

- For GEO=0 or 2, $PDeff = 4 \cdot HDIFeff + Weff$
- For GEO=1 or 3, $PDeff = 2 \cdot HDIFeff$
- Otherwise, $PDeff = M \cdot PD \cdot WMLT \cdot SCALE$

If you do not specify PS, then:

- For GEO=0 or 1, $PSeff = 4 \cdot HDIFeff + Weff$
- For GEO=2 or 3, $PSeff = 2 \cdot HDIFeff$
- Otherwise, $PSeff = M \cdot PS \cdot WMLT \cdot SCALE$

Simulation calculates Weff and HDIFeff as follows:

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff = HDIFscaled \cdot WMLT$$

Note: The Weff value is not the same as the Weff value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WDscaled$ term is not subtracted.

Effective Saturation Current Calculations

The ACM=3 model calculates the MOS diode effective saturation currents the same as ACM=2.

Effective Drain and Source Resistances

The ACM=3 model calculates the effective drain and source resistances the same as ACM=2.

MOS Diode Equations

This section describes MOS diode equations.

DC Current

- Simulation parallels the drain and source MOS diodes with GMINDC conductance in the DC analysis.
- Simulation parallels the drain and source MOS diodes with GMIN conductance in the transient analysis.

The total DC current is the sum of the diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

- vbs > 0: $ibs = isbs \cdot (e^{\mathrm{vbs}/(N \cdot vt)} - 1)$
- vbd > 0: $ibd = isbd \cdot (e^{\mathrm{vbd}/(N \cdot vt)} - 1)$

Drain and Source Diodes Reverse Biased

- For 0>vbs>VNDS: $ibs = gsbs \cdot vbs$
- For vbs < VNDS: $ibs = gsbs \cdot VNDS + \left(\frac{gsbs}{NDS}\right) \cdot (vbs - VNDS)$
- For 0 > vbd > VNDS: $ibd = gsbd \cdot vbd$
- For vbd < VNDS: $ibd = gsbd \cdot VNDS + \left(\frac{gsbd}{NDS}\right) \cdot (vbd - VNDS)$

The following equations calculate values used in the preceding equations:

$|gsbs| = |isbs|$
$|gdbd| = |isbd|$

Using MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. Simulation evaluates the diffusion capacitance in terms of the small signal conductance of the diode and a TT model parameter, representing

the transit time of the diode. The depletion capacitance depends on which ACM you choose.

To calculate bias-dependent depletion capacitance, define C0BS, C0BD, C0BS_SW, and C0BD_SW intermediate quantities. These depend on geometric parameters, such as ASeff and PSeff, calculated under various ACM specifications.

For ACM=3, the C0BS_SW and C0BD_SW intermediate quantities include an extra term to account for CJGATE.

ACM=2 includes the CJGATE parameter for backward compatibility. Therefore, the default behavior of CJGATE makes the C0BS_SW and C0BD_SW intermediate quantities the same as for previous versions. The default patterns are:

- If you do not specify CJSW or CJGATE, both default to zero.
- If you do not specify CJGATE, it defaults to CJSW, which defaults to zero.
- If you specify CJGATE, but you do not specify CJSW, then CJSW defaults to zero.

Simulation calculates the C0BS, C0BS_SW, C0BD, and C0BD_SW intermediate quantities as follows.

```
C0BS = CJscaled*ASeff
   C0BD = CJscaled*ADeff
```

- If (ACM= 0 or 1), then:

```
C0BS_SW = CJSWscaled*PSeff
   C0BD_SW = CJSWscaled*PDeff
```

- If (ACM=2) and (PSeff < Weff), then:

```
C0BS_SW = CJGATEscaled*PSeff
```

- If (ACM=2) and (PSeff > Weff), then:

```
C0BS_SW = CJSWscaled*(PSeff-Weff) + CJGATEscaled*Weff
```

- If (ACM=2) and (PDeff < Weff), then:

```
C0BD_SW = CJGATEscaled*PDeff
```

- If (ACM=2) and (PDeff > Weff), then:

```
C0BD_SW = CJSWscaled*(PDeff-Weff) + CJGATEscaled*Weff
```

- If (ACM=3), then:

```
C0BS_SW = CJSWscaled*PSeff + CJGATEscaled*Weff
   C0BD_SW = CJSWscaled*PDeff + CJGATEscaled*Weff
```

Source Diode Capacitance

- If (C0BS + C0BS_SW) > 0 and vbs < 0, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$$

$$+ \text{C0BS\_SW} \cdot \left(1 - \frac{vbs}{PHP}\right)^{-MJSW}$$

If (C0BS + C0BS_SW) > 0 and vbs > 0, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$$

$$+ \text{C0BS\_SW} \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right)$$

Otherwise, if (C0BS + C0BS_SW) ≤ 0, then:

For vbs < 0: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$

For vbs > 0: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$

Drain Diode Capacitance

If (C0BD + C0BD_SW) > 0, then:

For vbd < 0:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$$

$$+ PDeff \cdot \text{C0BD\_SW} \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For vbd > 0:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right)$$

$$+ \text{C0BD\_SW} \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right)$$

Otherwise, if (ADeff · CJscaled + PDeff · CJSWscaled) ≤ 0, then:

For vbd < 0: $capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$

For vbd > 0: $capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right)$

Common Threshold Voltage Equations

Common Threshold Voltage Parameters

The parameters described in this section apply to all MOSFET models except Levels 5 and 13.

Table 13 MOSFET Common Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
DELVTO	V	0.0	Zero-bias threshold voltage shift.
GAMMA	$V^{1/2}$	0.527625	Body effect factor. If you do not set GAMMA, simulation calculates it from NSUB.
NGATE	$1/cm^3$	-	Polysilicon gate doping, used for analytical models only. Undoped polysilicon is represented by a small value. If NGATE ≤ 0.0, it is set to 1e+18.
NSS	$1/cm^2$	1.0	Surface state density.
NSUB (DNB, NB)	$1/cm^3$	1e15	Substrate doping.

Table 13 MOSFET Common Threshold Voltage Parameters (Continued)

Name (Alias)	Units	Default	Description
PHI	V	0.576036	Surface potential. NSUB default=1e15.
TPG (TPS)	-	1.0	Type of gate material for analytical models. LEVEL 4 TPG default=0. The TPG value can be: • TPG = 0 al-gate. • TPG = 1 same as source-drain diffusion. • TPG = -1 gate type opposite to source-drain diffusion.
VTO (VT)	V	-	Zero-bias threshold voltage.

Calculating PHI, GAMMA, and VTO

Use the PHI, GAMMA, and VTO model parameters to calculate threshold voltages. If you do not specify these parameters, simulation calculates them as follows, except for the LEVEL 5 model.

If you do not specify PHI, then:

$$PHI = 2 \cdot vt \cdot \ln\left(\frac{NSUB}{ni}\right)$$

If you do not specify GAMMA, then:

$$GAMMA = \frac{(2 \cdot q \cdot \varepsilon si \cdot NSUB)^{1/2}}{COX}$$

The following equations determines the energy gap (eg) and intrinsic carrier concentration used in the above equations:

$$eg = 1.16 - 7.02e\text{-}4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e{+}10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]} (1/\mathrm{cm}^3)$$

In the preceding equation, $tnom = TNOM + 273.15$.

If you do not specify VTO, then for Al-Gate (TPG=0), the following equation determines the Φ ms work function:

$$\Phi ms = -\frac{eg}{2} - \text{type} \cdot \frac{PHI}{2} - 0.05$$

In the preceding equation, *type* is +1 for n-channel or -1 for p-channel.

For Poly-Gate (TPG=±1), the following equations determine the work function.

If you do not specify the NGATE model parameter, then:

$$\Phi ms = type \cdot \left(- TPG \cdot \frac{eg}{2} - \frac{PHI}{2} \right)$$

If you specify NGATE, then:

$$\Phi ms = type \cdot \left[- TPG \cdot vt \cdot \ln\left(\frac{NGATE}{ni} \right) - \frac{PHI}{2} \right]$$

If you do not specify the VTO model parameter, then the following equation determines the VTO voltage:

$$VTO = vfb + type \cdot (GAMMA \cdot PHI^{1/2} + PHI)$$

In the preceding equation, $vfb = \Phi ms - \frac{q \cdot NSS}{COX} + DELVTO$.

If you specify VTO, then:

$$VTO = VTO + DELVTO$$

MOSFET Impact Ionization

Impact ionization current is available for all MOSFET levels. ALPHA, VCR, and IIRAT are the controlling parameters. IIRAT sets the fraction of the impact ionization current sent to the source.

$$I_{ds} = I_{ds\_}\texttt{normal} + \texttt{IIRAT} \cdot \texttt{I\_impact}$$
$$I_{db} = I_{db\_}\texttt{diode} + (1 - \texttt{IIRAT}) \cdot \texttt{I\_impact}$$

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

Table 14 Impact Ionization Model Parameters

Name (Alias)	Units	Default	Description
ALPHA	1/V	0.0	Impact ionization current coefficient
LALPHA	µm/V	0.0	ALPHA length sensitivity
WALPHA	µm/V	0.0	ALPHA width sensitivity
VCR	V	0.0	Critical voltage
LVCR	µm · V	0.0	VCR length sensitivity
WVCR	µm · V	0.0	VCR width sensitivity
IIRAT		0.0	Portion of impact ionization current sent to the source

Calculating the Impact Ionization Equations

The following equations calculates the I_impact current due to the impact ionization effect:

$$\text{I\_impact} = Ids \cdot ALPHAeff \cdot (vds - vdsat) \cdot e^{\frac{-VCReff}{vds - vdsat}}$$

The following equations calculate values used in the preceding equation:

$$ALPHAeff = ALPHA + LALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right)$$

$$+ WALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$VCReff = VCR + LVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right)$$

$$+ WVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

The following equations calculate the LREFeff and WREFeff values used in the preceding equations:

$$LREFeff = LREF + XLREF - 2 \cdot LD$$
$$WREFeff = WREF + XWREF - 2 \cdot WD$$

Calculating Effective Output Conductance

You can use the element template to directly output *gds*. For example:

```
.PRINT I(M1) gds=LX8(M1)
```

If you use impact ionization current, gds is the derivative of I_{ds} only, rather than the total drain current, which is I_{ds}+I_{db}.

The complete drain output conductance is:

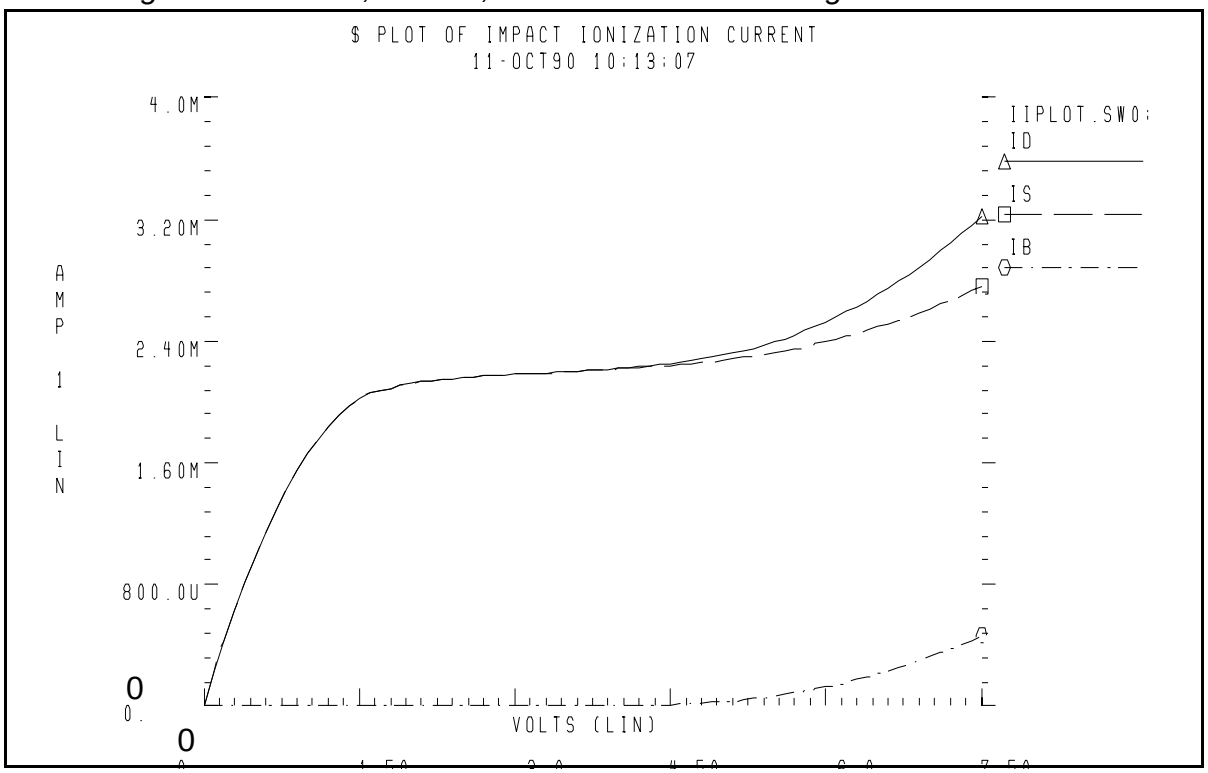
$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of the M1 device:

```
.PRINT rout=PAR('1.0/(LX8(M1)+LX10(M1))')
```

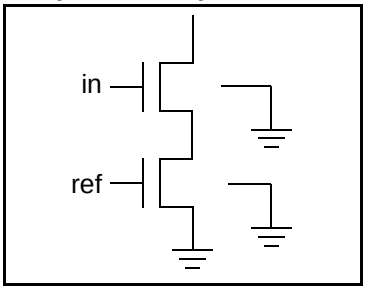
Figure 15 Drain, Source, and Bulk Currents for vgs=3 with IIRAT=0.5



Cascoding Example

Drain-to-bulk impact ionization current limits the use of cascoding to increase output impedance. The following cascode example shows the effect of changing IIRAT. If IIRAT is less than 1.0, the drain-to-bulk current lowers the output impedance of the cascode stage.

Figure 16 Low-frequency AC Analysis Measuring Output Impedance



Cascode Circuit

Example

```
iirat      gout_ac       rout
   0.0       8.86E-6       113 K
   0.5       4.30E-6       233 K
   1.0       5.31E-8       18.8 Meg
```

The input file for this example is located in the following directory:

`$installdir/demo/hspice/mos/cascode.sp`

MOS Gate Capacitance Models

You can use capacitance model parameters with all MOSFET model statements.

Three fixed-capacitance parameters (CGDO, CGSO, and CGBO) represent gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances to model charge storage, use fixed and nonlinear gate capacitances and junction capacitances. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of the CAPOP model parameter.

To model MOS gate capacitances as a nonlinear function of terminal voltages, use Meyer's piecewise linear model for all MOS levels. The charge conservation model is also available for MOSFET model Levels 2 through 7, 13, and 27. For LEVEL 1, you must specify the TOX model parameter to invoke the Meyer model. The next three sections describe the Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause "*timestep too small"* errors if you do not specify other nodal capacitances.

Selecting Capacitor Models

When you select a gate capacitance model, you can choose various combinations of capacitor models and DC models. You can incrementally update older DC models with new capacitance equations, without having to move to a new DC model. You can use the CAPOP model parameter to select the gate capacitance and validate the effects of different capacitance models.

The CAPOP capacitance model selection parameter selects the capacitor models to use for modeling the MOS gate capacitance:

- gate-to-drain capacitance
- gate-to- source capacitance
- gate-to-bulk capacitance.

You can use CAPOP to select several versions of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models (DC model level in parentheses below). Other models are designated as general; any DC model can use them.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Parameterized Modified Meyer gate-capacitance model (general default)
CAPOP=3	Parameterized Modified Meyer gate-capacitance model with Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model (specialized, LEVEL 2)
CAPOP=12	Ward-Dutton model (specialized, LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (default for Levels 13, 28, 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the specified DC model.

Table 15 CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects
2	2	11
3	2	12
13, 28, 39	13	13
Other levels	2	11

The proprietary models (Levels 5, 17, 21, 22, 25, 31, 33), the SOS model (LEVEL 27), and models higher than 49 have their own built-in capacitance routines.

Transcapacitance

If a capacitor has two terminals (1 and 2) with charges named Q1 and Q2 on the two terminals that sum to zero (for example, Q1=-Q2), then the charge is a function of the voltage difference between the terminals (V12=V1-V2). One quantity (C=dQ1/dV12) completely describes the small-signal characteristics of the device.

If a capacitor has four terminals, the sum of the charges on the four terminals must equal zero (Q1+Q2+Q3+Q4=0). They can depend only on voltage differences, but they are otherwise arbitrary functions. Because three independent charges (Q1, Q2, Q3) are functions of three independent voltages (V14, V24, V34), you must specify nine derivatives to describe the small-signal characteristics.

You can consider the four charges separately as functions of the four terminal voltages, Q1(V1,V2,V3,V4), ... Q4(V1,V2,V3,V4). The derivatives form a four-by-four matrix, dQi/dVj, i=1,.4, j=1,.4. Simulation directly interprets this matrix as AC measurements.

If you apply an AC voltage signal to the j terminal and you ground the other terminals to AC, and if you measure AC current into the *i* terminal, then the current is the imaginary constant times 2*pi*frequency times dQi/dVj.

- Because the charges add up to zero, each column of this matrix must add up to zero.
- Because the charges can depend only on voltage differences, each row must add up to zero.

In general, the matrix is not symmetrical:

```
dQi/dVj need not equal dQj/dVi
```

This is not an expected event because it does not occur for the two-terminal case. For two terminals, because the rows and columns must add up to zero, dQ1/dV2 must equal dQ2/dV1.

$$\frac{dQ1}{dV1} + \frac{dQ2}{dV1} = 0 \qquad \frac{dQ1}{dV1} + \frac{dQ1}{dV2} = 0$$

For three or more terminals, this relation does not generally hold.

The terminal input capacitances are the diagonal matrix entries:

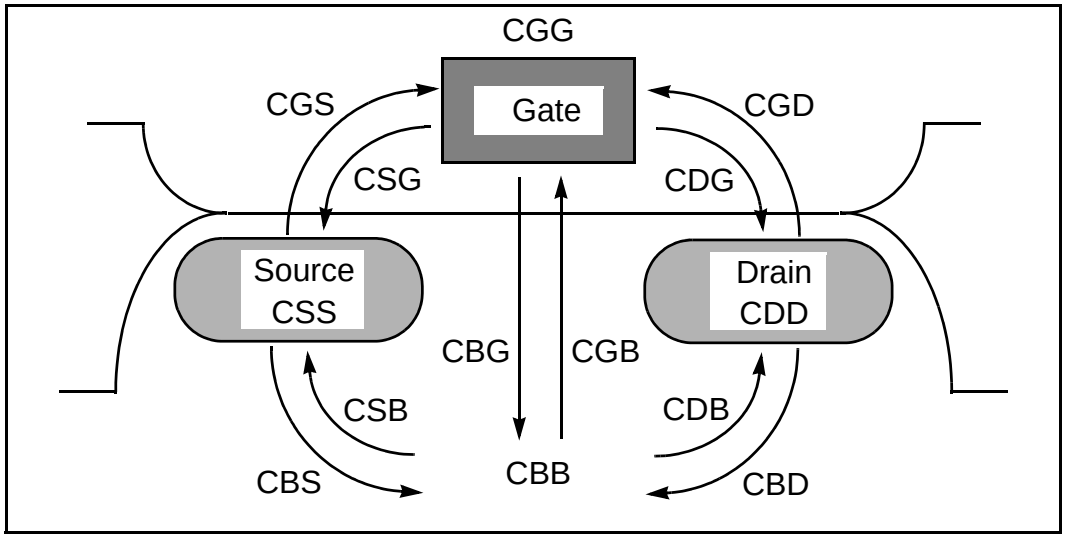
```
Cii = dQi/dVi    i=1,.4
```

The transcapacitances are the negative of off-diagonal entries:

```
Cij = -dQi/dVj    i not equal to j
```

All of the C values are normally positive.

Figure 17 MOS Capacitances



In Figure 17, Cij determines the current transferred out of the i node from a voltage change on the j node. The arrows, representing direction of influence, point from node j to node i.

A MOS device with terminals named D G S B provides:

$$CGG = \frac{dQg}{dVG} \qquad CGD = -\frac{dQg}{dVD} \qquad CDG = -\frac{dQD}{dVG}$$

- CGG represents input capacitance: a change in gate voltage requires a current equal to CGGxdVG/dt into the gate terminal.
- CGD represents Miller feedback: a change in drain voltage creates a current equal to CGGxdVG/dt out of the gate terminal.
- CDG represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To show how CGD might not equal CDG, the following example is a simplified model with no bulk charge with a gate charge as a function of VGS only, and with the 50/50 channel charge partitioned into QS and QD:

$$QG = Q(vgs) \qquad QS = -0.5 \cdot Q(vgs)$$

$$QD = -0.5 \cdot Q(vgs) \qquad QB = 0$$

Consequently:

$$CGD = -\frac{dQG}{dVD} = 0 \qquad CDG = -\frac{dQD}{dVG} = 0.5 \cdot \frac{dQ}{dvgs}$$

Therefore, this model has Miller feedthrough, but no feedback.

Operating Point Capacitance Printout

The operating point printout reports six capacitances:

Table 16 Operating Point Capacitance

Capacitance	Value
cdtot	dQD/dVD
cgtot	dQG/dVG
cstot	dQS/dVS

Table 16 Operating Point Capacitance (Continued)

Capacitance	Value
cbtot	dQB/dVB
cgs	-dQG/dVS
cgd	-dQG/dVD

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For the Meyer models, where charges such as QD are not well defined, Table 17 shows the printout quantities.

Table 17 Capacitance Printout for Meyer Models

Capacitance	Value
cdtot	cgd+cdb
cgtot	cgs+cgd+cgb
cstot	cgs+csb
cbtot	cgb+csb+cdb
cgs	cgs
cgd	cgd

Element Template Printout

The MOS element template printouts for gate capacitance are LX18 to LX23 and LX32 to LX34. From these nine capacitances, you can construct the complete four-by-four matrix of transcapacitances. The nine LX printouts are:

```
LX18(m) = dQG/dVGB = CGGBO
   LX19(m) = dQG/dVDB = CGDBO
   LX20(m) = dQG/dVSB = CGSBO
```

```
LX21(m) = dQB/dVGB = CBGBO
LX22(m) = dQB/dVDB = CBDBO
LX23(m) = dQB/dVSB = CBSBO
LX32(m) = dQD/dVG = CDGBO
LX33(m) = dQD/dVD = CDDBO
LX34(m) = dQD/dVS = CDSBO
```

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For an NMOS device with source and bulk grounded:

- LX18 is the input capacitance.
- LX33 is the output capacitance.
- LX19 is the Miller feedback capacitance (gate current induced by voltage signal on the drain).
- LX32 is the Miller feedthrough capacitance (drain current induced by the voltage signal on the gate).

A device operating with node 3 as electrical drain—for example an NMOS device with node 3 at higher voltage than node 1—is in *reverse mode*.

The LX values are physical, but you can translate them into electrical definitions by interchanging D and S:

```
CGG(reverse) = CGG = LX18
   CDD(reverse) = CSS = dQS/dVS = d(-QG-QB-QD)/dVS =
      -LX20-LX23-LX34
   CGD(reverse) = CGS = -LX20
   CDG(reverse) = CSG = -dQS/dVG = d(QG+QB+QD)/dVG =
      LX18+LX21+LX32
```

For Meyer models, QD and other charges are not well defined. The formulas (such as LX18= CGG, LX19= -CGD) are still true, but the transcapacitances are symmetrical; for example, CGD=CDG. In terms of the six independent Meyer capacitances (cgd, cgs, cgb, cdb, csb, and cds), the LX printouts are:

```
LX18(m) = CGS+CGD+CGB
   LX19(m) = LX32(m) = -CGD
   LX20(m) = -CGS
   LX21(m) = -CGB LX22(m) = -CDB
```

```
LX23(m) = -CSB
LX33(m) = CGD+CDB+CDS
LX34(m) = -CDS
```

Calculating Gate Capacitance

The following input file example shows a gate capacitance calculation in detail for a BSIM model. TOX is chosen so that:

$$\frac{eox}{tox} = 1e-3F/m^2$$

In this example, Vfb0, phi, and k1 are chosen so that vth=1v. The AC sweep is chosen so that the last point is:

$$2 \cdot \pi \cdot freq = 1e6s^{-1}$$

Input File

The input file is located in the following directory:

`$installdir/demo/hspice/mos/calcap.sp`

Calculations

$$Leff = 0.6u \qquad \frac{eox}{tox} = 1e-3F/m^2$$

$$Cap = \frac{Leff \cdot Weff \cdot eox}{tox} = 60e-15F$$

BSIM equations for internal capacitance in saturation with xqc=0.4:

$$body = 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364 \cdot (PHI0 + vsb))}\right) \cdot \frac{K1}{\sqrt{(PHI0 + vsb)}}$$

$$= 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364)}\right) = 1.3062$$

$$cgg = Cap \cdot \left(1 - \frac{1}{(3 \cdot body)}\right) = Cap \cdot 0.7448 = 44.69F$$

$$cgd = 0 \qquad cdg = \left(\frac{4}{15}\right) \cdot Cap = 16F \qquad cdd = 0$$

Gate-drain overlap = $(ld + meto) \cdot Weff \cdot \frac{eox}{tox} = 20e-15F$

Adding the overlaps:

$cgg = 44.69F + 2 \cdot 20F = 84.69F$ $cgd = 20F$

$cdg = 36F$ $cdd = 20F$

Drain-bulk diode cap $= cj \cdot ad = (0.5e-4) \cdot (200e-12) = 10F$

Adding the diodes:

$cgg = 84.69F$ $cgd = 20F$

$cdg = 36F$ $cdd = 30F$

Results

```
subckt
   element  0:m
   model    0:nch
   cdtot     30.0000f
   cgtot     84.6886f
   cstot     65.9999f
   cbtot     43.4213f
   cgs       61.2673f
   cgd       20.0000f
```

The calculation and simulation results match.

Plotting Gate Capacitances

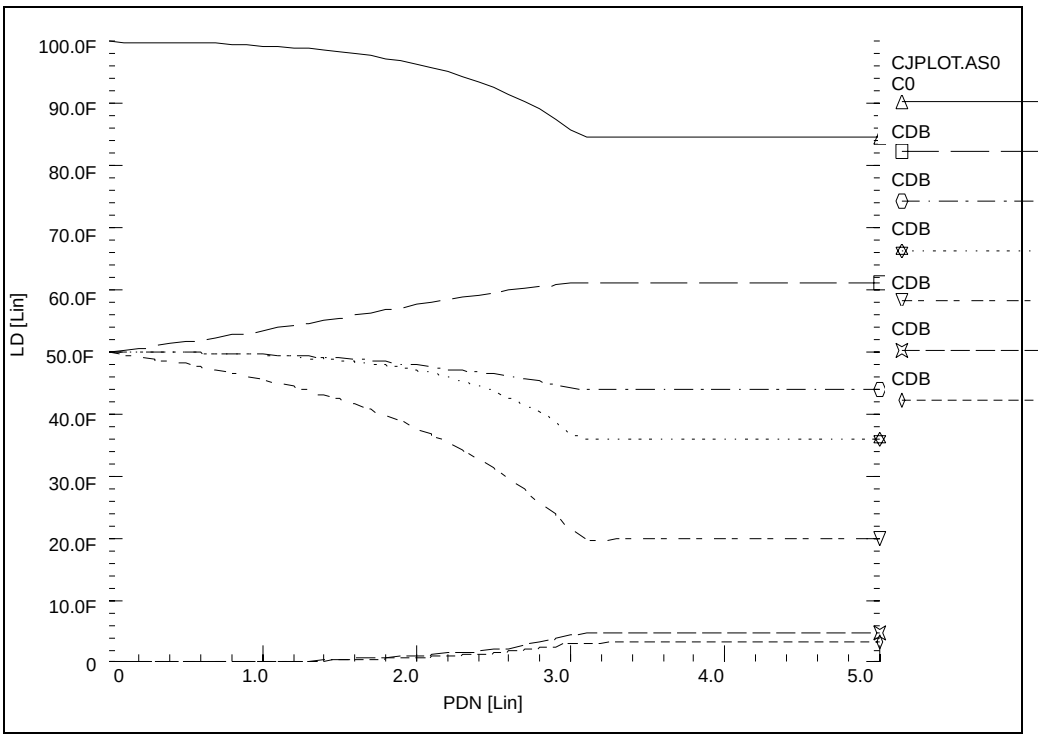
The following input file shows how to plot gate capacitances as a function of bias. Set **.OPTION** DCCAP to turn on capacitance calculations for a DC sweep. The model used is the same as for the previous gate capacitance calculations.

Example

This example netlist is located in the following directory:

`$installdir/demo/hspice/mos/gatcap.sp`

Figure 18 Gate Capacitance



Capacitance Control Options

The **.OPTION** SCALM, CVTOL, DCSTEP, and DCCAP control options affect the CAPOP models.

- SCALM scales the model parameters.
- CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see CAPOP=3 — Gate Capacitances (Simpson Integration) on page 86).
- DCSTEP models capacitances with a conductance during DC analysis.
- DCCAP calculates capacitances in DC analysis.

Scaling

.OPTION SCALM scales the CGBO, CGDO, CGSO, COX, LD, and WD parameters according to fixed rules, which are a function of the parameter's units. If the model parameter's units are in meters, simulation multiplies the parameter by SCALM. For example:

- The LD parameter uses units in meters; to obtain its scaled value, simulation multiplies the value of LD by SCALM.
- If the units are in meters squared, simulation multiplies the parameter by $SCALM^2$.
- If the units are in reciprocal meters, the parameter's value is divided by SCALM. For example, because CGBO is in farads/meter, the value of CGBO is divided by SCALM.
- If the units are in reciprocal meters squared, then the parameter is divided by $SCALM^2$.

For the scaling equations specific to each CAPOP level, see the individual CAPOP subsections.

MOS Gate Capacitance Model Parameters

Table 18 Basic Gate Capacitance Parameters

Name (Alias)	Units	Default	Description
CAPOP	-	2.0	Capacitance model selector.
COX (CO)	F/m2	3.453e-4	Oxide capacitance. If you do not specify COX, simulation calculates it from TOX. The default corresponds to the TOX default of 1e-7: $COXscaled = COX/SCALM^2$
TOX	m	1e-7	Oxide thickness, calculated from COX (if you specify COX). The program uses the default if you do not specify COX. For TOX>1, simulation assumes that the unit is Angstroms. A level-dependent default can override it. See specific MOSFET levels in this manual.

Table 19 Gate Overlap Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGBO (CGB)	F/m	0.0	Gate-bulk overlap capacitance per meter channel length. If you set WD and TOX, but you do not set CGBO, then simulation calculates CGBO. CGBOscaled = CGBO/SCALM
CGDO (CGD, C2)	F/m	0.0	Gate-drain overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGDO, then simulation calculates CGDO. CGDOscaled = CGDO/SCALM
CGSO (CGS, C1)	F/m	0.0	Gate-source overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGSO, then simulation calculates CGSO. CGSOscaled = CGSO/SCALM
LD (LATD, DLAT)	m		Lateral diffusion into channel from source and drain diffusion. • If you do not specify either LD or XJ, then the LD default=0.0. • If you specify XJ but you do not specify LD, then simulation calculates LD from XJ. • LD default=0.75 · XJ for all levels except LEVEL 4 for which LD default=0.75. LDscaled = LD · SCALM LEVEL 4: LDscaled = LD · XJ · SCALM
METO	m	0.0	Fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation. METOscaled = METO · SCALM
WD	m	0.0	Lateral diffusion into channel from bulk along width. WDscaled = WD · SCALM

Table 20 Meyer Capacitance Parameters CAPOP=0, 1, 2

Name (Alias)	Units	Default	Description
CF1	V	0.0	Modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (for CAPOP=2 only)
CF2	V	0.1	Modified MEYER control for transition of cgs from weak to strong inversion region (for CAPOP=2 only)
CF3		1.0	Modified MEYER control for the cgs and cgd transition from the saturation region to the linear region as a function of vds (for CAPOP=2 only)
CF4		50.0	Modified MEYER control for the contour of the cgb and cgs smoothing factors
CF5		0.667	Modified MEYER control for the capacitance multiplier for cgs in the saturation region
CF6		500.0	Modified MEYER control for contour of cgd smoothing factor
CGBEX		0.5	cgb exponent (for CAPOP=1 only)

Table 21 Charge Conservation Parameters (CAPOP=4)

Name (Alias)	Units	Default	Description
XQC		0.5	Coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases.

Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13

Parameter rules for the gate capacitance charge sharing coefficient (XQC & XPART) in the saturation region:

- If you do not specify either XPART or XQC, then simulation uses the 0/100 model.
- If you specify both XPART and XQC, then XPART overrides XQC.
- If you specify XPART but you do not specify XQC, then:
  - XPART=0 → 40/60
  - XPART=0.4 → 40/60
  - XPART=0.5 → 50/50
  - XPART=1 → 0/100
  - XPART = any other value less than 1 → 40/60
  - XPART >1 → 0/100If XQC is specified:
- If you specify XQC but you do not specify XPART, then:
  - XQC=0 → 0/100
  - XQC=0.4 → 40/60
  - XQC=0.5 → 50/50
  - XQC=1 → 0/100
  - XQC = any other value less than 1 → 40/60
  - XQC>1 → 0/100

The only difference is the treatment of the 0 parameter value.

After you specify XPART/XQC, the gate capacitance ramps from 50/50 at Vds=0 volt (linear region) to the value (with Vds sweep) in the saturation region in XPART/XQC. Ramping the charge-sharing coefficient ensures smooth gate capacitance characteristics.

Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly or the program can calculate them. Either way, these overlap capacitors must be added into the respective voltage-variable capacitors before integration, and before the DC operating point reports the combined parallel capacitance.

Gate-to-Bulk Overlap Capacitance

If you specify CGBO, then:

$$CGBOeff = M \cdot Leff \cdot CGBOscaled$$

Otherwise:

$$CGBOeff = 2 \cdot WDscaled \cdot Leff \cdot COXscaled \cdot M$$

Gate-to-Source Overlap Capacitance

If you specify CGSO, then:

$$CGSOeff = Weff \cdot CGSOscaled$$

Otherwise:

$$CGSOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

Gate-to-Drain Overlap Capacitance

If you specify CGDO, then:

$$CGDOeff = Weff \cdot CGDOscaled$$

Otherwise:

$$CGDOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

Simulation calculates the Leff value for each model differently, and saves this value in the corresponding model section. The Weff calculation is not the same as the weff value in the LEVEL 1, 2, 3, 6, 7 and 13 models.

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

The 2·WDscaled factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vth-PH1: $cgb = cap$

Depletion, vgs < vth: $cgb = cap \cdot \frac{vth - vgs}{PH1}$

Strong Inversion, vgs ≥ vth: $cgb = 0$

Gate-Source Capacitance (cgs)

Accumulation: $vgs \le vth - \frac{PHI}{2}$ $cgs = 0$

Depletion, vgs ≤ vth: $cgs = CF5 \cdot cap + \frac{cap \cdot (vgs - cth)}{0.75 \cdot PHI}$

Strong Inversion Saturation Region:

vgs > vth and vds ≥ vdsat

$cgs = CF5 \cdot cap$

Strong Inversion Linear Region:

vgs > vth and vds < vdsat

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vdsat - vds}{2 \cdot (vdsat + vsb) - vds - vsb}\right]^2\right\}$$

Gate-Drain Capacitance (cgd)

The gate-drain capacitance has value only in the linear region.

Strong Inversion Linear Region:

vgs > vth and vds < vdsat

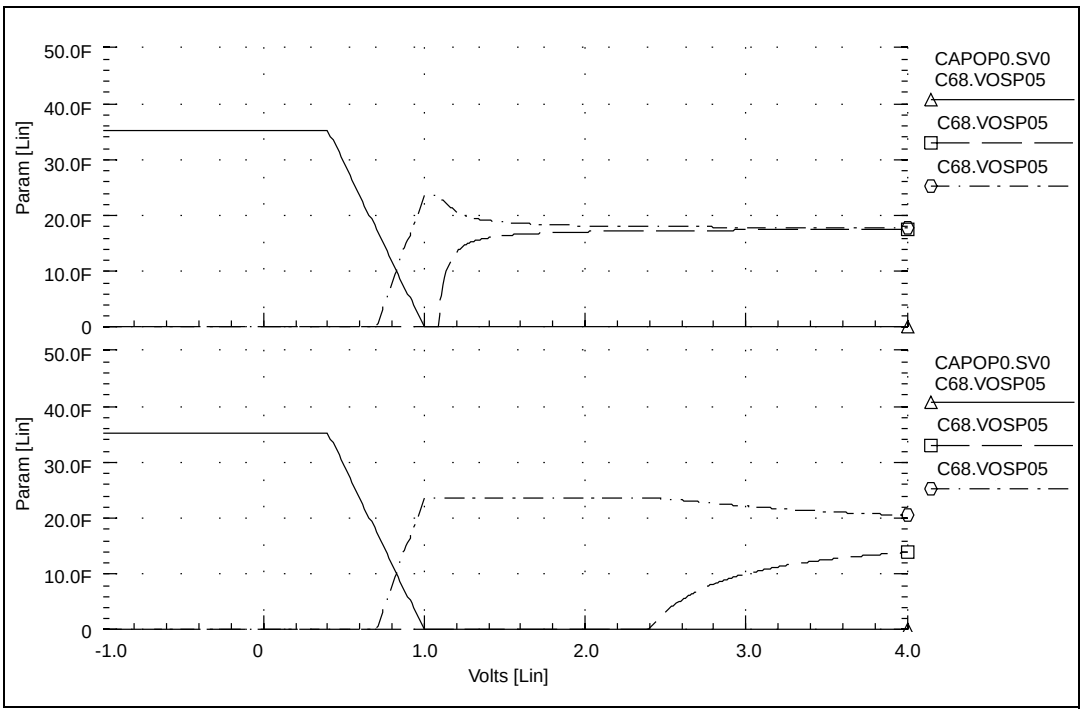
$$cgd = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vdsat + vsb}{2 \cdot (vdsat + vsb) - vds - vsb}\right]^2\right\}$$

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/capop0.sp`

Figure 19 CAPOP=0 Capacitances



CAPOP=1 — Modified Meyer Gate Capacitances

Define: $cap = COXscaled \cdot Weff \cdot Leff$

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. You cannot change the values of these parameters.

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb – vsb

$$cgb = cap$$

Depletion, vgs ≤vth

$$cgb = \frac{cap}{\left[1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right]^{CGBEX}}$$

Strong Inversion, vgs > vth

$$cgb = \frac{G^{+} \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (vsb + PHI)^2 + vsb + PHI}{GAMMA^2}\right]^{CGBEX}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs ≤ vth

$$cgs = CF5 \cdot cap \cdot G^{-} \cdot D^{-}$$

Weak Inversion, vgs < vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{\frac{vgs - vth}{0.1} \cdot \left[1 - \left(\frac{0.1 - vds}{0.2 - vds}\right)^2 - D^{-}\right] + D^{-}\right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\}$$

High vds (vds ≥ 0.1)

Accumulation, vgs ≤vth

$$cgs = CF5 \cdot cap \cdot G^{-}$$

Saturation Region, vgs < vth + vds

$$cgs = CF5 \cdot cap$$

Linear Region, vgs ≥ vth + vds

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\}$$

Gate-Drain Capacitance (cgd)

Low vds (vds < 0.1)

Accumulation, vgs ≤ vth

$$cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{+}$$

Weak Inversion, vgs < vth + 0.1

$$cgd = CF5 \cdot cap \cdot \left\{ D^{+} + \frac{vgs - vgh}{0.1} \cdot \max\left[0, 1 - \left(\frac{0.1}{0.2 - vds} \right)^{2} - D^{+} \right] \right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+}, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^{2} \right\}$$

High vds (vds ≥ 0.1)

Accumulation, vgs ≤ vth: $cgd = CF5 \cdot cap \cdot G^{-} \cdot D^{+}$

Saturation Region, vgs < vth + vds: $cgd = CF5 \cdot cap \cdot D^{+}$

Strong Inversion, vgs ≥ vth + vds:

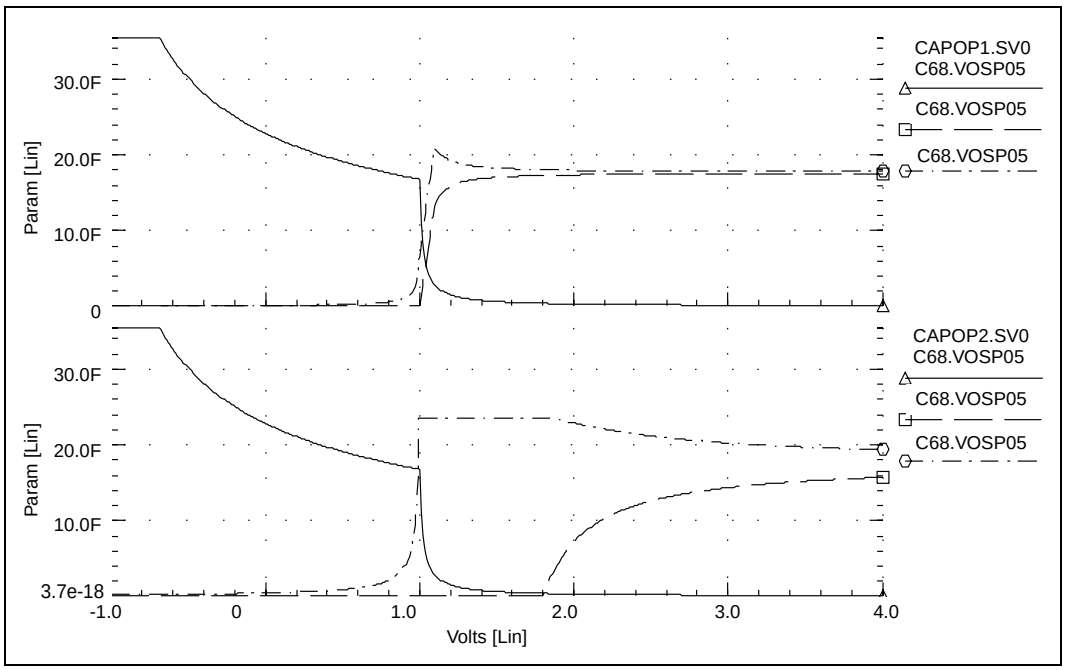
$$cgd = CF5 \cdot cap \cdot \max\left\{ D^{+}, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^{2} \right\}$$

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/capop1.sp`

Figure 20 CAPOP=1 Capacitances



CAPOP=2—Parameterized Modified Meyer Capacitance

The CAPOP=2 Meyer capacitance model is the more general form of Meyer capacitance. The CAPOP=1 Meyer capacitance model is the special case of CAPOP=2 if CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. You cannot change the values of these parameters.

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb - vsb: $cgb = cap$

Depletion, vgs ≤ vth:

$$cgs = \frac{cap}{\left(1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$$

Inversion, vgs > vth:

$$cgb = \frac{G^{+} \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^{2}}\right]^{1/2}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs < vth – CF1:

$$cgs = CF5 \cdot cap \cdot G^{-} \cdot D^{-}$$

Depletion, vgs ≤ vth + CF2 – CF1:

$$cgs = CF5 \cdot cap \cdot \left\{\frac{vgs - vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot CF2 - vds}\right)^{2} - D^{-}\right] + D^{-}\right\}$$

Strong Inversion, vgs > vth + max (CF2 – CF1, CF3 · vds)
UPDATE=0

Strong Inversion, vgs > vth + CF2 – CF1,UPDATE=1:

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth + CF1 - vds}{2 \cdot (vgs - vth + CF1) - vds}\right]^{2}\right\}$$

High vds (vds ≥ 0.1)

Accumulation, vgs < vth – CF1:

$$cgs = CF5 \cdot cap \cdot G^{-} \cdot D^{+}, \qquad CF1 \neq 0$$

$$cgs = CF5 \cdot cap \cdot G^{-}, \qquad CF1 = 0$$

Weak Inversion, vgs < vth + CF2 – CF1, CF1 ≠ 0:

$$cgs = CF5 \cdot cap \cdot \max\left(\frac{vgs - vth + CF1}{CF2}, D^{+}\right)$$

Saturation Region, vgs < vth + CF3 · vds:

$$cgs = CF5 \cdot cap$$

Linear Region, vgs > vth + CF3 · vds:

$$cgs = CF5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2\right\},\quad \text{UPDATE=0,}\quad \text{CF1=0}$$

$$cgs = CG5 \cdot cap \cdot \left\{1 - \left[\frac{vgs - vth - CF3 \text{ Þ } vds}{2 \cdot (vgs - vth) - CF3 \text{ Þ } vds}\right]^2\right\},\quad \text{UPDATE=1}$$

Gate-Drain Capacitance (cgd)

Low vds, (vds < 0.1)

Accumulation, vgs ≤ vth – CF1:

$$cgd = CF5 \cdot cap \cdot G^- \cdot D^-$$

Weak Inversion, vgs < vth + CF2 – CF1:

$$cgd = CF5 \cdot cap \cdot \left\{D^- + \frac{vgs - vth + CF1}{CF2} \cdot \max\left[0, 1 - \left(\frac{CF2}{2 \cdot CF2 - vds}\right)^2 - D^-\right]\right\}$$

Strong Inversion, vgs ≥ vth + CF2 – CF1:

$$cgd = CF5 \cdot cap \cdot \max\left\{D^-, 1 - \left[\frac{vgs - vth + CF1}{2 \cdot (vgs - vth + CF1) - vds}\right]^2\right\}$$

High vds (vds > 0.1)

Accumulation, vgs ≤ vth – CF1:

$$cgd = CF5 \cdot cap \cdot G^- \cdot DD^+$$

Saturation Region, vgs ≤ vth + CF3 · vds:

$$cgd = CF5 \cdot cap \cdot DD^+$$

DD^+ is a function of CF3, if UPDATE=1.

Linear Region, vgs > vth + CF3 · vds:

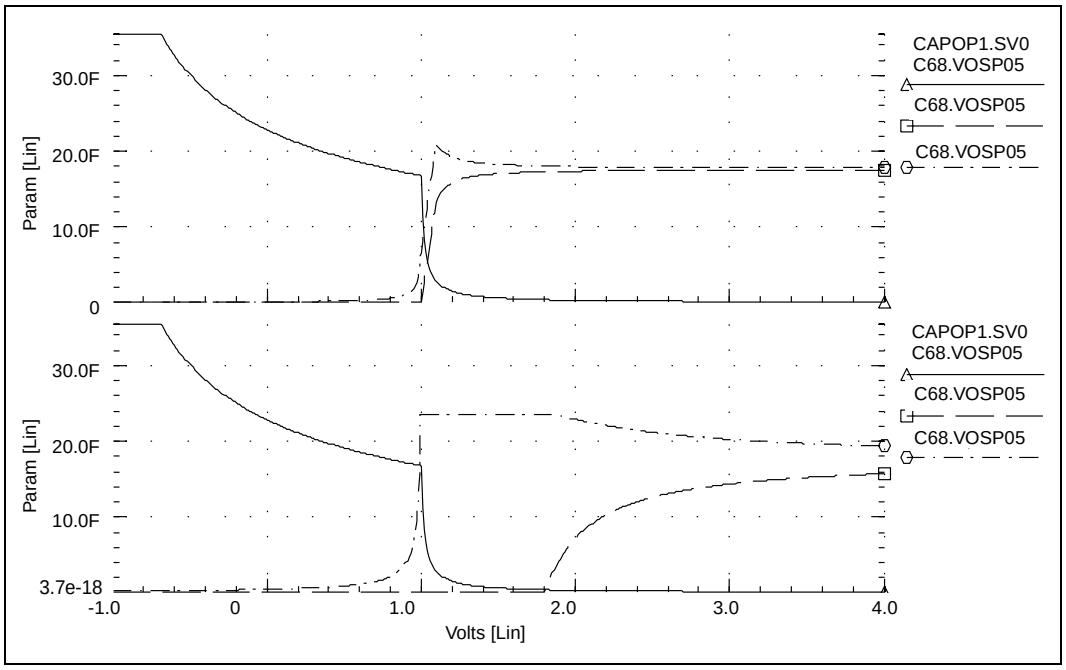
$$cgd = CF5 \cdot cap \cdot \max\left\{DD^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - CF3 \text{ Þ } vds}\right]^2\right\}$$

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/capop2.sp`

Figure 21 CAPOP=2 Capacitances



CAPOP=3 — Gate Capacitances (Simpson Integration)

The CAPOP 3 model uses the same set of equations and parameters as the CAPOP 2 model. Simulation obtains the charges using Simpson numeric integration instead of the box integration found in the CAPOP 1, 2, and 6 models.

Gate capacitances are not constant values with respect to voltages. The incremental capacitance best describes the capacitance values:

$$C(v) = \frac{dq(v)}{dv}$$

In the preceding equation, q(v) is the charge on the capacitor, and v is the voltage across the capacitor.

The formula for calculating the differential is difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

The charge is:

$$q(v) = \int_0^v C(v)dv$$

To calculate the current:

$$i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right)\int_0^v C(v)dv$$

For small intervals:

$$I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$$

In SPICE, the following equation approximates the integral:

$$I(n+1) = \left(\frac{V(n+1) - V(n)}{t(n+1) - t(n)}\right) \cdot \left(\frac{C[V(n+1)] + C[V(n)]}{2}\right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. To accurately estimate the charge, use Simpson's numerical integration rule. This method provides charge conservation control.

To use this model parameter:

1. Set the CAPOP model parameter to 3 and use the existing CAPOP=2 model parameters.
2. Modify the **.OPTION** RELV (relative voltage tolerance), **.OPTION** RELMOS (relative current tolerance for MOSFETs), and **.OPTION** CVTOL (capacitor voltage tolerance) settings.

The default of 0.5 is a good nominal value for CVTOL. The CVTOL option uses the following equation to set the number of integration steps:

$$n = \frac{|V(n+1) - V(n)|}{CVTOL}$$

Using a large value for CVTOL decreases the number of integration steps for the n to n+1 time interval; this yields slightly less accurate integration results. Using a small CVTOL value increases the computational load, and sometimes severely.

CAPOP=4 — Charge Conservation Capacitance Model

The charge conservation method (See *Ward, Donald E. and Robert W. Dutton "A Charge-Oriented Model for MOS Transistor"*) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in LEVEL 3 models. Also, the channel charge partition is not continuous from the linear region to the saturation region.

In the Synopsys MOSFET device models, these problems are corrected. If you specify the CAPOP=4 model parameter, then simulation uses the level-dependent recommended charge conservation model. The XQC model parameter selects the ratio of channel charge partitioning between drain and source.

For example, if you set XQC=.4, then in the saturation region, 40% of the channel charge is associated with the drain and the remaining 60% is associated with the source. In the linear region, the ratio is 50/50. Simulation uses an empirical equation to make a smooth transition from 50/50 (linear region) to 40/60 (saturation region).

The capacitance coefficients are the derivative of gate, bulk, drain, and source charges, and are continuous. LEVEL 2, 3, 4, 6, 7, and 13 models include a charge-conservation capacitance model. To invoke this model, set CAPOP=4.

The following example compares only the CAPOP=4 charge conservation capacitance and the CAPOP=9 improved charge conservation capacitance for the LEVEL 3 model. The CGS and CGD capacitances for CAPOP=4 model (SPICE2G.6) show discontinuity at the boundary between the saturation and linear regions. The CAPOP=9 model does not have discontinuity. For comparison, the modified Meyer capacitances (CAPOP=2) is also provided. The shape of CGS and CGD capacitances resulting from CAPOP=9 are much closer to those of CAPOP=2.

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/mcap3.sp`

Figure 22 CAPOP=4, 9 Capacitances for LEVEL 3 Model

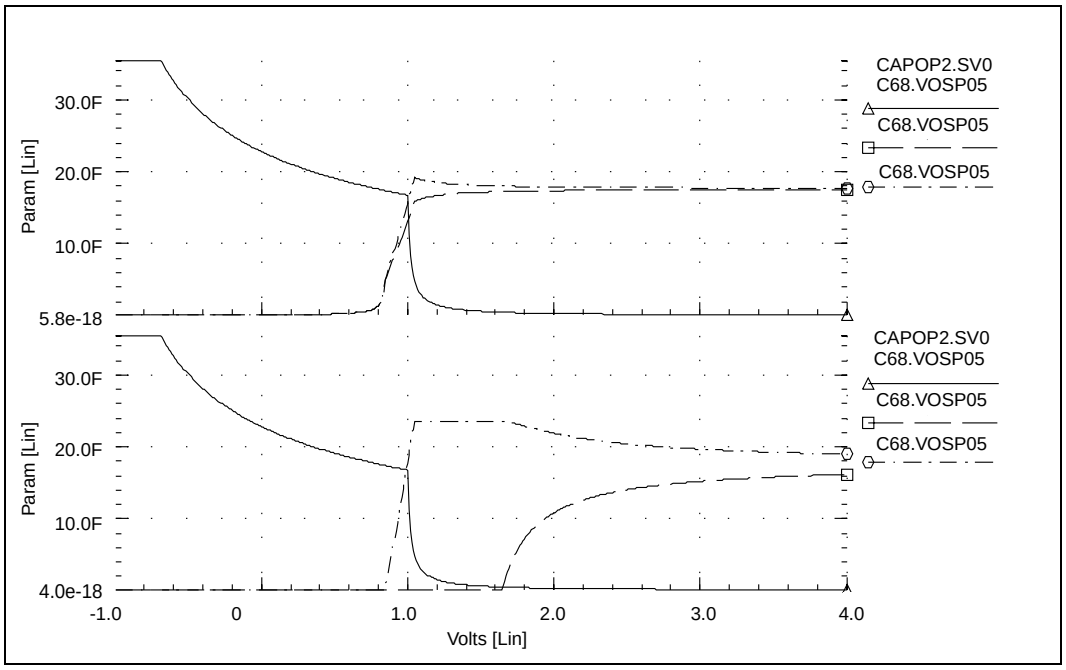
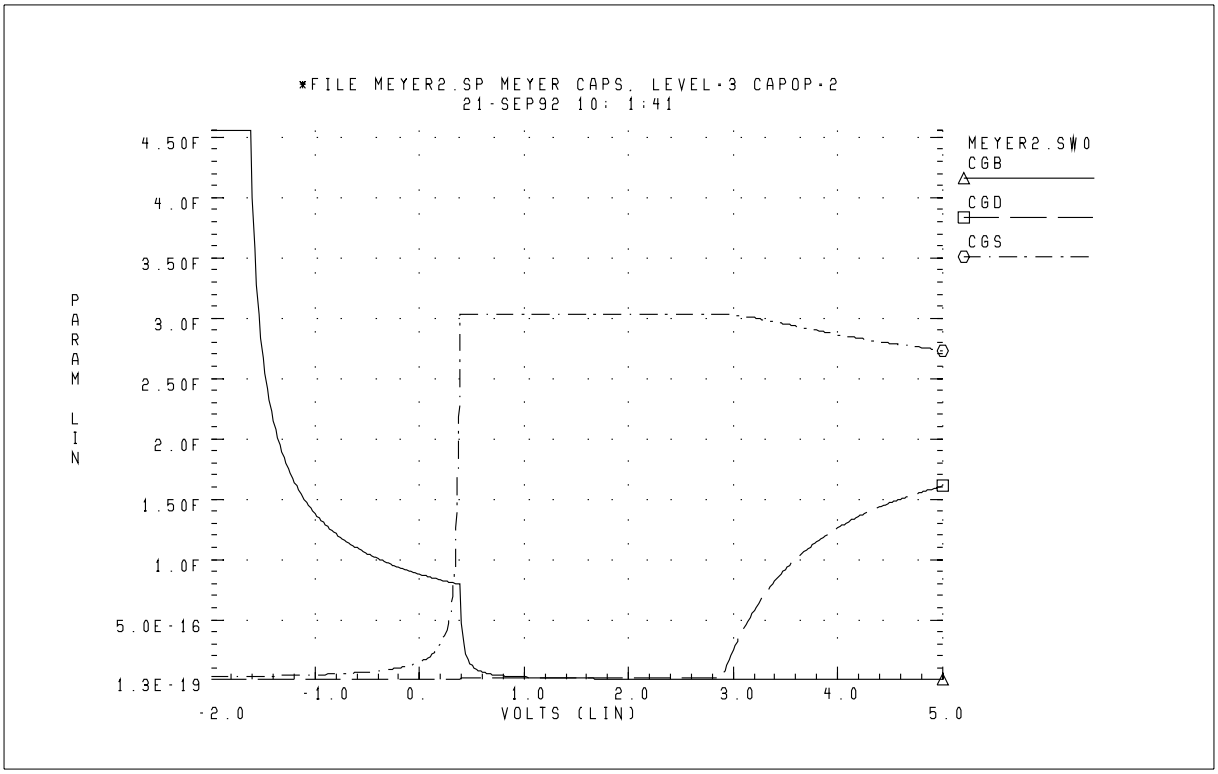


Figure 23 CAPOP=2 Capacitances for LEVEL 3 Model



The example below tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chaterjee ‘An Investigation of the Charge Conservation Problem’) and compares the Meyer and charge conservation models. As the graph in Figure 25 shows, the charge conservation model returns more accurate results.

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/chrgpump.sp`

Figure 24 Charge Pump Circuit

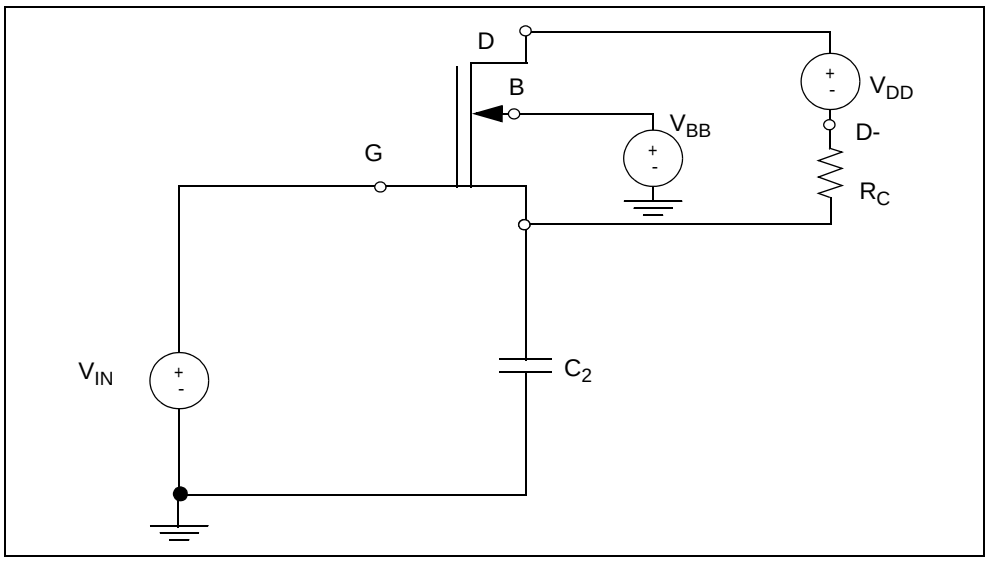
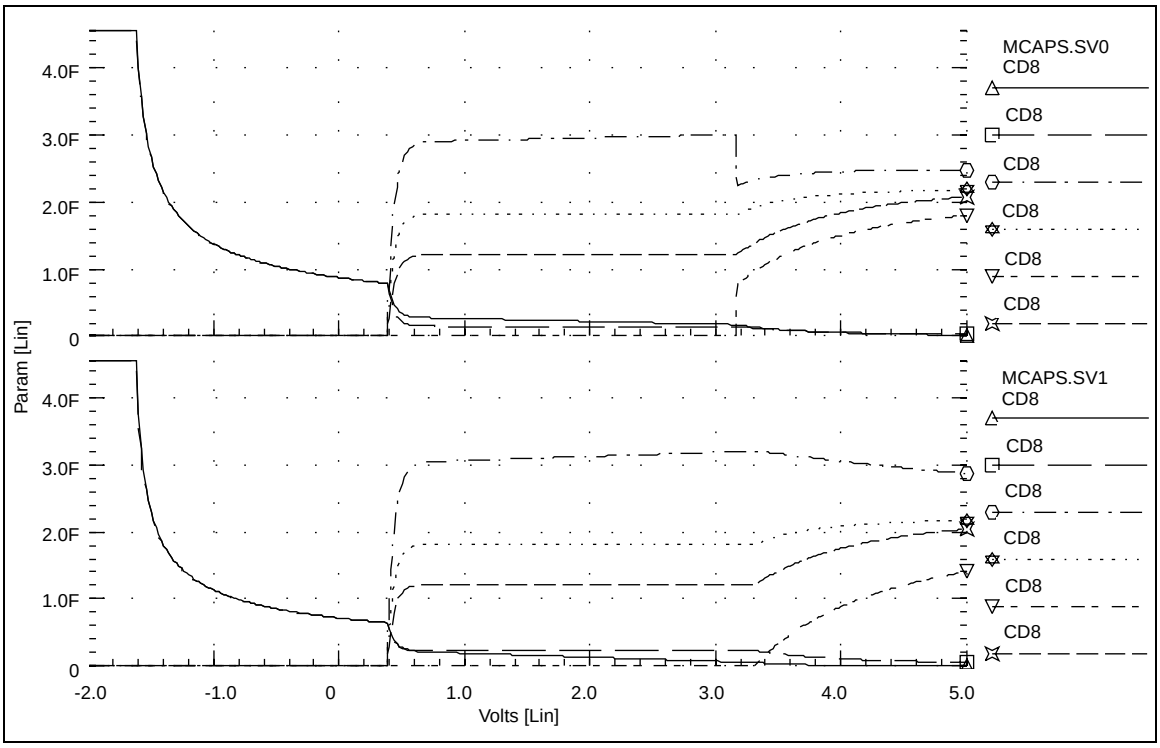


Figure 25 Charge Conservation Test: CAPOP=2 or 9



The following example applies a pulse through a constant capacitance to the gate of a MOS transistor. Ideally, if the model conserves charge, then the voltage at node 20 should become zero when the input pulse becomes zero. Consequently, the model that provides voltage closer to zero for node 20 conserves the charge better. The results of the CAPOP=4 model are better than the CAPOP=2 model.

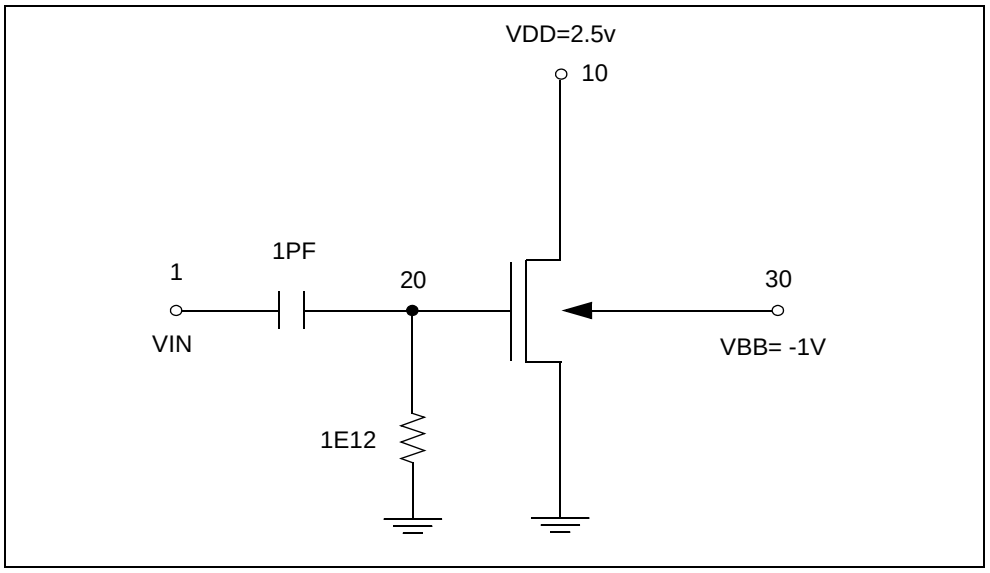
This example compares charge conservation models in SPICE2G.6 and Synopsys device models. The results indicate that the Synopsys device models are more accurate.

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/mcap2_a.sp`

Figure 26 Charge Conservation Test Circuit



CAPOP=5 — No Gate Capacitance

If CAPOP=5 for no capacitors, then simulation does not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define:

$$vgst = vgs - \frac{(vth + vfb)}{2}$$

$$cox = \frac{\varepsilon ox}{TOX \cdot 1e\text{-}10} \cdot Weff \cdot Leff$$

The following equations calculate the cgs gate capacitance in the different regions.

0.5 · (vth + vfb) > vgs

$$cgs = 0$$

0.5 · (vth + vfb) <vgs <vth

For vgst < vds:

$$cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

For vgst > vds:

$$cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

vgs > vth

For vgst < vds:

$$cgs = \frac{2}{3} \cdot cox$$

For vgst > vds:

$$cgs = arg \cdot \frac{2}{3} \cdot cox \qquad arg = vgst \cdot \frac{(3 \cdot vgst - 2 \cdot vds)}{(2 \cdot vgst - vds)^2}$$

The following equations calculate the cgd gate capacitance in the different regions.

vgs < vth

$$cgd = 0$$

vgs > vth and vgst < vds

$$cgd = 0$$

vgs > vth and vgst > vds

$$cgd = arg \cdot \frac{2}{3} \cdot cox$$

$$arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

The following equation combines the cgb gate capacitance with the calculation of both oxide capacitance and depletion capacitance:

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

Simulation calculates the oxide capacitance (cgbx) as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance (cd) is voltage-dependent:

$$cd = \frac{\varepsilon si}{wd} \cdot Weff \cdot Leff \qquad wd = \left(\frac{2 \cdot \varepsilon si \cdot vc}{q \cdot NSUB}\right)^{1/2}$$

vc = The effective voltage from channel to substrate (bulk)

The following equations show vc under various conditions:

vgs + vsb < vfb $vc = 0$

vgs + vsb > vfb $vc = vgs + vsb - vfb$

vgst > 0, vgs < vth, vgst < vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

vgst > 0, vgs < vth, vgst > vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

vgs > vth, vgst < vds $vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$

vgs > vth, vgst > vds $vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$

CAPOP=11 — Ward-Dutton model specialized (LEVEL 2)

CAPOP=12 — Ward-Dutton model specialized (LEVEL 3)

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

See LEVEL 13 BSIM Model on page 324.

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See LEVEL 39 BSIM2 Model on page 358.

Calculating Effective Length and Width for AC Gate Capacitance

For some MOS processes and parameter extraction method. AC analysis might need different Leff and Weff values than for DC analysis. For AC gate capacitance calculations, substitute the LDAC and WDAC model parameters for LD and WD in the Leff and Weff calculations. You can use LD and WD in Leff and Weff calculations for DC current.

To use LDAC and WDAC, enter XL, LD, LDAC, XW, WD, and WDAC in the **.MODEL** statement. The model uses the following equations for DC current calculations.

$$Leff = L + XL - 2 \cdot LD$$

$$Weff = W + XW - 2 \cdot WD$$

The model parameters also use the following equations to calculate the AC gate capacitance:

$$Leff = L + XL - 2 \cdot LDAC$$

$$Weff = W + XW - 2 \cdot WDAC$$

The noise calculations use the DC Weff and Leff values.

Use LDAC and WDAC with the standard XL, LD, XW, and WD parameters. Do not use LDAC and WDAC with other parameters, such as DL0 and DW0.

Noise Models

This section describes how to use noise models.

Table 22 Noise Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent.
KF		0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V^2F.
NLEV		2.0	Noise equation selector.
GDSNOI		1.0	Channel thermal noise coefficient (use with NLEV=3).

The MOSFET model noise equations have a selector parameter, NLEV, that selects either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

You can model thermal noise generation in the drain and source resistors as two sources, inrd and inrs (units amp/$(Hz)^{1/2}$) as shown in Figure 10 on page 37. The following equations calculate the values of these sources:

$$inrs = \left(\frac{4kt}{rs}\right)^{1/2} \qquad inrd = \left(\frac{4kt}{rd}\right)^{1/2}$$

You can model the channel thermal noise and the flicker noise as the ind current source, which the following equation defines:

$$ind^2 = (channel \text{ thermal noise})^2 + (\text{flicker noise})^2$$

If the NLEV model parameter is less than 3, then:

$$channel \text{ thermal noise} = \left(\frac{8kT \cdot gm}{3}\right)^{1/2}$$

The preceding formula, used in both saturation and linear regions, can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation, which is valid in both linear and saturation regions. See *Tsividis, Yanis P., Operation and Modeling of the MOS Transistor, McGraw-Hill, 1987, p. 340*.

For NLEV=3:

$$channel \text{ thermal noise} = \left(\frac{8kt}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNOI\right)^{1/2}$$

The following equations calculate the *a* value used in the preceding equation:

$$a = 1 - \frac{vds}{vdsat} \qquad \text{Linear region}$$

$$a = 0 \qquad \text{Saturation region}$$

Use the AF and KF parameters in the small-signal AC noise analysis to determine the equivalent flicker noise current generator, which connects the drain to the source.

NLEV=0 (SPICE): $\text{flicker noise} = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Leff^2 \cdot f}\right)^{1/2}$

For NLEV=1, $Leff^2$ in the above equation is replaced by Weff · Leff.

NLEV=2, 3: $\text{flicker noise} = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}}\right)^{1/2}$

Parameter	Description
RD, V^2/Hz	Output thermal noise due to drain resistor.
RS, V^2/Hz	Output thermal noise due to source resistor.
RX	Transfer function of channel thermal or flicker noise to the output. This is not a noise, it is a transfer coefficient, reflecting the contribution of channel thermal or flicker noise to the output.
ID, V^2/Hz	Output channel thermal noise: ID = RX^2Þ (channel thermal noise)^2.
FN, V^2/Hz	Output flicker noise: FN = RX^2Þ (flicker noise)^2.
TOT, V^2/Hz	Total output noise: TOT = RD + RS + ID + FN.

Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The TLEV and TLEVC parameters select the temperature equations used to calculate the temperature effects on the model parameters.

Table 23 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Low field mobility, UO, temperature exponent.
CTA	1/°K	0.0	Junction capacitance (CJ) temperature coefficient. If TLEVC=1, CTA overrides the default temperature compensation.

Table 23 Temperature Effects Parameters (Continued)

Name (Alias)	Units	Default	Description
CTP	1/°K	0.0	Junction sidewall capacitance (CJSW) temperature coefficient. If TLEVC=1, CTP overrides the default temperature compensation.
EG	eV		Energy gap for pn junction diode for TLEV=0 or 1, default=1.11; for TLEV=2, default=1.16 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide
F1EX		0	Bulk junction bottom grading coefficient
GAP1	eV/°K	7.02e-4	First bandgap correction factor (from Sze, alpha term). 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide
GAP2	°K	1108	Second bandgap correction factor (from Sze, beta term). 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide
LAMEX	1/°K	0	LAMBDA temperature coefficient.
N		1.0	Emission coefficient.
MJ		0.5	Bulk junction bottom grading coefficient.
MJSW		0.33	Bulk junction sidewall grading coefficient.
PTA	V/°K	0.0	Junction potential (PB) temperature coefficient. If you set TLEVC to 1 or 2, PTA overrides the default temperature compensation.

Table 23 Temperature Effects Parameters (Continued)

Name (Alias)	Units	Default	Description
PTC	V/°K	0.0	Fermi potential (PHI) temperature coefficient. If you set TLEVC to 1 or 2, PTC overrides the default temperature compensation.
PTP	V/°K	0.0	Junction potential (PHP) temperature coefficient. If TLEVC=1 or 2, PTP overrides the default temperature compensation.
TCV	V/°K	0.0	Threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel.
TLEV		0.0	Temperature equation level selector. Set TLEV=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEV for ASPEC.
TLEVC		0.0	Temperature equation level selector for junction capacitances and potentials. Interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEVC for ASPEC.
TRD	1/°K	0.0	Temperature coefficient for drain resistor.
TRS	1/°K	0.0	Temperature coefficient for source resistor.
XTI		0.0	Saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode.

MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) include length and width sensitivity parameters as shown in Table 24. Use these parameters with the Automatic Model Selector to enable more accurate modeling for various

device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Table 24 MOS Temperature Coefficient Sensitivity Parameters

Parameter	Description	Sensitivity Parameters		
		Length	Width	Product
BEX	Low field mobility, UO, temperature exponent	LBEX	WBEX	PBEX
FEX	Velocity saturation temperature exponent	LFEX	WFEX	PFEX
TCV	Threshold voltage temperature coefficient	LTCV	WTCV	PTCV
TRS	Temperature coefficient for source resistor	LTRS	WTRS	PTRS
TRD	Temperature coefficient for drain resistor	LTRD	WTRD	PTRD

Temperature Equations

This section describes how to use temperature equations.

Energy Gap Temperature Equations

These equations set the energy gap for temperature compensation:

TLEV = 0 or 1:

$$egnom = 1.16 - 7.02e{-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e{-}4 \cdot \frac{t^2}{t + 1108.0}$$

TLEV = 2:

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

$$isbd(t) = isbd(tnom) \cdot e^{facln/N}$$

$$isbs(t) = isbs(tnom) \cdot e^{facln/N}$$

The following equation calculates the facln value used in the preceding equations:

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

MOSFET Diode Models on page 39 defines the *isbd* and *isbs* values.

MOS Diode Capacitance Temperature Equations

TLEVC selects the temperature equation level for MOS diode capacitance.

TLEVC=0:

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1\right)\right]$$

TLEVC=1:

$$PB(t) = PB - PTA \cdot \Delta t \qquad PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t) \qquad CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t) \qquad CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

TLEVC=2:

$$PB(t) = PB - PTA \cdot \Delta t \qquad PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)}\right)^{MJSW}$$

TLEVC=3:

$$PB(t) = PB + dpbdt \cdot \Delta t \qquad PHP(t) = PHP + dphpdt \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB}\right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\Delta t}{PHP}\right)$$

If TLEVC=3 and TLEV=0 or 1, then:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHP\right]}{tnom}$$

TLEV=2:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Surface Potential Temperature Equations

TLEVC=0:

$$PHI(t) = PHI \cdot \left(\frac{t}{tnom}\right) - vt(t) \text{ Þ} \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1:

$$PHI(t) = PHI - PTC \text{ Þ} \Delta t$$

If you do not specify the PHI parameter, simulation calculates it as:

$$PHI(t) = 2 \cdot vt(t) \cdot \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, ni, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \left(\frac{t}{tnom}\right)^{3/2} \cdot \exp\left[EG \cdot \left(\frac{t}{tnom} - 1\right) \cdot \left(\frac{1}{2 \cdot vt(t)}\right)\right]$$

TLEVC=2: $PHI(t) = PHI - PTC \text{ Þ} \Delta t$

TLEVC=3: $PHI(t) = PHI + dphidt \cdot \Delta t$

If TLEVC=3 and TLEV=0 or 1, then:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHI\right]}{tnom}$$

TLEV=2:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHI\right]}{tnom}$$

Threshold Voltage Temperature Equations

The threshold temperature equations are:

TLEV=0:

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=1:

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=2:

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Channel Length Modulation Temperature Equation

If you specify the LAMEX model parameter, then the temperature modifies the LAMBDA value.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t)$$

Calculating Diode Resistance Temperature Equations

The following equations are examples of the effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t)$$

$$RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

3

Common MOSFET Model Parameters

Lists and describes parameters that are common to several or all MOSFET model levels.

Parameters that are unique to a specific MOSFET model level are described in later chapters, as part of the description of the specific model level that uses the parameter.

Basic MOSFET Model Parameters

In this section,

- Table 25 lists the basic MOSFET model parameters
- Table 26 lists effective width and length parameters
- Table 27 lists threshold voltage parameters
- Table 28 lists mobility parameters.

Table 25 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
LEVEL		1.0	DC model selector: • LEVEL=1 (default) is the Schichman-Hodges model. • LEVEL=2 is the Grove-Frohman model. • LEVEL=3 is an empirical model. • LEVEL=4 is a modified version of Level 2. • LEVEL=5 is the IDS model with enhancement and depletion modes. • LEVEL=6 is the Lattin-Jenkins-Grove model us using ASPEC-style parasitics. • LEVEL=7 is the Lattin-Jenkins-Grove model us using SPICE-style parasitics. • LEVEL=8 is an advanced model using finite differences. • LEVEL=13 is the University of California (UC) Berkeley BSIM1 model. • LEVEL=27 is the SOSFET model. • LEVEL=28 is a Synopsys proprietary model, based on the UC Berkeley BSIM1 model, Level 13. • LEVEL=38 is the Cypress Depletion model. • LEVEL=39 is the UC Berkeley BSIM2 model. • LEVEL=40 is the Hewlett-Packard amorphous-silicon Then-Film Transistor (a-Si TFT) model.	All levels

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
LEVEL *(continued)*			• LEVEL=47 is the UC Berkeley BSIM3 version 2 model. • LEVEL=49 is a Synopsys proprietary model, based on the UC Berkeley BSIM3 version 3 model, Level 53. • LEVEL=50 is the Philips MOS9 model. • LEVEL=53 is the original UC Berkeley BSIM3 version 3 model, not modified as Level 49 is. • LEVEL=54 is the UC Berkeley BSIM4 model. • LEVEL=55 is the EPFL-EKV model. • LEVEL=57 is the UC Berkeley BSIM3-SOI Partially-Depleted (PD) model. • LEVEL=58 is the University of Florida SOI model. • LEVEL=59 is the UC Berkeley BSIM3-SOI Fully-Depleted (FD) model. • LEVEL=60 is the UC Berkeley BSIM3-SOI Dynamically-Depleted (DD) model. • LEVEL=61 is the Rensselaer Polytechnic Institute (RPI) a-Si TFT model. • LEVEL=62 is the Rensselaer Polytechnic Institute (RPI) poly-silicon Thin-Film Transistor (Poli-Si TFT) model. • LEVEL=63 is the Philips MOS11 model. • LEVEL=64 is the Hiroshima STARC IGFET (HiSIM) model.	All Levels
ACM	-	0	Selects MOS S/D parasitics. ACM=0 is SPICE style. Use ACM=2 or 3 for LDD.	39
ALPHA	V^{-1}	0	Impact ionization coefficient. This parameter includes geometry-sensitivity parameters. Choose between BSIM2 (A10>0 and HSPICE (ALPHA>0) impact ionization modeling. *Do not use both.*	39

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
CAPOP	-	*	MOS gate cap model selector: CAPOP=39 for BSIM2 or CAPOP=13 for BSIM1. CAPOP=4 is the same as CAPOP=13. • If SPICE3=0, default CAPOP=13 • If SPICE3=1, default CAPOP=39	4, 13 39
CGBO	F/m	-	Gate-to-bulk overlap capacitance. If you specify WD and TOX, but you do not specify CGBO, then simulation calculates CGBO.	39
CGDO	F	1.0p	TFT gate-to-drain overlap capacitance.	40
	F/m	-	Gate-to-drain overlap capacitance. If you specify TOX, and you specify either LD or METO, but you do not specify CGDO, then simulation calculates CGDO.	39
CGSO	F	1.0p	TFT gate-to-source overlap capacitance.	40
	F/m	-	Gate-to-source overlap capacitance. If you specify TOX, but you do not specify either LD or METO, and you do not specify CGSO, then simulation calculates CGSO.	39
CHI		0.5	Temperature exponential part.	40
CJ	F/m^2	0	Source/drain bulk zero-bias junction capacitance.	39
CJSW	F/m	0	Sidewall junction capacitance.	39
CLM (GDS)		0.0	Selects a channel length modulation equation.	6, 7, 8
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area. If you do not specify COX, simulation calculates it from TOX.	1, 2, 3, 8
CSC	F/m^2	10µ	Space charge capacitance.	40

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
DEFF		2.0	Drain voltage effect for the TFT leakage current.	40
DERIV		1	Derivative method selector: • DERIV=0: analytic • DERIV=1: finite difference	3, 39
DP	µm	1.0	Implant depth (depletion model only).	5, 38
ECRIT (ESAT)	V/cm	0.0	Critical electric field for the carrier velocity saturation. From Grove: • electrons 6e4 • holes 2.4e4. Zero indicates an infinite value. The ECRIT equation is more stable than VMAX. Simulation estimates ECRIT as: ECRIT = 100 · (VMAX / UO)	2, 8
	V/cm	0.0	Drain-source critical field. Zero indicates an infinite value, typically 40,000 V/cm.	6, 7
ECV	V/µm	1000	Critical field.	5, 38
FEFF		0.5	Frequency effect constant.	40
FREQ	Hz	400	Frequency of the device.	40
GO	ohm^{-1}	10e-15	Conductance of the TFT leakage current.	40
IIRAT	-	0	Impact ionization source bulk current partitioning factor. One corresponds to 100% source. Zero corresponds to 100% bulk.	39
JS	A/m^2	0	Source/drain bulk diode reverse saturation current density.	39
K2		2.0	Temperature exponential part.	40

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
KAPPA	V^{-1}	0.2	Saturation field factor. The channel length modulation equation uses this parameter.	3
KCS		2.77	Implant capacitance integration constant.	38
KP (BET, BETA)	A/V^2		Intrinsic transconductance parameter. If you specify U0 and TOX, but you do not specify KP, simulation computes the parameter from: KP = UO · COX. • Level 1 default=2.0718e-5 (NMOS), 8.632e-6 (PMOS). • Level 2, 3 default=2.0e-5	1, 2, 3
LAMBDA (LAM, LA)	V^{-1}	0.0	Channel length modulation.	2, 8
MJ	-	0.5	Source/drain bulk junction grading coefficient.	39
MJSW		0.33	Sidewall junction grading coefficient.	39
NEFF		1.0	Total channel charge (fixed and mobile) coefficient.	2
NI	cm^{-2}	2e11	Implant doping (depletion model only).	5, 38
NU		0.0	First order temperature gradient.	40
PB	V	0.8	Source/drain bulk junction potential.	39
PBSW	V	PB	Sidewall junction potential.	39
PSI		1e-20	Temperature exponential part.	40
RD	ohm	1.0K	(External) drain resistance.	40
RS	ohm	1.0K	(External) source resistance.	40
RSH	ohm/sq	0	Source/drain sheet resistance.	39

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
SNVB	1/(V·cm3)	0.0	Slope of the doping concentration versus vsb (element parameter). (Multiplied by 1e6).	8
SPICE3	-	0	Selects SPICE3 model compatibility. For accurate SPICE3 BSIM2, set SPICE3=1.	39
TAU	s	10n	Relaxation time constant.	40
TCV	V/C	0	Zero-bias threshold voltage temperature coefficient. The sign of TCV adjusts automatically for NMOS and PMOS to decrease the magnitude of the threshold with rising temperature.	39
TOX	m	1e-7	Gate oxide thickness.	1, 2, 3, 8
	Å	0.0	Oxide thickness.	5, 38
	m	7.0e-8	Oxide thickness.	27
TRD	1/K	0.0	Temperature coefficient for the Rd drain diffusion and contact resistances.	54
TREF		1.5	Temperature gradient of UO.	40
TRS	1/K	0.0	Temperature coefficient for the Rs source diffusion and contact resistances.	54
TUH		1.5	Implant channel mobility temperature exponent (depletion model only).	5
UO	$cm^2/(V·s)$		Carrier mobility. Default for LEVEL 40 is 1.0.	1, 40
UO (UB, UBO)	$cm^2/(V·s)$	600 (N) 250 (P)	Low-field bulk mobility.Simulation calculates this parameter from the KP value that you specify.	2

Table 25 Basic MOSFET Model Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
VB0 (VB)	V	0.0	Reference voltage for the GAMMA switch. • If vsb < VB0, the equation uses GAMMA. • If vsb > VB0, the equation uses LGAMMA.	6, 7
VCR	V	0	Impact ionization critical voltage. This parameter includes geometry-sensitivity parameters.	39
VMAX (VMX, VSAT)	m/s	0.0	Maximum drift velocity of the carriers. Zero indicates an infinite value. Default VMAX value for Level 40 is 1e6.	2, 3, 8, 40
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of the carriers. Selects a calculation scheme to use for vdsat. Zero indicates an infinite value. Typical values: • electrons8.4e6 cm/s • holes4.3e6 cm/s	6, 7
VTIME	s	10m	Voltage stress.	40
ZENH		1.0	Mode flag (enhancement). Set ZENH=0.0 for the depletion mode.	5

Table 26 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
DEL	m	0.0	Channel length reduction on each side: $DEL_{scaled} = DEL \cdot SCALM$ MOSFET Level 13 does not support DEL.	1, 2, 3, 6, 7, 8, 38
DEL (WDEL)	µm	0.0	Channel length reduction on each side	5

Table 26 Effective Width and Length Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
DELVTO	V	0	Threshold voltage shift. This parameter is type sensitive. For example, DELVTO>0 increases the magnitude of the n-channel threshold, decreases the magnitude of the p-channel threshold, and adds to the element-line DELVTO parameter.	39
LATD (LD)	μm	1.7 · XJ	Lateral diffusion on each side	5, 38
LDAC	m		This parameter is the same as LD, but if you specify LDAC in the **.MODEL** statement, it replaces LD in the Leff calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 38, 39
LMLT		1.0	Gate length shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 39
			Scale MOSFET drawn length	54
LD (DLAT, LATD)	m		Lateral diffusion into the channel from the source and the drain diffusion. • If you do not specify LD and XJ: LD Default=0.0 • If you specify XJ, but you do not specify LD, simulation calculates LD as: LD default=0.75 · XJ LD_{scaled} = LD · SCALM	1, 2, 3, 6, 7, 8, 13, 28
LD	m	0	Lateral diffusion under the gate (per side) of the S/D junction. Use this parameter to calculate L_{eff} only if DL=0: LD_{scaled} = LD · SCALM	39

Table 26 Effective Width and Length Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
LREF	m	0.0	Channel length reference: $LREF_{scaled} = LREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity.	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	Reference channel length to adjust the length of the BSIM model parameters. For Berkeley compatibility (LREF-> ∞), use: LREF=0. $LREF_{scaled} = LREF \cdot SCALM$	39
OXETCH	µm	0.0	Oxide etch	5, 38
Px	*[x]P*µµ^2	0	P*x* is a Synopsys proprietary, WL-product sensitivity parameter, where *x* is a model parameter with length and width sensitivity.	39
WD	m	0.0	Lateral diffusion into the channel from the bulk along the width: $WD_{scaled} = WD \cdot SCALM$	1, 2, 3, 6, 7, 8, 13
	m	0	Channel stop lateral diffusion under the gate (per side). Use this parameter to calculate W_{eff} only if DW=0. WD scaled=WD · SCALM	39
WDAC	m		This parameter is the same as WD, but if you specify WDAC in the **.MODEL** statement, it replaces WD in the Weff calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 39
WMLT		1.0	Diffusion layer and width shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 54
	-	1.0	Diffusion and gate width shrink factor.	39
			Scale MOSFET drawn width	54

Table 26 Effective Width and Length Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
WREF	m	0.0	Channel width reference: $WREF_{scaled} = WREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity.	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	Reference device width to adjust the width of the BSIM model parameters. For Berkeley compatibility (WREF-> ∞), use WREF=0: $WREF_{scaled} = WREF \cdot SCALM$	39
XJ	m	0.0	Metallurgical junction depth: $XJ_{scaled} = XJ \cdot SCALM$	1, 2, 3, 6, 7, 8
	μm	1.5	Junction depth	5, 38
XL (DL, LDEL)	m	0.0	Length bias accounts for the masking and etching effects (length): $XL_{scaled} = XL \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28, 39
XL	m	0	Difference between the physical (on the wafer) and the drawn reference channel length. Use this parameter to calculate L_{eff} only if DL=0: XLscaled = XL · SCALM	39, 54
XLREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel length: XLREFscaled = XLREF · SCALM	28, 39
XW (DW, WDEL)	m	0.0	Width bias accounts for the masking and etching effects (width): $XW_{scaled} = XW \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28
XW	m	0	Difference between the physical (on the wafer) and the drawn S/D active width. Use this parameter to calculate W_{eff} only if DW=0: $XW_{scaled} = XW \cdot SCALM$	39, 54

Table 26 Effective Width and Length Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
XWREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel width: XWREFscaled = XWREF · SCALM	28, 39

Table 27 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
BetaGam		1.0	Body effect transition ratio.	38
CAV		0.0	Thermal voltage multiplier for the weak inversion equation.	8
DELTA		0.0	Narrow width factor for adjusting the threshold.	2, 3, 8
DNB (NSUB)	cm^{-3}	0.0	Surface doping density.	5, 38
	$1/cm^3$	1.0e15	Substrate doping.	6, 7
DNS (NI)	$1/cm^3$	0.0	Surface substrate doping.	6, 7
DVIN	V	0.0	Adjusts the empirical surface inversion voltage.	38
DVSBC	V	0.0	Adjusts the empirical body effect transition voltage.	38
E1		3.9	Dielectric constant of first film.	40
E2		0.0	Dielectric constant of second film.	40
ETA	V^{-1} (Level 40)	0.0	Static feedback factor for adjusting the threshold voltage (difficulty of band bending).	3, 40
		0.0	Drain-induced barrier lowering (DIBL) effect coefficient for the threshold voltage.	8
		0.0	Channel-length independent drain-induced barrier lowering.	38

Table 27 Threshold Voltage Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
FDS		0.0	Field, drain to source. Controls the threshold reduction due to the source-drain electric field.	6, 7
FSS (NFS)	$cm^{-2} \cdot V^{-1}$	0.0	Number of fast surface states	5, 38
GAMMA	$V^{1/2}$	0.5276	Body effect factor. If you do not specify GAMMA, simulation calculates it from NSUB.	1, 2, 3, 8
	$V^{1/2}$		Body effect factor. • If you do not specify GAMMA, simulation calculates it from DNB. • GAMMA is the body effect, if vsb < VB0. • If vsb > VB0, simulation uses LGAMMA. GAMMA, LGAMMA, and VB0 perform a two-step approximation of a non-homogeneous substrate.	6, 7
LBetaGam.	µm	0.0	BetaGam dependence on the channel length.	38
LDVSBC	V·µm	0.0	Adjusts the L-dependent body effect transition voltage.	38
LETA(DIBL)	µm	0.0	Channel-length dependent drain-induced barrier lowering.	38
LGAMMA	$V^{1/2}$	0.0	This parameter is the body effect factor if vsb > VB0. If you use the Poon-Yau GAMMA expression, LGAMMA is the junction depth in microns. Simulation multiplies LGAMMA by SCALM.	6, 7
LND	µm/V	0.0	ND length sensitivity.	2, 3, 6, 7, 8
LN0	µm	0.0	N0 length sensitivity.	2, 3, 6, 7, 8
LVT (LVTO)	V·µm	0.0	VT dependence on the channel length.	38

Table 27 Threshold Voltage Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
ND	V^{-1} (1/V)	0.0	Drain subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
N0		0.0	Gate subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
NFS (DFS, NF, DNF)	$cm^{-2} \cdot V^{-1}$	0.0	Fast surface state density.	1, 2, 3, 6, 7, 8
NFS	cm^2	0.0	Fast surface state density.	40
NSS	cm^2	0.0	Surface state density.	40
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. If you do not specify NSUB, simulation calculates it from GAMMA.	1, 2, 3, 8
NWE	m	0.0	Narrow width effect, direct compensation of VTO: NWEscaled = NWE · SCALM	6, 7
NWM		0.0	Narrow width modifier.	5, 38
		0.0	Narrow width modulation of GAMMA.	6, 7
PHI	V	0.576	Surface inversion potential. If you do not specify PHI, HSPICE calculates it from NSUB.	1, 2, 3, 8
	V	0.8	Built-in potential.	5, 38
	V	0.0	Surface potential.	40
SCM		0.0	Short-channel drain source voltage multiplier	5, 38
		0.0	Short-channel modulation of GAMMA.	6, 7
T1	m	280n	First thin film thickness.	40
T2	m	0.0	Second thin film thickness.	40
TDVSBC	V/K	0.0	Body effect transition voltage shift due to the temperature.	38

Table 27 Threshold Voltage Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
UFDS		0.0	High field FDS.	6, 7
UPDATE		0.0	Selects different versions of the LEVEL 6 model. For the UPDATE=1 or 2 alternate saturation voltage, simulation modifies the MOB=3 mobility equation and the RS and RD series resistances so they are compatible with ASPEC. UPDATE=1 is a continuous Multi-Level GAMMA model.	6, 7
VFDS	V	0.0	Reference voltage for selecting FDS or UFDS: • Uses FDS if vds ≤ VFDS. • Uses UFDS if vds > VFDS.	6, 7
VSH	V	0.0	Threshold voltage shifter for reducing the zero-bias threshold voltage (VTO) as a function of the ratio of LD to Leff.	6, 7
VT (VTO)	V	0.0	Extrapolated threshold voltage	5, 38
VTO (VT)	V	0.0	Zero-bias threshold voltage. If you do not specify VTO, simulation calculates it.	1, 2, 3, 6, 7, 8, 40
WBetaGam	μm	0.0	BetaGam dependence on the channel width.	38
WDVSBC	V·μm	0.0	Adjusts the W-dependent body effect transition voltage.	38
WETA	μm	0.0	Channel-width dependent drain-induced barrier lowering.	38
WEX			Weak inversion exponent.	6, 7
WIC		0.0	Subthreshold model selector.	2, 3, 6, 7, 8
WND	μm/V	0.0	ND width sensitivity.	2, 3, 6, 7, 8

Table 27 Threshold Voltage Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
WN0	μm	0.0	N0 width sensitivity.	2, 3, 6, 7
WVT (WVTO)	V·μm	0.0	VT dependence on the channel width.	38

Use curve fitting to determine the mobility parameters. Generally, you should set UTRA between 0.0 and 0.5. Nonzero values for UTRA can result in negative resistance regions at the onset of saturation.

Table 28 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
BEX	-	-1.5	Surface channel mobility temperature exponent.	38, 39
BFRC	$Å \cdot s/(cm^2 \cdot V)$	0.0	Field reduction coefficient variation due to the substrate bias.	38
FACTOR			Mobility degradation factor. Default=1.0.	6, 7
FEX	-	0	Temperature exponent for velocity saturation.	39
FRC	$Å \cdot s/cm^2$	0.0	Field reduction coefficient.	5, 38
FRCEX (F1EX)		0.0	Temperature coefficient for *FRC*.	38
FSB	$V^{1/2} \cdot s/cm^2$	0.0	Lateral mobility coefficient.	5, 38
HEX(TUH)		-1.5	Implant channel mobility temperature exponent.	38
KBeta1		1.0	Effective implant-channel mobility modifier.	38

Table 28 Mobility Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
KI0(KIO)		1.0	Residue current coefficient.	38
LBFRC	10^{-4}Å·s/(cm·V)	0.0	BFRC sensitivity to the effective channel length.	38
LFRC	10^{-4}Å·s/cm	0.0	FRC sensitivity to the effective channel length.	38
LKBeta1	μm	0.0	Length-dependent implant-channel mobility modifier.	38
LKI0(LKIO)	μm	0.0	Length-dependent residue current coefficient.	38
LUO(LUB)	cm^{2}· μm/(V·s)	0.0	UO sensitivity to the effective channel length.	38
LVFRC	10^{-4}Å·s/(cm·V)	0.0	VFRC sensitivity to the effective channel length.	38
LFSB	$10^{-4}V^{1/2}$ · s/cm	0.0	FSB sensitivity to the effective channel length.	38
MOB		0.0	Selects a mobility equation. You can set this parameter to MOB=0 or MOB=7. MOB=7 changes both the model and the channel length calculation. The MOB=7 flag invokes the channel length modulation and mobility equations in MOSFET LEVEL 3. In MOSFET Level 8, you can set MOB to 2, 3, 6, or 7.	2, 6, 7, 8
THETA	V^{-1}	0.0	Mobility modulation. MOSFET models use THETA only if MOB=7. A typical value is THETA=5e-2.	2, 40

Table 28 Mobility Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
	V^{-1}	0.0	Mobility degradation factor.	3
UB (UO)	$cm^2/(V \cdot s)$	0.0	Low field bulk mobility	5
UCRIT	V/cm	1.0e4	Critical field for mobility degradation, UCRIT. This parameter is the limit where UO surface mobility begins to decrease as specified in the empirical relation.	2
	V/cm	1e4	• MOB=6, UEXP>0 Critical field for the mobility degradation. UEXP operates as a switch. • MOB=6, UEXP≤0 Critical field for mobility degradation. Typical value is 0.01 V^{-1}.	8
UEFF			Effective mobility at the specified analysis temperature.	6, 7
UEXP (F2)		0.0	Critical field exponent in the empirical formula that characterizes the surface mobility degradation. Typical value in MOSFET Level 8 with MOB=6 is 0.01 V^{-1}.	2, 8
UH	$cm^2/(V \cdot s)$	900 (N) 300 (P)*	Implant - channel mobility * (For depletion model only)	5, 38
UHSAT	µm/V	0.0	Implant-channel mobility saturation factor.	38
UO (UB, UBO)	$cm^2/(V \cdot s)$	600 (N) 250 (P)	Low-field bulk mobility.Simulation calculates this parameter from the KP value that you specify.	2, 3, 6, 7, 8, 38

Table 28 Mobility Parameters (Continued)

Name (Alias)	Units	Default	Description	Level
UTRA		0.0	Transverse field coefficient (mobility). Traditional SPICE does not use UTRA. HSPICE can use UTRA, but simulation issues a warning, because UTRA can hinder convergence.	2, 8
VFRC	$Å \cdot s/(cm^2 \cdot V)$	0.0	Field reduction coefficient variation due to the drain bias.	38
VST	cm/s	0.0	Saturation velocity.	5, 38
WBFRC	$10^{-4} Å \cdot s/(cm \cdot V)$	0.0	BFRC sensitivity to the effective channel width.	38
WFRC	$10^{-4} Å \cdot s/cm$	0.0	FRC sensitivity to the effective channel width.	38
WFSB	$10^{-4} V^{1/2} \cdot s/cm$	0.0	FSB sensitivity to the effective channel width.	38
WKBeta1	µm	0.0	Width-dependent implant-channel mobility modifier.	38
WKI0 (WKIO)	µm	0.0	Width-dependent residue current coefficient.	38
WUO(WUB)	$cm^2 \cdot µm/(V \cdot s)$	0.0	UO sensitivity to the effective channel width.	38
WVFRC	$10^{-4} Å \cdot s/(cm \cdot V)$	0.0	VFRC sensitivity to the effective channel width.	38

4

Standard MOSFET Models: Level 1 to 40

Lists and describes standard MOSFET models (Levels 1 to 40).

This chapter describes the following standard MOSFET models (Levels 1 to 40):

- LEVEL 1 IDS: Schichman-Hodges Model
- LEVEL 2 IDS: Grove-Frohman Model
- LEVEL 3 IDS: Empirical Model
- LEVEL 4 IDS: MOS Model
- LEVEL 5 IDS Model
- LEVEL 6/LEVEL 7 IDS: MOSFET Model
- LEVEL 7 IDS Model
- LEVEL 8 IDS Model
- LEVEL 27 SOSFET Model
- LEVEL 38 IDS: Cypress Depletion Model
- LEVEL 40 HP a-Si TFT Model

For information about standard MOSFET Models Levels 50 to 64, see Chapter 5, Standard MOSFET Models: Levels 50 to 64. For information on BSIM MOSFET models (based on models developed by the University of California at

Berkeley), see Chapter 6, BSIM MOSFET Models: Levels 13 to 39 and Chapter 7, BSIM MOSFET Models: Levels 47 to 65.

LEVEL 1 IDS: Schichman-Hodges Model

Use the LEVEL 1 MOSFET model if accuracy is less important to you than simulation turn-around time. For digital switching circuits, especially if you need only a “qualitative” simulation of the timing and the function, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions of any TTL-compatible input buffers in the circuit.

The LAMBDA channel-length modulation parameter is equivalent to the inverse of the Early voltage for the bipolar transistor. LAMBDA measures the output conductance in the saturation. If you specify this parameter, the MOSFET has a finite but constant output conductance in saturation. If you do not specify LAMBDA, the LEVEL 1 model assumes zero output conductance.

LEVEL 1 Model Parameters

MOSFET Level 1 uses only the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters.

LEVEL 1 Model Equations

The LEVEL 1 model equations follow.

IDS Equations

The LEVEL 1 model does not include the carrier mobility degradation, the carrier saturation effect, or the weak inversion model. This model determines the DC current:

Cutoff Region, $vgs \leq vth$ $\quad I_{ds} = 0.0$

Linear Region, $v_{ds} < v_{gs} - v_{th}$

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot \left(v_{gs} - v_{th} - \frac{v_{ds}}{2}\right) \cdot v_{ds}$$

Saturation Region, $vds \geq vgs - v_{th}$

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot (v_{gs} - v_{th})^2$$

Effective Channel Length and Width

The Level 1 model calculates the effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

vsb ≥ 0 $$v_{th} = v_{bi} + GAMMA \cdot (PHI + v_{sb})^{1/2}$$

vsb < 0 $$v_{th} = v_{bi} + GAMMA \cdot \left(PHI^{1/2} + 0.5\frac{v_{sb}}{PHI^{1/2}}\right)$$

The preceding equations define the built-in voltage (v_{bi}) as:

$$v_{bi} = v_{fb} + PHI \text{ or } v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

Note: See Common Threshold Voltage Equations on page 58 for calculation of VTO, GAMMA, and PHI if you do not specify them.

Saturation Voltage, v_{sat}

The saturation voltage for the LEVEL 1 model is due to the channel pinch-off at the drain side. The following equation computes this voltage:

$$v_{sat} = v_{gs} - v_{th}$$

The LEVEL 1 model does not include the carrier velocity saturation effect.

LEVEL 2 IDS: Grove-Frohman Model

This section describes the parameters and equations for the LEVEL 2 IDS: Grove-Frohman model.

LEVEL 2 Model Parameters

MOSFET Level 2 uses only the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters.

LEVEL 2 Model Equations

The LEVEL 2 model equations follow.

IDS Equations

This section describes how the LEVEL 2 MOSFET model calculates the drain current of n-channel and p-channel MOSFETs.

Cutoff Region, $vgs \leq vth$

$I_{ds} = 0$ *(see subthreshold current)*

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

The following equations calculate values used in the preceding equation:

$$v_{de} = min(v_{ds}, v_{dsat})$$

$$\eta = 1 + DELTA \cdot \frac{\pi \cdot \varepsilon si}{4 \cdot COX \cdot W_{eff}} \qquad \beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

Effective Channel Length and Width

The Level 2 model calculates effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = VTO - GAMMA \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

To include the narrow width effect, use v_{bi} and η. To include the narrow width effect, specify the DELTA model parameter. The effective γ specifies the short-channel effect. To include short-channel effects, the XJ model parameter must be greater than zero.

$$\gamma = GAMMA \cdot \left\{ 1 - \frac{XJ_{scaled}}{2 \cdot L_{eff}} \cdot \left[\left(1 + \frac{2 \cdot W_s}{XJ_{scaled}} \right)^{1/2} + \left(1 + \frac{2 \cdot W_d}{XJ_{scaled}} \right)^{1/2} - 2 \right] \right\}$$

The following equations determine the W_s and W_d depletion widths:

$$W_s = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{sb}) \right]^{1/2}$$

$$W_d = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{ds} + v_{sb}) \right]^{1/2}$$

If you do not specify parameters such as VTO, GAMMA, and PHI, simulation calculates them automatically. The Level 2 model uses these parameters to calculate the threshold voltage. (See Common Threshold Voltage Equations on page 58).

Saturation Voltage, v_{dsat}

If you do not specify the VMAX model parameter, the program computes the saturation voltage due to channel pinch off at the drain side. If you specify the corrections for small-size effects, then:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{1 - \left[1 + 4 \cdot \left(\frac{\eta}{\gamma}\right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb}\right)\right]^{1/2}\right\}$$

$$v_{dsat} = v_{sat}$$

If you specify ECRIT, the program modifies v_{sat} to include carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECRIT \cdot L_{eff}$$

Note: If you specify VMAX, simulation calculates a different v_{dsat} value. Refer to the Vladimirescu document[1] for details.

Mobility Reduction, u_{eff}

The mobility of carriers in the channel decreases as speeds of the carriers approach their scattering limited velocity. The mobility degradation for the LEVEL 2 MOS model uses two different equations, depending on the MOB mobility equation selector value.

If MOB=0, (default):

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th} - UTRA \cdot v_{ds})}\right]^{UEXP}$$

Because u_{eff} is less than UO, the program uses the above equation if the bracket term is less than one; otherwise the program uses u_{eff}=UO.

If MOB=7, THETA≠0

$$u_{eff} = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

vgs<vth, ueff = UO

If MOB=7, THETA=0

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th})}\right]^{UEXP}$$

If MOB=7, VMAX>0

$$u_{eff} = \frac{u_{eff}}{1 + u_{eff} \cdot \frac{vde}{VMAX \cdot L_{eff}}}$$

Channel Length Modulation

To include the channel length modulation effect, the LEVEL 2 MOS model modifies the I_{ds} current:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda \cdot v_{ds}}$$

If you do not specify the LAMBDA model parameter, the model calculates the λ value.

LAMBDA>0:

λ = LAMBDA

VMAX>0, NSUB>0, and LAMBDA<0

$$\lambda = \frac{X_d}{NEFF^{1/2} \cdot L_{eff} \cdot v_{ds}} \cdot \left\{\left[\left(\frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}}\right)^2 + v_{ds} - v_{dsat}\right]^{1/2} - \frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}}\right\}$$

VMAX=0, NSUB>0, and LAMBDA<0

If MOB=0

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \frac{v_{ds} - v_{dsat}}{4} + \left[1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right]^{1/2} \right\}^{1/2}$$

This equation does not include the effect of the field between the gate and the drain. It also tends to overestimate the output conductance in the saturation region.

If MOB=7

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\frac{v_{ds} - v_{dsat}}{4} + \left(1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right)^{1/2} \right]^{1/2} - 1 \right\}$$

This equation does not include the effect of the field between the gate and the pinch-off point. It also tends to overestimate the output conductance in the saturation region.

The following equation calculates the X_d value used in the two preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

Modifying I_{ds} by a factor of $(1 - \lambda \cdot v_{ds})$ is equivalent to replacing Leff with:

$$Le = L_{eff} - \lambda \cdot v_{ds} \cdot L_{eff}$$

To prevent the channel length (Le) from becoming negative, the value of Le is limited.

If Le < xwb, then simulation replaces Le with:

$$\frac{\text{xwb}}{1 + \frac{xwb - Le}{xwb}}$$

The following equation calculates the xwb value used in the preceding equation:

$$xwb = X_d \cdot PB^{1/2}$$

Subthreshold Current, I_{ds}

The fast surface states model parameter (NFS) characterizes this region of operation. For NFS>0 the model determines the modified threshold voltage (von):

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[\eta + (PHI + v_{sb})^{1/2} \cdot \frac{\partial \gamma}{\partial v_{sb}} + \frac{\gamma}{2 \cdot (PHI + v_{sb})^{1/2}} + \frac{q \cdot NFS}{COX} \right]$$

In the preceding equations, vt is the thermal voltage.

The following equation calculates the I_{ds} current for v_{gs}<von:

$$I_{ds} = I_{ds}(von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

vgs>von: $I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$

The following equation calculates the vde value used in the preceding equation:

$$vde = \min(v_{ds}, v_{dsat})$$

Note: The modified threshold voltage (von), due to NFS specification, is also used in strong inversion instead of v_{th}, mostly in the mobility equations.

If WIC=3, the Level 2 model calculates the subthreshold current differently. In this case the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

$N0_{eff}$ and ND_{eff} are functions of effective device width and length.

LEVEL 3 IDS: Empirical Model

This section describes the LEVEL 3 IDS: Empirical model parameters and equations.

LEVEL 3 Model Parameters

MOSFET Level 3 uses only the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters.

LEVEL 3 Model Equations

The LEVEL 3 model equations follow.

IDS Equations

The following equations describe how the LEVEL 3 MOSFET model calculates the I_{ds} drain current.

Cutoff Region, vgs < vth

$I_{ds} = 0$ (See subthreshold current)

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left(v_{gs} - v_{th} - \frac{1 + fb}{2} \text{Þ} vde \right) \cdot vde$$

The following equations calculate values used in the preceding equation:

$$\beta = KP \cdot \frac{W_{eff}}{L_{eff}} = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

$$vde = \min(v_{ds}, v_{dsat})$$

$$fb = f_n + \frac{GAMMA \cdot f_s}{4 \cdot (PHI + v_{sb})^{1/2}}$$

Note: In the above equation, the factor 4 should be 2, but because SPICE uses a factor of 4, this model uses a factor of 4 as well.

The f_n parameter specifies the narrow width effect:

$$f_n = \frac{DELTA}{W_{eff}} \cdot \frac{1}{4} \cdot \frac{2\pi \cdot E_{si}}{COX}$$

The f_s term expresses the effect of the short channel:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \left\{ \frac{LD_{scaled} + W_c}{XJ_{scaled}} \cdot \left[1 - \left(\frac{W_p}{XJ_{scaled} + W_p} \right)^2 \right]^{1/2} - \frac{LD_{scaled}}{XJ_{scaled}} \right\}$$

$$W_p = X_d \cdot (PHI + v_{sb})^{1/2}$$

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

$$W_c = XJ_{scaled} \cdot \left[0.0631353 + 0.8013292 \cdot \left(\frac{W_p}{XJ_{scaled}} \right) - 0.01110777 \left(\frac{W_p}{XJ_{scaled}} \right)^2 \right]$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 3 model:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

$$LREFF = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

The following equation calculates the effective threshold voltage, including the device size and terminal voltage effects:

$$v_{th} = v_{bi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^3} \cdot v_{ds} + GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = v_{fb} + PHI \text{ or } v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

VTO is the extrapolated zero-bias threshold voltage of a large device. If you do not specify VTO, GAMMA, or PHI, simulation computes these values (see Common Threshold Voltage Equations on page 58).

Saturation Voltage, v_{dsat}

The LEVEL 3 model determines the saturation voltage due to the channel pinch-off at the drain side.The VMAX parameter specifies the reduction of the saturation voltage due to the carrier velocity saturation effect.

$$v_{sat} = \frac{v_{gs} - v_{th}}{1 + f_b}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equations:

$$v_c = \frac{VMAX \cdot L_{eff}}{us}$$

The next section defines the *us* surface mobility parameter. If you do not specify the VMAX model parameter, then:

$$v_{dsat} = v_{sat}$$

Effective Mobility, u_{eff}

The Level 3 model defines the carrier mobility reduction due to the normal field as the effective surface mobility (us).

$v_{gs} > v_{th}$: $$us = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

The VMAX model parameter model determines the degradation of mobility due to the lateral field and the carrier velocity saturation.

VMAX>0: $$u_{eff} = \frac{us}{1 + \frac{vde}{v_c}}$$

Otherwise: $$u_{eff} = us$$

Channel Length Modulation

For $v_{ds}>v_{dsat}$, this model computes the channel length modulation factor. The VMAX model parameter value determines the amount of channel length reduction (ΔL).

VMAX = 0

$$\Delta L = X_d \cdot [KAPPA \cdot (v_{ds} - v_{dsat})]^{1/2}$$

VMAX>0

$$\Delta L = -\frac{E_p \cdot X_d^2}{2} + \left[\left(\frac{E_p \cdot X_d^2}{2}\right)^2 + KAPPA \cdot X_d^2 \cdot (v_{ds} - v_{dsat})\right]^{1/2}$$

In the preceding equation, E_p is the lateral electric field at the pinch off point. The following equation approximates its value:

$$E_p = \frac{v_c \cdot (v_c + v_{dsat})}{L_{eff} \cdot v_{dsat}}$$

The following equation computes the I_{ds} saturation current:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

To prevent a zero denominator, the ΔL value is limited:

If $\Delta L > \frac{L_{eff}}{2}$

then $\Delta L = L_{eff} - \frac{\left(\frac{L_{eff}}{2}\right)^2}{\Delta L}$

Subthreshold Current, I_{ds}

This region of operation is characterized by the model parameter for the fast surface state (NFS). The following equation determines the modified threshold voltage (von):

NFS>0 $von = v_{th} + fast$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})}{2 \cdot (PHI + v_{sb})}\right]$$

The following equations calculate the I_{ds} current:

v_{gs}<*von:*

$$I_{ds} = I_{ds}(von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

vgs>von:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

Note: Strong inversion does not use the modified threshold voltage.

If WIC=3, the model calculates subthreshold current differently. In this case, the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

The isub subthreshold current for LEVEL=3 is the same as for LEVEL=13 (see ids Subthreshold Current on page 335).

$N0_{eff}$ and ND_{eff} are functions of the effective device width and length.

Compatibility Notes

Synopsys Device Model versus SPICE3

Differences between the Synopsys Level 3 MOSFET device model and Berkeley SPICE3 can arise in the following situations:

Small XJ **Level** 3 and SPICE3 differ for small XJ values, typically >0.05 microns. Do not use such small values for XJ; they are physically unreasonable. XJ calculates the short-channel reduction of the GAMMA effect:

$$GAMMA \rightarrow f_s \cdot GAMMA$$

f_S is normally less than or equal to 1. For very small values of XJ, f_S can be greater than one. The Synopsys Level 3 model imposes the limit $f_S \leq 1.0$, but SPICE3 allows $f_S > 1.0$.

ETA **I**n this model, 8.14 is the constant in the ETA equation, which varies the v_{ds} threshold. Berkeley SPICE3 uses 8.15.

Solution: To convert a SPICE3 model to the Synopsys Level 3 MOSFET device model, multiply ETA by 815/814.

NSUB Missing If you do not specify NSUB in SPICE3, the KAPPA equation becomes inactive. The Synopsys Level 3 MOSFET model generates a default NSUB from GAMMA, and the KAPPA equation is active.

Solution: If you do not specify NSUB in the SPICE3 model, set KAPPA=0 in the Synopsys Level 3 MOSFET model.

LD Missing If you do not specify LD, simulation uses the default (0.75XJ). The SPICE3 default for LD is zero.

Solution: If you do not specify LD in the SPICE3 model, set LD=0 in the Level 3 MOSFET model.

Name	Symbol	Value
Boltzmann constant	k	= 1.3806226e-23J· K^{-1}
Electron charge	e	= 1.6021918e-19C

Name	Symbol	Value
Permittivity of silicon dioxide	ε_{ox}	= 3.45314379969e-11F/m
Permittivity of silicon	ε_{si}	= 1.035943139907e-10F/m

Temperature Compensation

The input file example located in the following directory verifies temperature dependence for MOSFET Level 3:

`$installdir/demo/hspice/mos/tempdep.sp`

This simple model, with XJ=0 and KAPPA=0, has a saturation current:

$$I_{ds} = \frac{beta \cdot 0.5 \cdot (v_{gs} - v_{tm})^2}{1 + fb}$$

$$beta = COX \cdot \left(\frac{W}{L}\right) \cdot UO(t) \quad fb = \frac{GAMMA}{(4 \cdot \sqrt{phi(t)})}$$

Using the model parameters in the input file, and the preceding equations, produces these results:

$$beta = (1.2e-3) \cdot \left(\frac{t}{tref}\right)^{BEX}$$

$$v_{tm} = 0.8 - TCV \cdot (t - tref)$$

$$phi(t) = 0.64 \cdot \left(\frac{t}{tref}\right) - vtherm \cdot \left(egarg + 3 \cdot \log\left(\frac{t}{tref}\right)\right)$$

At room temperature:

$$beta = (1.2e-3)$$

$$v_{tm} = 0.8$$

$$phi(t) = 0.64$$

$$I_{ds} = (1.2e-3)\cdot 0.5\cdot \frac{(2-0.8)^2}{1+\frac{0.2}{\sqrt{0.64}}} = 6.912e-4$$

At T=100:

$$beta = 1.2e-3\cdot(1.251551)^{-1.5} = 0.570545e-4$$

$$v_{tm} = 0.8-(1.5e-3)\cdot 75 = 0.6875$$

$$egarg = 9.399920 \quad vtherm = 3.215466e-2$$

$$phi(t) = 0.64\cdot 1.251551 - 0.3238962 = 0.4770964$$

$$I_{ds} = beta\cdot 0.5\cdot \frac{(2-vt)^2}{1+\frac{0.2}{\sqrt{phi(t)}}} = 5.724507e-4$$

Simulation results:

```
T=25, id=6.91200e-04
   T=100, id=5.72451e-04
```

These results agree with the hand calculations.

LEVEL 4 IDS: MOS Model

The LEVEL 4 MOS model is the same as the LEVEL 2 model with the following exceptions:

- No narrow width effects: h = 1
- No short-channel effects: γ = GAMMA
- For lateral diffusion, LD_{scaled} = LD · XJ · SCALM. If you specify XJ, the LD default = 0.75. If you do not specify XJ, the default is 0.
- TPG, the model parameter for type of gate materials, defaults to zero (AL gate). The default is 1 for other levels. If you do not specify VTO, this parameter computes VTO (see Common Threshold Voltage Equations on page 58).
- Starting in 2001.4.2, MOSFET Level 4 and Level 9 support both M and AREA scaling.

LEVEL 5 IDS Model

This section describes the LEVEL 5 IDS model parameters and equations.

Note: This model uses micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 5. Level 5 does not use the SCALM option.

LEVEL 5 Model Parameters

MOSFET Level 5 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 5.

Table 29 Capacitance Parameters for MOSFET Level 5

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	μm	0.0	Metal overlap on gate

Use the ZENH flag mode parameter to select one of two modes: enhancement or depletion.

Parameter	Description
ZENH=1	This enhancement model (default mode) is a portion of the Synopsys MOS5 device model, and is identical to AMI SPICE MOS LEVEL 4.
ZENH=0	This depletion model is revised in the Synopsys MOS5 device model (from previous depletion mode) and is identical to AMI SPICE MOS LEVEL 5.

The Synopsys enhancement and depletion modes are basically identical to the AMI models. However, the Synopsys enhancement and depletion modes let you choose either SPICE or ASPEC temperature compensation.

- TLEV=1 (default) uses ASPEC-style temperature compensation.
- TLEV=0 uses SPICE-style temperature compensation.

CAPOP=6 represents AMI Gate Capacitance in the Synopsys device models. CAPOP=6 is the default setting for LEVEL 5 only. LEVEL 5 models can also use CAPOP =1, 2, 3.

The ACM parameter defaults to 0 in LEVEL 5, invoking SPICE-style parasitics. You can also set ACM to 1 (ASPEC) or to 2 (Synopsys device models). All MOSFET models follow this convention.

You can use **.OPTION SCALE** with the LEVEL 5 model; however, you cannot use the SCALM option, due to the difference in units.

You *must* specify the following parameters for MOS LEVEL 5: VTO (VT), TOX, UO (UB), FRC, and NSUB (DNB).

IDS Equations

Cutoff Region, vgs<vth

$I_{ds} = 0$ (See Subthreshold Current, Ids on page 148)

On Region, vgs>vth

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma \cdot [(\Phi_f + vde + v_{sb})^{3/2} - (\Phi_f + v_{sb})^{3/2}] \right\}$$

The following equations calculate values used in the preceding equation:

$$vde = min(v_{ds}, v_{dsat})$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$\Phi_f = 2 \cdot v_{tm} \cdot \ln\left(\frac{DNB}{ni}\right)$$

The following equation calculates the gate oxide capacitances per unit area:

$$cox = \frac{E_{ox}}{TOX \cdot 1E\text{-}10} \quad \text{F/m}$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 5 model:

$$W_{eff} = W_{scaled} \cdot WMLT + OXETCH$$

$$L_{eff} = L_{scaled} \cdot LMLT - 2 \cdot (LATD + DEL)$$

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (\Phi_f + v_{sb})^{1/2}$$

The following equations calculate values used in the preceding equation:

$$v_{bi} = v_{fb} + \Phi_f = VTO - \gamma_0 \cdot \Phi_f^{1/2}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot DNB)^{1/2}}{cox}$$

Note: You must specify DNB and VTO parameters for the LEVEL 5 model. The Synopsys device model uses DNB to compute γ_0, and ignores the GAMMA model parameter.

The following equation computes the γ effective body effect, including the device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

If SCM < 0, then scf = 0.

Otherwise:

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_{sb} + \Phi_f)^{1/2} \right]^{1/2} - 1 \right\}$$

IF NWM<0, then ncf = 0.

Otherwise:

$$ncf = \frac{NWM \cdot X_d \cdot (\Phi_f)^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage due to the channel pinch-off at the drain side:

$$v_{sat} = v_{gs} - v_{bi} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{bi} + \Phi_f + v_{sb}) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV does not equal 1000, the program modifies v_{sat} to include the carrier velocity saturation effect:

$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$, where $v_c = ECV \cdot L_{eff}$

Mobility Reduction, UB_{eff}

The following equation computes the mobility degradation effect in the LEVEL 5 MOSFET model:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot L_e} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate the L_e value used in the preceding equation:

$L_e = L_{eff}$ linear region

$L_e = L_{eff} - \Delta L$ saturation region

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

The LEVEL 5 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{DNB \cdot \ln\left(\frac{1e20}{DNB}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and DNB is in cm^{-3}.

Subthreshold Current, I_{ds}

The Fast Surface State (FSS) characterizes this region of operation if it is greater than 1e10. The following equation then calculates the effective threshold voltage, separating the strong inversion region from the weak inversion region:

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_f + v_{sb})^{1/2}}\right]$$

In the preceding equations, vt is the thermal voltage.

The following equations calculate I_{ds}.

Weak Inversion Region, $v_{gs} < v_{th}$

$$I_{ds} = (von, vde, v_{sb}) \cdot e^{\frac{v_{gs} - von}{fast}}$$

Strong Inversion Region, vgs>vth

$$I_{ds} = I_{ds}(v_{gs}, vde, v_{sb})$$

Note: Strong inversion also use the modified threshold voltage (von) that FSS produces; that is, the mobility equations use von instead of v_{th}.

Depletion Mode DC Model ZENH=0

The LEVEL 5 MOS model uses depletion mode devices as the load element in contemporary standard n-channel technologies[2]. This model assumes a silicon gate construction with an ion implant used to obtain the depletion characteristics. A special model is required for depletion devices, because the implant used to create the negative threshold also results in a complicated impurity concentration profile in the substrate. The implant profile changes the basis for the traditional calculation of the QB bulk charge. The additional charge from the implant, QBI, must be calculated.

This implanted layer also forms an additional channel, offering a conductive pathway through the bulk silicon as well as through the surface channel. This second pathway can cause difficulties when trying to model a depletion device using existing MOS models.

The surface channel partially shields the bulk channel from the oxide interface, and the mobility of the bulk silicon can be substantially higher. Yet with all of these differences, a depletion model still can share the same theoretical basis as the Ihantola and Moll gradual channel model.

The depletion model differs from the Ihantola and Moll model:

- Implant charge accounted for.
- Finite implant thickness (DP).
- Assumes two channels: a surface channel and a bulk channel.
- Bulk channel has a bulk mobility (UH).
- Assumes that the bulk gain is different from the surface gain.

In the depletion model, the gain is lower at low gate voltages and higher at high gate voltages. Due to this variation in gain, the enhancement models cannot accurately represent a depletion device. The physical model for a depletion device is basically the same as an enhancement model, except that a one-step profile with DP depth approximates the depletion implant.

Due to the implant profile, simulation calculates the drain current equation by region. The MOSFET Level 5 model has three regions: depletion, enhancement, and partial enhancement.

Depletion Region, v_{gs} - v_{fb} < 0

The bulk channel dominates the low gate voltage region.

Enhancement Region, v_{gs} - v_{fb} > 0, v_{ds} < v_{gs} - v_{fb}

High gate voltage and low drain voltage define the enhancement region. In this region, both channels are fully turned on.

Partial enhancement region, v_{gs} - v_{fb} > 0, v_{ds} > v_{gs} - v_{fb}

The region has high gate and drain voltages so the surface region is partially turned on and the bulk region is fully turned on.

IDS Equations, Depletion Model LEVEL 5

Depletion, v_{gs}-v_{fb} <0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

Enhancement, v_{gs}-v_{fb} >vde>0

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \text{Þ} cav \text{Þ} \gamma \text{Þ} [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$+ \beta \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, v_{gs}-v_{fb}<vde

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$+ \left(\frac{1}{2}\beta - \beta 1 \ \text{Þ} cav \right) \cdot (v_{gs} - v_{fb})^2$$

The following equations calculate values used in the preceding equations:

$$\beta 1 = UH \cdot \frac{W_{eff}}{L_{eff}} \qquad \beta = UBeff \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$cav = \frac{cox \cdot cs}{cox + cs} \qquad cs = \frac{2.77 E_{si}}{DP \cdot 1e\text{-}4}$$

$$\Phi_d = v_{tm} \cdot \ln\left(\frac{DNB \cdot nd}{ni^2} \right) \qquad nd = \frac{NI \cdot 1e4}{DP}$$

$$vde = \min(v_{ds}, v_{dsat})$$

The following sections describe the saturation voltage, threshold voltage, and effective γ.

Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equations calculate the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{fb} - \beta d \cdot [vch - \gamma \cdot (\Phi_d + v_{sb})^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$v_{fb} = VTO + \beta d \cdot (vch - \gamma_0 \ \text{Þ} \Phi_d^{1/2})$$

$$\beta d = \frac{UH \cdot cav}{UB \cdot cox} \qquad vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB} \qquad nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The following equation computes the effective γ, including the small device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equation:

If SCM ≤0, then scf=0. Otherwise:

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_b + \Phi_d)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM ≤0, then ncf=0. Otherwise:

$$ncf = \frac{NWM \cdot X_d \cdot \Phi_d^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equation:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Note: If $v_{gs} \le v_{th}$, the surface is inverted and a residual DC current exists. If v_{sb} is large enough to make $v_{th} > vin_{th}$, then v_{th} is the inversion threshold voltage. To determine the residual current, this model inserts vin_{th} into the I_{ds}, v_{sat}, and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current).

The inversion threshold voltage at a specified v_{sb} is vin_{th}, which the following equation computes:

$$vinth = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage (v_{sat}):

$$v_{sat} = v_{gs} - v_{fb} + vch + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + vch + v_{sb} + \Phi_d) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

IF ECV is not equal to 1000 (V/µm), the Synopsys device models modify v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat} + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The surface mobility (UB) depends on terminal voltages as follows:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot le} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate values used in the preceding equation:

$L_e = L_{eff}$ Linear region

$L_e = L_{eff} - \Delta L$ Saturation region

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

Modify the I_{ds} current to model the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL parameter is in microns, if XJ is in microns and na1 is in cm^{-3}.

Subthreshold Current, I_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, then this model considers the subthreshold characteristics. The Level 5 MOSFET model uses the subthreshold model only if the number of fast surface states (FSS) is greater than 1e10. The following equation determines the effective threshold voltage (von):

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_d + v_{sb})^{1/2}}\right]$$

If von < vin_{th}, then simulation substitutes vin_{th} for von.

Note: The Level 5 MOSFET device model uses the following subthreshold model only if v_{gs} < von, and if the device is either in partial or full enhancement mode. Otherwise, it uses the model in enhancement mode (ZENH=1). The subthreshold current calculated below includes the residual DC current.

If v_{gs} <von then:

Partial Enhancement, v_{gs}-v_{fb} < vde

$$I_{ds} = \beta 1 \cdot \left\{q \cdot NI \cdot vde + cav \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2}\right]\right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}]\right\}$$

$$+\frac{1}{2}\cdot\left(\beta\cdot e^{\frac{v_{gs}-von}{fast}}-\beta 1\ Þcav\right)\cdot(von-v_{fb})^2$$

Full Enhancement, v_{gs}-v_{fb} vde > 0

$$I_{ds}\ =\ \beta 1\cdot\left\{q\cdot NI\cdot vde-\frac{2}{3}\ Þcav\ Þ\gamma[(vde+v_{sb}+\Phi_d)^{3/2}-(v_{sb}+\Phi_d)^{3/2}]\right\}$$

$$+\beta\cdot\left[(von-v_{fb})\cdot vde-\frac{vde^2}{2}\right]\cdot e^{\frac{v_{gs}-von}{fast}}$$

Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/ml5iv.sp`

LEVEL 6/LEVEL 7 IDS: MOSFET Model

These models represent ASPEC, MSINC, and ISPICE MOSFET model equations. The only difference between LEVEL 6 and LEVEL 7 equations is the handling of the parasitic elements and the method of temperature compensation. See Table 28 on page 122 and Channel Length Modulation on page 133 for those model parameters.

LEVEL 6 and LEVEL 7 Model Parameters

MOSFET Levels 6 and 7 use the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. These levels also use the parameters described in this section, which apply only to MOSFET Levels 6 and 7.

Table 30 Alternate Saturation Model Parameters

Name (Alias)	Units	Default	Description
KA		1.0	Alternate saturation model: coefficient for the short-channel vds scaling factor.
KU		0.0	Lateral field mobility parameter.
MAL		0.5	Alternate saturation model: exponent of the short-channel vds scaling factor.
MBL		1.0	Exponent for mobility reduction due to the source-drain electric field.
NU		1.0	Mobility reduction due to the source-drain electric field.

UPDATE Parameter for LEVEL 6 and LEVEL 7

The general form of the I_{ds} equation for LEVEL 6 is the same as the LEVEL 2 MOS model. However, the small size effects, mobility reduction, and channel length modulation are included differently. Also, you can use the multi-level GAMMA capability to model MOS transistors with ion-implanted channels.

The LEVEL 6 model can represent the ASPEC, MSINC, or ISPICE MOSFET model. Use the UPDATE model parameter to invoke different versions of the LEVEL 6 model.

UPDATE=0

This is the original Synopsys Level 6 MOSFET device model, which is not quite compatible with the ASPEC model. It has some discontinuities in the weak inversion, mobility equations (MOB=3), and multi-level GAMMA equations.

UPDATE=1

This enhanced version of the LEVEL 6 model contains improved multi-level GAMMA equations. The saturation voltage, drain-source current, and conductances are continuous.

UPDATE=2

This version of the LEVEL 6 model is compatible with the ASPEC model. The multi-level GAMMA model is not continuous as it is in the ASPEC program. See ASPEC Compatibility on page 180.

- Set UPDATE to 1.0 to use changes to the device equations.
- Set UPDATE to 1.0 or 2 to use the default RS and RD handling.

These values and changes provide a more accurate ASPEC model.

UPDATE=1 or 2:

TOX	= 690
UO (UB)	= 750 $cm^2/(V \cdot s)$ (N-ch)
UTRA (F3)	= 0.0

UPDATE=0:

TOX	= 1000
UO (UB)	= 750 $cm^2/(V \cdot s)$ (N-ch)
UTRA (F3)	= 0.0

If you do not specify LDIF, then the RD and RS values change in the MOSFET:

UPDATE=1 or 2 and LDIF=0:

$$RD = \frac{(RD + NRD \cdot RL)}{M}$$

$$RS = \frac{(RS + NRS \cdot RL)}{M}$$

Note: The ASPEC program does not use the M multiplier.

LDIF≠0:

$$RD = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RD + NRD \cdot \frac{RL}{M}$$

$$RS = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RS + NRS \cdot \frac{RL}{M}$$

The vde value in the mobility equations change for the alternate saturation model:

$$vde = \min\left(\frac{vds}{vfa}, vsat\right), \quad \text{UPDATE = 1 or 2}$$

$$vde = \min(vds, vfa \cdot vsat), \quad \text{UPDATE = 0}$$

The impact ionization equation calculates the saturation voltage:

$$vdsat = vfa \cdot vsat, \quad \text{UPDATE= 1 or 2}$$

$$vdsat = vsat, \quad \text{UPDATE= 0}$$

The MOB=3 mobility equation changes:

UPDATE= 1 or 2 and $(vgs - vth)^{F2}$ *> VF1:*

$$ueff = \frac{UB}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

UPDATE= 0 and $(vgs - vth)^{F2}$ *> VF1:*

$$ueff = \frac{UB}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

LEVEL 6 Model Equations, UPDATE=0,2

IDS Equations

$$ids = \beta \cdot \left\{ \left(vgs - vbi - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \gamma \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right] \right\}$$

The following equations calculate values used in the preceding equation:

$$vde = \min(vds, vdsat)$$

$$\eta = 1 + \frac{NWEscaled}{weff}$$

$$\beta = ueff \cdot COX \cdot \frac{weff}{Leff}$$

- The η, vbi, and γ values define the narrow-width effect.
- The NWE or NWM model parameters also specify the narrow-width effect.
- The vbi and γ parameters specify the short-channel effect.

Effective Channel Length and Width

The following equations calculate the effective channel length and width from the drawn length and width:

$$leff = Lscaled \cdot LMLT + XLscaled - 2 \cdot (LDscaled + DELscaled)$$

$$weff = M \cdot (Wscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled)$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \cdot (LDscaled + DELscaled)$$

$$WREFeff = M \cdot (WREFscaled \cdot WMLT + XWscaled - 2 \cdot WDscaled)$$

Threshold Voltage, vth

The following equation determines the effective threshold voltage:

$$vth = vbi + \gamma \cdot (PHI + vsb)^{1/2}$$

The vbi and γ built-in voltage value depends on the specified model parameters.

Single-Gamma, VBO=0

If you set the VBO model parameter to zero, simulation uses the single-gamma model, which treats the LGAMMA parameter as a junction depth. To modify the GAMMA parameter for the short-channel effect, this model then uses the scf factor, which the Poon and Yau formulation computes. In this case, simulation multiplies LGAMMA by the SCALM option.

$$scf = 1 - \frac{LGAMMA}{leff} Þ\left\{\left[1 + \frac{2 \cdot LAMBDA}{LGAMMA} \cdot (PHI + vsb)^{1/2}\right]^{1/2} - 1\right\}$$

The XJ model parameter modifies the GAMMA model parameter by the short-channel factor (gl):

$$gl = 1 - \frac{XJscaled}{leff} Þ\left\{\left[1 + \frac{2 \cdot LAMBDA}{XJscaled} \cdot (PHI + vsb + SCM \cdot vds)^{1/2}\right]^{1/2} - 1\right\}$$

The gl factor generally replaces the scf factor for the multi-level GAMMA model.

The gw factor modifies GAMMA to compute the narrow-width effect:

$$gw = \frac{1 + NWM \cdot xd}{weff}$$

The following equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB}\right)^{1/2}$$

Finally, the effective γ, including short-channel and narrow-width effects, is $\gamma = GAMMA \cdot gw \cdot gl \cdot scf$.

Effective Built-in Voltage, vbi

The Level 6 model includes the narrow-width effect. This effect is the increase in threshold voltage due to the extra bulk charge at the edge of the channel. To use this effect with the NWE model parameter, modify vbi.

Modify vbi to use the short-channel effect, which decreases threshold voltage due to the induced potential barrier-lowering effect. To include this effect, you must specify either the FDS parameter, or the UFDS and VFDS model parameters.

The following equations calculate vbi, which sums up the preceding features.

vds<VFDS, or VFDS=0

$$vbi = VTO - \gamma \cdot PHI^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

vds>VFDS

$$\mathrm{vbi} = \mathrm{VTO} - \gamma \cdot \mathrm{PHI}^{1/2} + (\eta - 1) \cdot (\mathrm{PHI} + \mathrm{vsb}) - \frac{\mathrm{LDscaled}}{\mathrm{leff}} \cdot \mathrm{VSH} - \frac{\mathrm{esi}}{\mathrm{COX} \cdot \mathrm{Leff}} \cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

The preceding equations describe piecewise linear variations of vbi as a function of vds. If you do not specify VFDS, this model uses the first equation for vbi.

Note: The Level 6 MOSFET device model calculates model parameters such as VTO, PHI, and GAMMA, if you did not specify them (see Common Threshold Voltage Equations on page 58).

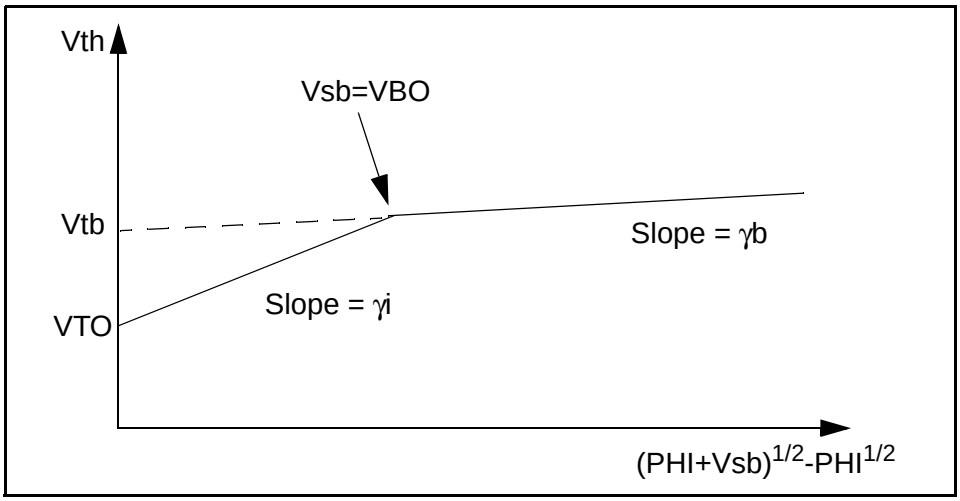
Multi-Level Gamma, VBO>0

Use Multi-Level Gamma to model MOS transistors with Ion-Implanted channels. The doping concentration under the gate is approximated as step functions.

- GAMMA represents the corresponding body effects coefficient for the implant layer.
- LGAMMA represents the corresponding body effects coefficient for the substrate.

Figure 27 shows the variation of vth as a function of vsb for Multi-Level Gamma.

Figure 27 Threshold Voltage Variation



The following equations calculate the threshold voltage for different regions:

Channel Depletion Region is in the Implant Layer, vsb<VBO

$$\gamma = \gamma i$$

$$vth = vbi + \gamma i \cdot (vsb + PHI)^{1/2}$$

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2}$$

Channel Depletion Region Expands into the Bulk, vsb>VBO

$$\gamma = \gamma b$$

$$vth = vbi + \gamma b \cdot (vsb + PHI)^{1/2}$$

$$vbi = vtb - \gamma b \cdot (PHI)^{1/2}$$

For the threshold voltage to be continuous at vsb=VBO, vtb must be:

$$vtb = VTO + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}]$$

- γi is the effective value of GAMMA.
- γb is the effective value of LGAMMA.

The model computes them as γ in single-gamma models, except the scf factor is 1.0.

$$\gamma i = GAMMA \cdot gw \cdot gl$$

$$\gamma b = LGAMMA \cdot gw \cdot gl$$

Effective Built-in Voltage, vbi for VBO>0

For vds<VFDS

if vsb≤VBO:

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

if vsb>VBO:

$$vbi = VTO - \gamma b \cdot (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1) + (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot FDS \cdot vds$$

For vds>VFDS

if vsb≤VBO:

$$vbi = VTO - \gamma i \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + vsb) - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

if vsb>VBO:

$$vbi = VTO - \gamma b \cdot (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1) \cdot PHI + vsb - \frac{LDscaled}{Leff} \cdot VSH - \frac{\varepsilon si}{COX \cdot Leff} \cdot [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

Saturation Voltage, vdsat (UPDATE=0,2)

The following formula determines the saturation voltage due to channel pinch-off at the drain side:

$$vsat = \frac{vgs - vbi}{\eta} + \frac{1}{2}\left(\frac{\gamma}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma}\right)^2 \cdot \left(\frac{vgs - vbi}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

The following equation calculates the reduction of the saturation voltage due to the carrier velocity saturation effect:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

In the preceding equation, determines vc if the ECRIT model parameter >0, or VMAX >0, and KU≤1. If you specify both ECRIT and VMAX, then simulation uses only the VMAX equation. However, this model does not use the VMAX equation if MOB=4 or MOB=5, because these mobility equations already contain a velocity saturation term.

$$vc = ECRIT \cdot Leff \quad \text{or} \quad vc = \frac{VMAX \cdot Leff}{ueff}$$

Because vsb>VBO, γ switches from γι to γβ, and the ids, vsat, and conductance values are not continuous as in the following example. To correct this discontinuity problem, specify the UPDATE=1 model parameter. The next section discusses this improvement.

Example

An example of a multi-level gamma model with UPDATE=0 is located in the following directory:

```
$installdir/demo/hspice/mos/tgam2.sp
```

Figure 28 Variation of IDS, VTH and VDSAT for UPDATE=0

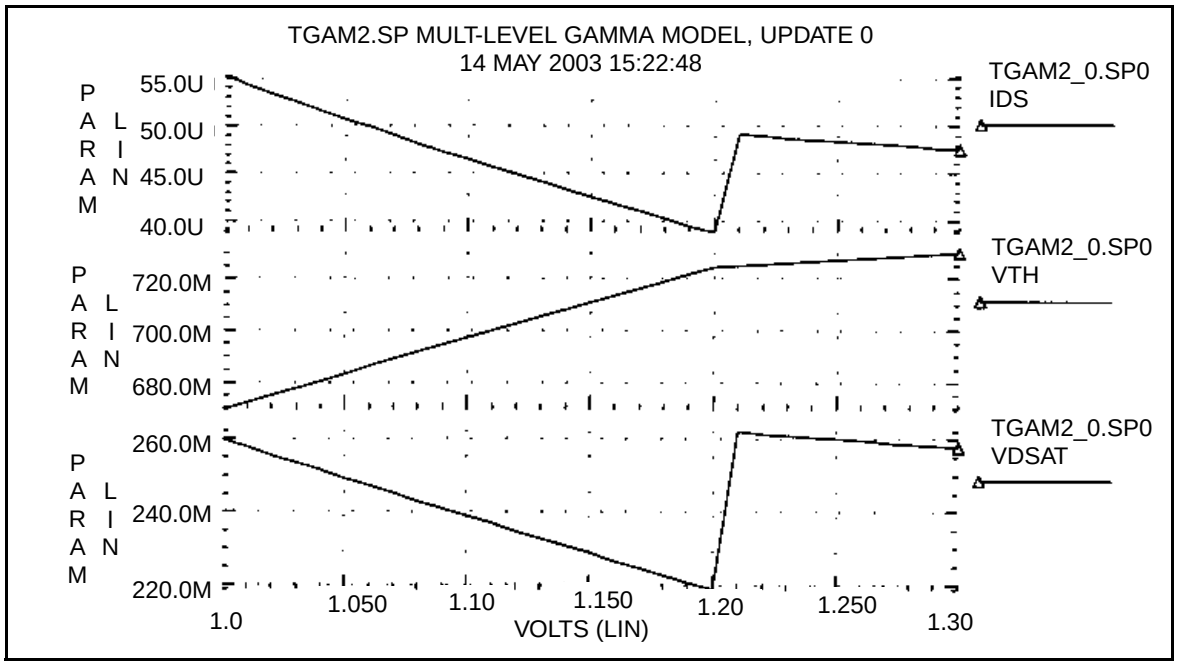
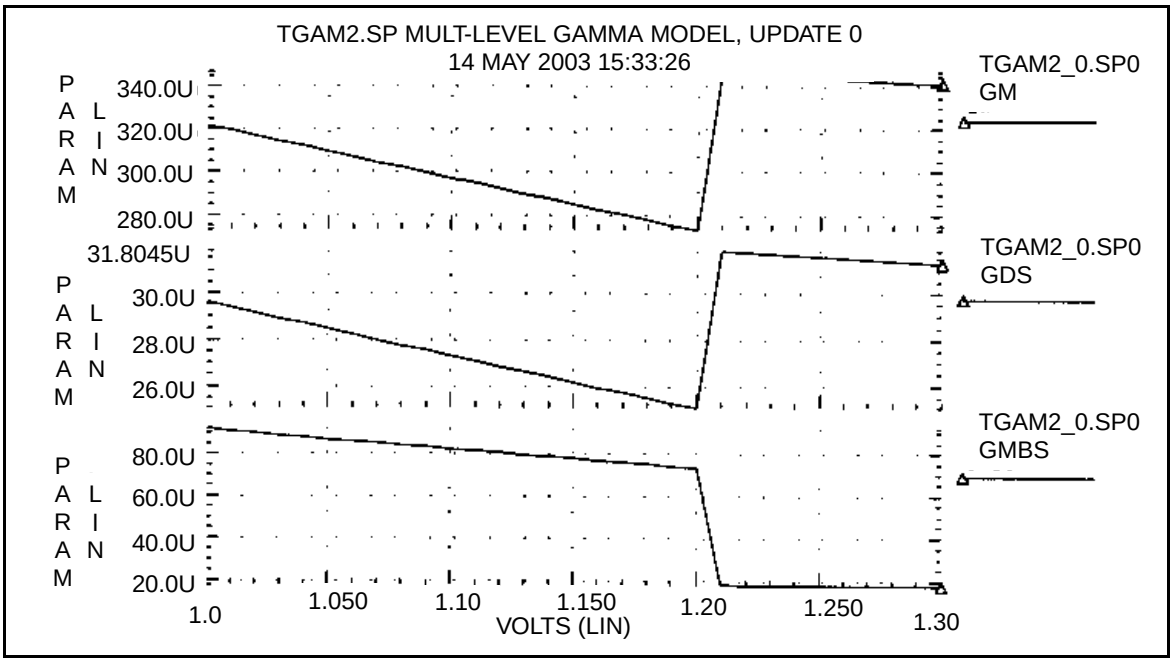


Figure 29 Variation of GM, GDS and GMBS for UPDATE=0



Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of vsb for UPDATE=0.

Improved Multi-Level Gamma, UPDATE=1

As demonstrated in previous sections, the regular Multi-Level Gamma displays some discontinuities in saturation voltage and drain current. This occurs because when v_{sb} is less than VBO, simulation sets γ to γi and uses it to calculate i_{ds} and vsat. This is not correct; if (vds + vsb) exceeds VBO, then the depletion regions at the drain side expands into the substrate region, and the v_{sat} computation must use γb instead of γi. Because $v_{sat} = v_{gs} - v_{th}$ (drain), this model uses γi to compute the threshold voltage at the drain for vsb<VBO. As a result, the existing model overestimates the threshold voltage ($\gamma i > \gamma b$), and underestimates the saturation voltage and the drain current in the saturation region.

This causes a discontinuous increase in the saturation drain current, crossing from the vsb<VBO region to the vsb>VBO region.

The improved Multi-Level model upgrades the saturation voltage and drain current equations, compared to the regular Multi-Level model. To use the improved model, set the model parameter to UPDATE=1.

Example

You can see an example of a multi-level gamma model with UPDATE=2 using a netlist from a previous example. Change UPDATE=0 to UPDATE=2 in the netlist located in the following directory:

```
$installdir/demo/hspice/mos/tgam2.sp
```

Figure 30 Variation of IDS, VTH and VDSAT for UPDATE=2

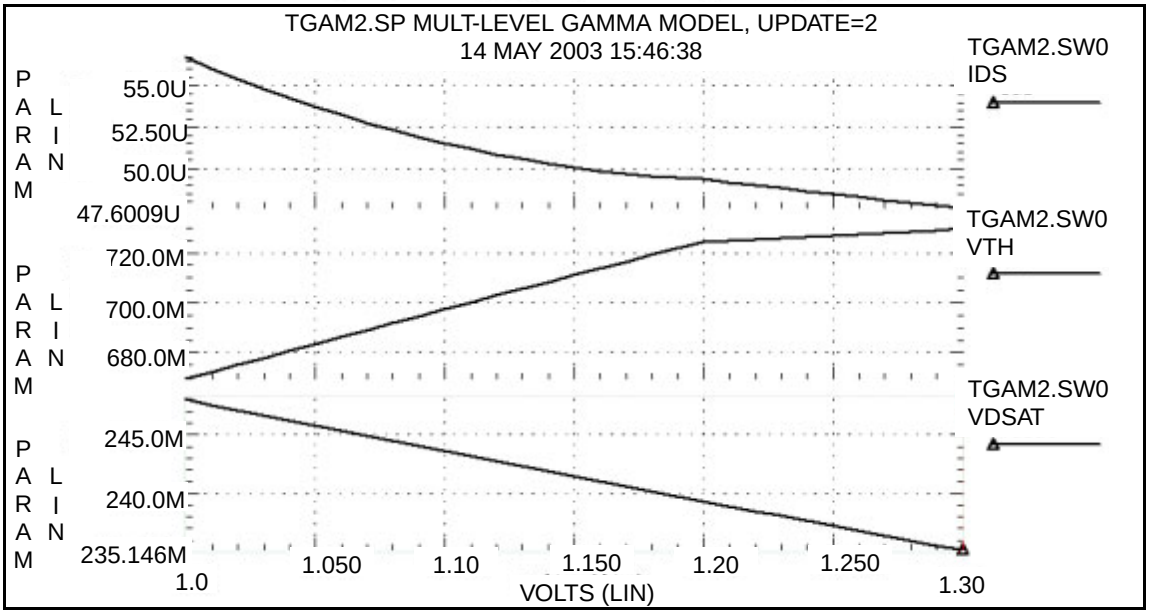
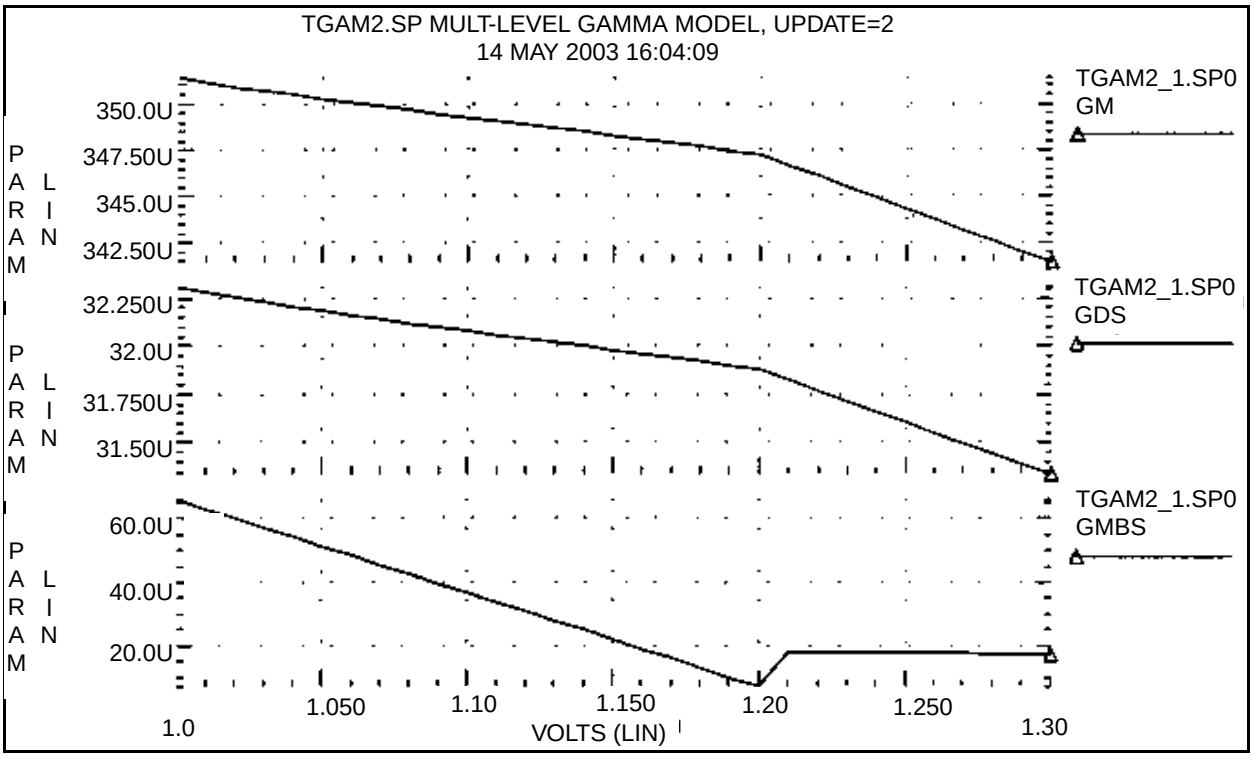


Figure 31 Variation of GM, GDS and GMBS for UPDATE=2



Each plot compares IDS, VTH, VDSAT, GM, GDS, and GMBS as a function of vsb for UPDATE=1.

Saturation Voltage, vsat

To obtain the right value for vsat, the following equations calculate two trial values of vsat corresponding to γi and γb:

$$vsat1 = \frac{vgs - vbi1}{\eta} + \frac{1}{2}\left(\frac{\gamma i}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma i}\right)^2 \cdot \left(\frac{vgs - vbi1}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

$$vsat2 = \frac{vgs - vbi2}{\eta} + \frac{1}{2}\left(\frac{\gamma b}{\eta}\right)^2 \cdot \left\{1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma b}\right)^2 \cdot \left(\frac{vgs - vbi2}{\eta} + PHI + vsb\right)\right]^{1/2}\right\}$$

- vbi1 is the built-in potential corresponding to γi.
- vbi2 is the built-in potential corresponding to γb.
- If (vdsat1 + vsb) ≤ VBO, then vdsat = vdsat1
- If (vdsat2 + vsb) > VBO, then vdsat = vdsat2

To obtain vdsat, vc modifies vsat for the carrier velocity saturation.

LEVEL 6 IDS Equations, UPDATE=1

You can use one of three equations for ids, depending on the region of operation. To derive these equations, this model integrates the bulk charge (vgs - vth (v) - v) from the source to the drain.

For vsb<VBO-vde, the model forms an entire gate depletion region in the implant layer.

$$ids = \beta \cdot \left\{ \left(vgs - vbi1 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma i \cdot \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right] \right\}$$

In the preceding equation, vbi1 is the same as vbi for vsb≤VBO.

For vsb ≥ VBO, the entire gate depletion region expands into the bulk area.

$$ids = \beta \cdot \left\{ \left(vgs - vbi2 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot \gamma b \cdot \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right] \right\}$$

In the preceding equation, vbi2 is the same as vbi for vsb>VBO.

$$ids = \beta \cdot \left\{ \left(vgs - vbi2 - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \cdot yi \cdot \left[(VBO + PHI)^{3/2} - (vsb + PHI)^{3/2} \right] \right\}$$

$$+ (\gamma i - \gamma b) \cdot (VBO + PHI)^{1/2} \cdot \left(VBO - vsb \right) \Bigg\}$$

For VBO-vde<vsb<VBO, the source side gate depletion region is in the implant layer, but the drain side gate depletion region expands into the bulk area.

Alternate DC Model (ISPICE model)

To invoke this model, set the KU>1 model parameter. Then, the model computes vfu and vfa scale factors to scale both the vds voltage and the ids current. These scale factors are functions of ECRIT and the vgs voltage. The following equations compute the vfa and vfu factors:

$$vfu = 1 - \frac{KU}{(\alpha^2 + KU^2)^{1/2} + \alpha(KU - 1)}$$

$$vfa = KA \cdot vfu^{(2 \cdot MAL)}$$

The following equation calculates the α value used in the preceding equations:

$$\alpha = \frac{ECRIT \cdot Leff}{vgs - vth}$$

Note: The vfu factor is always less than one.

The following equation modifies the ids current:

NU=1

$$ids = vfu^{(2 \cdot MBL)} \cdot ids$$

For NU=0, the $vfu^{(2 \cdot MBL)}$ factor is set to one.

The ids current is a function of the effective drain to source voltage (vde):

$$vde = \min(vds/vfa, vsat)$$

$$vdsat = vfa \cdot vsat$$

This alternate model is generally coupled with the mobility normal field equations (MOB=3) and the channel length modulation drain field equation (CLM=3).

The mobility equations use the following vde and vds values:

$$vde = \min(vds, vfa \cdot vsat), \quad \text{UPDATE=0}$$

$$vds = \min(vds/vfa, vsat), \quad \text{UPDATE=1,2}$$

Subthreshold Current, ids

is the choice of two different equations, selected through The WIC (Weak Inversion Choice) model parameter characterizes this region of operation.

Parameter	Description
WIC=0	No weak inversion (default)
WIC=1	ASPEC-style weak inversion
WIC=2	Enhanced HSPICE-style weak inversion

In addition to WIC, set the NFS parameter. NFS represents the number of fast states per centimeter squared. Reasonable values for NFS range from 1e10 to 1e12.

WIC=0, no weak inversion

WIC=1, the vth threshold voltage increases by the fast term

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

In the preceding equations, vt is the thermal voltage. The following equation specifies the ids current for vgs<von:

$$ids = ids(von, vde, vsb) \cdot e^{\frac{vgs - von}{fast}}$$

if vgs<von, then $ids = ids(vge, vde, vsb)$.

Note: Strong inversion conditions do not use the modified threshold voltage (von).

WIC=2

The subthreshold region is limited between the cutoff region and the strong inversion region. If the gate voltage is less than vth-PHI, this model cannot include any weak inversion conduction. However, this model can still include diffusion conduction from the drain-to-bulk rather than from the drain-to-source.

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}}\right]$$

Cutoff Region, vgs ≤ vth - PHI

$$ids = 0$$

Weak Inversion, vth - PHI < vgs ≤ von

$$ids = ids(von, vde, vsb) \cdot \left(1 - \frac{von - vgs}{fast + PHI}\right)^{WEX}$$

Strong Inversion, vgs > von

$$ids = ids(vgs, vde, vsb)$$

Note: Strong inversion conditions do not use the modified threshold voltage (von).

If WIC=3, simulation calculates the subthreshold current differently. In this case, the ids current is:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

N0eff and NDeff are functions of the effective device width and length.

Effective Mobility, ueff

All mobility equations have the following general form:

$$ueff = UO \cdot factor$$

Parameter	Description
ueff	Effective mobility at the specified a specified analysis temperature.
factor	Mobility degradation factor. Default=1.0

Use the MOB model parameter to select the mobility modulation equation used in the Level 6 MOSFET model.

Parameter	Description
MOB 0	No mobility reduction (default)
MOB 1	Gm equation
MOB 2	Frohman-Bentchkowski equation
MOB 3	Normal field equation
MOB 4	Universal field mobility reduction
MOB 5	Universal field mobility reduction with an independent drain field

Parameter	Description
MOB 6	Modified MOB 3 equations (lateral field effect included)
MOB 7	Modified MOB 3 equations (lateral field effect not included)

The following sections describe these equations.

MOB=0 Default, No Mobility

factor = 1.0No mobility reduction

Table 31 MOB=1 Gm Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Gate field mobility reduction
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor

Use the MOB=1 equation for transistors with constant source-to-bulk voltage, because the factor does not contain a vsb term. This equation sometimes over-estimates mobility for small gate voltages and large back-bias, such as depletion pull-ups.

$$factor = \frac{1}{1 + F1 \cdot (vgs - vb1 - F3 \cdot vde)}$$

$$vde = \min(vds, vdsat)$$

Note: In the alternate saturation model, vde is different if UPDATE=0 than if UPDATE=1. See Alternate DC Model (ISPICE model) on page 168. Also, if VMAX>0, then vde=min (vds, vsat). If you do not specify VMAX, then vde=min (vds, vdsat).

Table 32 MOB=2 Frohman-Bentchkowski Equation

Name (Alias)	Units	Default	Description
F1	V/cm	0.0	Critical gate-bulk electric field at which mobility reduction becomes significant.
UEXP (F2)		0.0	Mobility exponent. Use a factor of 0.36 for n-channel and 0.15 for p-channel.
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor.
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of carriers. The VMAX setting determines which calculation scheme vdsat uses. Zero indicates an infinite value.

The mobility reduction equation (MOB=2)[3] produces good results for high gate voltages and drain fields with constant back-bias. Typically, you can use this equation for p-channel pull-ups and n-channel pull-downs. The VMAX value selects the proper vdsat calculation scheme. MOB=2 (SPICE default) corresponds to MSINC UN=2.

$$factor = \left[\frac{F1 \cdot \varepsilon si}{COX \cdot (vgs - vbi - F3 \cdot vde)}\right]^{F2}$$

vde is the same in this equation as in the MOB=1 equation.

Table 33 MOB=3 Normal Field Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Low-field mobility multiplier
F4		1.0	Mobility summing constant
UEXP (F2)		0.0	Mobility exponent

Table 33 MOB=3 Normal Field Equation (Continued)

Name (Alias)	Units	Default	Description
UTRA (F3)	1/V	0.0	High-field mobility multiplier
VF1	V	0.0	Low to high field mobility (voltage switch)

This equation is the same as MSINC UN=1.

$(vgs - vth)^{F2} \leq$ VF1:

$$factor = \frac{1}{F4 + F1 \cdot (vgs - vth)^{F2}}$$

If UPDATE=0, and $(vgs-vth)^{F2} >$ VF1:

$$factor = \frac{1}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

If UPDATE=1, 2 and $(vgs-vth)^{F2} >$ VF1:

$$factor = \frac{1}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

Table 34 MOB=4 and MOB=5 Universal Field Mobility Reduction

Name (Alias)	Units	Default	Description
ECRIT	V/cm	0.0	Critical electric drain field for mobility reduction. Zero indicates an infinite value.
F1	V/cm	0.0	Source-drain mobility reduction field (typical values are 1e4 to 5e8).
MOB		0.0	Selects a mobility equation: • Set MOB=4 for the critical field equation. • Set MOB=5 for the critical field equation with an independent drain field.
UEXP (F2)	$1/V^{1/2}$	0.0	Bulk mobility reduction factor (typical values are 0 to 0.5).
UTRA (F3)	V/cm	0.0	Critical electric drain field for mobility reduction.

The MOB=4 equation is the same as the MSINC UN=3 equation. The MOB=5 equation is the same as MOB=4, except that F3 substitutes for ECRIT in the vc expression.

The MOB=5 equation provides a better fit for CMOS devices in the saturation region. Do not specify a VMAX value, because the mobility equation calculates the velocity saturation.

$$factor = \frac{1}{1 + \frac{COX}{F1 \cdot \varepsilon ox} \cdot (vgs - cth) + \frac{vde}{vc} + F2 \cdot (vsb + PHI)^{1/2}}$$

- *If MOB=4, then* $vc = ECRIT \cdot Leff$.
- *If MOB=5, then* $vc = F3 \cdot Leff$.

Note: If you use the alternate saturation model, vde is different for UPDATE=0 than it is for UPDATE=1, 2.

MOB=6, 7 Modified MOB=3:

This mobility equation is the same as MOB=3, except that the equation uses VTO instead of vth. If you specify MOB=6, the following equation modifies the ids current:

$$ids = \frac{ids}{1 + F1 \cdot \left(vgs - vth - \frac{vde}{2}\right) + \frac{UTRA}{Leff} \cdot vde}$$

Channel Length Modulation

The basic MOSFET current equation for ids describes a parabola, where the peak corresponds to the drain-to-source saturation voltage (vdsat). Long-channel MOSFETs generally demonstrate ideal behavior. For vds voltages greater than vdsat, ids current does not increase. As channel length decreases, current in the saturation region continues to increase.

The simulator models this increase in current as a decrease in the effective channel length. Except for CLM=5 and 6, this model calculates the channel length modulation equations only when the device is in the saturation region.

The Level 6 MOSFET model provides several channel length modulation equations; all (except CLM=5) modify the ids equation:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

ΔL is the change in channel length due to MOSFET electric fields.

The CLM model parameter designates the channel length modulation equation for the Level 6 MOSFET device model:

Parameter	Description
CLM = 0	No channel length modulation (default)
CLM = 1	One-sided step depletion layer drain field equation
CLM = 2	Frohman's electrostatic fringing field equation
CLM = 3	One-sided step depletion layer drain field equation with carrier velocity saturation
CLM = 4	Wang's equation: linearly graded depletion layer
CLM = 5	Synopsys channel length modulation
CLM = 6	Synopsys ΔL equations

The following sections describe these equations and the associated model parameters.

CLM=0 No Channel Modulation—Default

$$\Delta L = 0$$

This is the default channel length equation, representing no channel length modulation; it corresponds to MSINC GDS=0.0.

Table 35 CLM=1 Step Depletion Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KL		0.0	Empirical constant (saturation voltage)
LAMBDA (LAM, LA)	$cm/V^{1/2}$	1.137e-4	Channel length modulation. If you do not specify s, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.

$$\Delta L = LAMBDA \cdot (vds - vdsat)^{1/2} \cdot \left(\frac{vdsat}{vsat}\right)^{KL}$$

If you do not specify LAMBDA, simulation calculates it as:

$$LAMBDA = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB}\right)^{1/2}$$

This is a one-sided step depletion region formulation by Grove: ΔL varies with the depletion layer width, which is a function of the difference between the effective saturation voltage (vdsat) and the drain-to-source channel voltage (vds). Typically, you can use this equation for long channels and high dopant concentrations. This corresponds to GDS=1 in MSINC.

Table 36 CLM=2 Electrostatic Fringing Field

Name (Alias)	Units	Default	Description
A1		0.2	First fringing field factor, gate-drain
A2		0.6	Second fringing field factor, gate-vdsat

$$\Delta L = \frac{\varepsilon si}{COX} \cdot \frac{vds - vdsat}{A1 \cdot (vds - vgs + vbi) + A2 \cdot (vgs - vbi - vdsat)}$$

You can use the fringing field equation or electrostatic channel length reduction (developed by Frohman-Bentchkowski) to model short-channel enhancement transistors. In MSINC, the equivalent equation is GDS=2.

Table 37 CLM=3 Carrier Velocity Saturation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KA		1.0	vds scaling factor for velocity saturation.
KCL		1.0	Exponent for vsb scaling factor.
KU		0.0	Velocity saturation switch. If KU ≤ 1, simulation uses the standard velocity saturation equation.
LAMBDA (LAM, LA)	$cm/V^{1/2}$	1.137e-4	Channel length modulation. If you do not specify LAMBDA, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.
MAL		0.5	vds exponent for velocity saturation.
MCL		1.0	Short channel exponent.

$$\Delta L = vfu^{(2 \cdot MCL)} \cdot LAMBDA \cdot$$

$$[(vds - vfa \text{ Þ} vsat + KCL \cdot vsb + PHI)^{1/2} - (KCL \cdot vsb + PHI)^{1/2}]$$

This equation is an extension of the first depletion layer equation, CLM=1. It includes effects of carrier velocity saturation, and source-to-bulk voltage (vsb) depletion layer width. It represents the basic ISPICE equation. See Alternate DC Model (ISPICE model) on page 168 for definitions of *vfa* and *vfu*.

Table 38 CLM=4, Wang's Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
A1	m	0.2	Junction depth: A1scaled = A1 · SCALM
DND	cm^{-3}	1e20	Drain diffusion concentration

Linearly Graded Depletion Layer:

$$\Delta L = \left[\frac{2.73e5 \cdot A1scaled}{DNB \cdot \ln\left(\frac{DND}{DNB}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

Wang's equation can include junction characteristics to calculate the channel length modulation. The equation assumes that the junction approximates a linearly-graded junction, and provides a value of 0.33 for the exponent. This equation is similar to MSINC GDS=3.

Table 39 CLM=5, Channel Length Modulation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	amp/V^2	0	Constant coefficient
VGLAM	1/V	0	Constant coefficient

If CLM=5, the ids current increases by idssat:

$$idssat = \frac{weff}{Leff} \cdot LAMBDA \cdot vds \cdot (vgs - vth) \cdot [1 + VGLAM \cdot (vgs - vth)]$$

$$ids = ids + idssat$$

Note: The equation adds the idssat term to ids in all regions of operation. Also, LAMBDA is a function of the temperature.

Table 40 CLM=6, ΔL Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	1/V^{KL}	0	vds coefficient
LAM1	1/m	0	Channel length coefficient
KL		0	vds exponent
VGLAM	1/V	0	Gate drive coefficient

Unlike the other CLM values, this equation calculates the channel length modulation (ΔL) in all regions of operations, and uses it to modify the ids current.

$$\Delta L = \frac{Leff \cdot LAMBDA \cdot vds^{KL} \cdot [1 + VGLAM \cdot (vgs - vth)]}{1 + LAM1 \cdot Leff}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

Note: LAMBDA is a function of the temperature.

ASPEC Compatibility

To make MOSFET models compatible with ASPEC, specify ASPEC=1 in the **.OPTION** statement and LEVEL=6 in the associated MOSFET model statement.

If you assign the element parameters without keynames, specify the parameters in the same sequence as in the general format. The Level 6 MOSFET model assigns parameters in the order that you list them in the element statement. If parameter names are also element keynames, simulation reports errors.

If you use the ASPEC option, several program variations occur. The LEVEL model parameter is set to 6.

Note: Setting LEVEL=6 in the model does not invoke ASPEC.

MOSFET Option	WL = 1
General Options	SCALE = 1e-6 SCALM = 1e-6

ASPEC sets the SCALE and SCALM options so it effectively changes the default units in parameters that these options affect. Parameter values must be consistent with these scaling factors.

LEVEL	=	6
ACM	=	1
CJ	=	0.0
IS	=	0.0
NSUB	=	1e15
PHI	=	1 · Φ_f (the Fermi potential)
TLEV	=	1
TLEVC	=	1

Note: Do not calculate NSUB from GAMMA, if UPDATE=1 or 2.

TLEV (TLEVC) selects the ASPEC method of updating temperatures for the CJ, CJSW, PB, PHP, VTO, and PHI parameters.

Note: If you explicitly enter PHI, this model does not update it for temperature. SCALM does not affect how simulation scales parameters for the ASPEC mode. If you specify SCALM when you use ASPEC, the Level 7 MOSFET model generates an error stating that it ignores SCALM.

LEVEL 7 IDS Model

The LEVEL 7 model is the same as the LEVEL 6 model except for the PHI value.

If you specify PHI, then:

For LEVEL=6:

$\Phi_s = \frac{PHI}{2}$, where Φ_S is the surface potential.

For LEVEL=7:

$\Phi_s = PHI$

To transform a LEVEL 7 equation to LEVEL 6, make the following substitution:

$$PHI \rightarrow 2 \cdot PHI$$

To transform a LEVEL 6 model into a LEVEL 7 model, make the following substitution:

$$PHI(Level\ 7) = PHI(Level\ 6)/2$$

LEVEL 8 IDS Model

The LEVEL 8 MOSFET model, derived from research at Intersil and General Electric, is an enhanced version of the LEVEL 2 ids equation. LEVEL 2 differs from LEVEL 8 in the following areas:

- effective substrate doping
- threshold voltage
- effective mobility
- channel length modulation
- subthreshold current.

LEVEL 8 Model Parameters

MOSFET Level 8 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. This level also uses the parameters described in this section, which apply only to MOSFET Level 8.

Table 41 Channel Length Modulation Parameters, MOSFET Level 8

Name (Alias)	Units	Default	Description
A1		0.2	Channel length modulation exponent (CLM=8)
CLM		7	Channel length modulation equation selector
LAM1	1/m	0.0	Channel length modulation length correction
LAMBDA (LAM, LA)		0.0	Channel length modulation coefficient

LEVEL 8 Model Equations

This section lists the LEVEL 8 model equations.

IDS Equations

LEVEL 8 ids equations are the same as in the LEVEL 2 model (see LEVEL 2 Model Equations on page 130).

Effective Channel Length and Width

The Level 8 model calculates the effective channel length and width from the drawn length and width (see LEVEL 2 Model Equations on page 130).

Effective Substrate Doping, nsub

The SNVB model parameter varies the substrate doping concentration linearly as a function of vsb:

$$nsub = NSUB + SNVB \cdot vsb$$

The preceding equation computes γ, ϕ, and xd parameters for nsub:

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{si} \cdot q \cdot nsub}}{COX}$$

$$\Phi = 2 \cdot vt \cdot \ln\left(\frac{nsub}{ni}\right)$$

$$xd = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q \cdot nsub}}$$

If SNVB is zero, then γ = GAMMA. You can adjust the γ value for the short-channel effect the same way as in the LEVEL 2 model. NSUB calculates the ϕ value.

Threshold Voltage, vth

ETA specifies the threshold voltage reduction due to the potential barrier lowering effect.

$$vbi = VTO - g \cdot \sqrt{\Phi} - \frac{8.14e\text{-}22 \cdot ETA}{COX \cdot L_{eff}^3} \cdot vds + (\eta - 1) \cdot (vsb + \Phi)$$

$$vth = vbi + g \cdot \sqrt{vsb + \Phi}$$

Modify γ for the short-channel effect, the same as in the LEVEL 2 model to obtain the effective γ.

Saturation Voltage vdsat

Level 8 computes the vsat saturation voltage the same way as in the LEVEL 2 model. This model includes the carrier velocity effect only if ECRIT is greater than zero.

ECRIT > 0:

$$vdsat = vsat + vc - \sqrt{vsat^2 + vc^2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECRIT \cdot L_{eff}$$

ECRIT ≤ 0 or MOB=7:

$$vdsat = vsat$$

This model computes *vsat* as in the LEVEL=2 model (see Saturation Voltage, v_{dsat} on page 132).

Effective Mobility, ueff

The MOB mobility equation selector controls the mobility reduction equations. In the LEVEL 8 model, set MOB to 2, 3, 6, or 7. Default=6.

MOB=2 Mobility Reduction

$$u_{eff} = UO \cdot \left[\frac{\varepsilon_{se} \cdot UCRIT}{COX \cdot (vgs - vth - UTRA \cdot vde)} \right]^{UEXP}$$

MOB=3 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + \frac{2.1e\text{-}8 \cdot (vgs + vth + egfet - \Phi)}{6 \cdot TOX}}$$

In the preceding equation, *egfet* is the silicon energy gap at the analysis temperature:

$$egfet = 1.16 - \frac{7.02e\text{-}4 \cdot t^2}{t + 1108}$$

In the preceding equation, *t* is the temperature in degrees Kelvin.

If VMAX>1:

$$u_{eff} = \frac{u_{eff}}{1 + \frac{u_{eff}}{VMAX \cdot L_{eff}} \cdot vde}$$

MOB=6 Mobility Reduction

For UEXP>0:

If $(vgs - vth) > \frac{\varepsilon_{si} \cdot UCRIT}{COX}$

then $u_{eff} = \frac{UO \cdot \left[\frac{\varepsilon_{si} \cdot UCRIT}{COX \cdot (vgs - vth)}\right]^{UEXP}}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$

otherwise, $u_{eff} = \frac{UO}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$

For UEXP=0:

$$u_{eff} = \frac{UO}{[1 + UCRIT \cdot (vgs - vth)] \cdot \left(1 + \frac{UTRA}{L_{eff}} \cdot vde\right)}$$

UCRIT for UEXP=0 has a dimension of (1/V).

MOB=7 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + UTRA \cdot \left(vgs - vbi - \eta \cdot \frac{vde}{2} + \frac{body}{vde} \right)}$$

The following equation calculates the body value used in the preceding equation:

$$body = \frac{2}{3} \cdot \gamma \cdot [(vde + vsb + \Phi)^{3/2} - (vsb + \Phi)^{3/2}]$$

Channel Length Modulation

The CLM equation selector controls the channel length modulation equations. In the LEVEL 8 model, set CLM to 6, 7, or 8. Default=7.

CLM=6 SPICE Channel Length Modulation

If LAMBDA=0:

$$\lambda = \frac{xd}{leff \cdot vds} \cdot \sqrt{\frac{vds - vdsat}{4} + \sqrt{1 + \left(\frac{vds - vdsat}{4} \right)^2}}$$

Otherwise, $\lambda = LAMBDA$.

Then:

$$\Delta L = \frac{\lambda \cdot L_{eff} \cdot vds}{1 + LAM1 \cdot L_{eff}}$$

Note: The LEVEL 2 model has no LAM1 term.

This model modifies the current for the channel length modulation effect in the entire regions:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

CLM=7 Intersil Channel Length Modulation

If CLM=7, this model computes ΔL only for the saturation region.

vds > vdsat

$$\Delta L = \frac{LAMBDA \cdot L_{eff}}{1 + LAM1 \cdot L_{eff}} \cdot (vds - vdsat)$$

$$ids = \frac{ids}{L - \frac{\Delta L}{L_{eff}}}$$

CLM=8

If CLM=8, this model computes ΔL only for the saturation region.

vds > vdsat

$$\Delta L = \frac{L_{eff}}{1 + \frac{(1 + LAM1 \cdot L_{eff}) \cdot (1 + vde)^{A1}}{LAMBDA \cdot (vds - vde)}}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Subthreshold Current Ids

The LEVEL 8 model has different subthreshold current equations, depending on the value of the CAV model parameter.

Define:

$$fast = vt \cdot \left[\eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + \Phi)^{1/2}} + \frac{\varepsilon_{si} \cdot q \cdot SNVB \cdot \sqrt{vsb + \Phi}}{\gamma \cdot COX^2}\right]$$

CAV≠0

$$von = vth + CAV \cdot fast$$

Subthreshold Region, vgs < von

If vgs>vth:

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left\{\left[\frac{1}{fast} - \frac{(CAV - 2) \cdot (vgs - vth)}{2 \cdot CAV^2 \cdot fast^2}\right](vgs - vth)\right\}}$$

If vgs≤vth

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1-\frac{CAV}{2}\right)} \cdot e^{\left(\frac{vgs-vth}{fast}\right)}$$

CAV=0

If CLM=8: $von = vth + 3 \cdot fast$

otherwise: $von = vth + 2 \cdot fast$

Subthreshold Region, vgs<von

$$ids = ids(von, vde, vsb) \cdot e^{\left(\frac{vgs-von}{fast}\right)}$$

If WIC=3, the next equation calculates the ids subthreshold current:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

N0eff and NDeff are functions of effective device width and length.

LEVEL 27 SOSFET Model

MOSFET Level 27 is a three-terminal silicon-on-sapphire (SOS) FET transistor model.[4] This SOSFET model is based on a sapphire insulator that isolates the substrate and models the behavior of SOS devices more accurately than standard MOSFET models with physically unreal parameter values. The SOSFET model also includes a charge conservation model (based on the Ward and Dutton model).

Because the defaults of the SOSFET model parameters depend on the channel length, you must specify the SOSLEV model parameter to select either the 5 μm or 3 μm processing model.

SOSLEV=1 selects the 5 μm model; otherwise, this model automatically uses the 3 μm value, including the second-order effects (default=3 μm).

Note: This model does not include bulk nodes. If you specify bulk nodes, simulation ignores them.

This model does not use the ACM model parameter, because it does not include any junction diodes. Also, the only value that the CAPOP model parameter accepts is 7. Seven is its own charge conservation model, which you cannot use in other MOSFET models.

Temperature compensation equations for the VTO and UO SOSFET model parameters are the same as those in the MOSFET model.

Note: This model includes a special option for bulk nodes for silicon on sapphire. In the model definition, if you specify -1 for the bulk node, this model generates a special node for each element. This bulk node is named in the form, B#<*element name*>, where the element name is the name of the defined element. Use this name in any statement, such as a .PRINT statement to refer to the bulk node in the element.

Syntax

```
.MODEL mname PMOS <LEVEL=27> <SOSLEV=val>
   + <pname1=val1>

.MODEL mname NMOS <LEVEL=27> <SOSLEV=val>
   + <pname=val1>
```

You can use this **.MODEL** syntax to include a MOSFET Level 27 model in your HSPICE netlist. For a general description of the **.MODEL** statement, see the *HSPICE Command Reference*.

Parameter	Description
mname	Model name.
PMOS	Identifies a p-channel MOSFET model.
NMOS	Identifies an n-channel MOSFET model.
LEVEL	Model level selector.
SOSLEV	Selects the processing model. If you set SOSLEV=1, the default=5µm. The automatic default=3µm.
pname	Parameter model.

LEVEL 27 Model Parameters

Table 42 5-μm Model Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
LD	m		Lateral diffusion. The default=0.6μ (n- type), 0.3μ (p-type).
RSH	ohm/sq		Drain and source diffusion sheet resistance. The default=25 (n¦-type), 100 (p-type).
SOSLEV		1	Model index.
TOX	m	7.0e-8	Oxide thickness.
UO	$cm^2/(V \cdot s)$		Surface mobility. Default=350 (n-type), 220 (p-type).
VTO	V		Threshold voltage. Default=1.25 (n-type), -1.25 (p-type).

Table 43 3-μm Model Parameters

Name (Alias)	Units	Default	Description
A	m/V	0.1μm	Channel length shortening coefficient (2nd effect)
ALPHA	V/m		Threshold voltage length dependence. Default=0.15μ (n-type), 0.18μ (p-type).
CAPOP		7	Capacitance model selector.

Table 43 3-μm Model Parameters (Continued)

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=4.6e-10 (n-type), 3.6e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type).
EC	V/m		Critical electric field for velocity saturation (2nd effect). The default=3.0e6 (n-type), 7.5e6 (p-type).
FB			Body effect coefficient (2nd effect). Default=0.15 (n-type), 0 (p-type).
LD	m		Lateral diffusion. Default=0.3μ (n-type), 0.2μ (p-type).
LEVEL		27	Model level selector.
RSH	ohm/sq		Drain and source diffusion sheet resistance. Default=25 (n-type), 80 (p-type).
SOSLEV		2	Model index.
THETA	1/V		Mobility degradation coefficient (2nd effect). Default=0.055 (n-type), 0.075 (p-type).
TOX	m	3.4e-8	Oxide thickness.
UO	$cm^2/(V \cdot s)$		Surface mobility. Default=370 (n-type), 215 (p-type).
VTO	V		Threshold voltage. Default=0.83 (n-type), -0.74 (p-type).

Example

The netlist for this example is located in the following directory:

```
$installdir/demo/hspice/mos/ml27iv.sp
```

Non-Fully Depleted SOI Model

Several MOSFET models are currently available for SOS/SOI applications. The 3-terminal SOS model (LEVEL=27) is stable for circuit design usage, but has some limitations. This model does not provide for depleted bulk. Use it only with applications that are not fully depleted and that do not consider kink effects.

The following circuit example is a 4-terminal SOI model for incompletely depleted bulk with the kink effect. Its sub-circuit allows a parasitic capacitance to the substrate. In this example, the bulk is the region under the channel. This model assumes that the substrate is the conductive layer under the insulator.

- For SOI, the insulator is usually silicon dioxide and the substrate is silicon.
- For SOS, the insulator is sapphire and the substrate is the metal that contacts the back of the integrated circuit die.

Model Components

This model consists of the following subcomponents:

- Core IDS model: any level works because the impact ionization and weak inversion models are common to all DC levels. The example uses a LEVEL=3 DC MOS model.
- Subthreshold model: the WIC=3 model parameter allows the older models to use the more advanced models found in the BSIM (LEVEL=13, LEVEL=28) models. The N0 model parameter should have a typical value around 1.0.
- Impact ionization model: set ALPHA and VCR parameters to enable the impact ionization model, which is available to all MOS DC equations. Typical values are ALPHA=0.1 and VCR=18.
- Charge conservation gate cap model (CAPOP=9, XQC=.4) prevents the floating bulk node from obtaining extreme values.
- The automatic periphery diode area calculation method (ACM) is set to 3 to automatically calculate the source and drain resistances and diode junction leakage, and the capacitance. (ACM=3 CJ=0 CJSW=0 CJGATE=4e-10 JS=0 JSW=1e-9 LD=.1u HDIF=1.5u RS=40 RD=40 N=1).

Note: These models assume that the source/drain diffusions extend to the buried oxide. The area part of the diode has no capacitance to bulk. However, the subcircuit includes linear capacitors to the substrate.

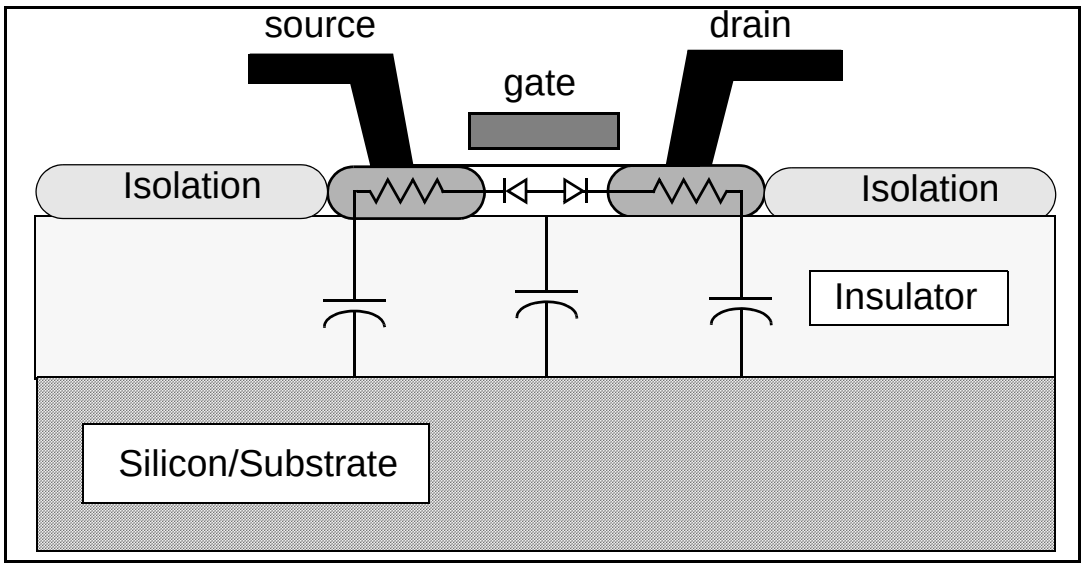
Obtaining Model Parameters

Use the optimizing capabilities in the Level 27 MOSFET model to obtain the core IDS model parameters.

Use the optimizer to obtain the core model, subthreshold, and impact ionization parameters. The subthreshold model selected is an improved BSIM type of model that was altered for the older models. The charge conservation model is more charge conserving than the original Ward-Dutton model in SPICE 2G6.

Calculating the automatic diode area and the resistance estimates the junction capacitance, saturation current, and resistance as a function of the transistor width. Use the VNDS and NDS parameters for a piecewise linear approximation to reverse the junction current characteristics.

Figure 32 Non Fully Depleted SOI Model

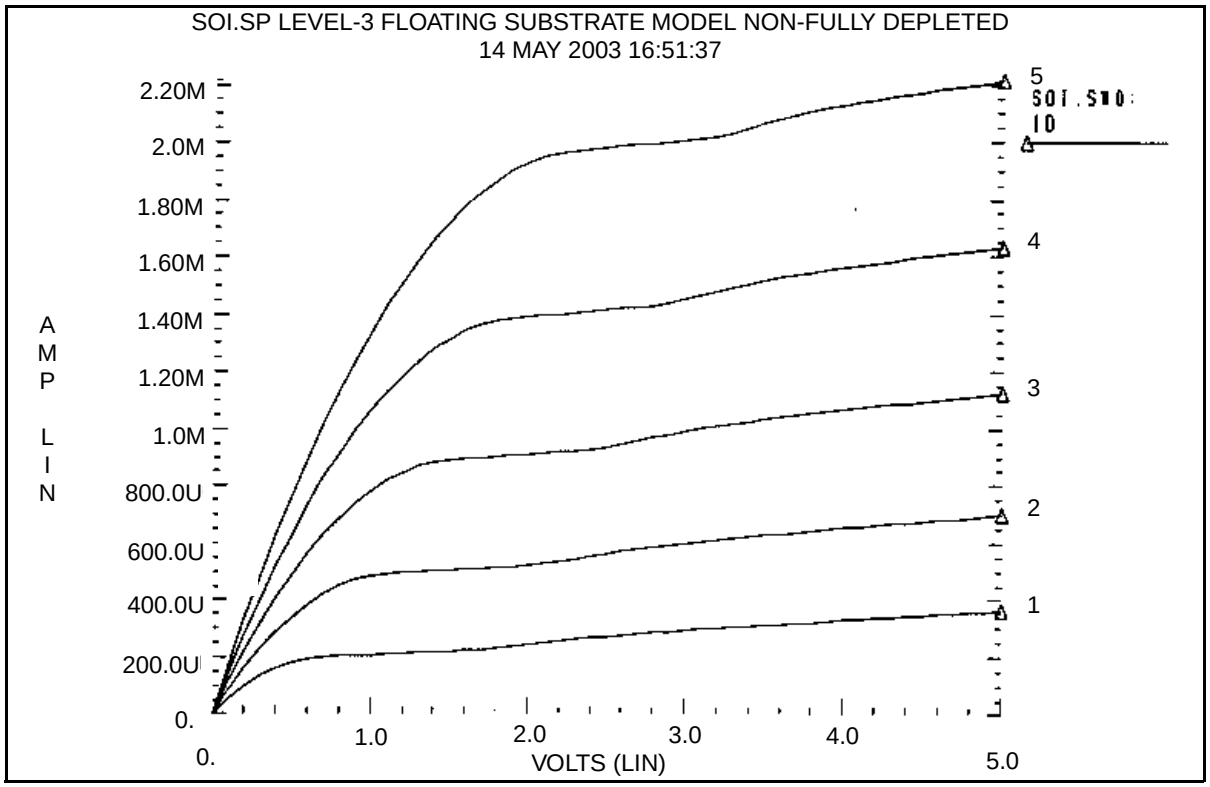


Example

The netlist for this example is located in the following directory:

`$installdir/demo/hspice/mos/ssoi.sp`

Figure 33 LEVEL 3 Floating Bulk Model



Fully Depleted SOI Model Considerations

Fully depleted transistors require additional modeling equations. The first-order effects are:

- Threshold sensitivity to the substrate.
- No kink current.
- Silicon thickness limits the minimum depletion capacitance.

Lack of these effects does not seriously affect an inverter, because the source-to-substrate voltage does not move. Digital circuits with good gate drive are not seriously affected, because a large gate voltage renders a small Vth shift to a small change in the IDS current.

The substrate threshold sensitivity can affect circuits such as analog amplifiers that include transistors at back-bias and low gate voltages.

LEVEL 38 IDS: Cypress Depletion Model

The LEVEL 38 Cypress Depletion MOSFET model (Cypress Semiconductor Corporation) is a further development of the Synopsys Level 5 MOSFET device model. Level 38 features:

- BSIM-style length and width sensitivities
- Degraded body effect at high substrate bias (second GAMMA)
- Empirical fitting parameters for Ids current calculations in the depletion mode of operations
- A comprehensive surface mobility equation
- Drain-induced barrier lowering

At the default parameter settings, the LEVEL 38 model is basically backwards-compatible with LEVEL 5 /ZENH=0.0 with the exception of the surface mobility degradation equation (see the discussion on the next page). Refer to the documentation for LEVEL 5 for the underlying physics that forms the foundation for the Huang-Taylor construct.

In LEVEL 38, the temperature compensation for threshold is ASPEC-style, concurring with the default in LEVEL 5. This section describes the model parameters that are unique to this depletion model. It also describes additional temperature compensation parameters.

LEVEL 38 lets you use all Synopsys device model capacitance options (CAPOP). CAPOP=2 is the default setting for LEVEL 38. If you set CAPOP=6 (AMI capacitance model), LEVEL 38 capacitance calculations become identical to those of LEVEL 5.

The ACM default parameter (ACM=0 in LEVEL 38) invokes SPICE-style parasitics. You can set ACM to 1 (ASPEC), or to 2 (Synopsys device model). All MOSFET models follow this convention.

You can use **.OPTION SCALE** with the LEVEL 5 MOSFET device model. However, you cannot use the SCALM option, due to the difference in units. You also cannot use the DERIV option.

You *must* specify the following parameters for MOS LEVEL 38: VTO (VT), TOX, UO (UB), FRC, ECV, and NSUB (DNB).

As with LEVEL 5, this model calculates the Ids current according to three gate voltage regions:

Depletion Region, vgs - vfb < 0

The low gate voltage region, which the bulk channel dominates.

Enhancement Region, vgs - vfb > 0, vds < vgs - vfb

The region defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.

Partial enhancement region, vgs - vfb > 0, vds > vgs - vfb

This region has high gate and drain voltages so the surface region is partially turned on, and the bulk region is fully turned on.

To better model depletion region operations, empirical fitting constants have been added to the original Huang-Taylor mechanism to account for the effects caused by nonuniform channel implants and also to make up for an oversight in the average capacitance construct[5]. The enhancement region uses a significantly more elaborate surface mobility model.

Body effect in LEVEL 38 is calculated in two regions[6].

Bulk body effect, vsb-vsbc > 0

With sufficiently high (and negative) substrate bias (exceeding vsbc), the depletion region at the implanted channel-substrate junction reaches the Si-oxide interface. Under such circumstances, the free carriers can accumulate only at the interface (as in an enhancement device) and the bulk doping level determines the body effect.

Implant-dominated body effect, vsb-vsbc < 0

Before reaching vsbc, and as long as the implant dose overwhelms the substrate doping level, the deeply-buried transistor (due to the implant) dominates the body effect of the depletion mode device. The $\bar{\gamma}$ body effect coefficient is proportional to both the substrate doping and to the first-order implant depth. In Level 38, the BetaGam empirical parameter amplifies the body effect due to deep implant.

Model parameters that start with L or W represent geometric sensitivities. In the model equations, three model parameters determine the zX quantity (X is the variable name):

- Large-and-wide channel case value (X).
- Length sensitivity (LX).
- Width sensitivity (WX).

The model calculates these parameters according to zX=X+LX/Leff+WX/Weff. For example, the following equation calculates the zero field surface mobility:

$$zUO = UO + \frac{LUO}{leff} + \frac{WUO}{weff}$$

Note: This model uses mostly micrometer units rather than meter units. Units and defaults are often unique in LEVEL 38. The finite difference method calculates the I_{ds} derivatives that define the gm, gds, and gmbs small signal gains. This model does not use the SCALM and DERIV options.

LEVEL 38 Model Parameters

MOSFET Level 38 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. This level also uses the parameters described in this section, which apply only to MOSFET Level 38.

Table 44 Capacitance Parameters

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	µm	0.0	Metal overlap on gate

LEVEL 38 Model Equations

IDS Equations

Depletion, vgs-vfb <0

$$ids = \beta 1 \cdot \left\{ q \,.\, zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. -\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

Enhancement, vgs-vfb vde >0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} + \beta \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, vgs-vfb<vde

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} + \left(\frac{1}{2}\beta - \frac{1}{2}\beta 1 \text{ Þ} cav \right) \cdot (vgs - vfb)^2$$

The following equations calculate values used in the preceding equations:

$$\beta 1 = \frac{zKBeta1}{1 + UHSAT \cdot \frac{vde}{Leff}} \cdot UH \cdot \frac{Weff}{Leff}$$

$$\beta = UBeff \cdot cox \cdot \frac{Weff}{Leff} \qquad cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{KCS \cdot \varepsilon Si}{DP \cdot 1e\text{-}4} \qquad Phid = vt \cdot \ln\left(\frac{DNB \cdot nd}{ni^2}\right)$$

$$nd = \frac{NI \cdot 1e4}{DP} \qquad vde = \min(vds, vdsat)$$

The temperature dependence of the mobility terms assume the ordinary exponential form:

$$UH(t) = UH(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

$$zUO(t) = zUO(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

The following equation calculates the continuity term at the body effect transition point:

$$Icrit = -\frac{2}{3} \cdot cav \cdot [(vde + vsbc + Phid)^{3/2} - (vsbc + Phid)^{3/2}] \cdot \gamma \cdot \left(\frac{1}{zBetaGam} - 1\right)$$

This model uses the preceding equation if vsb>vsbc. Otherwise:

$$Icrit = 0$$

The following sections describe saturation voltage, threshold voltage, body effect transition voltage, and the $\bar{\gamma}$ body effect coefficient.

Threshold Voltage, vth

The VTO model parameter, often called the “pinch-off,” is a zero-bias threshold voltage extrapolated from a large device operating in the depletion mode. The following equation calculates the effective pinch-off threshold voltage, including the device size effects and the terminal voltages:

$$vth = vfb - \beta d \cdot [vch - \bar{\gamma} \cdot (Phid + vsb)^{1/2} + vcrit]$$

The following equations calculate values used in the preceding equation:

$$vfb = zVTO - zETA \cdot vds + \beta d \cdot (vch - \gamma_0 \cdot Phid^{1/2})$$

$$vcrit = \left(\gamma - \frac{\gamma}{zBetaGam}\right) \cdot (Phid + vsbc)^{1/2} \quad \text{for vsb > vsbc; 0 otherwise.}$$

$$\beta d = \frac{UH \cdot cav}{zUO \cdot cox} \qquad vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot \varepsilon si \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB} \qquad nd = \frac{NI}{DP \cdot 1e\text{-}4}$$

The following equation computes the effective $\bar{\gamma}$, including small device size effects:

$$\bar{\gamma} = \frac{\gamma}{zBetaGam} \quad \text{for vsb>vsbc, and =g otherwise.}$$

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equations:

If SCM ≤0, then $scf = 0$.

Otherwise:

$$scf = \frac{XJ}{Leff} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot vds + vsb + Phid)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM ≤0, then $ncf = 0$.

Otherwise:

$$ncf = \frac{NWM \cdot xd \cdot (Phid)^{1/2}}{Weff}$$

This equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB} \right)^{1/2}$$

The following equation calculates the body effect transition point:

$$Vsbc = \frac{qDP^2}{2\varepsilon si} \left(\frac{NI}{DP \cdot 1e-4} - DNB \right) + zDVSBC + TDVSBC \cdot (t–tnom) - Phid$$

If vgs ≤ vth, this model inverts the surface and includes a residual DC current. If vsb is large enough to make vth > vinth, then vth is the inversion threshold voltage.

To determine the residual current, simulation inserts vinth into the ids, vsat, and mobility equation in place of vgs (except for vgs in the exponential term of the subthreshold current). The following equation computes the inversion threshold voltage (vinth) at a specified vsb:

$$vinth = vfb - \frac{q \cdot NI}{cox} - vsb + DVIN–zETA \cdot vds$$

Saturation Voltage, vdsat

This equation determines the vsat saturation voltage:

$$vsat = vgs - vfb + vch + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (vgs - vfb + vch + vsb + Phid) \right]^{1/2} \right\}$$

$$vdsat = vsat$$

Simulation modifies vsat to include the carrier velocity saturation:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECV \cdot Leff$$

Mobility Reduction, UBeff

The UB surface mobility depends on the terminal voltages:

$$UBeff = \frac{1}{\frac{1}{zUO} + \frac{(zFRC + zVFRC \cdot vde + zBFRC \cdot vsb) \cdot (vgs - vfb)}{TOX} + \frac{vde}{VST \cdot Le} + zFSB \cdot vsb^{1/2}}$$

The following equations calculate *Le* for the preceding equation:

$Le = Leff$ Linear region

$Le = Leff - \Delta L$ Saturation region

At elevated temperatures, the following equation calculates the zFRC value used in the preceding equation:

$$zFRC(t) = zFRC(tnom) \cdot \left(\frac{t}{tnom} \right)^{FRCEX}$$

ΔL is the channel length modulation effect, defined in the next section. v_{fb} assumes the role of v_{th} in the LEVEL 5 mobility equation. The degradation parameters are semi-empirical, and are grouped according to their (linearized) mathematical dependencies instead of their physical origin to better provide parameter extraction.[7]

Channel Length Modulation

To include the channel length modulation, modify the ids current:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

The following equation calculates ΔL for the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)}\right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and na1 is in cm^{-3}.

Subthreshold Current, ids

If device leakage currents become important for operation near or below the normal threshold voltage, the model considers the subthreshold characteristics. In the presence of surface states, this equation determines the effective threshold voltage (von):

$$von = max(vth, vinth) + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (Phid + vsb)^{1/2}}\right]$$

If vgs <von, then:

Partial Enhancement, 0< vgs-vfb < vde

$$ids = \beta 1 \cdot \left\{q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2}\right]\right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit\right\}$$

$$+ \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{vgs - von}{fast}} - \beta 1 \cdot cav\right) \cdot (von - vfb)^2$$

Full Enhancement, vgs-vfb -vde > 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

$$+ \beta \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{vgs - von}{fast}}$$

Depletion, vgs-vfb < 0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} \cdot e^{\frac{vgs - von}{fast}}$$

Example Model File

```
$ file Depstor.mod
   .MODEL DEPSTOR NMOS LEVEL=38
   * PARASITIC ELEMENTS
   + ACM=1
   + LD=0.15u WD=0.2u $ for LEFF AND WEFF
   + CJ=0.3E-16 MJ=0.4 PB=0.8 JS=2.0E-17 $ INTRINSIC DIODE
   + CJSW=0 MJSW=0.3
   + BULK=98 $ DEFAULT NODE FOR SUBSTRATE
   * THRESHOLD
   + VTO=-2.5 LVT=-0.25 WVT=0
   + leta=0.02 eta=0.0 weta=0.0
   + TCV=0.003   $ TEMPERATURE COEFFICIENT
   *  MISC
   + DVIN=0.5 PHI=0.75
   + NFS=2e10    DNB=3.0E16
```

Mobility Model

```
+ UH= 1300
   + UO=495   FRC= 0.020 FSB=5e-5    VFRC=-1e-4    BFRC=-0
   + LUO=-100 LFRC=.03   LFSB=-1e-5  LVFRC=-.002   LBFRC=-
   1e-3
```

```
   + WUO=-30 WFRC=-0.01 WFSB=5e-5  WVFRC=-0.00  + WBFRC=-
   0.4e-3
   + KI0= .9 KBETA1=.5   LKI0=0.16   LKBETA1=-0.15
   + WKI0=0.0   WKBETA1=-0.0
   + BEX=-1.3 TUH=-1.0 Frcex=1.0
```

Body Effect

```
+ NWM=0.5   SCM=.1
   + DVSBC=0.1   LDVSBC=0  WDVSBC=0
   + TDVSBC=.002
   + BetaGam=0.9   LBetaGam=-.2 WBetaGam=.1
```

Saturation

```
+ ECV=   2.9  VST=8000   UHSAT=0
   * CHANNEL LENGTH MODULATION
   + XJ= 0.1
   * OXIDE THICKNESS AND CAPACITANCE
   + TOX=165 CGSO=0 CAPOP=2
   * CHANNEL IMPLANT
   + NI=1.5e12     KCS=3  DP=0.25
   *.END
```

LEVEL 40 HP a-Si TFT Model

The Synopsys Level 40 MOSFET device model represents a Hewlett-Packard amorphous silicon thin-film transistor model.

MOSFET Level 40 uses only the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters.

Using the HP a-Si TFT Model

1. Set LEVEL=40 to identify the model as the HP a-Si TFT model.
2. Default value for L is 10µm, and the default value for W is 40 µm.
3. Use the “M” designation for MOSFET rather than the “A” designation for a-Si TFT in the netlist.
4. Use the “NMOS” or “PMOS” designation for device type rather than the “NAT” or “PAT” designation.

Note: Because of the unavailability of p-channel TFTs, PMOS model testing has been limited.

5. LEVEL 40 is a three-terminal model. It lacks bulk nodes so simulation does not append any parasitic drain-bulk or source-bulk diodes to this model. You can specify a fourth node, but it does not affect the simulation results (except for GMIN terms).
6. Parasitic resistances and overlap capacitances are constant. They are not scaled with width, length, and temperature.
7. Capacitance expressions in this model do not conserve charge.
8. The TREF parameter is an exponent in an expression for mobility temperature dependence.
9. Other models use the BEX parameter for similar mobility temperature dependence expressions. The HP a-Si TFT TREF model parameter is not the same as the TREF reference temperature in other models. The reference temperature for the HP a-Si TFT model is 312 K (or 38.85 ^{o}C); you cannot modify it. Experimental results from TFT manufacturers indicate that amorphous silicon materials are most stable at this temperature.
10. The default room temperature is 25^{o} C in Synopsys circuit simulators, but is 27^{o} C in most other simulators. When comparing to other simulators, set the nominal simulation temperature to 27^{o} C by using either .TEMP 27 or **.OPTION** TNOM=27 in the netlist. Although the reference temperature of the HP a-Si TFT model is fixed at 312^{o} K (or 38.85 ^{o}C), the behavior of the model adjusts to other simulation temperatures that you specify, or that are defaults in Synopsys circuit simulators. In the Level 40 MOSFET model, temperature dependency is enabled.
11. The default CAPOP value is 40, which is the HP a-Si TFT non-charge-conserving capacitance model. CAPOP values of 0, 1, 2, 3, 4, 5, 9, 12, or 13 have not been thoroughly tested.
12. The DERIV default is zero, which selects the analytical method. Set DERIV to 1 to select the finite difference method.

Effect of SCALE and SCALM

.OPTION SCALE has the same effect for LEVEL 40 as for other Synopsys device models, such as MOSFET Level 3 or Level 28. If you specify the L and W values in microns rather than meters (for example, L=1 rather than L=1µ or 1e-6), set **.OPTION** SCALE=1e-6.

The SCALM option is disabled in the LEVEL 40 model. For standard MOSFET models (such as LEVEL 3), SCALM affects the scale of model parameters such as XL, XW, LD, WD, CJ, and CJSW.

Because the LEVEL 40 model ignores the SCALM option, you can mix LEVEL 40 models in a simulation with other models that use SCALM.

In general, netlists for Synopsys simulators should be as standard as possible. Also, you should convert L and W to meters scale instead of microns scale so that you can use the netlist without **.OPTION** SCALE=1E-6. If you follow these recommendations, a system-level simulation can use I/O sub-circuits from different vendors.

Noise Model

The LEVEL 40 model uses the standard NLEV=0 noise model inherited from other Synopsys MOSFET models.

DELVTO Element

You can use DELVTO and DTEMP on the element line with LEVEL 40.

Device Model and Element Statement Example

```
.MODEL nch nmos LEVEL=40 UO=0.4229 VTO=1.645 PHI=1.25 NSS=0
   + NFS=2.248E+21 VMAX=1231
   + THETA=-0.01771 ETA=0.0002703 T1=2.6E-07 T2=0 E1=3.9
   E2=0
   + GO=9.206E-15 NU=0 K2=2 CHI=0.5
   + PSI=1E-20 VTIME=0.01 TREF=1.5 CGSO=5.203E-14
   CGDO=4.43E-14
   + CSC=0.0001447 RD=5097
   + RS=5097 FREQ=1E+06 DEFF=2.15 TAU=1.64E-07 FEFF=0.5
   MCKT 1 2 3 nch L=1e-05 W=4e-05
```

LEVEL 40 Model Equations

The following equations show model parameters in all capital letters; working variables are in lower case. Model parameters and the vgs and vds bias voltages are inputs. Ids, gm, and gds are the DC outputs. The Cgs gate-to-source capacitance and the Cgd gate-to-drain capacitance are the AC outputs. The electron charge is q, the Boltzmann's constant is k, and the permittivity of a vacuum is $\varepsilon 0$.

This model applies the SCALE value before evaluating the equations, and scales by M after evaluation.

gm_{tft} and gds_{tft} variables are intermediate, not final, quantities.

For a complete description of TFT technology and the device physics underlying these equations, see the Hewlett-Packard HP IC-CAP manual.

Initially, $Cgdi = 0$, $Cgsi = 0$, $phi = PHI$, $vto = VTO$, and $uo = UO$.

If $uo = 0$, then $uo = 1$.

The following equation computes the Cfm dielectric capacitance per unit area:

If $T1 \neq 0$ and $T2 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E1 \cdot E2)}{((T2 \cdot E1) + (T1 \cdot E2))}$

If $T1 = 0$ and $T2 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E2)}{T2}$

If $T2 = 0$ and $T1 \neq 0$, then $Cfm = \frac{(\varepsilon 0 \cdot E1)}{T1}$

$kp = uo \cdot Cfm \cdot 10^{-4}$

TEMP is the Synopsys device simulation temperature, specified in ^{o}C, but converted to ^{o} K internally to evaluate these equations.

$$vt = \frac{(k \cdot TEMP)}{q}$$

$$eg = (2 \cdot 10^{4} \cdot (TEMP - 312)) + 1.4$$

$$vto = vto + (DELVTOmodel \cdot type) + (DELVTOelement \cdot type)$$

$$vbi = vto \qquad ratio = \frac{TEMP}{312}$$

If $VTIME \leq 1$, then $uo = uo \cdot (ratio^{TREF})$ and $kp = kp \cdot (ratio^{TREF})$

Note: TREF is an exponent in adjusting the temperature. It is not the reference temperature of this device model.

$$vfb = vto - (0.5 \cdot PHI) + (0.5 \cdot (1.4 - eg))$$

$$vbi = vfb + (0.5 + PHI \cdot ratio)$$

$vto = vbi$ (printback definition)

$phi = phi \cdot ratio$ (printback definition)

$vfb = vbi - phi$ (printback definition)

$vdsat = 0$

$beta = kp \cdot W \cdot L$

$vth = vbi + (ETA \cdot vds)$

If $NU \neq 0$ $K2 \neq 0$ $PSI \neq 0$ and $VTIME > 1$, then:

$vth = vth + f(vgs, vds, NU, K2, PSI, CHI, VTIME, TEMP)$

$von = vth$

If $NFS \neq 0$, then:

$$xn = 1 + \left(\frac{(q \cdot NFS \cdot 10^4 \cdot W \cdot L)}{Cfm}\right)$$

$von = f(vth, (vt \cdot xn))$

Cutoff Region (NFS = 0, vgs ≤ von)

If $NFS = 0$ and $vgs \leq von$, then:

$Cgdi = 0 \qquad Cgsi = 0$

$Ids = GO \cdot f(vgs, (DEFF \cdot vds))$

$gm = GO \qquad gds = GO \cdot DEFF$

Noncutoff Region (NFS ≠ 0)

- If $vgs > von$, then $vgsx = vgs$.
- If $vgs \leq von$, then $vgsx = von$.

Mobility modulation by vgs: $ueff = f(uo, \eta, vgs, THETA)$

If $VMAX > 0$, then:

$$vdsc = \frac{L \cdot VMAX}{ueff}$$

$$vdsat = (vgsx - vth) + vdsc - \sqrt{((vgsx - vth)^2 + vdsc^2)}$$

$$Cfmlw = \frac{(Cfm \cdot CSC)}{(Cfm + CSC)} \cdot L \cdot W$$

$Cfmlw$ is the series combination of the dielectric and space charge capacitance for the MIS structure.

If vds < vdsat, then:

$$vdsx = vds \qquad epsfm = Cfm \cdot \frac{(T2 + T1)}{\varepsilon 0}$$

$epsfm$ is the effective equivalent dielectric constant of the insulator layers.

$$fval = 0.8 + \left(\frac{epsfm - 0.8}{1 + (2 \cdot \pi \cdot FREQ \cdot TAU)^2}\right)$$

$$Cgdi = f(Cfmlw \cdot f(efm, 0.8) \cdot (\exp(fval, FEFF, vgs - vth - vds)))$$

$$Cgsi = f(Cfmlw \cdot f(efm, 0.8) \cdot (\exp(fval, FEFF, (vgs - vth), vds)))$$

Otherwise, vds ≥ vdsat:

$$vdsx = vdsat \qquad Cgdi = Cfmlw \qquad Cgsi = \frac{Cfmlw}{2}$$

If $vdsx \neq 0$, then $cdnorm = vdsx \cdot \left(vgsx - vth - \frac{vdsx}{2}\right)$.

Normalized drain current:

$$gm_{tft} = vdsx \qquad gds_{tft} = vgsx - vth - vdsx$$

$$cd1 = beta \cdot cdnorm$$

Drain current without velocity saturation effect:

$$beta = beta \cdot fgate \qquad idrain = beta \cdot cdnorm$$

$$gm_{tft} = (beta \cdot gm_{tft}) + (dfgdvg \cdot cd1)$$

Velocity saturation factor—if $VMAX \neq 0$, then:

$$fdrain = \frac{1}{\left(1 + \left(\frac{vdsx}{vdsc}\right)\right)}$$

$$dfddvg = -dfgdvg \cdot \frac{((fdrain^2) \cdot vdsx)}{(vdsc \cdot fgate)}$$

$$dfddvd = \frac{-(fdrain^2)}{vdsc}$$

Strong inversion current:

$$gm_{tft} = (fdrain \cdot gm_{tft}) + (dfddvg \cdot idrain)$$

$$gds_{tft} = (fdrain \cdot gds_{tft}) + (dfddvd \cdot idrain)$$

$$idrain = fdrain \cdot idrain \qquad beta = beta \cdot fdrain$$

$$Ids = idrain \cdot f(GO, vgs, DEFF, vds)$$

$$gm = f(gm_{tft}, GO)$$

$$gds = f(gds_{tft}, GO, DEFF)$$

Weak inversion current—if $vgs < von$, then:

$$idrain = idrain \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$Ids = idrain + f(GO, vgs, DEFF, vds)$$

$$gm_{tft} = \frac{idrain}{(vt \cdot xn)} \qquad gm = f(gm_{tft}, GO)$$

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = gds_{tft} + f(GO, DEFF)$$

$vdsx = 0$:

$$Ids = f(GO \cdot vgs, DEFF, vds)$$

$$gm = GO$$

$$gds_{tft} = beta \cdot (vgsx - vth)$$

If $NFS \neq 0$ and $vgs < von$, then:

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right) \qquad gds = f(gds_{tft}, GO, DEFF)$$

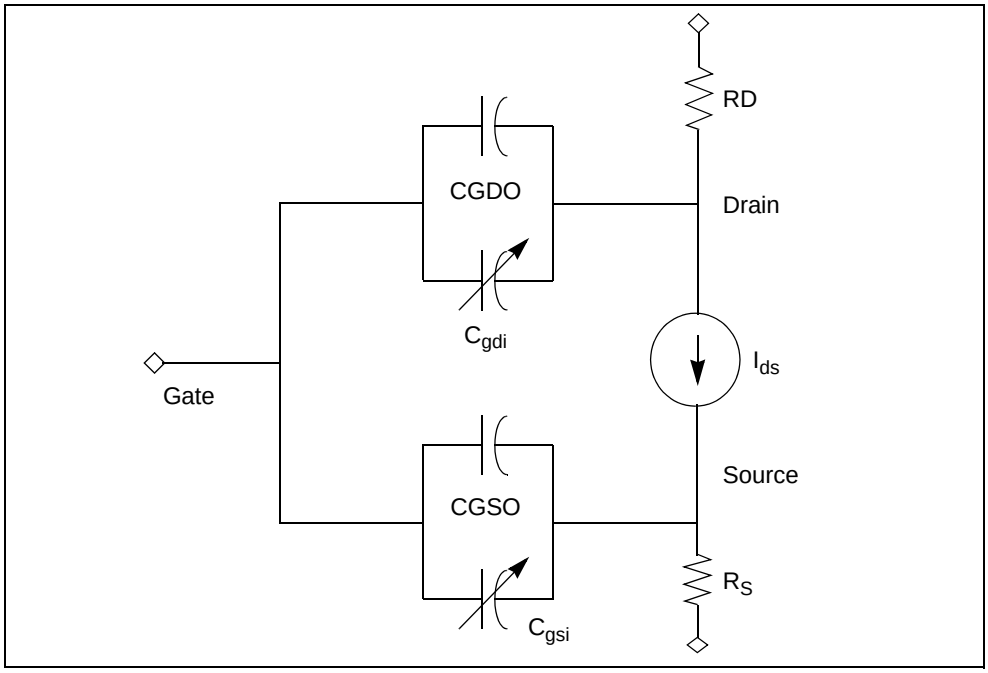
Cgd, Cgs

$$Cgd = Cgdi + CGDO \qquad Cgs = Cgsi + CGSO$$

LEVEL 40 Model Topology

Figure 34 shows the topology of the LEVEL 40 model.

Figure 34 LEVEL 40 HP a-Si TFT Topology



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5

Standard MOSFET Models: Levels 50 to 64

Lists and describes standard MOSFET models (Levels 50 to 64).

The MOSFET models described in this chapter are the most currently developed and widely used of the standard MOSFET models. Synopsys MOSFET device models have introduced Levels that are compatible with models developed by the University of Florida, Rensselaer Polytechnic Institute, and others.

This chapter describes the following standard MOSFET models (Levels 50 to 64):

- Level 50 Philips MOS9 Model
- Level 55 EPFL-EKV MOSFET Model
- Level 58 University of Florida SOI
- Level 61 RPI a-Si TFT Model
- Level 62 RPI Poli-Si TFT Model
- Level 63 Philips MOS11 Model
- Level 64: STARC HiSIM Model

For information about standard MOSFET Models Levels 1 to 40, see Chapter 4, Standard MOSFET Models: Level 1 to 40. For information on BSIM MOSFET models (based on models developed by the University of California at

Berkeley), see Chapter 6, BSIM MOSFET Models: Levels 13 to 39 and Chapter 7, BSIM MOSFET Models: Levels 47 to 65.

Level 50 Philips MOS9 Model

The Philips MOS Model 9, Level 902, is available as Level 50 in the Synopsys models (based on the “Unclassified Report NL-UR 003/94” by R.M.D.A. Velghe, D.B.M. Klaassen, and F.M. Klaassen).

MOSFET Level 50 incorporates all features of Philips MOS 9, except for the gate noise current. You can select one of two versions of MOSFET Level 50:

- ACM Parasitic Diode Model by using the JS, JSW, N, CJ, CJSW, CJGATE, MJ, MJSW, PB, PHP, ACM, and HDIF parameters. This version does not use the older IS parameter. To use this model, select the JUNCAP=0 (default) parameter.
- Philips JUNCAP Parasitic Diode Model. To use this version, select the JUNCAP=1 model parameter.

For additional information regarding the MOS Model-9, see:

http://www-us.semiconductors.com/Philips_Models

Table 45 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
LER	m	1.1e-6	1.25e-6	Reference Leff
WER	m	20.0e-6	20.0e-6	Reference Weff
LVAR	m	-220.0e-9	-460.0e-9	Variation in gate length
LAP	m	100.0e-9	25.0e-9	Lateral diffusion per side
WVAR	m	-25.0e-9	-130.0e-9	Variation in active width
WOT	m	0.0	0.0	Channel-stop diffusion per side
TR	°C	21.0	21.0	Reference temperature for model

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
VTOR	V	730.0e-3	1.1	Threshold voltage at zero bias
STVTO	V/K	-1.2e-3	-1.7e-3	Temperature dependence of VTO
SLVTO	Vm	-135.0e-9	35.0e-9	Length dependence of VTO
SL2VTO	Vm^2	0.0	0.0	Second length dependence of VTO
SWVTO	Vm	130.0e-9	50.0e-9	Width dependence of VTO
KOR	$V^{-1/2}$	650.0e-3	470.0e-3	Low-back-bias body factor
SLKO	$V^{-1/2}m$	-130.0e-9	-200.0e-9	Length dependence of KO
SWKO	$V^{-1/2}m$	2.0e-9	115.0e-9	Width dependence of KO
KR	$V^{-1/2}$	110.0e-3	470.0e-3	High-back-bias body factor
SLK	$V^{-1/2}m$	-280.0e-9	-200.0e-9	Length dependence of K
SWK	$V^{-1/2}m$	275.0e-9	115.0e-9	Width dependence of K
PHIBR	V	650.0e-3	650.0e-3	Strong inversion surface potential
VSBXR	V	660.0e-3	0.0	Transition voltage for dual-k-factor model
SLVSBX	Vm	0.0	0.0	Length dependence of *VSBX*
SWVSBX	Vm	-675.0e-9	0.0	Width dependence of *VSBX*
BETSQ	AV^{-2}	83.0e-6	26.1e-6	Gain factor of infinite square transistor
ETABET	-	1.6	1.6	Exponent of temperature dependence of gain factor

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
THE1R	V^{-1}	190.0e-3	190.0e-3	Gate-induced mobility reduction coefficient
STTHE1R	V^{-1}/K	0.0	0.0	Temperature dependence coefficient *THE1R*
SLTHE1R	$V^{-1}m$	140.0e-9	70.0e-9	Length dependence coefficient of *THE1R*
STLTHE1	$V^{-1}m/K$	0.0	0.0	Temperature dependence of the length dependence for *THE1R*
SWTHE1	$V^{-1}m$	-58.0e-9	-80.0e-9	Width dependence coefficient of *THE1R*
THE2R	$V^{-1/2}$	12.0e-3	165.0e-3	Back-bias induced mobility reduction coefficient
STTHE2R	$V^{-1/2}/K$	0.0	0.0	Temperature dependence coefficient*THE2R*
SLTHE2R	$V^{-1/2}m$	-33.0e-9	-75.0e-9	Length dependence coefficient of *THE2R*
STLTHE2	$V^{-1/2}$ m/K	0.0	0.0	Temperature dependence of the length dependence for *THE2R*
SWTHE2	$V^{-1/2}m$	30.0e-9	20.0e-9	Width dependence coefficient of *THE2R*
THE3R	V^{-1}	145.0e-3	27.0e-3	Lateral field induced mobility reduction coefficient
STTHE3R	V^{-1}/K	-660.0e-6	0.0	Temperature dependence coefficient of *THE3R*
SLTHE3R	$V^{-1}m$	185.0e-9	27.0e-9	Length dependence coefficient of *THE3R*

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
STLTHE3	$V^{-1}m/K$	-620.0e-12	0.0	Temperature dependence of the length dependence for *THE3R*
SWTHE3	$V^{-1}m$	20.0e-9	11.0e-9	Width dependence coefficient of *THE3R*
GAM1R	-	145.0e-3	77.0e-3	Drain-induced threshold shift coefficient for high gate drive
SLGAM1	-	160.0e-9	105.0e-9	Length dependence of *GAM1R*
SWGAM1	-	-10.0e-9	-11.0e-9	Width dependence of *GAM1R*
ETADSR	-	600.0e-3	600.0e-3	Exponent of drain dependence of *GAM1R*
ALPR	-	3.0e-3	44.0e-3	Channel length modulation factor
ETAALP	-	150.0e-3	170.0e-3	Exponent of length dependence of *ALPR*
SLALP	-	-5.65e-3	9.0e-3	Coefficient of length dependence of *ALPR*
SWALP	m	1.67e-9	180.0e-12	Coefficient of width dependence of *ALPR*
VPR	V	340.0e-3	235.0e-3	Characteristic voltage for channel length modulation
GAMOOR	-	18.0e-3	7.0e-3	Drain-induced threshold shift coefficient, at zero gate drive, and zero back-bias
SLGAMOO	m^2	20.0e-15	11.0e-15	Length dependence of *GAMOOR*

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
ETAGAMR	-	2.0	1.0	Exponent of back-bias dependence of zero gate-drive, drain-induced threshold shift
MOR	-	500.0e-3	375.0e-3	Subthreshold slope factor
STMO	K^{-1}	0.0	0.0	Temperature dependence coefficient *MOR*
SLMO	$m^{1/2}$	280.0e-6	47.0e-6	Length dependence coefficient of *MOR*
ETAMR	-	2.0	1.0	Exponent of back-bias dependence of the subthreshold slope
ZET1R	-	420.0e-3	1.3	Weak-inversion correction factor
ETAZET	-	170.0e-3	30.0e-3	Exponent of length dependence of *ZET1R*
SLZET1	-	-390.0e-3	-2.8	Length dependence coefficient of *ZET1R*
VSBTR	V	2.1	100.0	Limiting voltage for back-bias dependence
SLVSBT	Vm	-4.4e-6	0.0	Length dependence of *VSBTR*
A1R	-	6.0	10.0	Weak-avalanche current factor
STA1	K^{-1}	0.0	0.0	Temperature coefficient of *A1R*
SLA1	m	1.3e-6	-15.0e-6	Length dependence of *A1R*
SWA1	m	3.0e-6	30.0e-6	Width dependence of *A1R*

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
A2R	V	38.0	59.0	Exponent of weak-avalanche current
SLA2	Vm	1.0e-6	-8.0e-6	Length dependence of *A2R*
SWA2	Vm	2.0e-6	15.0e-6	Width dependence of *A2R*
A3R	-	650.0e-3	520.0e-3	Factor of minimum drain bias, above which avalanche sets in
SLA3	m	-550.0e-9	-450.0e-9	Length dependence of *A3R*
SWA3	m	0.0	-140.0e-9	Width dependence of *A3R*
TOX	m	25.0e-9	25.0e-9	Oxide thickness
COL	F/m	320.0e-12	320.0e-12	Gate overlap capacitance per unit width
WDOG	m	0	0	Characteristic drawn gate width, below which dogboning appears
FTHE1	-	0	0	Coefficient describing the width dependence of THE1 for W < WDOG
NFMOD		0		Flicker noise selector. 0 selects the old flicker noise model added in release 98.4
NTR	J	24.4e-21	21.1e-21	Thermal noise coefficient
NFR	V^2	70.0e-12	21.4e-12	Flicker noise coefficient
NFAR	$V^{-1}m^{-2}$	7.15e+22	1.53xe+22	1st flicker noise coefficient added in release 98.4
NFBR	$V^{-1}m^{-2}$	2.16e+06	4.06e+06	2nd flicker noise coefficient added in release 98.4

Table 45 MOSFET Level 50 Model Parameters (Continued)

Name	Unit	Default (N)	Default (P)	Description
NFCR	V^{-1}	0.0	2.92e-10	3rd flicker noise coefficient added in release 98.4
SL3VTO	V	0	0	Third coefficient of the length dependence of V_{TO}
SL2KO	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K_0
SL2K	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K
LP1	M	1E-6	1E-6	Characteristic length of the first profile
FBET1	-	0	0	Relative mobility decrease due to the first profile
LP2	M	1E-8	1E-8	Characteristic length of the second profile
FBET2	-	0	0	Relative mobility decrease due to the second profile
GTHE1	-	0	0	Parameter that selects either the old (=0) or the new (=1) scaling rule of θ_1
SL2GAMOO	-	0	0	Second coefficient of the γ_{00} length dependence

JUNCAP Model Parameters

The following are JUNCAP model parameters specifically for the Philips MOS 9 (Level 50) model.

Table 46 JUNCAP Model Parameters, MOSFET Level 50

Name	Unit	Default	Description
JUNCAP	-	0	JUNCAP flag: 0-off, 1-on.
DTA	^oC	0.0	Temperature offset of JUNCAP element relative to T_A.
VR	V	0.0	Voltage at which simulation determines the parameters.
JSGBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to electron-hole generation at $V=V_R$.
JSDBR	$A*m^{-2}$	1.00e-3	Bottom saturation-current density due to diffusion from back contact.
JSGSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to electron-hole generation at $V=V_R$.
JSDSR	$A*m^{-1}$	1.00e-3	Sidewall saturation-current density due to diffusion from back contact.
JSGGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to electron-hole generation at $V=V_R$
JSDGR	$A*m^{-1}$	1.00e-3	Gate edge saturation-current density due to diffusion from back contact.
NB	-	1.00	Emission coefficient of the bottom forward current.
NS	-	1.00	Emission coefficient of the sidewall forward current.
NG	-	1.00	Emission coefficient of the gate edge forward current.
CJBR	$F*m^{-2}$	1.00e-12	Bottom junction capacitance at $V=V_R$.

Table 46 JUNCAP Model Parameters, MOSFET Level 50 (Continued)

Name	Unit	Default	Description
CJSR	$F*m^{-1}$	1.00e-12	Sidewall junction capacitance at $V=V_R$.
CJGR	$F*m^{-1}$	1.00e-12	Gate edge junction capacitance at $V=V_R$.
VDBR	v	1.00	Diffusion voltage of the bottom junction at $T=T_R$.
VDSR	v	1.00	Diffusion voltage of the sidewall junction at $T=T_R$.
VDGR	v	1.00	Diffusion voltage of the gate edge junction at $T=T_R$.
PB	-	0.40	Bottom-junction grading coefficient.
PS	-	0.40	Sidewall-junction grading coefficient.
PG	-	0.40	Gate edge-junction grading coefficient.
TH3MOD	-	1	Switch that activates THE3-clipping: • If TH3MOD == 1 (default), effective THE3 can be slightly negative, and clipping does not occur. • If TH3MOD == 0, this model clips the effective THE3 to more than zero.

Using the Philips MOS9 Model

1. Set Level=50 to identify the model as the Philips MOS Model 9.
2. The default room temperature is 25 ^oC in Synopsys circuit simulators, but is 27 ^oC in most other simulators. When comparing to other simulators, set the simulation temperature to 27 use .**TEMP** 27 or **.OPTION** TNOM=27.
3. The model parameter set must include the TR model reference temperature, which corresponds to TREF in other model levels. The default for TR is 21.0^oC to match the Philips simulator.
4. This model has its own charge-based capacitance model. Level 50 ignores the CAPOP parameter, which selects different capacitance models.
5. This model uses analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.

6. DTEMP increases the temperature of individual elements relative to the circuit temperature. Set DTEMP on the element line.
7. Defaults are nonzero so use the **.MODEL** statement to set every model parameter listed in the Level 50 Model Parameters table.
8. Use the JUNCAP model parameter to select one of two available parasitic junction diode models, ACM or JUNCAP. JUNCAP=1 selects the Philips JUNCAP model, JUNCAP=0 (default) selects the ACM model.
9. Philips added a switch named TH3MOD to MOS Model 9. You can use this switch to re-activate effective THE3 clipping, which was removed in an earlier version of this model.
   - If TH3MOD == 1 (default), effective THE3 can be slightly negative, and clipping does not occur.
   - If TH3MOD == 0, this model clips the effective THE3 to more than zero.

Model Statement Example

```
.model nch nmos Level=50
+ ler  = 1e-6 wer = 10e-6
+ lvar  = 0.0 lap = 0.05e-6
+ wvar  = 0.0 wot = 0.0
+ tr  =  27.00 vtor = 0.8
+ stvto  = 0 slvto = 0
+ sl2vto  = 0 swvto = 0
+ kor  = 0.7 slko = 0
+ swko  = 0 kr = 0.3
+ slk  = 0 swk = 0
+ phibr  = 0.65 vsbxr = 0.5
+ slvsbx  = 0 swvsbx = 0
+ betsq  = 120e-6 etabet = 1.5
+ the1r  = 0.3 stthe1r = 0
+ slthe1r  = 0 stlthe1 = 0
+ swthe1  = 0 the2r = 0.06
+ stthe2r  = 0 slthe2r = 0
+ stlthe2  = 0 swthe2 = 0
+ the3r  = 0.1 stthe3r = 0
+ slthe3r  = 0 stlthe3 = 0
+ swthe3  = 0 gam1r = 0.02
+ slgam1  = 0 swgam1 = 0
+ etadsr  = 0.60 alpr = 0.01
+ etaalp  = 0 slalp = 0
```

```
+ swalp  = 0 vpr = 0.4
+ gamoor  = 0.006 slgamoo = 0
+ etagamr  = 2.0 mor = 0.5
+ stmo  = 0 slmo = 0
+ etamr  = 2.0 zet1r = 1.0
+ etazet  = 0.5 slzet1 = 0
+ vsbtr  = 2.5 slvsbt = 0
+ a1r  = 10 sta1 = 0
+ sla1  = 0 swa1 = 0
+ a2r  = 30 sla2 = 0
+ swa2  = 0 a3r = 0.8
+ sla3  = 0 swa3 = 0
+ tox  = 15.00e-9 col = 0.3e-9
+ ntr  = 2.0e-20 nfr = 5.0e-11
+ acm  = 2 hdif = 1u
+ js  = 1e-3 cj = 1e-3
+ mj  = 0.5 pb = 0.8
+ cjsw  = 1e-9 cjgate = 1e-9
+ mjsw  = 0.3 php = 0.8
```

Level 55 EPFL-EKV MOSFET Model

The EPFL-EKV MOSFET model is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

- The intrinsic part of the MOSFET includes the equations and parameters used to simulate the EPFL-EKV MOSFET model.
- The extrinsic part of the MOSFET model includes series resistances of the source and drain diffusions, junction currents, and capacitances.

Single Equation Model

The EPFL-EKV MOSFET model is a *single expression*, which preserves continuity of first-order and higher-order derivatives with respect to any terminal voltage in the entire range of validity of the model. This section describes the analytical expressions of first-order derivatives as transconductances and transcapacitances, you can use them in simulation.

Effects Modeled

The EPFL-EKV MOSFET model version 2.6 models the following physical effects:

- Basic geometrical and process-related aspects, such as oxide thickness, junction depth, and effective channel length and width.
- Effects of the doping profile.
- Substrate effect.
- Modeling of weak, moderate, and strong inversion behavior.
- Modeling of mobility effects due to vertical and lateral fields, and velocity saturation.
- Short-channel effects, such as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), and the reverse short channel effect (RSCE).
- Modeling of the substrate current due to impact ionization.
- Quasi-static charge-based dynamic model.
- Thermal and flicker noise modeling.
- Short-distance geometry-dependent and bias-dependent device matching.

Coherence of Static and Dynamic Models

Simulation derives all aspects of the static, the quasi-static, and the non-quasi-static (NQS) dynamic and noise models, from the normalized transconductance-to-current ratio. These expressions use symmetric normalized forward and reverse currents.

- For quasi-static dynamic operations, you can use a charge-based model for the node charges and trans-capacitances or a simpler capacitances model.
- The dynamic model, including the time constant for the NQS model, is described in symmetrical terms of the forward and reverse normalized currents.

The charge formulation also expresses the effective mobility dependence of a local field.

Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$V_G = V_{GB}$ Intrinsic gate-to-bulk voltage

$V_S = V_{SB}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB}$ Intrinsic drain-to-bulk voltage

V_S and V_D are the intrinsic source and drain voltages so the voltage drop over the extrinsic resistive elements must already be accounted for externally.

V_D is the electrical drain voltage, where $V_D \geq V_S$. Bulk reference handles the model symmetrically with respect to source and drain. This symmetry is inherent in common MOS technologies (excluding non-symmetric source-drain layouts).

Note: Intrinsic model equations are presented for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channel. That is, simulation reverses the polarity of the voltages (V_G, V_S, V_D, VFB, VTO, and TCV) before computing the P-channel current, which has a negative sign. No other distinctions are made between N-channel and P-channel, except the η factor for calculating the effective mobility.

Figure 35 Level 55 Equivalent Circuit

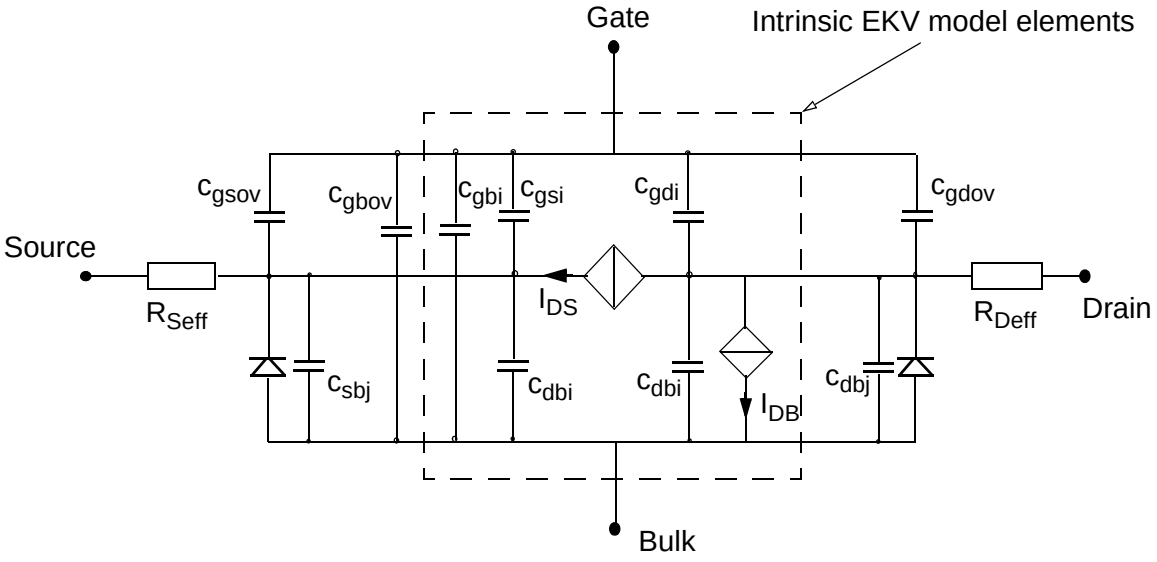


Figure 35 represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, this figure shows only the intrinsic capacitances from the simpler capacitances model. However, you can also use a charge-based transcapacitances model in simulation.

Table 47 Device Input Variables

Name	Unit	Default	Description
L	m	-	Channel length
W	m	-	Channel width
M or NP	-	1.0	Parallel multiple device number
N or NS	-	1.0	Series multiple device number

EKV Intrinsic Model Parameters

Name	Unit	Default	Range	Description
COX[a]	F/m^2	0.7E-3	-	Gate oxide capacitance per unit area
XJ	m	0.1E-6	$\geq$ 1.0E-9	Junction depth
DW[b]	m	0	-	Channel width correction
DL	m	0	-	Channel length correction

a. This model can calculate the default value of COX as a function of TOX.

b. DL and DW parameters are usually negative; see the effective length and width calculation.

Name	Unit	Default[a]	Range	Description
VTO[b]	V	0.5	-	Long-channel threshold voltage
GAMMA	$\sqrt{V}$	1.0	$\geq$ 0	Body effect parameter

Name	Unit	Default[a]	Range	Description
PHI	V	0.7	≥ 0.1	Bulk Fermi potential (*2)
KP	A/V^2	50.0E-6	-	Transconductance parameter
E0 (EO)	V/m	1.0E12	≥ 1E5	Mobility reduction coefficient
UCRIT	V/m	2.0E6	≥ 1E5	Longitudinal critical field

a. This model can calculate the default values of VTO, GAMMA, PHI, and KP as a function of TOX, NSUB, UO, and VFB for statistical circuit simulation.

b. As V_G, VTO also references the bulk.

Name	Unit[a]	Default	Range	Description
TOX[b]	m	-	≥ 0	Oxide thickness
NSUB[c]	cm^{-3}	-	≥ 0	Channel doping
VFB[d]	V	-	-	Flat-band voltage
UO[e]	$cm^2/$	-	≥ 0	Low-field mobility
VMAX[f]	m/s	-	≥ 0	Saturation velocity
THETA[g]	1/V	0	≥ 0	Mobility reduction coefficient

a. In this example, cm is the basic unit for NSUB and UO. TOX and VMAX are in m.

b. Optional parameter for calculating COX.

c. Optional parameter for the dependence of GAMMA on COX, and for calculating PHI.

d. Optional parameter for calculating VTO as a function of COX, GAMMA, or PHI.

e. Optional parameter for the dependence of KP on COX.

f. Optional parameter for calculating UCRIT.

g. Optional parameter for mobility reduction due to the vertical field.

The preceding parameters accommodate the scaling behavior of the process and basic intrinsic model parameters, and statistical circuit simulation. Simulation uses the TOX, NSUB, VFB, UO, and VMAX parameters only if you

did not specify COX, GAMMA, PHI, VTO, KP, or UCRIT. You can also use a simpler mobility reduction model, due to the vertical field. Simulation uses the THETA mobility reduction coefficient only if you did not specify E0.

Name	Unit	Default	Range	Description
LAMBDA	-	0.5	≥ 0	Depletion length coefficient (channel length modulation)
WETA	-	0.25	-	Narrow-channel effect coefficient
LETA	-	0.1	-	Short-channel effect coefficient

Name	Unit	Default	Range	Description
Q0 (QO)	$A \cdot s/m^2$	0	-	Reverse short channel effect peak charge density
LK	m	0.29E-6	≥ 1.0E-8	Reverse short channel effect characteristic length

Name	Unit	Default	Range	Description
IBA	1/m	0	-	First impact ionization coefficient
IBB	V/m	3.0E8	≥ 1.0E8	Second impact ionization coefficient
IBN	-	1.0	≥ 0.1	Saturation voltage factor for impact ionization

Name	Unit	Default	Description
TCV	V/K	1.0E-3	Threshold voltage temperature coefficient
BEX	-	-1.5	Mobility temperature exponent
UCEX	-	0.8	Longitudinal critical field temperature exponent
IBBT	1/K	9.0E-4	Temperature coefficient for IBB

Name	Unit	Default	Description
AVTO	Vm	0[a]	Area related threshold voltage mismatch parameter
AKP	m	0	Area related gain mismatch parameter
AGAMMA	$\sqrt{Vm}$	0	Area related body effect mismatch parameter

a. Only DEV values apply to the statistical matching parameters (AVTO, AGAMMA, AKP) for Monte-Carlo type simulations. Default is 1E-6 for all three parameters in some implementations to allow sensitivity analysis of the matching parameters. Do not specify LOT for AVTO, AGAMMA, or AKP.

Name	Unit	Default	Description
KF	-[a]	0	Flicker noise coefficient
AF	-	1	Flicker noise exponent

a. The unit for KF might depend on the flicker noise model that you select, if these options are available.

Name	Unit	Default	Description
NQS[a]	-	0	Non-Quasi-Static (NQS) operation switch
SATLIM[b]	-	exp(4)	Ratio defining the i_f/i_r saturation limit.
XQC[c]	-	0.4	Charge/capacitance model selector

a. NQS=1 switches Non-Quasi-Static operation on, default is off (the NQS model option might not be available in all implementations).

b. Only used for operating point information. (the SATLIM option might not be available in all implementations).

c. Selects either the charges/transcapacitances (default) or the capacitances-only model. XQC=0.4: charges/transcapacitances model; XQC=1: capacitances only model. (the XQC model option might not be available in all implementations).

Static Intrinsic Model Equations

Basic Definitions

$\varepsilon_{si} = SCALE \cdot 1.045 \times 10^{-12} [F/m]$ Permittivity of silicon

$\varepsilon_{ox} = SCALE \cdot 34.5 \times 10^{-12} [F/m]$ Permittivity of silicon dioxide

$q = 1.602 \times 10^{-19} [C]$ Magnitude of electron charge

$k = 1.3807 \times 10^{-23} [JK^{-1}]$ Boltzmann constant

$T_{ref} = 300.15 [K]$ Reference temperature

T_{nom} $[K]$ *Nominal* temperature of model parameters

T $[K]$ Model simulation temperature

$V_t(T) = \frac{k \cdot T}{q}$ Thermal voltage

$E_g(T) = \left(1.16 - 0.000702 \cdot \frac{T^2}{T + 1108}\right) [eV]$ Energy gap

$n_i(T) = 1.45 \times 10^{16} \cdot \left(\frac{T}{T_{ref}}\right) \cdot \exp\left(\frac{E_g(T_{ref})}{2 \cdot V_t(T_{ref})} - \frac{E_g(T)}{2 \cdot V_t(T)}\right) [m^{-3}]$ *I*ntrinsic carrier *concentration*

Parameter Preprocessing

Handling of Model Parameters for P-Channel MOSFETs

For P-channel devices, simulation reverses the sign of VFB, VTO, and TCV before processing. Therefore, VTO and TCV are usually positive and VFB is usually negative for N-channel, and vice versa for P-channel MOSFETs.

Initializing Intrinsic Parameters

The basic intrinsic model parameters are related to the fundamental process parameters as in early SPICE models:

COX→TOX
GAMMA and PHI →NSUB
VTO→VFB
KP→UO
UCRIT→VMAX

For statistical circuit simulation, you should introduce parameter variations on the level of the latter parameters. You can also use these dependencies to analyze device scaling and to obtain parameter sets from other MOSFET models. Therefore, you can use the following relations:

If you do not specify COX, simulation initializes it as:

$$COX = \begin{cases} \varepsilon_{ox}/TOX & \text{for: } TOX > 0 \\ default & otherwise \end{cases}$$

If you do not specify GAMMA, simulation initializes it as:

$$GAMMA = \begin{cases} \dfrac{\sqrt{2q\varepsilon_{si} \cdot (NSUB \cdot 10^6)}}{COX} & \text{for: } NSUB > 0 \\ default & otherwise \end{cases}$$

If you do not specify PHI, simulation initializes it as:

$$PHI = \begin{cases} 2V_t(T_{nom}) \cdot \ln\left(\dfrac{NSUB \cdot 10^6}{n_i(T_{nom})}\right) & \text{for: } NSUB > 0 \\ default & otherwise \end{cases}$$

If you do not specify VTO, simulation initializes it as:

$$VTO = \begin{cases} VFB + PHI + GAMMA \cdot \sqrt{PHI} & \text{if you specify VFB} \\ default & \text{otherwise} \end{cases}$$

If you do not specify DP, simulation initializes it as:

$$KP = \begin{cases} (UO \cdot 10^{-4}) \cdot COX & \text{for: } UO > 0 \\ default & otherwise \end{cases}$$

If you do not specify UCRIT, simulation initializes it as:

$$UCRIT = \begin{cases} VMAX/(UO \cdot 10^{-4}) & \text{for: } VMAX > 0, UO > 0 \\ default & otherwise \end{cases}$$

If you do not specify E0, simulation uses a simplified mobility model with the THETA parameter:

$$E0 = \begin{cases} 0 & \text{if you specify THETA} \\ default & otherwise \end{cases}$$

Note: The E0 value is zero, indicating to use the simplified mobility model is used in conjunction with THETA, instead of the standard mobility model.

Optional parameters might not be available in all implementations.

Default Values and Parameter Ranges

If you do not define a specific model parameters, simulation either initializes it according to the above relations, or sets it to its default value. Certain parameters restrict their numerical range to avoid numerical problems, such as divisions by zero. If you specify a parameter value outside the specified range (see the range column in the parameter tables), then simulation sets its value to the closest acceptable value.

Intrinsic Parameters Temperature Dependence

$$VTO(T) = VTO - TCV \cdot (T - T_{nom})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{nom}}\right)^{BEX} \qquad UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{nom}}\right)^{UCEX}$$

$$PHI(T) = PHI \cdot \frac{T}{T_{nom}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom}) \cdot \frac{T}{T_{nom}} + E_g(T)$$

$$IBB(T) = IBB \cdot [1.0 + IBBT \cdot (T - T_{nom})]$$

Bulk Referenced Intrinsic Voltages

Simulation refers all voltages to the local substrate (see Bulk Reference and Symmetry on page 226):

$V_G = V_{GB} = V_{GS} - V_{BS}$ Intrinsic gate-to-bulk voltage

$V_S = V_{SB} = -V_{BS}$ Intrinsic source-to-bulk voltage

$V_D = V_{DB} = V_{DS} - V_{BS}$ Intrinsic drain-to-bulk voltage

For P-channel devices, simulation inverts all signs before processing.

Effective Channel Length and Width

$$W_{eff} = W + DW \qquad L_{eff} = L + DL$$

Note: Unlike the convention in other MOSFET models, DL and DW usually permit a negative value due to the above definition.

Short Distance Matching

The inverse of the square root of the transistor area usually suitably describes a random mismatch between two transistors with an identical layout and close to each other. The following relationships have been adopted:

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}\right)$$

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

These model equations apply only in Monte-Carlo and sensitivity simulations. Because negative values for both KP_a and $GAMMA_a$ are not physically meaningful, simulation clips them at zero.

Reverse Short-channel Effect (RSCE)

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2 \qquad C_A = 0.028 \qquad \xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1\right)$$

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\varepsilon})\right]^2}$$

Effective Gate Voltage Including RSCE

$$V_G' = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a\sqrt{PHI}$$

Effective substrate factor including charge-sharing for short and narrow channels

Pinch-off voltage for narrow-channel effect:

$$V_{P0} = \begin{cases} V_G' - PHI - GAMMA_a\left(\sqrt{V_G' + \left(\frac{GAMMA_a}{2}\right)^2} - \frac{GAMMA_a}{2}\right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \le 0 \end{cases}$$

Effective substrate factor accounting for charge-sharing:

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}]$$

Note: This equation prevents a negative value in the square roots argument in the subsequent code.

$$\gamma° = GAMMA_a - \frac{\varepsilon_{si}}{COX} \cdot \left[\frac{LETA}{L_{eff}} \cdot (\sqrt{V'_S} + \sqrt{V'_D}) - \frac{3 \cdot WETA}{W_{eff}} \cdot \sqrt{V_{P0} + PHI}\right]$$

$$\gamma' = \frac{1}{2} \cdot (\gamma° + \sqrt{\gamma°^2 + 0.1 \cdot V_t})$$

Note: This equation prevents the effective substrate factor from becoming negative.

Pinch-off Voltage Including Short-Channel and Narrow-Channel Effects

$$V_P = \begin{cases} V_G' - PHI - \gamma' \cdot \left(\sqrt{V_G' + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2}\right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \le 0 \end{cases}$$

Note: The pinch-off voltage accounts for channel doping effects, such as the threshold voltage and the substrate effect.

For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it also becomes a function of the source and drain voltage due to the charge-sharing effect.

Slope Factor

$$n = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 4V_t}}$$

Note: The slope factor (or body effect factor) is primarily a function of the gate voltage, and links to the weak inversion slope.

Large Signal Interpolation Function

F(v) is the large-signal interpolation function, relating normalized currents to normalized voltages. A simple and accurate expression for the transconductance-to-current ratio consistently formulates:

- The static large-signal interpolation function.
- The dynamic model for the intrinsic charges (and capacitances).
- The intrinsic time constant and the thermal noise model for the whole range of current, from weak to strong inversion.

$$\frac{g_{ms} \cdot V_t}{I_{DS}} = \frac{1}{\sqrt{0.25 + i} + 0.5}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5 \qquad v = 2y + \ln(y)$$

You cannot analytically invert this equation. However, you can use a Newton-Raphson iterative scheme to invert this equation. Currently, this model uses a simplified algorithm that avoids iteration, leading to a continuous expression for the large signal interpolation function.

The (inverted) large signal interpolation function has the following asymptotes in strong and weak inversion:

$$F(v) = \begin{cases} (v/2)^2 & \text{for: } v >> 0 \\ \exp(v) & \text{for: } v << 0 \end{cases}$$

Forward Normalized Current

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

Velocity Saturation Voltage

$$V_C = UCRIT \cdot NS \cdot L_{eff}$$

Note: This equation accounts for the NS multiple series device number:

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2} \right]$$

Note: The V_{DSS} variable is half the value of the actual saturation voltage.

Drain-to-source Saturation Voltage for Reverse Normalized Current

$$V'_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right)} - \frac{1}{2} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t} \right) - 0.6 \right]$$

Channel-length Modulation

$$\Delta V = 4 \cdot V_t \cdot \sqrt{LAMBDA \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t} \right) + \frac{1}{64}} \qquad V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2} \qquad L_C = \sqrt{\frac{\varepsilon_{si}}{COX} \cdot XJ}$$

$$\Delta L = LAMBDA \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot UCRIT} \right)$$

Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation

$$L' = NS \cdot L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{UCRIT}$$

$$L_{min} = NS \cdot L_{eff} / 10$$

Note: These equations also account for the NS multiple series device number.

$$L_{eq} = \frac{1}{2} \cdot (L' + \sqrt{L'^2 + L_{min}^2})$$

Note: This equation prevents the equivalent channel length from becoming zero or negative.

Reverse Normalized Current

Reverse normalized current:

$$i_r' = F\left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}'^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS}')^2 + \Delta V^2}}{V_t}\right]$$

Reverse normalized current for the mobility model, intrinsic charges/ capacitances, the thermal noise model, and the NQS time-constant:

$$i_r = F\left[\frac{V_P - V_D}{V_t}\right]$$

Transconductance Factor and Mobility Reduction Due to Vertical Field

$$\beta_0 = KP_a \cdot \frac{NP \cdot W_{eff}}{L_{eq}}$$

Note: The NP (or M) device parameter returns accurate results for simulating parallel devices. Using NS (or N) for series devices is only approximate.

L_{eq} accounts for multiple NS series device numbers.

$$\eta = \begin{cases} 1/2 & for \quad NMOS \\ 1/3 & for \quad PMOS \end{cases}$$

$$q_{B0} = GAMMA_a \cdot \sqrt{PHI}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{COX}{E0 \cdot \varepsilon_{si}} \cdot q_{B0}\right)$$

$$\beta = \frac{\beta_0'}{1 + \frac{COX}{E0 \cdot \varepsilon_{si}} \cdot V_t \cdot |q_B + \eta \cdot q_I|}$$

For the definition of the q_B normalized depletion and the q_I inversion charges refer to the Normalized Intrinsic Node Charges: on page 241. Use β_0' to ensure that $\beta \approx \beta_0$ when $q_I << q_B$. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. You do not need to specify the substrate bias dependency, because the model includes the depletion charge.

Note: The resulting mobility expression also depends on V_{DS}.

Simple Mobility Reduction Model

For compatibility with the former EKV model versions (before v2.6), you can choose the simpler mobility reduction model, which uses the THETA parameter.

If you do *not* specify the E0 model parameter (see Parameter Preprocessing on page 231), simulation uses the simpler mobility model:

$$V_P' = \frac{1}{2} \cdot (V_P + \sqrt{V_P^2 + 2V_t^2})$$

$$\beta = \frac{\beta_0}{1 + THETA \cdot V_P'}$$

Specific Current

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

Drain-to-source Current

$$I_{DS} = I_S \cdot (i_f - i_r')$$

For P-channel devices, I_{DS} has a negative sign.

This drain current expression is a single equation, valid in all operating regions:

- weak, moderate and strong inversion
- non-saturation
- saturation

This current is therefore not only continuous among all of these regions, but also continuously derivable.

Transconductances

Simulation derives the transconductances from the drain current:

$$g_{mg} \equiv \frac{\partial I_{DS}}{\partial V_G} \qquad g_{ms} \equiv -\frac{\partial I_{DS}}{\partial V_S} \qquad g_{md} \equiv \frac{\partial I_{DS}}{\partial V_{DS}}$$

In the following relationships, the source for the derivatives is a reference:

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = g_{mg} \qquad g_{mbs} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = g_{ms} - g_{mg} - g_{md} \qquad g_{ds} \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = g_{md}$$

This model includes the analytic derivatives.

Impact Ionization Current

$$V_{ib} = V_D - V_S - IBN \cdot 2 \cdot V_{DSS}$$

$$I_{DB} = \begin{cases} I_{DS} \cdot \frac{IBA}{IBB} \cdot V_{ib} \cdot \exp\left(\frac{-IBB \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \le 0 \end{cases}$$

Note: The factor 2 in the v_{ib} expression accounts for the fact that the numerical value of V_{DSS} is half of the actual saturation voltage. The substrate current is a component of the total extrinsic drain current, flowing from the drain to the bulk. This model therefore expresses the total drain current as $I_D = I_{DS} + I_{DB}$.

The substrate current therefore also affects the total extrinsic conductances, especially the drain conductance.

Quasi-static Model Equations

MOSFET Level 55 includes both a charge-based model for transcapacitances, allowing charge-conservation during transient analysis, you can select a simpler capacitances-based model instead.

Note: The charges model is symmetrical in terms of the forward and reverse normalized currents—that is, the model is symmetrical for both the drain and source sides.

The pinch-off voltage in the dynamic model provides the short-channel effects (such as charge-sharing and reverse short-channel effects).

Dynamic Model for the Intrinsic Node Charges

$$n_q = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 10^{-6}}}$$

Normalized Intrinsic Node Charges:

$$x_f = \sqrt{\frac{1}{4} + i_f} \qquad x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2 x_f + 4x_r x_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2 x_r + 4x_f x_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^{\,2} + x_f x_r + x_r^{\,2}}{x_f + x_r} - 1 \right)$$

$$q_B = \begin{cases} (-GAMMA_a \cdot \sqrt{V_P + PHI + 10^{-6}}) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \le 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{ox} is a fixed oxide charge, which simulation assumes is zero. The preceding equations express the charge conservation among the four nodes of the transistor.

Total Charges:

$$C_{ox} = COX \cdot NP \cdot W_{eff} \cdot NS \cdot L_{eff}$$

$$Q_{(I,B,D,S,G)} = C_{ox} \cdot V_t \cdot q_{(I,B,D,S,G)}$$

Intrinsic Capacitances

Transcapacitances

Simulation derives the intrinsic capacitances from the node charges for the terminal voltages:

$$C_{xy} = \pm \frac{\partial}{\partial V_y}(Q_x) \qquad x, y = G, D, S, B$$

The preceding equation uses the positive sign if x=y or the negative sign otherwise. This equation produces simple, continuous analytical expressions for all transcapacitances in terms of the xf pinch-off voltage, the xr slope factor, and derivatives thereof, from weak to strong inversion, and from non-saturation to saturation.

Normalized Intrinsic Capacitances

Set XQC=1 to select a simplified capacitive dynamic model that uses the five intrinsic capacitances corresponding to the Level 55 Equivalent Circuit on page 226. This model ignores the slight bias dependence of the n slope factor. The result is the following simple set of functions:

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_f + x_r)^2}\right) \qquad c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_f + x_r)^2}\right)$$

$$c_{gb} = \left(\frac{n_q - 1}{n_q}\right) \cdot (1 - c_{gs} - c_{gd})$$

$$c_{sb} = (n_q - 1) \cdot c_{gs} \qquad c_{db} = (n_q - 1) \cdot c_{gd}$$

Total Intrinsic Capacitances

$$C_{(gs,\,gd,\,gb,\,sb,\,db)} = C_{ox} \cdot c_{(gs,\,gd,\,gb,\,sb,\,db)}$$

Intrinsic Noise Model Equations

The I_{NDS} current source models the noise between the intrinsic source and the drain. This noise includes a thermal noise component and a flicker noise component, and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$

Thermal Noise

The following equation calculates the PSD thermal noise component:

$$S_{thermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |q_I|$$

The preceding thermal noise expression is valid in all regions of operation, including for small V_{DS}.

Flicker Noise

The following equation calculates the PSD flicker noise component:

$$S_{flicker} = \frac{KF \cdot g_{mg}^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{AF}}$$

In some implementations, you can select different expressions.

Operating Point Information

At operating points, the following information displays to help in circuit design.

Numerical values of model internal variables

The following are the intrinsic charges and capacitances:

V_G, V_S, V_D, I_{DS}, I_{DB}, g_{mg}, g_{ms}, g_{mbs}, g_{md}, V_P, n, β, IS, if, ir', t, t0.

Transconductance efficiency factor

$$tef = g_{ms} \cdot V_t / I_{DS}$$

Early voltage

$$VM = I_{DS} / g_{md}$$

Overdrive voltage

$$n \cdot (V_P - V_S) \approx V_G - VTO_a - n \cdot V_S$$

For P-channel devices, $n \cdot (V_P - V_S)$ has a negative sign.

SPICE-like threshold voltage

$$VTH = VTO_a + \Delta V_{RSCE} + \gamma' \cdot \sqrt{V'_S} - GAMMA_a \cdot \sqrt{PHI}$$

This expression is the SPICE-like threshold voltage (the source). It also accounts for charge-sharing and reverse short-channel effects on the threshold voltage.

For P-channel devices, VTH has a negative sign.

Saturation voltage

$$VDSAT = 2V_{DSS} + 4V_t$$

For P-channel devices, VDSAT has a negative sign.

Saturation / non-saturation flag:

$$'SAT' \quad or \quad '1' \qquad for \quad \frac{i_f}{i_r} > SATLIM$$

$$'LIN' \quad or \quad '0' \qquad for \quad \frac{i_f}{i_r} \leq SATLIM$$

Note: Some simulators implement the operating point differently (some information might not be available).

Estimation and Limits of Static Intrinsic Model Parameters

If you do not have access to a parameter extraction facility, simulation can roughly estimate the EKV intrinsic model parameters from the SPICE level 2/3 parameters as indicated in Table 48. Pay attention to the units of the parameters. This estimation method generally returns reasonable results. Nevertheless, be aware that the underlying modeling in SPICE Level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore, it is preferred if parameter extraction is made directly from measurements.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits, nor to the range specified in the parameter tables. These limits may be helpful for obtaining physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

Table 48 Static Intrinsic Model Limits

Name	Unit	Default	Example	Lower	Upper	Estimation[a]
COX	F/m^2	0.7E-3	3.45E-3	-	-	$\varepsilon ox/TOX$
XJ	m	0.1E-6	0.15E-6	0.01E-6	1E-6	XJ
VTO	V	0.5	0.7	0	2	VTO
GAMMA	$\sqrt{V}$	1.0	0.7	0	2	$\sqrt{2q\varepsilon_{si} \cdot NSUB}/COX$
PHI[b]	V	0.7	0.5	0.3	2	$2V_t \cdot \ln(NSUB/n_i)$
KP	A/V^2	50E-6	150E-6	10E-6	-	$UO \cdot COX$
E0	V/m	1.0E12	200E6	$0.1/(0.4 \cdot TOX)$	-	$0.2/(THETA \cdot TOX)$
UCRIT	V/m	2.0E6	2.3E6	1.0E6	25E6	VMAX/UO
DL	m	0	-0.15*L_{min}	-0.5*L_{min}	0.5*L_{min}	$XL - 2 \cdot LD$
DW	m	0	-0.1*W_{min}	-0.5*W_{min}	0.5*W_{min}	$XW - 2 \cdot WD$
LAMBDA	-	0.5	0.8	0	3	-

Table 48 Static Intrinsic Model Limits (Continued)

Name	Unit	Default	Example	Lower	Upper	Estimation[a]
LETA	-	0.1	0.3	0	2	-
WETA	-	0.25	0.2	0	2	-
Q0	As/	0.0	230E-6	0	-	-
LK	m	0.29E-6	0.4E-6	0.05E-6	2E-6	-
IBA	1/m	0.0	2.0E8	0.0	5.0E8	$ALPHA \cdot VCR/L_C$
IBB	V/m	3.0E8	2.0E8	1.8E8	4.0E8	VCR/L_C
IBN	-	1.0	0.6	0.4	1.0	-

a. Also compare with optional process parameters.

b. The minimum value of PHI also determines the minimum value of the pinch-off voltage. Due to the intrinsic temperature dependence of PHI, higher temperatures use a lower value, which limits the range of simulation for small currents.

ε_{ox} =0.0345E-9 F/m q = 1.609E-19 C k = 1.381E-23 J/K $L_c = \sqrt{\varepsilon_{si} \cdot XJ/COX}$

ε_{si} = 0.104E-9 F/m n_i = 1.45E16 m^{-3} V_t = kT/q = 0.0259 V (at room temperature)

Note: Parameters in this table use m (meter) as the length unit. L_{min} is the minimum drawn length of transistors. W_{min} is the minimum drawn width of transistors. Example values are shown for enhancement N-channel devices.

Model Updates Description

Synopsys has made several improvements to the original EKV v2.6 MOSFET model. Wherever possible, these enhancements maintain backward compatibility with previous versions.

Revision I, September 1997

Description: The narrow channel effect on the substrate factor was revised to improve the transcapacitances behavior. The narrow channel effect is no longer a function of the v_s source voltage, but of the v_p pinch-off voltage.

Consequence: the WETA and DW narrow channel effect parameters require different numerical values to achieve the same effect.

Revision II, July 1998

Intrinsic time constant

Description: Simulation calculates the τ_0 intrinsic time constant as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the KP parameter.

Consequence: The NQS time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the NQS time constant at high V_G, and additional dependence on short-channel effects.

Thermal noise

Description: Simulation calculates the $S_{thermal}$ thermal noise power spectral density as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the KP parameter.

Consequence: $S_{thermal}$ has an additional gate voltage and short-channel effect dependence.

Optional process parameters to calculate electrical intrinsic parameters

Description: This option calculates the electrical parameters as a function of the optional parameters:

COX and GAMMA→TOX
PHI→NSUB
VTO→VFB
KP→UO
UCRIT→VMAX

cm is the length unit for the NSUB and UO parameters.

Consequence: These parameters accommodate scaling behavior and allow meaningful statistical circuit simulation, due to decorrelation of physical effects. If you use these optional parameters, this version is compatible with former revisions, except for the default calculation of the parameters.

Optional simplified mobility model

Description: The simple mobility model used in former model versions by using the THETA parameter, was reinstated as an option.

Consequence: This mobility model simplifies adaptation from earlier model versions to the current version.

Parameter synonyms

Description: You can use E0 and Q0 as synonyms for the EO and QO parameters.

Consequence: This option accommodates some simulators that use only alphabetic characters.

Operating point information

Description: This enhancement models the analytical expression for the SPICE-like VTH threshold voltage in the operating point information to include the charge-sharing and reverse short-channel effects. This option modifies the analytical expression for the VDSAT saturation voltage in the operating point information so it has a non-zero value in weak inversion.

Consequence: This enhancement improves design information.

Corrections from EPFL R11, March, 1999

Equation 45, Equation 53, Equation 54, and Equation 58 were corrected for multiple series device behavior by using the NS parameter.

Corrections from EPFL R12, July 30, 1999

EPFL released the following corrections.

Correction 1- 99/07/30 mb (r12) corrected dGAMMAprime_dVG (narrow channel). An error in the analytical model derivatives of the GAMMAprime variable affected the transconductances and transcapacitances.

Correction 2- 99/07/30 mb (r12) prevents PHI from being smaller than 0.2, both at init and after updating the temperature. For some CMOS technologies, PHI parameter values are as low as 400mV, required to account for particular process details. If you increase the temperature from room temperature, PHI decreases due to its built-in temperature dependence. As a result, PHI attains very low values or even becomes negative when it reaches 100degC. For the model to function at these temperatures, PHI has a lower limit of 200mV. The usual range for this parameter is well above this value (600mV to 1V).

Correction 3- 99/06/28 mb (r12) fixed COX/KP initialization (rg).

Correction 4- 99/05/04 mb (r12) completed parameter initialization for XQC, DL, and DW, and removed IBC and ibc (cd).

Level 58 University of Florida SOI

UFSOI includes non-fully depleted (NFD) and fully depleted (FD) SOI models (a dynamic mode must not operate between NFD and FD) that separately describe two main types of SOI devices. The UFSOI version 4.5F model is Level 58 in the Synopsys MOSFET models. This model is described in the *UFSOI Model User's Manual* at:

http://www.soi.tec.ufl.edu/

Some processes use an external contact to the body of the device. The Synopsys MOSFET model supports only a 4-terminal device, which includes drain, front gate, source, and back gate (or substrate). The additional body contact is currently not supported so it floats.

The effects of parasitic diodes in SOI are different from those in the bulk MOSFET. The SOI model does not include the MOSFET *junction* model (ACM), developed for bulk MOSFETs.

The general syntax for MOSFET Level 58 in a netlist is:

```
Mxxx nd ngf ns <ngb> mname <L=val> <W=val> <M=val>
+ <AD=val> <AS=val> <PD=val> <PS=val> <NRD=val>
+ <NRS=val> <NRB=val> <RTH=val> <CTH=val> <off>
+ <IC=Vds,Vgfs,VGbs>
```

In the preceding syntax, angle brackets denote optional parameters. The arguments are identical to those for the BSIM3-SOI model, but the thermal resistance and capacitance have different names.

Table 49 Thermal Resistance and Capacitance Names

Name	Description
RTH	Thermal resistance, unit in $K \cdot W^{-1}$, default is 0.0.
CTH	Thermal capacitance, unit in $W \cdot s \cdot K^{-1}$, default is 0.0.

Notes:

- The default value for channel length (L) and width (W) is 1.0e-6.
- The present version supports only 4 nodes (only floating-body devices). AB is typically zero; specify it accordingly.
- If you activate the self-heating option (on the model line), RTH and CTH define the thermal impedance of the device. Typical values are 5e3 (for RTH) and 1e-12 (for CTH), but these can vary widely from one device to another.
- For M > 1, you must specify W, AD, AS, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH per gate finger.
- The initial condition (IC) is in the following order: Vds drain voltage, Vgfs front gate voltage, and Vbgs back gate voltage.

Level 58 FD/SOI MOSFET Model Parameters

The following tables describe Level 58 model parameters for the fully depleted (FD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 50 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	0	Model selector (0: FD)
BJT	-	1	1	Parasitic bipolar flag (0: off; 1: on)
SELFT	-	0	0	Self-heating flag: • 0: no self-heating • 1: approximate model • 2: full self-heating

Table 50 MOSFET Level 58 Flag Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
TPG	-	1	-	Type of gate polysilicon: • +1: opposite to body • -1: same as body
TPS	-	-1	-	Type of substrate: • +1: opposite to body • -1: same as body

Table 51 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	$(3\text{-}8)\text{x}10^{-9}$	Front-gate oxide thickness
TOXB	m	0.5e-6	$(80\text{-}400)\text{x}10^{-9}$	Back-gate oxide thickness
NSUB	cm^{-3}	1.0e15	$10^{15}\text{-}10^{17}$	Substrate doping density
NGATE	cm^{-3}	0.0	$10^{19}\text{-}10^{20}$	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm^{-3}	5.0e19	$10^{19}\text{-}10^{20}$	Source/drain doping density
TB	m	0.1e-6	$(30\text{-}100)\text{x}10^{-9}$	Film (body) thickness
NBODY	cm^{-3}	5.0e16	$10^{17}\text{-}10^{18}$	Film (body) doping density
LLDD	m	0.0	$(0.05\text{-}0.2)\text{x}10^{-6}$	LDD/LDS region length (0 for no LDD)
NLDD	cm^{-3}	5.0e19	$1\text{x}10^{19}$	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	$(0.05\text{-}0.15)\text{x}10^{-6}$	Channel-length reduction
DW	m	0.0	$(0.1\text{-}0.5)\text{x}10^{-6}$	Channel-width reduction

Table 52 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm^{-2}	0.0	~ 10^{10}	Front oxide fixed charge (normalized)
NQFB	cm^{-2}	0.0	~ 10^{11}	Back oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	~ ± 10^{12}	Effective sidewall fixed charge (0 for no narrow-width effect)
NSF	$cm^{-2}{\cdot}eV^{-1}$	0.0	~10^{10}	Front surface state density
NSB	$cm^{-2}{\cdot}eV^{-1}$	0.0	~ 10^{11}	Back surface state density
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
UO	$cm^{2}{\cdot}V^{-1}{\cdot}s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
THETA	$cm{\cdot}V^{-1}$	7.0e2	(0.1-3)x10^{-6}	Mobility degradation coefficient
VSAT	$cm{\cdot}s^{-1}$	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity
ALPHA	cm^{-1}	0.0	2.45x10^{6}	Impact-ionization coefficient (0 for no impact ionization)
BETA	$V{\cdot}cm^{-1}$	0.0	1.92x10^{6}	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	$V{\cdot}cm^{-1}$	0.0	(4-8)x10^{9}	Exponential factor for gate-induced drain leakage (0 for no GIDL)
GAMMA	-	0.3	0.3-1.0	BOX fringing field weighting factor

Table 52 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
KAPPA	-	0.5	0.5-1.0	BOX fringing field weighting factor
JRO	$A \cdot m^{-1}$	1.0e-10	10^{-11}-10^{-9}	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	$(0.1\text{-}0.5)x10^{-6}$	Effective diffusion length in source/drain
SEFF	$cm \cdot s^{-1}$	1.0e5	$(0.5\text{-}5)x10^{5}$	Effective recombination velocity in source/drain
CGFDO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-drain overlap capacitance
CGFSO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-source overlap capacitance
CGFBO	$F \cdot m^{-1}$	0.0	0.0	Gate-body overlap capacitance
RD	ohm·m	0.0	200-1000	Specific drain parasitic resistance
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance
RHOB	ohm/sq.	0.0	$30x10^{3}$	Body sheet resistance
FNK	F·A	0.0	$0\text{-}10^{-2}$	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Table 53 MOSFET Level 58 Optional Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	10^{-7}-10^{-5}	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V_{DS} averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance

Level 58 NFD/SOI MOSFET Model Parameters

The following tables describe the Level 58 model parameters for non fully depleted (NFD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 54 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	-	Model selector (1: NFD)
BJT	-	1	1	Parasitic bipolar flag: • 0: off • 1: on

Table 54 MOSFET Level 58 Flag Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
SELFT	-	0	0	Self-heating flag: • 0: no self-heating • 1: approximate model • 2: full self-heating
TPG	-	1	1	Type of gate polysilicon • +1: opposite to body • -1: same as body
TPS	-	-1	-1	Type of substrate • +1: opposite to body • -1: same as body)

Table 55 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	$(3\text{-}8)\text{x}10^{-9}$	Front-gate oxide thickness
TOXB	m	0.5e-6	$(80\text{-}400)\text{x}10^{-9}$	Back-gate oxide thickness
NSUB	cm^{-3}	1.0e15	$10^{15}\text{-}10^{17}$	Substrate doping density
NGATE	cm^{-3}	0.0	$10^{19}\text{-}10^{20}$	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm^{-3}	5.0e19	$10^{19}\text{-}10^{20}$	Source/drain doping density
TF	m	0.2e-6	$(3\text{-}8)\text{x}10^{-9}$	Silicon film thickness
TB	m	0.1e-6	$(30\text{-}100)\text{x}10^{-9}$	Film (body) thickness
THALO	m	0.0	-	Halo thickness (0 for no halo)
NBL	cm^{-3}	5.0e16	$10^{17}\text{-}10^{18}$	Low body doping density
NBH	cm^{-3}	5.0e17	$10^{19}\text{-}10^{20}$	Halo doping density

Table 55 MOSFET Level 58 Structural Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
NHALO	cm^{-3}	-	$\sim 10^{18}$	Halo doping density
LRSCE	m	0.0	$\sim 0.1 \times 10^{-6}$	Characteristic length for reverse short-channel effect (0 for no RSCE)
LLDD	m	0.0	$(0.05\text{-}0.2) \times 10^{-6}$	LDD/LDS region length (0 for no LDD)
NLDD	cm^{-3}	5.0e19	1×10^{19}	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	$(0.05\text{-}0.15) \times 10^{-6}$	Channel-length reduction
DW	m	0.0	$(0.1\text{-}0.5) \times 10^{-6}$	Channel-width reduction

Table 56 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm^{-2}	0.0	$\sim 10^{10}$	Front oxide fixed charge (normalized)
NQFB	cm^{-2}	0.0	$\sim 10^{11}$	Back oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	$\sim \pm\ 10^{12}$	Effective sidewall fixed charge (0 for no narrow-width effect)
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
UO	$cm^2 \cdot V^{-1} \cdot s^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility

Table 56 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
THETA	$cm \cdot V^{-1}$	7.0e2	$(0.1\text{-}3)x10^{-6}$	Mobility degradation coefficient
VSAT	$cm \cdot s^{-1}$	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity
ALPHA	cm^{-1}	0.0	$2.45x10^{6}$	Impact-ionization coefficient (0 for no impact ionization)
BETA	$V \cdot cm^{-1}$	0.0	$1.92x10^{6}$	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	$V \cdot cm^{-1}$	0.0	$(4\text{-}8)x10^{9}$	Exponential factor for gate-induced drain leakage (0 for no GIDL)
NTR	cm^{-3}	0.0	10^{14}-10^{15}	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)
JRO	$A \cdot m^{-1}$	1.0e-10	10^{-11}-10^{-9}	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	$(0.1\text{-}0.5)x10^{-6}$	Effective diffusion length in source/drain
SEFF	$cm \cdot s^{-1}$	1.0e5	$(0.5\text{-}5)x10^{5}$	Effective recombination velocity in source/drain
CGFDO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-drain overlap capacitance

Table 56 MOSFET Level 58 Electrical Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
CGFSO	$F \cdot m^{-1}$	0.0	$1x10^{-10}$	Gate-source overlap capacitance
CGFBO	$F \cdot m^{-1}$	0.0	0.0	Gate-body overlap capacitance
RD	ohm·m	0.0	200-1000	Specific drain parasitic resistance
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance
RHOB	ohm/sq.	0.0	$30x10^{3}$	Body sheet resistance
FNK	F·A	0.0	$0\text{-}10^{-2}$	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Table 57 Optional MOSFET Level 58 Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	$10^{-7}\text{-}10^{-5}$	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V_{DS}-averaging factor for mobility degradation

Table 57 Optional MOSFET Level 58 Parameters (Continued)

Parameter	Unit	Default	Typical Value	Description
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance

Notes:

- The model line must include Level=58 and NFDMOD=0 for FD, or NFDMOD=1 for NFD devices.
- Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative) and the reverse short-channel effect defined by LRSCE (and NBH or NHALO if specified); the latter effect is also turned off if you specify WKF.
- For floating-body devices, CGFBO is small; you should set it to 0.
- JRO and SEFF influence the gain of the BJT, but LDIFF affects only bipolar charge storage in the source/drain. If you specify THALO, then NBH and NHALO also influence the BJT gain.
- Loosely correlate the TAUO value with JRO in accord with basic pn-junction recombination/generation properties. Its default value is based on JRO, which is appropriate for short L; for long L, body generation predominates over that in the junctions so specify TAUO.
- The non-local impact-ionization model is physical so do not arbitrarily vary its parameters.
- The LDD option intensifies the model so set LLDD to 0 for large-scale circuit simulation, and add the unbiased LDD resistance to RD; this simplification stops if you specify NLDD > 1e19.

Level 58 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 14.

Level 61 RPI a-Si TFT Model

Level 61 in the Synopsys MOSFET models is an AIM-SPICE MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.

Model Features

Features of the AIM-SPICE MOS15 a-Si TFT model include:

- Modified charge control model; induced charge trapped in localized states
- Above threshold includes:
  - Field effect mobility becoming a function of gate bias
  - Band mobility dominated by lattice scattering
- Below threshold includes:
  - Fermi level located in deep localized states
  - Relate position of Fermi level, including the deep DOS, back to the gate bias
- Empirical expression for current at large negative gate biases for hole-induced leakage current
- Applies interpolation techniques to equations to unify the model

Using Level 61 with Synopsys Simulators

To simulate using the AIM-SPICE MOS15 a-Si TFT model:

1. Set Level=61 to identify the model as the AIM-SPCIE MOS15 a-Si TFT model.
2. The default value for L is 100µm, and the default value for W is 100µm.
3. Level 61 is a 3-terminal model. This model does not include a bulk node; therefore simulation does not append parasitic drain-bulk or source-build diodes are appended to the model. You can specify a fourth node, but it does not affect simulation results.

4. The default room temperature is 25 ^{o}C in Synopsys circuit simulators, but is 27 ^{o}C in most other simulators. When comparing to other simulators, use **.TEMP** 27 or **.OPTION TNOM**=27 to set the simulation temperature to 27 in the netlist.

Example

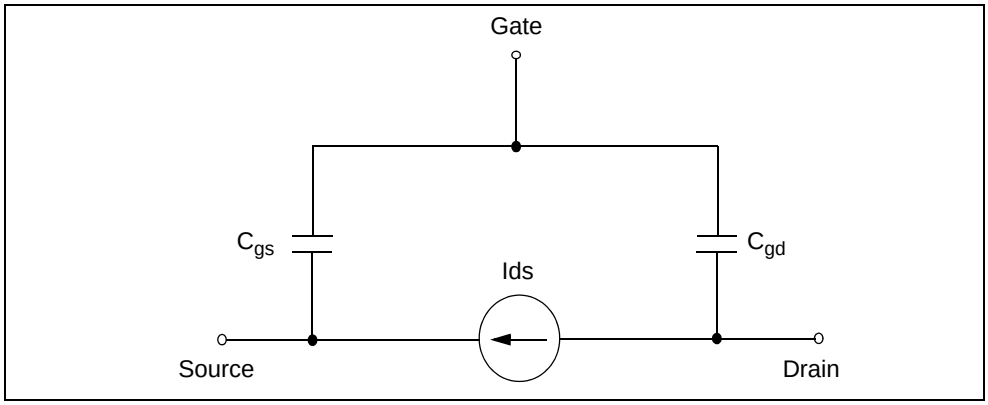
The following is an example of how Level 61 modifies the Synopsys MOSFET model and element statement.

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=61
+ alphasat = 0.6 cgdo = 0.0 cgso = 0.0 def0 = 0.6
+ delta = 5.0 el = 0.35 emu = 0.06 eps = 11
+ epsi = 7.4 gamma = 0.4 gmin = 1e23 iol = 3e-14
+ kasat = 0.006 kvt = -0.036 lambda = 0.0008 m = 2.5
+ muband = 0.001 rd = 0.0 rs = 0.0 sima0 = 1e-14
+ tnom = 27 tox = 1.0e-7 v0 = 0.12 vaa = 7.5e3
+ vdsl = 7 vfb = -3 vgsl = 7 vmin = 0.3 vto = 0.0
```

Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	F/m	0.0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0.0	Gate-source overlap capacitance per meter channel width
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	Activation energy of the hole leakage current
EMU	eV	0.06	Field effect mobility activation energy
EPS	-	11	Relative dielectric constant of the substrate
EPSI	-	7.4	Relative dielectric constant of the gate insulator
GAMMA	-	0.4	Power law mobility parameter

Name	Unit	Default	Description
GMIN	$m^{-3}eV^{-1}$	1E23	Minimum density of deep states
IOL	A	3E-14	Zero-bias leakage current parameter
KASAT	1/°X	0.006	Temperature coefficient of ALPHASAT
KVT	V/°X	-0.036	Threshold voltage temperature coefficient
LAMBDA	1/V	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	m^2/Vs	0.001	Conduction band mobility
RD	m	0.0	Drain resistance
RS	m	0.0	Source resistance
SIGMA0	A	1E-14	Minimum leakage current parameter
TNOM	^oC	25	Parameter measurement temperature
TOX	m	1E-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.5E3	Characteristic voltage for field effect mobility
VDSL	V	7	Hole leakage current drain voltage parameter
VFB	V	-3	Flat band voltage
VGSL	V	7	Hole leakage current gate voltage parameter
VMIN	V	0.3	Convergence parameter
VTO	V	0.0	Zero-bias threshold voltage

Equivalent Circuit



Model Equations

Drain Current

$$I_{ds} = I_{leakage} + I_{ab} \qquad I_{ab} = g_{ch} V_{dse}(1 + LAMBDA \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{[1 + (V_{ds}/V_{sate})^{M}]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)} \qquad g_{chi} = qn_s W \cdot MUBAND/L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}\left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA}$$

$$n_{sb} = n_{so}\left(\frac{t_m}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2\cdot V0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V0}\exp\left(-\frac{DEF0}{V_{th}}\right) \qquad N_c = 3.0\cdot 10^{25} m^{-3}$$

$$V_e = \frac{2\cdot V0\cdot V_{tho}}{2\cdot V0 - V_{th}} \qquad t_m = \sqrt{\frac{EPS}{2q\cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2}\left[1+\frac{V_{gt}}{VMIN}+\sqrt{DELTA^2+\left(\frac{V_{gt}}{VMIN}-1\right)^2}\right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2}\left[1+\frac{V_{gfb}}{VMIN}+\sqrt{DELTA^2+\left(\frac{V_{gfb}}{VMIN}-1\right)^2}\right]$$

$$V_{gfb} = V_{gs} - VFB \qquad I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL\left[\exp\left(\frac{V_{ds}}{VDSL}\right)-1\right]\exp\left(-\frac{V_{gs}}{VGSL}\right)\exp\left[\frac{EL}{q}\left(\frac{1}{V_{tho}}-\frac{1}{V_{th}}\right)\right]$$

$$I_{min} = SIGMA0\cdot V_{ds}$$

Temperature Dependence

$$V_{tho} = k_B\cdot TNOM/q \qquad V_{th} = k_B\cdot(TEMP)/q$$

$$V_{aat} = VAA\exp\left[\frac{EMU}{q\cdot GAMMA}\left(\frac{1}{V_{th}}-\frac{1}{V_{tho}}\right)\right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

$$C_{gs} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3}C_{gc}\left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}}\right)^2\right]$$

$$C_f = 0.5 \cdot EPS \cdot W \qquad C_{gs} = q\frac{dn_{sc}}{dV_{gs}}$$

$$n_{sc} = \frac{n_{sac}n_{sbc}}{n_{sac} + n_{sbc}} \qquad n_{sac} = \frac{EPSI \cdot V_{gte}}{q \cdot TOX}$$

$$n_{sbc} = n_{sb}$$

Level 62 RPI Poli-Si TFT Model

Level 62 is an AIM-SPICE MOS16 poly-silicon (Poli-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.

Model Features

Features of the AIM-SPICE MOS16 Poli-Si TFT model include:

- A design based on the crystalline MOSFET model
- Field effect mobility that becomes a function of the gate bias
- Effective mobility that accounts for trap states:
  - For low V_{gs}, it is the power law
  - For high V_{gs}, it is the constant
- Reverse bias drain current function of the electric field near the drain and the temperature
- A design independent of the channel length

- A unified DC model that includes all four regimes for channel lengths down to 4 µm:
  - Leakage (thermionic emission)
  - Subthreshold (diffusion-like model)
  - Above threshold (c-Si-like with mFet)
  - Kink (impact ionization with feedback)
- An AC model accurately reproduces the C_{gc} frequency dispersion
- Automatic scaling of model parameters that accurately model a wide range of device geometries

Using Level 62 with Synopsys Simulators

To simulate using the AIM-SPICE MOS16 Poli-Si TFT model:

1. Set `Level=62` to identify the model as the AIM-SPICE MOS16 Poli-Si TFT model.
2. The default value for `L` is 100µm, and the default value for `W` is 100µm.
3. Level 62 is a 3-terminal model. This model does not include a bulk node; therefore, simulation does not append a parasitic drain-bulk or source-bulk diode to the model. You can specify a fourth node, but it does not affect the simulation results.
4. The default room temperature is 25 ^{o}C in Synopsys circuit simulators, but is 27 ^{o}C in most other simulators. When comparing to other simulators, use `.TEMP 27` or .OPTION `TNOM=27` to set the simulation temperature to 27 ^{o}C in the netlist.

The following is an example of how Level 62 modifies a MOSFET device model and element statement:

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=62
+ asat = 1 at = 3e-8 blk = 0.001 bt = 0.0 cgdo = 0.0
+ cgso = 0.0 dasat = 0.0 dd = 1.4e-7 delta = 4.0
+ dg = 2.0e-7 dmu1 = 0.0 dvt = 0.0 dvto = 0.0 eb = 0.68
+ eta = 7 etac0 = 7 etac00 = 0 i0 = 6.0 i00 = 150
+ lasat = 0lkink = 19e-6 mc = 3.0 mk = 1.3 mmu = 3.0
+ mu0 = 100 mu1 = 0.0022 mus = 1.0 rd = 0.0 rdx = 0.0
+ rs = 0.0 rsx = 0.0 tnom = 27 tox = 1.0e=7 vfb = -0.1
+ vkink = 9.1 von = 0.0 vto = 0.0
```

Table 58 MOSFET Level 62 Model Parameters

Name	Unit	Default	Description
ASAT	-	1	Proportionality constant of Vsat
AT	m/V	3E-8	DIBL parameter 1
BLK	-	0.001	Leakage barrier lowering constant
BT	m·V	1.9E-6	DIBL parameter 2
CAPMOD	-	0	Model capacitance selector (zero recommended)
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
DASAT	1/°C	0	Temperature coefficient of ASAT
DD	m	1400 Å	Vds field constant
DELTA	-	4.0	Transition width parameter
DG	m	2000 Å	Vgs field constant
DMU1	$\chi\mu^2/\varsigma\sigma\times X$	0	Temperature coefficient of MU1
DVT	V	0	The difference between VON and the threshold voltage
DVTO	V/°C	0	Temperature coefficient of VTO
EB	EV	0.68	Barrier height of the diode
ETA	-	7	Subthreshold ideality factor
ETAC0	-	ETA	Capacitance subthreshold ideality factor at zero-drain bias

Table 58 MOSFET Level 62 Model Parameters (Continued)

Name	Unit	Default	Description
ETAC00	1/V	0	Capacitance subthreshold coefficient of the drain bias
I0	A/m	6.0	Leakage scaling constant
I00	A/m	150	Reverse diode saturation current
KSS	-	0	Small signal parameter (zero is recommended)
LASAT	M	0	Coefficient for length dependence of ASAT
LKINK	M	19E-6	Kink effect constant
MC	-	3.0	Capacitance knee shape parameter
MK	-	1.3	Kink effect exponent
MMU	-	3.0	Low field mobility exponent
MU0	cm^2/Vs	100	High field mobility
MU1	cm^2/Vs	0.0022	Low field mobility parameter
MUS	cm^2/Vs	1.0	Subthreshold mobility
RD	µ	0	Drain resistance
RDX	Ω	0	Resistance in series with C_{gd}
RS	µ	0	Source resistance
RSX	Ω	0	Resistance in series with C_{gs}
TNOM	°C	25	Parameter measurement temperature
TOX	m	1e-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VFB	V	-0.1	Flat band voltage

Table 58 MOSFET Level 62 Model Parameters (Continued)

Name	Unit	Default	Description
VKINK	V	9.1	Kink effect voltage
VON	V	0	On-voltage
VSI	V	2.0	vgs dependence parameter
VST	V	2.0	vgs dependence parameter
VTO	V	0	Zero-bias threshold voltage
ZEROC	-	0	Flag for capacitance calculations in capmod=1 • capmod=1: set the 0 capacitance value • capmod=0: calculation capacitance
XL	m	0	Length bias accounts for the masking and etching effects
XW	m	0	Width bias accounts for the masking and etching effects
LMLT	-	1	Length shrink factor
WMLT	-	1	Width shrink factor

Table 59 Model Parameters Specific to Version 2

Name	Unit	Default	Description
VERSION	-	1	1 = Version 1 2 = Version 2
ME (MS)	-	2.5	Long channel saturation transition parameter
META	-	1	ETA floating-body parameter
MSS	-	1.5	Vdse transition parameter
VMAX	m/s	4.00E+004	Saturation velocity

Table 59 Model Parameters Specific to Version 2 (Continued)

Name	Unit	Default	Description
THETA	M/V	0	Mobility degradation parameter
ISUBMOD	-	0	Channel length modulation selector: 0 – uses LAMBDA 1 – uses LS and VP
LAMBDA	1/V		Channel length modulation parameter
LS	-	3.50E-008	Channel length modulation parameter
VP	V	0.2	Channel length modulation parameter
INTDSNOD	-	1 if VERSION = 1 0 if VERSION = 2	Extrinsic series resistance mode selector: 0 - uses internal approximation for drain and source resistances 1 – uses drain and source resistances as extrinsic elements
VSIGMAT	V	VST, if specified 1.7, otherwise	VGS dependence parameter
VSIGMA	V	VSI, if specified 0.2, otherwise	VGS dependence parameter

Table 60 Self-Heating Parameters

Name	Unit	Default	Description
SHMOD	-	0	Self-heating flag
RTH0	m^oC/W	0	Thermal resistance per unit width
CTH0	Ws/m^oC	1.00E-005	Thermal capacitance per unit width
WTH0	m	0	Width offset for thermal resistance and capacitance scaling

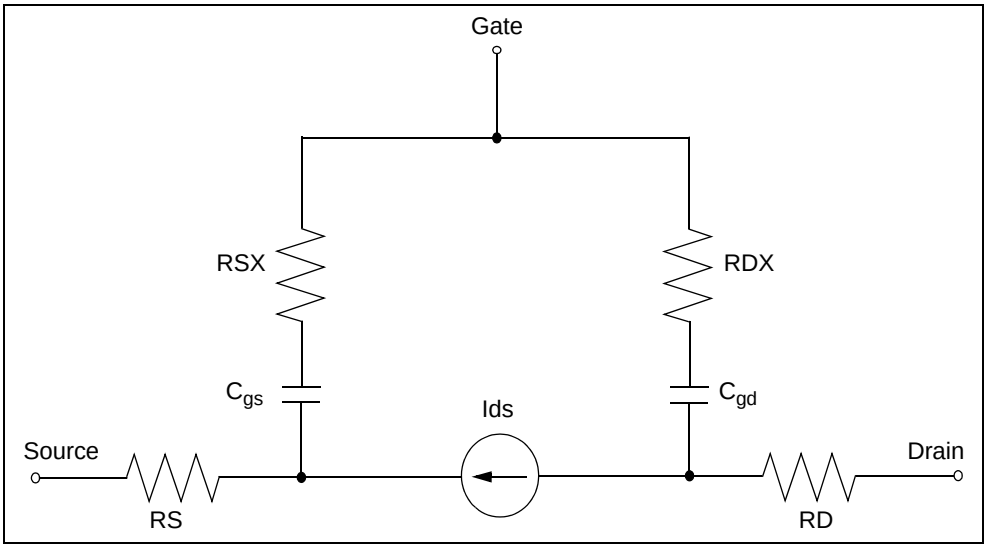
Table 61 ACM Parameters for Drain and Source Resistanance Calculus Specific to HSPICE

Name	Unit	Default	Description
ACM	-	-	Area calculation method
LD	m	0	Lateral diffusion into channel from source and drain diffusion
WD	m	0	Lateral diffusion into channel from bulk along width
HDIF	m	0	Length of heavily doped diffusion
LDIF	m	0	Length of heavily doped region adjacent to gate
RDC	ohm	0	Additional drain resistance due to contact
RSC	ohm	0	Additional source resistance due to contact
RSH	ohm/sq	0	Drain and source diffusion sheet resistance

Note:

Source and drain resistances are calculated similarly to other HSPICE MOSFET models, which are based on the value of ACM.

Equivalent Circuit



Model Equations

Drain Current

Total Current

$$I_{ds} = \left(\frac{I_a \cdot I_{sub}}{I_a + I_{sub}} + I_{leak}\right) \cdot (1 + I_{kink})$$

Subthreshold Current

The following is the expression for the subthreshold current:

$$I_{sub} = MUS \cdot C_{ox} \frac{W}{L} V_{sth}^{2} \exp\left(\frac{V_{GT}}{V_{sth}}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right]$$

$$I_{sub} = MUS \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^{2} \cdot \exp\left(\frac{V_{GT}}{V_{sth}}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right)$$

$$C_{OX} = \frac{\varepsilon_i}{T_{OX}} \qquad V_{sth} = ETA \cdot V_{th} \qquad V_{th} = \frac{k_B \cdot TEMP}{q}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{Teff} = V_{TX} - \frac{AT \cdot {V_{DS}}^2 + BT}{L_{eff} \cdot \left(1 + \exp\left(\frac{V_{GS} - VST - VTX}{VSI}\right)\right)}$$

In the preceding equations, $\varepsilon\tau$ is the dielectric constant of the oxide, and k_B is the Boltzmanns constant.

Above the $V_{GT} > 0$ threshold, the following equation calculates the conduction current:

$$I_a = \frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff}}{L_{eff}}\left(V_{GTE} \cdot V_{DS} - \frac{{V_{DS}}^2}{2 \cdot \alpha_{sat}}\right) \text{for } V_{DS} \le \alpha_{sat} V_{GTE}$$

$$\frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff} \cdot {V_{GTE}}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} \qquad \text{for } V_{DS} > \alpha_{sat} V_{GTE}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{MUO} + \frac{1}{\mu 1 \cdot \left(\frac{2 \cdot V_{GTE}}{V_{sth}}\right)^{MMU}}$$

$$V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1\right)^2}\right]$$

Subthreshold Leakage Current

Subthreshold leakage current is the result of the thermionic field emission of carriers through the grain boundary trap states as described in the following equations.

$$I_{leak} = IO \cdot W_{eff} \cdot \left[\exp\left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T}\right) - 1\right] \cdot (X_{TFE} + X_{TE}) + I_{diode}$$

$$X_{TFE} = \frac{X_{\text{TFE, lo}} \cdot X_{\text{TFE, hi}}}{X_{\text{TFE, lo}} + X_{\text{TFE, hi}}}$$

The following equations calculate values for the preceding equations:

$$X_{TE} = \exp(-W_C) \qquad W_C = \frac{E_C - E_t}{k \cdot T} = \frac{0.55eV}{k \cdot T}$$

$$X_{\text{TFE,lo}} = \frac{4\sqrt{\pi}}{3} \cdot f \cdot \exp\left(\frac{4}{27} \cdot f^2 - W_c\right) \quad for\ f \le f_{lo}$$

$$X_{\text{TFE, lo}}(f_{lo}) \cdot \exp\left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo}\right) \cdot (f - f_{lo})\right] \quad for\ f > f_{lo}$$

$$X_{\text{TFE,hi}} = \frac{2W_c}{3} \cdot \exp\left(1 - \frac{2W_c}{3}\right) \quad for\ f > f_{hi}$$

$$\left(1 - \frac{3\sqrt{W_c}}{2 \cdot f}\right)^{-1} \exp\left[\frac{-W_c^{3/2}}{f}\right] \quad for\ f \ge f_{hi}$$

$$f_{hi} = 3 \cdot \left(\frac{W_c^{3/2}}{2W_c - 3}\right)$$

$$f = \frac{F_{min}}{2}\left[1 + \frac{\frac{F_f}{F_{fo}}}{F_{min}} + \sqrt{DELTA^2 + \left(\frac{\frac{F_f}{F_{fo}}}{F_{min}} - 1\right)^2}\right]$$

$$F_{min} = 1e^{-4}$$

$$X_{\text{TFE,lo}}(f_{lo}) = \frac{2\sqrt{4\pi}}{3} \cdot f_{lo} \cdot \exp\left(\frac{4}{27} f_{lo}^{\ 2} - W_c\right)$$

$$F_f = \left(\frac{V_{DS}}{DD} - \frac{V_{GS} - VFB}{DG}\right)$$

$$F_{fo} = (k \cdot T)^{3/2} \cdot \left(\frac{4}{3} \cdot \frac{2\pi\sqrt{2m^*}}{q \cdot h}\right)$$

$$m^* = 0.27 \cdot m_0 \qquad f_{lo} = \frac{3}{2} \cdot (\sqrt{W_c + 1} - 1)$$

$$I_{diode} = IOO \cdot W_{eff} \cdot \exp\left(-\frac{EB}{k \cdot T}\right)\left[1 - \exp\left(-\frac{q \cdot V_{DS}}{k \cdot T}\right)\right]$$

Impact Ionization Effect

V_{GT} > 0ery large drain biases include the kink effect. Level 62 models this effect as impact ionization in a narrow region near the drain, and adds the I_{kink} impact ionization current to the drain current. The expression is:

$$I_{kink} = A_{kinkt} \cdot (V_{DS} - V_{DSE}) \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$A_{kinkt} = \frac{1}{VKINK}\left(\frac{LKINK}{L_{eff}}\right)^{MK}$$

$$V_{DSE} = \frac{VDS}{\left(1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^3\right)^{1/3}} - V_{th}$$

$$V_{DSAT} = \alpha_{sat} \cdot V_{GTE}$$

Threshold Voltage

If you do not specify VTO, then V_T=VON-DVT. Otherwise, V_T=VTO.

Temperature Dependence

$$V_{TX} = V_T - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = MU1 + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Capacitance

CAPMOD=0:

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSEX}}{2V_{DSAT} - V_{DSEX}}\right)^2\right]$$

$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{DSAT}}{2V_{DSAT} - V_{DSEX}}\right)^2\right]$$

$$C_f = 0.5 \cdot EPS \cdot W_{eff}$$

$$C_{gcd} = \frac{C_{OX}}{1 + \eta_{cd} \cdot \exp\left(-\frac{V_{GTX}}{\eta_{cd} \cdot V_{th}}\right)}$$

$$C_{gcs} = \frac{C_{OX}}{1 + ETAC0 \cdot \exp\left(-\frac{V_{GTX}}{ETAC0 \cdot V_{th}}\right)}$$

$$C_{OX} = \frac{W_{eff} \cdot L_{eff} \cdot \varepsilon_i}{TOX}, \eta_{cd} = ETAC0 + ETAC00 \cdot V_{DSEX}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

$$V_{GTX} = V_{GS} - V_{TX}$$

CAPMOD=1:

If ZEROC equals 1:

$$V_{gst} = V_{GS} - V_{TX}$$

$$Phi = 0.6$$

$$V_{gst} < \frac{-phi}{2} \qquad C_{gs} = C_{gd} = 0$$

$$\frac{-phi}{2} \le V_{gst} < 0 \qquad C_{gs} = \frac{4 \cdot V_{gst} \cdot C_{OX}}{3 \cdot Phi} + \frac{2 \cdot C_{OX}}{3}, C_{gd} = 0$$

$$V_{gst} \geq 0 \begin{cases} V_{DS} \geq V_{DSAT} & C_{gs} = \frac{2C_{OX}}{3},\ C_{gd} = 0 \\ V_{DS} < V_{DSAT} & C_{gd} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \\ & C_{gs} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSE}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \end{cases}$$

$$C_{OX} = \frac{\varepsilon_i \cdot W_{eff} \cdot L_{eff}}{T_{OX}} \qquad V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

Geometry Effect

$$W_{eff} = W + XW$$
$$L_{eff} = L + XL$$

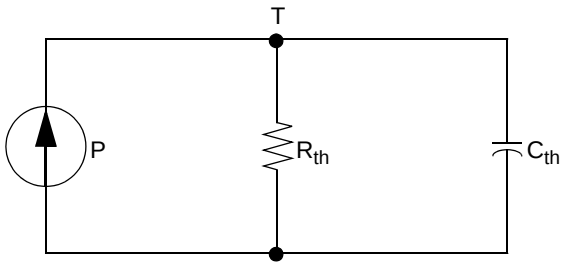
Self Heating

Self heating is turned on if self-heating parameters `SHMOD=1` and `RTH0 > 0`.

`SHMOD` and `RTH0` are also instance parameters. They override the corresponding model parameters.

The effective thermal resistance and capacitance equations and equivalent circuit are:

$$R_{th} = \frac{RTH0}{W_{eff} + WTH0_{eff}}$$
$$C_{th} = CTH0 \cdot (W_{eff} + WTH0_{eff})$$



Level 63 Philips MOS11 Model

The Philips MOS Model 11, Level 1100 and 1101, are available as Level 63 in the Synopsys MOSFET models (based on the “Unclassified Report NL-UR 2001/813” by R. Langevelde).

Philips MOS Model 11, Level 1101, is an updated version of Level 1100. It uses the same basic equations as Level 1100, but uses different geometry scaling rules. It includes two types of geometrical scaling rules: physical rules and binning rules. To select these scaling rules, use the Version parameter (1100, 11010, or 11011).

The parasitic diode model includes the Philips JUNCAP Parasitic Diode Model.

For more information about the MOS Model 11 and the Philips JUNCAP Parasitic Diode Model, see:

http://www.semiconductors.philips.com/Philips_Models

Using the Philips MOS11 Model

1. Set Level=63 to identify the model as Philips MOS Model 11.
2. Set the MOS11 version:
   - Set Version=1100 to identify the model as Philips MOS Model 11, Level 1100.
   - Set Version=11010 to identify the model as Philips MOS Model 11, Level 1101 (physical geometry scaling rules).
   - Set Version=11011 to identify the model as Philips MOS Model 11, Level 1101 (binning geometry scaling rules).

3. The default room temperature is 25 ^{o}C in Synopsys circuit simulators, but is 27 ^{o}C in most other simulators. When comparing to other simulators, use **.TEMP** 27 or **.OPTION TNOM**=27 to set the simulation temperature to 27 in the netlist.
4. The set of model parameters should always include the TR model reference temperature which corresponds to TREF in other levels in the Synopsys MOSFET model levels. The default for TR is 21.0 to match the Philips simulator.
5. This model has its own charge-based capacitance model. This model ignores the CAPOP parameter, which selects different capacitance models.
6. This model uses analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.
7. You can use DTEMP with this model to increase the temperature of individual elements, relative to the circuit temperature. Set DTEMP on the element line.
8. Because the defaults are non-zero, you should set *every* Level 63 model parameter in the Model Parameters table in the **.MODEL** statement.
9. The general syntax for the MOSFET element is the same as the other standard MOSFET models, other than PS and PD. In Level=63, PS and PD are the length of the sidewall of the source/drain, which is not under the gate.
10. Philips MOS11 has its own LMIN parameter, which has a different definition from that of HSPICE. To avoid the conflict with LMIN in simulation, Synopsys changed the LMIN parameter in the Level=63 MOSFET model to LLMIN.

Description of Parameters

Table 62 Level 63 MOS11 Parameters, Level 1100

Name	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	63	
VERSION	Version of this model		1100	

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
LER	Effective channel length, reference transistor	m	1E-6	1E-6
WER	Effective channel width, reference transistor	m	1E-5	1E-5
LVAR	Difference between the actual and programmed poly silicon gate length	m	0	0
LAP	Effective channel length reduction per side, due to lateral diffusion of the source/ drain dopant ions	m	4E-8	4E-8
WVAR	Difference between the actual and the programmed field oxide opening	m	0	0
WOT	Effective reduction of channel width per side due to the lateral diffusion of channel stop dopant ions	m	0	0
TR	Temperature at which simulation determines the parameters for the reference transistor		21	21
VFBR	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
STVFB	Coefficient of temperature dependence for VFB	V/K	5E-4	5E-4
KOR	Body-effect factor for the reference transistor	V1/2	0.5	0.5
SLKO	Coefficient of the length dependence of kO	V1/2m	0	0
SL2KO	Second coefficient of the length dependence of kO	V1/2m2	0	0
SWKO	Coefficient of the width dependence of kO	V1/2m	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
KPINV	Inverse of the body-effect factor, poly-silicon gate	V-1/2	0	0
PHIBR	Surface potential at the onset of strong inversion at the reference temperature	V	0.95	0.95
SLPHIB	Coefficient of the length dependence of $\phi\beta$	Vm	0	0
SL2PHIB	Second coefficient of the length dependence of $\phi\beta$	Vm2	0	0
SWPHIB	Coefficient of the width dependence of $\phi\beta$	Vm	0	0
BETSQ	Gain factor for an infinite square transistor at the reference temperature	AV-2	3.709E-4	1.15E-4
ETABET	Exponent of temperature dependence, gain factor	-	1.3	0.5
FBET1	Relative mobility decrease of the first lateral profile	-	0	0
LP1	Characteristic length of the first lateral profile	m	8E-7	8E-7
FBET2	Relative mobility decrease due to the second lateral profile	-	0	0
LP2	Characteristic length of the second lateral profile	m	8E-7	8E-7
THESRR	Mobility reduction coefficient, due to the surface roughness scattering for the reference transistor at the reference temperature	V-1	0.4	0.73
SWTHESR	Coefficient of the width dependence of θSR	m	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
THEPHR	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature	V-1	1.29E-2	1E-3
ETAPH	Exponent of the temperature dependence of θSR for the reference temperature	-	1.75	1.75
SWTHEPH	Coefficient of the width dependence of θSR	m	0	0
ETAMOBR	Effective field parameter for dependence on depletion/ inversion charge, reference transistor	-	1.4	3
STETAMOB	Coefficient of temperature dependence, ηMOB	K-1	0	0
SWETAMOB	Coefficient of the width dependence of ηMOB	m	0	0
NUR	Exponent of the field dependence of the mobility model minus 1,such as ν-1) at the reference temperature	-	1	1
NUEXP	Exponent of temperature dependence, ν parameter	-	5.25	3.23
THERR	Series resistance coefficient for the reference transistor at reference temperature	V-1	0.155	0.08
ETAR	Temperature dependence exponent of θR	-	0.95	0.4
SWTHER	Coefficient of the width dependence of θR	m	0	0
THER1	Numerator of gate voltage dependent part of the series resistance for the reference transistor	V	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
THER2	Denominator of the gate voltage dependent part of the series resistance for the reference transistor	V	1	1
THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	V-1	0.5	0.2
SLTHESAT	Coefficient of the length dependence of θSAT	-	1	1
THESATEXP	Exponent of the length dependence of θSAT	-	1	1
ETASAT	Exponent of the temperature dependence of θSAT	-	1.04	0.86
SWTHESAT	Coefficient of the width dependence of θSAT	m	0	0
THETHR	Coefficient of the self-heating for the reference transistor at the reference temperature	V-3	1E-3	1E-3
THETHEXP	Exponent of the length dependence of θTH	-	1	1
SWTHETH	Coefficient of the width dependence of θTH	m	0	0
SDIBLO	Drain-induced barrier-lowering parameter for the reference transistor	V-1/2	2E-3	1E-3
SDIBLEXP	Exponent of the length dependence of σDIBL	-	1.35	1.35
MOR	Parameter for the short-channel subthreshold slope for the reference transistor	-	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
MOEXP	Exponent of the length dependence of mO	-	1.34	1.34
SSFR	Static feedback parameter for the reference transistor	V-1/2	6.25E-3	6.25E-3
SLSSF	Coefficient of the length dependence of σSF	m	1E-6	1E-6
SWSSF	Coefficient of the width dependence of σSF	m	0	0
ALPR	Factor of the channel length modulation for the reference transistor	-	1E-2	1E-2
SLALP	Coefficient of the length dependence of α	-	1	1
ALPEXP	Exponent of the length dependence of α	-	1	1
SWALP	Coefficient of the width dependence of α	m	0	0
VP	Characteristic voltage, channel length modulation	V	5E-2	5E-2
LLMIN	Minimum effective channel length in a technology, calculates the m smoothing factor	m	1.5E-7	1.5E-7
A1R	Weak-avalanche current factor for the reference transistor at the reference temperature	-	6	6
STA1	Temperature dependence coefficient of a1	K-1	0	0
SLA1	Coefficient of the length dependence of a1	m	0	0
SWA1	Coefficient of the width dependence of a1	m	0	0
A2R	Exponent of the weak-avalanche current for the reference transistor	V	38	38
SLA2	Coefficient of the length dependence of a2	Vm	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
SWA2	Coefficient of the width dependence of a2	Vm	0	0
A3R	Drain-source voltage factor, above which weak-avalanche occurs for the reference transistor	-	1	1
SLA3	Coefficient of the length dependence of a3	m	0	0
SWA3	Coefficient of the width dependence of a3	m	0	0
IGINVR	Gain factor for the intrinsic gate tunneling current in the inversion for the reference transistor	AV-2	0	0
BINV	Probability factor for the intrinsic gate tunneling current in inversion	V	48	48
IGACCR	Gain factor for the intrinsic gate tunneling current in the accumulation for the reference transistor	AV-2	0	0
BACC	Probability factor for the intrinsic gate tunneling current in the accumulation	V	48	48
VFBOV	Flat-band voltage for the Source/Drain overlap extension	V	0	0
KOV	Body-effect factor for the Source/Drain overlap extensions	V1/2	2.5	2.5
IGOVR	Gain factor for the Source/Drain overlap tunneling current for reference transistor	AV-2	0	0
TOX	Thickness of the gate oxide layer	m	3.2E-9	3.2E-9
COL	Gate overlap capacitance per unit channel length	Fm-1	3.2E-10	3.2E-10
GATENOISE	Flag for inclusion/exclusion of the induced gate thermal noise	-	0	0

Table 62 Level 63 MOS11 Parameters, Level 1100 (Continued)

Name	Description	Units	NMOS	PMOS
NTR	Coefficient of the thermal noise at the actual temperature	J	1.656E-20	1.656E-20
NFAR	First coefficient of the flicker noise for the reference transistor	V-1m-4	1.573E22	1.573E22
NFBR	Second coefficient of the flicker noise for the reference transistor	V-1m-2	4.752E8	4.752E8
NFCR	Third coefficient of the flicker noise for the reference transistor	V-1	0	0

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling

Name	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	63	
VERSION	Version of this model		11010	
LVAR	Difference between the actual and the programmed poly silicon gate length	m	0	0
LAP	Effective channel length reduction per side, due to the lateral diffusion of source/ drain dopant ions	m	4E-8	4E-8
WVAR	Difference between the actual and programmed field oxide opening	m	0	0
WOT	Effective reduction of the channel width per side due to the lateral diffusion of the channel stop dopant ions	m	0	0
TR	Temperature at which simulation determines the reference transistor parameters		21	21

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
VFBR	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
STVFB	Temperature dependence coefficient of VFB	V/K	5E-4	5E-4
KOR	Body-effect factor for the reference transistor	V1/2	0.5	0.5
SLKO	Coefficient of the length dependence of kO	-	0	0
SL2KO	Second coefficient of the length dependence of kO	-	0	0
SWKO	Coefficient of the width dependence of kO	-	0	0
KPINV	Inverse of the body-effect factor, poly-silicon gate	V-1/2	0	0
PHIBR	Surface potential at the onset of strong inversion at the reference temperature	V	0.95	0.95
STPHIB	Temperature dependence coefficient of ϕB	VK-1	-8.5E-4	-8.5E-4
SLPHIB	Coefficient of the length dependence of ϕB	-	0	0
SL2PHIB	Second coefficient of length dependence of ϕB	-	0	0
SWPHIB	Coefficient of the width dependence of ϕB	-	0	0
BETSQ	Gain factor for an infinite square transistor at the reference temperature	AV-2	3.709E-4	1.15E-4
ETABETR	Exponent of the temperature dependence of the gain factor	-	1.3	0.5
SLETABET	Length dependence coefficient of $\eta\beta$R	-	0	0

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
FBET1	Relative mobility decrease due to first lateral profile	-	0	0
LP1	Characteristic length of first lateral profile	m	8E-7	8E-7
FBET2	Relative mobility decrease due to second lateral profile	-	0	0
LP2	Characteristic length of second lateral profile	M	8E-7	8E-7
THESRR	Mobility reduction coefficient, due to surface roughness scattering for reference transistor at reference temperature	V-1	0.4	0.73
ETASR	Exponent of temperature dependence of θSR	-	0.65	0.5
SWTHESR	Coefficient of the width dependence of θSR	-	0	0
THEPHR	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature	V-1	1.29E-2	1E-3
ETAPH	Exponent of the temperature dependence of θSR for the reference temperature	-	1.35	3.75
SWTHEPH	Coefficient of the width dependence of θSR	-	0	0
ETAMOBR	Effective field parameter, depletion/ inversion charge dependence for reference transistor	-	1.4	3
STETAMOB	Temperature dependence coefficient of ηMOB	K-1	0	0
SWETAMOB	Width dependence coefficient of ηMOB	-	0	0

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
NU	Exponent of field dependence, mobility model minus 1(such as ν-1) at reference temperature	-	2	2
NUEXP	Exponent of the temperature dependence of parameter ν	-	5.25	3.23
THERR	Series resistance coefficient for reference transistor at reference temperature	V-1	0.155	0.08
ETAR	Exponent of temperature dependence of θR	-	0.95	0.4
SWTHER	Coefficient of the width dependence of θR	-	0	0
THER1	Numerator of gate voltage dependent part of series resistance for reference transistor	V	0	0
THER2	Denominator of gate voltage dependent part of series resistance for the reference transistor	V	1	1
THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	V-1	0.5	0.2
SLTHESAT	Length dependence coefficient of θSAT	-	1	1
THESATEXP	Exponent of length dependence of θSAT	-	1	1
ETASAT	Exponent of temperature dependence of θSAT	-	1.04	0.86
SWTHESAT	Width dependence coefficient of θSAT	-	0	0
THETHR	Coefficient of self-heating for the reference transistor at the reference temperature	V-3	1E-3	0.5E-3

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
THETHEXP	Exponent of the length dependence of θTH	-	1	1
SWTHETH	Coefficient of the width dependence of θTH	-	0	0
SDIBLO	Drain-induced barrier-lowering parameter for the reference transistor	V-1/2	1E-4	1E-4
SDIBLEXP	Exponent of length dependence of σDIBL	-	1.35	1.35
MOR	Parameter for short-channel subthreshold slope for the reference transistor	-	0	0
MOEXP	Exponent of the length dependence of mO	-	1.34	1.34
SSFR	Static feedback parameter, reference transistor	V-1/2	6.25E-3	6.25E-3
SLSSF	Length dependence coefficient of σSF	-	1.0	1.0
SWSSF	Coefficient of the width dependence of σSF	-	0	0
ALPR	Factor of the channel length modulation for the reference transistor	-	1E-2	1E-2
SLALP	Coefficient of the length dependence of α	-	1	1
ALPEXP	Exponent of the length dependence of α	-	1	1
SWALP	Coefficient of the width dependence of α	-	0	0
VP	Characteristic voltage of the channel length modulation	V	5E-2	5E-2
LLMIN	Minimum effective channel length in technology, calculates smoothing factor m	M	1.5E-7	1.5E-7

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
A1R	Weak-avalanche current factor for reference transistor at reference temperature	-	6	6
STA1	Temperature dependence coefficient of a1	K-1	0	0
SLA1	Coefficient of the length dependence of a1	-	0	0
SWA1	Coefficient of the width dependence of a1	-	0	0
A2R	Exponent of the weak-avalanche current for the reference transistor	V	38	38
SLA2	Coefficient of the length dependence of a2	-	0	0
SWA2	Coefficient of the width dependence of a2	-	0	0
A3R	Drain-source voltage factor, above which weak-avalanche occurs for reference transistor	-	1	1
SLA3	Coefficient of the length dependence of a3	-	0	0
SWA3	Coefficient of the width dependence of a3	-	0	0
IGINVR	Gain factor for intrinsic gate tunneling current in inversion for reference transistor	AV-2	0	0
BINV	Probability factor for intrinsic gate tunneling current in inversion	V	48	87.5
IGACCR	Gain factor for intrinsic gate tunneling current in accumulation for reference transistor	AV-2	0	0
BACC	Probability factor for intrinsic gate tunneling current in accumulation	V	48	48
VFBOV	Flat-band voltage for the Source/Drain overlap extensions	V	0	0

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
KOV	Body-effect factor for the Source/Drain overlap extensions	V1/2	2.5	2.5
IGOVR	Gain factor for Source/Drain overlap tunneling current for reference transistor	AV-2	0	0
TOX	Thickness of the gate oxide layer	M	3.2E-9	3.2E-9
COL	Gate overlap capacitance per unit channel length	F	3.2E-16	3.2E-16
GATENOISE	In/exclusion flag of induced gate thermal noise	-	0	0
NT	Thermal noise coefficient at the actual temperature	J	1.656E-20	1.656E-20
NFAR	First coefficient of the flicker noise for the reference transistor	V-1m-4	1.573E23	3.825E24
NFBR	Second coefficient of the flicker noise for the reference transistor	V-1m-2	4.752E9	1.015E9
NFCR	Third coefficient of the flicker noise for the reference transistor	V-1	0	7.3E-8
MOO	Parameter for short-channel subthreshold slop		0	0
AGIDLR	Gain factor for gate-induced drain leakage current for a channel width of 1 um	AV**(-3)	0	0
BGIDL	Probability factor for gate-induced drain leakage current at the reference temperature	V	41.0	41.0

Table 63 Level 63 MOS11 Parameters, Level 11010: Physical Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
CGIDL	Factor for the lateral field dependence of the gate-induce drain leakage current		0	0
STBGIDL	Coefficient of the temperature dependence of BGIDL	VK**(-1)	-3.638e-4	-3.638e-4

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling

Name	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	63	
VERSION	Version of this model		11011	
LVAR	Difference between the actual and the programmed poly silicon gate length	m	0	0
LAP	Effective channel length reduction per side due to lateral diffusion of source/ drain dopant ions	m	4E-8	4E-8
WVAR	Difference between the actual and the programmed field oxide opening	m	0	0
WOT	Effective reduction, channel width per side due to lateral diffusion of channel stop dopant ions	m	0	0
TR	Temperature at which the parameters for the reference transistor have been determined	^{o}C	21	21
VFB	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
POKO	Coefficient, geometry independent ko part	V1/2	0.5	0.5

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLKO	Coefficient for the length dependent of ko	V1/2	0	0
PWKO	Coefficient for the width dependent of ko	V1/2	0	0
PLWKO	Coefficient, length times width ko dependent	V1/2	0	0
KPINV	Inverse of body-effect factor, poly-silicon gate	V-1/2	0	0
POPHIB	Coefficient, geometry independent ΦB part	V	0.950	0.950
PLPHIB	Coefficient for the length dependent of ΦB	V	0	0
PWPHIB	Coefficient for the width dependent of ΦB	V	0	0
PLWPHIB	Coefficient, length times width ΦB dependent	V	0	0
POBET	Coefficient, geometry independent β part	AV-2	1.922E-3	3.814E-4
PLBET	Coefficient for the length dependent of β	AV-2	0	0
PWBET	Coefficient for the width dependent of β	AV-2	0	0
PLWBET	Coefficient, width over length dependent of β	AV-2	0	0
POTHESR	Coefficient, geometry independent θSR part	V-1	3.562E-1	7.30E-1
PLTHESR	Coefficient for the length dependent part of θSR	V-1	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PWTHESR	Coefficient for the width dependent part of θSR	V-1	0	0
PLWTHESR	Coefficient, length times width, θSR dependent	V-1	0	0
POTHEPH	Coefficient, geometry independent θph part	V-1	1.290E-2	1.0E-3
PLTHEPH	Coefficient for the length dependent of θph	V-1	0	0
PWTHEPH	Coefficient for the width dependent of θph	V-1	0	0
PLWHEPH	Coefficient, length times width, θph dependent	V-1	0	0
POETAMOB	Coefficient, geometry independent ηmob part	-	1.40	3
PLETAMOB	Coefficient, length-dependent ηmob part	-	0	0
PWETAMOB	Coefficient, width-dependent ηmob part	-	0	0
PLWETAMOB	Coefficient, length times width dependent ηmob part	-	0	0
POTHER	Coefficient for the geometry-independent part of θR	V-1	8.12E-2	7.9E-2
PLTHER	Coefficient for the length-dependent part of θR	V-1	0	0
PWTHER	Coefficient for the width dependent part of θR	V-1	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLWTHER	Coefficient, length times width θR dependent	V-1	0	0
THER1	Numerator of the gate voltage dependent part of the series resistance for all transistors in bin	V	0	0
THER2	Denominator of the gate voltage dependent part of the series resistance for all transistors in the bin	V	1.0	1.0
POTHESAT	Coefficient for the geometry-independent part of θsat	V-1	2.513E-1	1.728E-1
PLTHESAT	Coefficient for length-dependent part of θsat	V-1	0	0
PWTHESAT	Coefficient for the width-dependent part of θsat	V-1	0	0
PLWTHESAT	Coefficient, length times width θsat dependent	V-1	0	0
POTHETH	Coefficient for the geometry-independent part of θTH	V-3	1.0E-5	0
PLTHETH	Coefficient for the length-dependent part of θTH	V-3	0	0
PWTHETH	Coefficient for the width-dependent part of θTH	V-3	0	0
PLWTHETH	Coefficient for the length times width θTH dependent part	V-3	0	0
POSDIBL	Coefficient for the geometry-independent part of σdibl	V-1/2	8.53E-4	3.551E-5
PLSDIBL	Coefficient for the length-dependent part of σdibl	V-1/2	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PWSDIBL	Coefficient for the width-dependent part of σdibl	V-1/2	0	0
PLWSDIBL	Coefficient, length times width dependent of σdibl	V-1/2	0	0
POMO	Coefficient for the geometry-independent part of m0	-	0	0
PLMO	Coefficient for the length-dependent part of m0	-	0	0
PWMO	Coefficient for the width-dependent part of m0	-	0	0
PLWMO	Coefficient for the length times width m0 dependent part	-	0	0
POSSF	Coefficient for the geometry-independent part of σsf	V-1/2	1.2E-2	1.0E-2
PLSSF	Coefficient for the length-dependent part of σsf	V-1/2	0	0
PWSSF	Coefficient for the width-dependent part of σsf	V-1/2	0	0
PLWSSF	Coefficient for the length times width σsf dependent part	V-1/2	0	0
POALP	Coefficient for the geometry-independent part of α	-	2.5E-2	2.5E-2
PLALP	Coefficient for the length-dependent part of α	-	0	0
PWALP	Coefficient for the width-dependent part of α	-	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLWALP	Coefficient for the length times width dependent part of α	-	0	0
VP	Characteristic voltage of the channel length modulation	V	5E-2	5E-2
POMEXP	Coefficient for the geometry-independent 1/m part	-	0.2	0.2
PLMEXP	Coefficient for the length-dependent part of 1/m	-	0	0
PWMEXP	Coefficient for the width dependent part of 1/m	-	0	0
PLWMEXP	Coefficient of the length times width 1/m dependent part	-	0	0
POA1	Coefficient of the geometry-independent a1 part	-	6.022	6.858
PLA1	Coefficient for the length-dependent part of a1	-	0	0
PWA1	Coefficient for the width-dependent part of a1	-	0	0
PLWA1	Coefficient for the length times width a1 dependent part	-	0	0
POA2	Coefficient for the geometry-independent a2 part	V	3.802E+1	5.732E+1
PLA2	Coefficient for the length-dependent part of a2	V	0	0
PWA2	Coefficient for the width-dependent part of a2	V	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLWA2	Coefficient of the length times width a2 dependent part	V	0	0
POA3	Coefficient of the geometry-independent a3 part	-	6.407E-1	4.254E-1
PLA3	Coefficient for the length-dependent part of a3	-	0	0
PWA3	Coefficient for the width-dependent part of a3	-	0	0
PLWA3	Coefficient for the length times width a3 dependent part	-	0	0
POIGINV	Coefficient for the geometry-independent part of IGINV	AV-2	0	0
PLIGINV	Coefficient for the length-dependent part of IGINV	AV-2	0	0
PWIGINV	Coefficient for the width-dependent part of IGINV	AV-2	0	0
PLWIGINV	Coefficient for the length times width dependent part of IGINV	AV-2	0	0
POBINV	Coefficient for the geometry-independent part of IGINV	V	48	48
PLBINV	Coefficient for the length-dependent part of IGINV	V	0	0
PWBINV	Coefficient for the width-dependent part of IGINV	V	0	0
PLWBINV	Coefficient for the length times width dependent part of IGINV	V	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
POIGACC	Coefficient for the geometry-independent part of IGACC	AV-2	0	0
PLIGACC	Coefficient for the length-dependent part of IGACC	AV-2	0	0
PWIGACC	Coefficient for the width-dependent part of IGACC	AV-2	0	0
PLWIGACC	Coefficient for the length times width dependent part of IGACC	AV-2	0	0
POBACC	Coefficient for the geometry-independent part of BACC	V	48	87.5
PLBACC	Coefficient for the length-dependent part of BACC	V	0	0
PWBACC	Coefficient for the width-dependent part of BACC	V	0	0
PLWBACC	Coefficient for the length times width dependent part of BACC	V	0	0
VFBOV	Flatband voltage for the source/drain overlap extensions	V	0	0
KOV	Body-effect factor for the source/drain overlap extensions	V1/2	2.5	2.5
POIGOV	Coefficient for the geometry-independent part of IGOV	AV-2	0	0
PLIGOV	Coefficient for the length-dependent part of IGOV	AV-2	0	0
PWIGOV	Coefficient for the width-dependent part of IGOV	AV-2	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLWIGOV	Coefficient for the width over length dependent part of IGOV	AV-2	0	0
TOX	Thickness of the gate oxide layer	m	3.2E-9	3.2E-9
POCOX	Coefficient for the geometry-independent COX part	F	2.98E-14	2.717E-14
PLCOX	Coefficient for the length-dependent part of COX	F	0	0
PWCOX	Coefficient for the width-dependent part of COX	F	0	0
PLWCOX	Coefficient for the length times width dependent part of COX	F	0	0
POCGDO	Coefficient for the geometry-independent CGDO part	F	6.392E-15	6.358E-15
PLCGDO	Coefficient for the length-dependent part of CGDO	F	0	0
PWCGDO	Coefficient for the width dependent part of CGDO	F	0	0
PLWCGDO	Coefficient for the width over length dependent part of CGDO	F	0	0
POCGSO	Coefficient for the geometry-independent part of CGSO	F	6.392E-15	6.358E-15
PLCGSO	Coefficient for the length-dependent part of CGSO	F	0	0
PWCGSO	Coefficient for the width-dependent part of CGSO	F	0	0
PLWCGSO	Coefficient for the width over length dependent part of CGSO	F	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
GATENOISE	Inclusion/exclusion flag of the induced gate thermal noise	-	0	0
NT	Coefficient for the thermal noise at the reference temperature	J	1.656E-20	1.656E-20
PONFA	Coefficient for the geometry-independent NFA part	V-1m-4	8.323E+22	1.90E+22
PLNFA	Coefficient for the length-dependent part of NFA	V-1m-4	0	0
PWNFA	Coefficient for the width-dependent part of NFA	V-1m-4	0	0
PLWNFA	Coefficient for the length times width dependent part of NFA	V-1m-4	0	0
PONFB	Coefficient for the geometry-independent NFB part	V-1m-2	2.514E+7	5.043E+6
PLNFB	Coefficient for the length-dependent part of NFB	V-1m-2	0	0
PWNFB	Coefficient for the width-dependent part of NFB	V-1m-2	0	0
PLWNFB	Coefficient for the length times width dependent part of NFB	V-1m-2	0	0
PONFC	Coefficient for the geometry-independent NFC part	V-1	0	3.627E-10
PLNFC	Coefficient for the length-dependent part of NFC	V-1	0	0
PWNFC	Coefficient for the width-dependent part of NFC	V-1	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLWNFC	Coefficient for the length times width dependent part of NFC	V-1	0	0
POTVFB	Coefficient for the geometry-independent part of ST;VFB	VK-1	5.0E-4	5.0E-4
PLTVFB	Coefficient for the length-dependent part of ST;VFB	VK-1	0	0
PWTVFB	Coefficient for the width-dependent part of ST;VFB	VK-1	0	0
PLWTVFB	Coefficient for the length times width dependent part of ST;VFB	VK-1	0	0
POTPHIB	Coefficient for the geometry-independent part of ST;ϕB	VK-1	-8.5E-4	-8.5E-4
PLTPHIB	Coefficient for the length-dependent part of ST;ϕB	VK-1	0	0
PWTPHIB	Coefficient for the width-dependent part of ST;ϕB	VK-1	0	0
PLWTPHIB	Coefficient for the length times width dependent part of ST;ϕB	VK-1	0	0
POTETABET	Coefficient for the geometry-independent part of $\eta\beta$	-	1.30	0.5
PLTETABET	Coefficient for the length-dependent part of $\eta\beta$	-	0	0
PWTETABET	Coefficient for the width-dependent part of $\eta\beta$	-	0	0
PLWTETABET	Coefficient for the length times width ηsr dependent part	-	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
POTETASR	Coefficient for the geometry-independent ηsr part	-	0.65	0.5
PLTETASR	Coefficient for the length-dependent part of ηsr	-	0	0
PWTETASR	Coefficient for the width-dependent part of ηsr	-	0	0
PLWTETASR	Coefficient for the length times width dependent part of ηsr	-	0	0
POTETAPH	Coefficient for the geometry-independent ηph part	-	1.35	3.75
PLTETAPH	Coefficient for the length-dependent part of ηph	-	0	0
PWTETAPH	Coefficient for the width-dependent part of ηph	-	0	0
PLWTETAPH	Coefficient for the length times width ηph dependent part	-	0	0
POTETAMOB	Coefficient for the geometry-independent part of ST:ηph	K-1	0	0
PLTETAMOB	Coefficient for the length-dependent part of ηph	K-1	0	0
PWTETAMOB	Coefficient for the width-dependent part of ηph	K-1	0	0
PLWTETAMOB	Coefficient for the length times width dependent part of ηph	K-1	0	0
NU	Exponent of the field dependence of the mobility model at the reference temperature	-	2	2

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
POTNUEXP	Coefficient for the geometry-independent νexp part	-	5.25	3.23
PLTNUEXP	Coefficient for the length-dependent part of νexp	-	0	0
PWTNUEXP	Coefficient for the width-dependent part of νexp	-	0	0
PLWTNUEXP	Coefficient fore the length times width dependent part of νexp	-	0	0
POTETAR	Coefficient for the geometry-independent ηR part	-	0.95	0.4
PLTETAR	Coefficient for the length-dependent part of ηR	-	0	0
PWTETAR	Coefficient for the width-dependent part of ηR	-	0	0
PLWTETAR	Coefficient for the length times width dependent part of ηR	-	0	0
POTETASAT	Coefficient for the geometry-independent part of ηSAT	-	1.04	0.86
PLTETASAT	Coefficient for the length-dependent part of ηSAT	-	0	0
PWTETASAT	Coefficient for the width-dependent part of ηSAT	-	0	0
PLWTETASAT	Coefficient for the length times width dependent part of ηSAT	-	0	0
POTA1	Coefficient for the geometry-independent ST;a1 part	K-1	0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PLTA1	Coefficient for the length-dependent part of ST;a1	K-1	0	0
PWTA1	Coefficient for the width-dependent part of ST;a1	K-1	0	0
PLWTA1	Coefficient for the length times width dependent part of ST;a1	K-1	0	0
POAGIDL	Coefficient for the geometry-independent part of AGIDL	AV**(-3)	0	0
PLAGIDL	Coefficient for the length dependence of AGIDL	AV**(-3)	0	0
PWAGIDL	Coefficient for the width dependence of AGIDL	AV**(-3)	0	0
PLWAGIDL	Coefficient for the width over length dependence of AGIDL	AV**(-3)	0	0
POBGIDL	Coefficient for the geometry independent part of BGIDL	V	41.0	41.0
PLBGIDL	Coefficient for the length dependence of BGIDL	V	0	0
PWBGIDL	Coefficient for the width dependence of BGIDL	V	0	0
PLWBGIDL	Coefficient for the length times width dependence of BGIDL	V	0	0
POCGIDL	Coefficient for the geometry independent part of CGIDL		0	0
PLCGIDL	Coefficient for the length dependence of CGIDL		0	0

Table 64 Level 63 MOS11 Parameters, Level 11011: Binning Geometry Scaling (Continued)

Name	Description	Units	NMOS	PMOS
PWCGIDL	Coefficient for the width dependence of CGIDL		0	0
PLWCGIDL	Coefficient for the length times width dependence of CGIDL		0	0
POTBGIDL	Coefficient for the geometry independent part of STBGIDL	VK**(-1)	-3.638e-4	-3.638e-4
PLTBGIDL	Coefficient for the length dependence of STBGIDL	VK**(-1)	0	0
PWTBGIDL	Coefficient for the width dependence of STBGIDL	VK**(-1)	0	0
PLWTBGIDL	Coefficient for the length times width dependence of STBGIDL	VK**(-1)	0	0

The following are JUNCAP model parameters specifically for the Philips MOS 11 (Level 63) model.

Table 65 Level 63 JUNCAP Parameters

Name	Description	Units	Default
DTA	Temperature offset of the JUNCAP element with respect to T_A	^oC	0
VR	Voltage at which simulation determines parameters	V	0
JSGBR	Bottom saturation-current density due to generating an electron hole at $V=V_R$	Am^{-2}	1E-03
JSDBR	Bottom saturation-current density due to diffusion from back contact	Am^{-2}	1E-03
JSGSR	Sidewall saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1E-03

Table 65 Level 63 JUNCAP Parameters (Continued)

Name	Description	Units	Default
JSDSR	Sidewall saturation-current density due to back-contact diffusion	Am^{-1}	1E-03
JSGGR	Gate edge saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1E-03
JSDGR	Gate edge saturation-current density due to back-contact diffusion	Am^{-1}	1E-03
NB	Emission coefficient of the bottom forward current	-	1
NS	Emission coefficient of the sidewall forward current	-	1
NG	Emission coefficient of the gate edge forward current	-	1
CJBR	Bottom junction capacitance at $V=V_R$	Fm^{-2}	1E-12
CJSR	Sidewall junction capacitance at $V=V_R$	Fm^{-1}	1E-12
CJGR	Gate edge junction capacitance at $V=V_R$	Fm^{-1}	1E-12
VDBR	Diffusion voltage of the bottom junction at $T=T_R$	V	1
VDSR	Diffusion voltage of the sidewall junction at $T=T_R$	V	1
VDGR	Diffusion voltage of the gate-edge junction at $T=T_R$	V	1
PB	Bottom junction grading coefficient	-	0.4
PS	Sidewall junction grading coefficient	-	0.4
PG	Gate edge junction grading coefficient	-	0.4

Note: All symbols refer to “Unclassified Report NL-UR 2001/813”.

Example 1

```
.model nch nmos level=63
+ VERSION =1100
+ LER = 1E-06 WER = 1E-05 LAP = -1.864E-08
+ TR = 21 VFBR = -1.038 SLPHIB = -1.024E-08
+ SL2PHIB = 1.428E-14 KOR = 5.763E-01 SLKO = 2.649E-08
```

```
+ SL2KO =-1.737E-14 KPINV = 2.2E-01 PHIBR = 0.85
+ BETSQ = 1.201E-04 ETABET = 1.3 FBET1 =-3.741000E-01
+ LP1 = 2.806E-06 LP2 = 1E-10 THESATEXP = 2
+ THESRR = 7.109E-01 THEPHR = 1E-03  TOX = 3.2E-09
+ ETAPH = 1.75E+00 ETAMOBR = 2.825 NUR = 1
+ NUEXP = 3.228 THERR = 1.267E-01 ETAR = 0.4
+ THER2 = 1 THESATR = 6.931E-02 SLTHESAT = 1
+ ETASAT = 8.753E-01 SSFR = 2.304E-03 VP = 5E-02
+ SLSSF = 1.002E-06 ALPR = 1.062E-02 SLALP = 9.957E-01
+ ALPEXP = 1.039 THETHR = 2.413E-03 THETHEXP = 1
+ SDIBLO = 1.06E-06 SDIBLEXP = 6.756 LLMIN = 2E-07
+ MOR = 1.05E-03 MOEXP = 3.146
+ A1R = 9.938E+04 STA1 = 9.3E-02 SLA1 =-2.805E-03
+ A2R = 4.047E+01 SLA2 = 1E-15
+ A3R = 7.54E-01 SLA3 =-8.705E-08
+ COL = 3.2E-10
+ NTR = 1.6237E-20 NFAR = 1 NFBR = 0
+ NFCR = 0 GATENOISE =0
+ CJBR = 1.347E-3 CJSR = 0.183E-9 CJGR = 0.374E-9
+ JSDBR = 0.027E-6 JSDSR = 0.040E-12 JSDGR = 0.100E-12
+ VR = 0.000
+ JSGBR = 1.900E-6 JSGSR =78.000E-12 JSGGR = 54.000E-12
+ VB = 20.000
+ VDBR = 0.828 VDSR = 0.593 VDGR = 0.500
+ PB = 0.394 PS = 0.171 PG = 0.193
+ NB = 1.000 NS = 1.000 NG = 1.000
```

Example 2

```
.model nch nmos level=63
+ VERSION = 11010
+ LVAR = 0.000000E+00
+ LAP = -1.864000E-08 WVAR = 0.000000E+00 WOT = 0.000000E+00
+ TR = 2.100000E+01 VFB = -1.038000E+00 STVFB = 0.000000E+00
+ SLPHIB = -1.024000E-08 SL2PHIB = 1.428000E-14 SWPHIB = 0.000000E+00
+ KOR = 5.763000E-01 SLKO = 2.649000E-08 SL2KO =-1.737000E-14
+ SWKO = 0.000000E+00 KPINV = 2.200000E-01 PHIBR = 8.500000E-01
+ BETSQ = 1.201000E-04 ETABETR = 1.300000E+00 FBET1 =-3.741000E-01
+ LP1 = 2.806000E-06 FBET2 = 0.000000E+00 LP2 = 1.000000E-10
+ THESRR = 7.109000E-01 SWTHESR = 0.000000E+00 THEPHR = 1.000000E-03
+ ETAPH = 1.750000E+00 SWTHEPH = 0.000000E+00 ETAMOBR = 2.825000E+00
+ STETAMOB =0.000000E+00 SWETAMOB =0.000000E+00 NU = 1.000000E+00
+ NUEXP = 3.228000E+00 THERR = 1.267000E-01 ETAR = 4.000000E-01
+ SWTHER = 0.000000E+00 THER1 = 0.000000E+00 THER2 = 1.000000E+00
+ THESATR = 6.931000E-02 SLTHESAT =1.000000E+00 THESATEXP =2.000000E+00
```

```
+ ETASAT = 8.753000E-01 SWTHESAT =0.000000E+00 SSFR = 2.304000E-03
+ SLSSF = 1.002000E-06 SWSSF = 0.000000E+00 ALPR = 1.062000E-02
+ SLALP = 9.957000E-01 ALPEXP = 1.039000E+00 SWALP = 0.000000E+00
+ VP = 5.000000E-02 THETHR = 2.413000E-03 THETHEXP =1.000000E+00
+ SWTHETH = 0.000000E+00 SDIBLO = 1.060000E-06 SDIBLEXP =6.756000E+00
+ MOR = 1.050000E-03 MOEXP = 3.146000E+00 LLMIN = 2.000000E-07
+ A1R = 9.938000E+04 STA1 = 9.300000E-02 SLA1 =-2.805000E-03
+ SWA1 = 0.000000E+00 A2R = 4.047000E+01 SLA2 = 1.000000E-15
+ SWA2 = 0.000000E+00 A3R = 7.540000E-01 SLA3 =-8.705000E-08
+ SWA3 = 0.000000E+00 TOX = 3.200000E-09 COL = 3.200000E-10
+ NT = 1.623700E-20 NFAR = 1.000000E-00 NFBR = 0.000000E+00
+ NFCR = 0.000000E+00 GATENOISE  =0.00000E-00 DTA = 0.000000E-00
```

Example 3

```
.model nch nmos level=63
+ LEVEL   = 63
+ VERSION = 11011
+ LVAR = 0   LAP = 4.0E-08   WVAR = 0.0 WOT = 0.0 TR = 21 VFB = -0.105E+01
+ POKO = 0.5 PLKO = 0.0   PWKO = 0.0   PLWKO = 0.0   KPINV= 0.0
+ POPHIB = 0.95   PLPHIB = 0.0   PWPHIB = 0.0   POBET = 1.922E-03
+ POTHESR = 3.562E-01 POTHEPH = 1.29E-02 POETAMOB = 1.4 POTHER = 8.120E-02
+ THER1 = 0.0   THER2 = 0.1E+01   POTHESAT = 0.2513   POTHETH   = 1.0E-5
+ POSDIBL = 8.530E-4   POSSF = 1.2E-2   POALP = 2.5E-2   VP = 5.0E-2
+ POMEXP = 0.2     POA1=   6.022     POA2 = 38.02     POA3 = 0.6407
+ POBINV = 48    POBACC = 48    KOV = 2.5     TOX = 3.2E-09
+ POCOX = 2.980E-14 POCGDO = 6.392E-15 POCGSO = 6.392E-15
+ NT = 1.656E-20  PONFA = 8.323E+22    PONFB = 2.514E+7
+ POTVFB = 5.0E-4    POTPHIB = -8.5E-4
+ POTETABET = 1.30    POTETASR = 0.65    POTETAPH = 1.350    NU = 2.0
+ POTNUEXP = 5.25     POTETAR = 0.95   POTETASAT = 1.040
```

Level 64: STARC HiSIM Model

HiSIM (Hiroshima-university STARC IGFET Model) is a publicly-available MOSFET model for circuit simulation. It uses drift-diffusion approximation, and a channel-surface-potential description. You can model all MOSFET characteristics closely, based on their physical origins by using fewer model parameters (about 90 model parameters); each parameter set is sufficient for all gate lengths. These model parameters are directly related to the MOSFET physics that a simulator can easily extract according to its physical meanings.

The STARC HiSIM model is Level 64 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=64
```

HSPICE HiSIM model code is based on the Spice3f5 version that Hiroshima University/STARC released at the following web site:

http://www.starc.jp/kaihatu/pdgr/hisim/hisim.html

Since the STARC HiSIM1.1.0 release, the Synopsys version of the HiSIM model has included a VERSION number parameter to facilitate backward compatibility. Starting in the 2003.03 release, Synopsys uses the STARC version control mechanism so you must enter an integer for the VERSION model parameter. For example, to specify HiSIM version 1.0.0, set the VERSION model parameter to 100. If you do not set the VERSION parameter, simulation issues a warning and automatically sets this parameter to 100.

You can set the VERSION value to:

- 100, 101, 102 (HiSIM1.0.* series)
- 110, 111, 112 (HiSIM1.1.* series)
- 120 (HiSIM1.2.*)

You can find more details about the differences between the HiSIM versions at the previously mentioned STARC web address.

Table 66 Level 64 Model Selectors

Parameter	Default	Description
LEVEL	64	Model selector
VERSION	100	Model version number
CORSRD	0(no)	Flag. Indicates whether to include the Rs and Rd contact resistors, and whether to solve equations iteratively. CORSRD=1(yes)
COOVLP	0	Overlap capacitance model selector. • COOVLP=-1, constant value • COOVLP=0, approximating the field linear reduction • COOVLP=1, considering the lateral impurity profile.

Table 66 Level 64 Model Selectors (Continued)

Parameter	Default	Description
COISUB	0	Substrate current model selector. • for VERSION < 110, COISUB=0 (yes), • otherwise, COISUB=1 (no)
COIIGS	0	Selects the gate tunneling current model. • COIIGS=0 (yes), • COIIGS=1 (no) VERSION < 111 does not support this model.
COGIDL	0	Selects the gate induced drain leakage (GIDL) current model. • COGIDL=0 (yes) • COGIDL=1 (no) VERSION < 111 does not support this model.
CONOIS	0	1/f noise model selector. • CONOIS=0 (no) • CONOIS=1 (yes)
COISTI	0	Selects the shallow-trench-isolation (STI) leakage current. • COISTI=0 (no) • COISTI=1 (yes), only if VERSION $\geq$ 110.

Table 66 Level 64 Model Selectors (Continued)

Parameter	Default	Description
NOISE	5	Channel thermal and flicker noises combination selector. • NOISE=1 Channel thermal noise = SPICE2 model Flicker noise= SPICE2 model • NOISE=2 Channel thermal noise = HiSIM1 model for the BSIM3 model Flicker noise = HiSIM1 model • NOISE=3 Channel thermal noise = SPICE2 model Flicker noise = HiSIM1 model • NOISE=4 Channel thermal noise = HiSIM1 model for the BSIM3 model Flicker noise = SPICE2 model • NOISE=5 Channel thermal noise = NONE Flicker noise = HiSIM1 model

Table 67 Level 64 Technological Parameters

Parameter	Default	Description
TOX	3.6e-9m	Oxide thickness
XLD	0.0m	Gate-overlap length
XWD	0.0m	Gate-overlap width
XPOLYD	0.0m	Difference between the gate-poly and the design lengths
TPOLY	0.0m	Height of the gate poly-Si
RS	0.0ohm*m	Source-contact resistance
RD	0.0ohm*m	Drain-contact resistance

Table 67 Level 64 Technological Parameters (Continued)

Parameter	Default	Description
NSUBC	5.94e+17cm^{-3}	Substrate-impurity concentration
NSUBP	5.94e+17cm^{-3}	Maxim pocket concentration
VFBC	-0.722729V	Flat-band voltage
LP	0.0m	Pocket penetration length
XJ	0.0m	Junction depth (if VERSION < 110)
XQY	0.0m	Distance from the drain junction to the maximum electric field point (if VERSION $\geq$ 110)

Table 68 Level 64 Temperature Dependence Parameters

Parameter	Default	Description
BGTMP1	9.03e-5eVK^{-1}	Bandgap narrowing
BGTMP2	3.05e-7eVK^{-2}	Bandgap narrowing

Table 69 Level 64 Quantum Effect Parameters

Parameter	Default	Description
QME1	0.0mV	Coefficient for the quantum mechanical effect
QME2	0.0V	Coefficient for the quantum mechanical effect
QME3	0.0m	Coefficient for the quantum mechanical effect

Table 70 Level 64 Poly Depletion Parameters

Parameter	Default	Description
PGD1	0.0V	Strength of the poly depletion
PGD2	0.0V	Threshold voltage of the poly depletion
PGD3	0.0	V_{ds} dependence of the poly depletion

Table 71 Level 64 Short Channel Parameters

Parameter	Default	Description
PARL1	1.0	Strength of the lateral-electric-field gradient
PARL2	2.2e-8m	Depletion width of the channel/contact junction
SC1	$13.5V^{-1}$	Short-channel coefficient 1
SC2	$1.8V^{-2}$	Short-channel coefficient 2
SC3	$0.0V^{-2}m$	Short-channel coefficient 3
SCP1	$0.0V^{-1}$	Short-channel coefficient 1 for the pocket
SCP2	$0.0V^{-2}$	Short-channel coefficient 2 for the pocket
SCP3	$0.0V^{-2}m$	Short-channel coefficient 3 for the pocket

Table 72 Level 64 Narrow Channel Parameters

Parameter	Default	Description
WFC	$0.0m*F/cm^2$	Voltage reduction
MUEPH2	0.0	Mobility reduction
W0	0.0log(cm)	Minimum gate width

Table 72 Level 64 Narrow Channel Parameters (Continued)

Parameter	Default	Description
WVTHSC	0.0	Short-channel effect at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110
NSTI	$0.0cm^{-3}$	Substrate-impurity concentration at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110
WSTI	0.0m	Width of the high-field region at the shallow-trench-isolation (STI), if VERSION ≥ 110

Table 73 Level 64 Mobility Parameters

Parameter	Default	Description
VDS0	0.05V	Drain voltage for extracting low-field mobility
MUECB0	$300.0cm^2/Vs$	Coulomb scattering
MUECB1	$30.0cm^2/Vs$	Coulomb scattering
MUEPH0	0.295	Phonon scattering
MUEPH1	1.0e7	Phonon scattering
MUETMP	0.0	Temperature dependence of phonon scattering
MUESR0	1.0	Surface-roughness scattering
MUESR1	7.0e8	Surface-roughness scattering
NDEP	1.0	Coefficient of the effective-electric field
NINV	0.5	Coefficient of the effective-electric field
NINVD	$0.0V^{-1}$	Modification of NINV
BB	2.0(NMOS) 1.0(PMOS)	High-field-mobility degradation
VMAX	1.0e7cm/s	Maximum saturation velocity

Table 73 Level 64 Mobility Parameters (Continued)

Parameter	Default	Description
VOVER	0.0	Velocity overshoot effect
VOVERP	0.0	L_{gate} dependence of the velocity overshoot
RPOCK1	$0.0V^{2}*m^{1/2}/A$	Resistance coefficient caused by the potential barrier
RPOCK2	0.0V	Resistance coefficient caused by the potential barrier
RPOCP1	0.0	Resistance coefficient caused by the potential barrier, if VERSION $\geq$ 110
RPOCP2	0.0	Resistance coefficient caused by the potential barrier, if VERSION $\geq$ 110

Table 74 Level 64 Channel Length Modulation Parameters

Parameter	Default	Description
CLM1	0.3	Hardness coefficient of the channel/contact junction
CLM2	0.0	Coefficient for the Q_B contribution
CLM3	0.0	Coefficient for the Q_I contribution

Table 75 Level 64 Substrate Current Parameters

Parameter	Default	Description
SUB1	$0.0V^{-1}$	Substrate current coefficient 1
SUB2	-70.0	Substrate current coefficient 2
SUB3	1.0	Substrate current coefficient 3

Table 76 Level 64 Gate Current Parameters

Parameter	Default	Description
GLEAK1	$0.0A*V^{-3/2}/C$	Gate current coefficient 1
GLEAK2	0.0	Gate current coefficient 2
GLEAK3	0.0	Gate current coefficient 3

Table 77 Level 64 GIDL Current Parameters

Parameter	Default	Description
GIDL1	$0.0A*m*V^{-3/2}/C$	GIDL current coefficient 1
GIDL2	$0.0V^{-1/2}/cm$	GIDL current coefficient 2
GIDL3	0.0	GIDL current coefficient 3

Table 78 Level 64 1/f Noise Parameters

Parameter	Default	Description
NFALP	2.0e-15	Contribution of the mobility fluctuation
NFTRP	1.0e11	Ratio of trap density to the attenuation coefficient
CIT	$0.0F/cm^2$	Capacitance caused by the interface trapped carriers
AF	1.0	SPICE2 flicker noise exponent
KF	0.0	SPICE2 flicker noise coefficient
EF	0.0	SPICE2 flicker noise frequency exponent

Table 79 Conserving Symmetry at V_{ds}=0 for Short-Channel MOSFETS

Parameter	Default	Description
VZADD0	1.0e-2V	Symmetry conservation coefficient
PZADD0	1.0e-3V	Symmetry conservation coefficient

Table 80 MOS DIODE

Parameter	Default	Description
JSO	1.0e-4Am^{-2}	Saturation current density
JSOSW	0.0Am^{-1}	Sidewall saturation current density
NJ	1.0	Emission coefficient
NJSW	1.0	Sidewall emission coefficient
XTI	3.0	Junction current temperature exponent coefficient
CJ	8.397247e-04Fm^{-2}	Bottom junction capacitance per unit area at zero bias
CJSW	5.0e-10Fm^{-1}	Source/drain sidewall junction capacitance per unit area at zero bias
CJSWG	5.0e-10Fm^{-1}	Source/drain gate sidewall junction capacitance per unit area at zero bias
MJ	0.5	Bottom junction capacitance grading coefficient
MJSW	0.33	Source/drain sidewall junction capacitance grading coefficient
MJSWG	0.33	Source/drain gate sidewall junction capacitance grading coefficient
PB	1.0V	Bottom junction build-in potential
PBSW	1.0V	Source/drain sidewall junction build-in potential

Table 80 MOS DIODE

Parameter	Default	Description
PBSWG	1.0V	Source/drain gate sidewall junction build-in potential
VDIFFJ	0.5V	Diode threshold voltage between source/drain and substrate

Table 81 Subthreshold Swing

Parameter	Default	Description
PTHROU	0.0	Correction for steep subthreshold swing

Note: Model parameter defaults in the above tables are valid only for versions 100 and 110. For other versions, please refer to the following table:

Table 82 Model Parameter Version Defaults

Parameter	Version=100, 110	Others
VMAX	1.00e+7	7.00e+6
BGTMP1	9.03e-5	90.25e-6
BGTMP2	3.05e-7	100.0e-9
TOX	3.60e-9	5.0e-9
RS	0.0	80.0e-6
RD	0.0	80.0e-6
VFBC	-0.722729	-1.0
NSUBC	5.94e+17	1.0e+17
PARL2	2.20e-8	1.0e+17
LP	0.0	15.0e-9

Table 82 Model Parameter Version Defaults (Continued)

Parameter	Version=100, 110	Others
NSUBP	5.94e+17	1.0e+17
SC1	13.5	0.0
SC2	1.8	0.0
PGD1	0.0	0.01
PGD2	0.0	1.0
PGD3	0.0	0.8
NINVD	0.0	1.0e-9
MUEPH1	1.00e+7	25.0e+3
MUEPH0	0.295	0.300
MUESR1	7.00e+8	2.0e+15
MUESR0	1.0	2.0
MUETMP	0.0	1.5
SUB1	0.0	10.0
SUB2	-70.0	20.0
SUB3	1.0	0.8
CJ	8.397247e-04	5.0e-04
CLM1	0.3	0.7
CLM2	0.0	2.0
CLM3	0.0	1.0
RPOCK1	0.0	0.01
RPOCK2	0.0	0.1

Table 82 Model Parameter Version Defaults (Continued)

Parameter	Version=100, 110	Others
RPOCP1	0.0	1.0
VOVER	0.0	0.01
VOVERP	0.0	0.1
QME1	0.0	40.0e-12
QME2	0.0	300.0e-12
GIDL1	0.0	5.0e-3 for HiSIM101, 5.0e-6 for others
GIDL2	0.0	1.0e+6
GIDL3	0.0	0.3
GLEAK1	0.0	0.01e+6 for HiSIM101, 10.0e+3 for others
GLEAK2	0.0	20.0e+6
GLEAK3	0.0	0.3
PZADD0	1.0e-3	5.0e-3
NFTRP	100.0e+9	10.0e+9
NFALP	2.00e-15	1.0e-16

To turn off the model effects, use the following settings:

- Short-Channel Effect SC1 = SC2 = SC3 = 0
- Reverse-Short-Channel Effect LP = 0
- Quantum-Mechanical Effect QME1 = QME2 = QME3 = 0
- Poly-Depletion Effect PGD1 = PGD2 = PGD3 = 0
- Channel-Length Modulation CLM1 = CLM2 = CLM3 = 0
- Narrow-Channel Effect WFC = MUEPH2 = 0

6

BSIM MOSFET Models: Levels 13 to 39

Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.

This chapter describes three of the earliest Berkeley Short Channel IGFET (BSIM) type MOSFET device models that HSPICE supports:

- LEVEL 13 BSIM Model
- LEVEL 28 Modified BSIM Model
- LEVEL 39 BSIM2 Model

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website:

http://www.eigroup.org/cmc/cmos/default.htm

For descriptions of the newest BSIM models that Synopsys supports, see Chapter 7, BSIM MOSFET Models: Levels 47 to 65.

LEVEL 13 BSIM Model

LEVEL 13 is based on the SPICE 2G.6 BSIM model, which models the device physics of small-geometry MOS transistors. To invoke the subthreshold region, set the N0 model parameter (low field weak inversion gate drive coefficient) to less than 200. Level 13 provides three MOSFET models:

- Wire (resistor) model, compatible with the SPICE BSIM interconnect model for polysilicon and metal layers. Simulates resistors and capacitors with interconnects.
- Capacitor model. Simulates only capacitors with interconnects.
- Diffusion model, compatible with SPICE BSIM diffusion models.

To set Level 13 model parameters, either:

- Enter model parameters as numbers (as in SPICE), or
- Assign the model parameters.

If you convert from SPICE to the Synopsys models, use the S keyletter for SPICE BSIM, or M for the Synopsys model. (see IDS and VGS Curves for PMOS and NMOS on page 347).

BSIM Model Features

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by source and drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of electrical parameters

LEVEL 13 Model Parameters

MOSFET Level 13 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 13.

Note: When you read parameter names, be careful about the difference in appearance between the upper case letter O, the lower case letter o, and the number zero (0).

For reference purposes only, simulation obtains the following default values from a medium size n-channel MOSFET device.

To specify LEVEL 13 parameters, use NMOS conventions, even for PMOS (for example, ETA0=0.02, not ETA0=-0.02).

Table 83 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. 13 is the BSIM model
CGBOM, (CGBO)	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDOM, (CGDO)	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSOM, (CGSO)	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
DL0	μm	0.0	Difference between drawn poly and electrical
DW0	μm	0.0	Difference between drawn diffusion and electrical
DUM1		0.0	Dummy (not used)
DUM2		0.0	Dummy (not used)
ETA0		0.0	Linear vds threshold coefficient
LETA	mm	0.0	Length sensitivity
WETA	μm	0.0	Width sensitivity
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient

Table 83 Transistor Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
LK1	$V^{1/2}\cdot\mu m$	0.0	Length sensitivity
WK1	$V^{1/2}\cdot\mu m$	0.0	Width sensitivity
K2		0.0	Linear vsb threshold coefficient
LK2	μm	0.0	Length sensitivity
WK2	μm	0.0	Width sensitivity
MUS	$cm^2/(V\cdot s)$	600	High drain field mobility
LMS (LMUS)	$\mu m\cdot cm^2/(V\cdot s)$	0.0	Length sensitivity
WMS (WMUS)	$\mu m\cdot cm^2/(V\cdot s)$	0.0	Width sensitivity
MUZ	$cm^2/(V\cdot s)$	600	Low drain field first order mobility
LMUZ	$\mu m\cdot cm^2/(V\cdot s)$	0.0	Length sensitivity
WMUZ	$\mu m\cdot cm^2/(V\cdot s)$	0.0	Width sensitivity
N0		0.5	Low field weak inversion gate drive coefficient (a value of 200 for N0 disables the weak inversion calculation)
LN0		0.0	Length sensitivity
WN0		0.0	Width sensitivity
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
LNB		0.0	Length sensitivity
WNB		0.0	Width sensitivity

Table 83 Transistor Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
LND		0.0	Length sensitivity
WND		0.0	Width sensitivity
PHI0	V	0.7	Two times the Fermi potential
LPHI	V·μm	0.0	Length sensitivity
WPHI	V·μm	0.0	Width sensitivity
TREF	°C	25.0	Reference temperature of model (local override of TNOM)
TOXM, (TOX)	μm, (m)	0.02	Gate oxide thickness (simulation interprets TOXM or TOX >1 as Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
LU0	μm/V	0.0	Length sensitivity
WU0	μm/V	0.0	Width sensitivity
U1	μm/V	0.0	Drain field mobility reduction factor
LU1	$\mu m^2/V$	0.0	Length sensitivity
WU1	$\mu m^2/V$	0.0	Width sensitivity
VDDM	V	50	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage

Table 83 Transistor Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
LVFB	V·μm	0.0	Length sensitivity
WVFB	V·μm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
LX2E	μm/V	0.0	Length sensitivity
WX2E	μm/V	0.0	Width sensitivity
X2M (X2MZ)	$cm^2/(V^2 \cdot s)$	0.0	Vsb correction to the low field first-order mobility
LX2M (LX2MZ)	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu m \cdot cm^2/(V^2 \cdot s)$	0.0	Width sensitivity
X2MS	$cm^2/(V^2 \cdot s)$	0.0	Vbs reduction to the high-drain field mobility
LX2MS	$\mu m Þ cm^2/(V^2 \cdot s)$	0.0	Length sensitivity
WX2MS	$\mu m Þ cm^2/(V^2 \cdot s)$	0.0	Width sensitivity
X2U0	$1/V^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
LX2U0	$\mu m/V^2$	0.0	Length sensitivity
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
X2U1	$\mu m/V^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
LX2U1	$\mu m^2/V^2$	0.0	Length sensitivity
WX2U1	$\mu m^2 / V^2$	0.0	Width sensitivity

Table 83 Transistor Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
X3E	1/V	0.0	Vds correction to the linear vds threshold coefficient
LX3E	µm/V	0.0	Length sensitivity
WX3E	µm/V	0.0	Width sensitivity
X3MS	cm^2/ (V^2Þ s)	5.0	Vds reduction to the high-drain field mobility
LX3MS	µmÞcm^2/(V^2Þs)	0.0	Length sensitivity
WX3MS	µmÞcm^2/(V^2Þs)	0.0	Width sensitivity
X3U1	µm/V^2	0.0	Vds reduction to the drain field mobility reduction factor
LX3U1	µm^2/V^2	0.0	Length sensitivity
WX3U1	µm^2/V^2	0.0	Width sensitivity
XPART		1.0	Selects a gate capacitance charge-sharing coefficient

Table 84 Diffusion Layer Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
CJW, (CJSW)	F/m	0.0	Zero-bias bulk junction sidewall capacitance
CJM, (CJ)	F/m^2	4.5e-5	Zero-bias bulk junction bottom capacitance
DS	m	0.0	Average size variation due to the side etching or the mask compensation (not used)
IJS, (JS)	A/m^2	0	Bulk junction saturation current

Table 84 Diffusion Layer Parameters, MOSFET Level 13 (Continued)

Name (Alias)	Units	Default	Description
JSW	A/m	0.0	Sidewall bulk junction saturation current
MJ0, (MJ)		0.5	Bulk junction bottom grading coefficient
MJW, (MJSW)		0.33	Bulk junction sidewall grading coefficient
PJ, (PB)	V	0.8	Bulk junction bottom potential
PJW, (PHP)	V	0.8	Bulk junction sidewall potential
RSHM, (RSH)	ohm/sq	0.0	Sheet resistance/square
WDF	m	0.0	Default width of the layer (not used)

The wire model includes poly and metal layer process parameters.

Table 85 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ and MUS mobility parameters.
FEX		0.0	Temperature exponent for the U1 mobility reduction factor.
TCV	V/°K	0.0	Flat-band voltage temperature coefficient.
TREF	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the **TNOM** option, which defaults to 25 °C.

Sensitivity Factors of Model Parameters

To denote the L (channel length) and W (channel width) sensitivity factors of a basic electrical parameter in a transistor, add L and W characters at the start of the name. For example, VFB0 sensitivity factors are LVFB and WVFB. If A0 is a

basic parameter, then LA and WA are the corresponding L and W sensitivity factors of this parameter. Do not use the SCALM option to scale LA and WA.

The Level 13 MOSFET model uses the following equation to obtain this parameter value:

$$A = A0 + LA \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WA \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

Specify LA and WA in units of microns times the units of A0.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the *z* character, followed by the parameter name.

Example

$VFB0 = -0.350v \qquad LVFB = -0.1v\mu$

$WVFB = 0.08v \cdot \mu \qquad Leff = 1 \cdot 10^{-6}m = 1\mu$

$Weff = 2 \cdot 10^{-6}m = 2\mu \qquad LREFeff = 2 \cdot 10^{-6}m = 2\mu$

$WREFeff = 1 \cdot 10^{-5}m = 10\mu$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$zvfb = -0.35v - 0.05v + 0.032v \qquad zvfb = -0.368v$

.MODEL VERSION Changes to BSIM Models

You can use the VERSION parameter in the **.MODEL** statement to move LEVEL 13 BSIM and LEVEL 39 BSIM2 models between versions. Using the

VERSION parameter in a LEVEL 13 **.MODEL** statement results in the following changes to the BSIM model.

Model Version	Effect of VERSION on BSIM model
9007B	Introduced the LEVEL 13 BSIM model: no changes
9007D	Removed the K2 limit
92A	Changed the TOX parameter default from 1000 A to 200 A
92B	Added the K2LIM parameter, which specifies the K2 limit
93A	Introduced the gds constraints
93A.02	Introduced the VERSION parameter
95.1	Fixed the nonprinting TREF and incorrect GMBS problems
96.1	Changed the flatband voltage temperature adjustment

LEVEL 13 Equations

This section lists the LEVEL 13 model equations.

Effective Channel Length and Width

The effective channel length and width for LEVEL 13 depends on the specified model parameters.

If you specify DL0, then:

$$Leff = Lscaled \cdot LMLT - DL0 \text{ Þ} 1e\text{-}6$$

$$LREFeff = LREFscaled \cdot LMLT - DL0 \text{ Þ} 1e\text{-}6$$

Otherwise, if you specify XL or LD:

$$Leff = Lscaled \cdot LMLT + XLscaled - 2 \text{ Þ} LDscaled$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \text{ Þ} LDscaled$$

If you specify DW0, then:

$$Weff = Wscaled \cdot WMLT - DW0 \text{ Þ} 1e\text{-}6$$

$$WREFeff = WREFscaled \cdot WMLT - DW0 \text{ Þ} 1e\text{-}6$$

Otherwise, if you specify XW or WD, then:

$$Weff = Wscaled \cdot WMLT + XWscaled - 2 \text{ Þ} WDscaled$$

$$WREFeff = WREFscaled \cdot WMLT + XWscaled - 2 \text{ Þ} WDscaled$$

IDS Equations

Process-oriented model parameters model the device characteristics. Simulation maps these parameters into model parameters at a specific bias voltage. The ids equations are as follows:

Cutoff Region, vgs ≤ vth

$ids = 0$ (see subthreshold current)

On Region, vgs >vth

For the vds<vdsat triode region:

$$ids = \frac{\beta}{1 + xu1 \cdot vds} \cdot \left[(vgs - vth) \cdot vds - \frac{body}{2} \text{ Þ} vds^2 \right]$$

For the vds≥vdsat saturation region:

$$ids = \frac{\beta}{2 \cdot body \cdot arg} \cdot (vgs - vth)^2$$

The following equations calculate values used in the preceding equation:

$$\beta = ueff \cdot COX \cdot \frac{Weff}{Leff}$$

$$ueff = \frac{uo}{1 + xu0 \cdot (vgs - vth)}$$

$$xu0 = zu0 - zx2u0 \text{ Þ} vsb$$

Simulation uses quadratic interpolation, through three data points to calculate the uo carrier mobility.

$$uo|_{vds = 0} = MUZ - zx2mz \text{ Þ} vsb$$

$$uo|_{vds = VDDM} = zmus - zx2ms \text{ Þ} vsb$$

Simulation also calculates the sensitivity of uo to vds at vds=VDDM, which is zx3ms.

The following equation calculates the body factor:

$$body = 1 + \frac{g \cdot zk1}{2 \cdot (zphi + vsb)^{1/2}}$$

The following equation calculates the g value used in the preceding equation:

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (zphi + vsb)}$$

The following equation calculates the *arg* term in the saturation region:

$$arg = \frac{1}{2} \cdot [1 + vc + (1 + 2 \cdot vc)^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$vc = \frac{xu1 \cdot (vgs - vth)}{body}$$

$$xu1 = zu1 - zx2u1 \cdot vsb + zx3u1 \cdot (vds - VDDM), \quad \text{UPDATE=2}$$

$$xu1 = \frac{zu1 - zx2u1 \cdot vsb + zx3u1 \cdot (vds - VDDM)}{Leff}, \quad \text{UPDATE=0, 1}$$

Threshold Voltage

You can express the threshold voltage as:

$$vth = zvfb + zphi + gamma \cdot (zphi + vsb)^{1/2} - xeta \cdot vds$$

The following equations calculate values used in the preceding equation:

$$gamma = zk1 - zk2 \cdot (zphi + vsb)^{1/2}$$

$$xeta = zeta - zx2e \cdot vsb + zx3e \cdot (vds - VDDM), \quad \text{UPDATE=0, 2}$$

$$xeta = zeta + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM), \quad \text{UPDATE=1}$$

Saturation Voltage (vdsat)

The following equation calculates the saturation voltage in the BSIM Level 13 model:

$$vdsat = \frac{vgs - vth}{body \cdot arg^{1/2}}$$

ids Subthreshold Current

Simulation calculates the isub subthreshold current if zn0 is less than 200:

$$isub = \frac{Ilim \cdot Iexp}{Ilim + Iexp}$$

The following equations calculate values used in the preceding equation:

$$Iexp = \beta_o \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{vgs - vth}{xn \cdot vt}} \cdot \left(1 - e^{-\frac{vds}{vt}}\right)$$

$$Ilim = 4.5 \cdot \beta_o \cdot vt^2 \qquad \beta_o = uo \cdot COX \cdot \frac{Weff}{Leff}$$

$$xn = zn0 - znb \cdot vsb + znd \cdot vds$$

Simulation also adds the isub current to the ids current in the strong inversion.

Resistors and Capacitors Generated with Interconnects

Refer to the wire model table (resistor element) for the model parameters that you used. For an example, see Wire Model for Poly and Metal Layers on page 347.

Resistances:

$$r = RSH \cdot \frac{Leff}{Weff}$$

Capacitances:

$$c = COX \cdot Leff \cdot Weff + 2 \cdot CAPSW \cdot (Leff + Weff)$$

Temperature Effect

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX}$$ UPDATE=0, 1

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX}$$ UPDATE=0, 1

$$uo(t) = uo\left(\frac{t}{tnom}\right)^{BEX}$$ UPDATE=2

$$xu1(t) = xu1 \cdot \left(\frac{t}{tnom}\right)^{FEX}$$

$$zvfb(t) = zvfb - \Delta t \cdot TCV$$

The following equation calculates the Δt value used in the preceding equations:

$$\Delta t = t - tnom$$

Charge-Based Capacitance Model

The LEVEL 13 capacitance model conserves charge and has nonreciprocal attributes. Using charge as the state variable guarantees charge conservation. To obtain the total stored charge in each of the gate, bulk, and channel regions, integrate the distributed charge densities/area of the active region.

The XPART: 40/60 model parameter or 0/100 in the saturation region, partitions the channel charge into drain and source components. This partitioning smoothly changes to 50/50 in the triode region.

- XPART=0 selects 40/60 drain/source charge-partitioning in the saturation region. That is, 40% of the channel charge in the saturation region is at the source, and 60% is at the drain.
- XPART=1 selects 0/100 for drain/source charge-partitioning in the saturation region. That is, 100% of the channel charge in the saturation region is i at the source; there is no drain charge.
- XPART=0.5 selects 50/50 partitioning. Half of the channel charge in the saturation region is at the source, and half is at the drain.

Define: $vtho = zvfb + zphi + zk1 \cdot (zphi + vsb)^{1/2}$

$cap = COX \cdot Leff \cdot Weff \qquad vpof = \frac{vgs - vtho}{body}$

$$argx = \frac{body \cdot vds}{12 \cdot (vgs - vtho - 0.5 \text{ Þ} body \text{ Þ} vds)}$$

If $(vgs - vtho - 0.5 \text{ Þ} body \text{ Þ} vds) \leq 1e\text{-}8$ then:

$$argx = \frac{1}{6}$$

$$argy = \frac{(vgs - vtho)^2 - 0.75 \text{ Þ} body \text{ Þ} (vgs - vtho) \text{ Þ} vds + 0.15 \cdot body^2 \cdot vds^2}{6 \cdot (vgs - vtho - 0.5 \text{ Þ} body \text{ Þ} vds)^3}$$

If $(vgs - vtho - 0.5 \text{ Þ} body \text{ Þ} vds) \leq 1e\text{-}8$ then:

$$argy = \frac{4}{15}$$

Regions Charge Expressions

Accumulation Region, vgs ≤ vtho, vgs ≤ zvfb - vsb

$Qg = cap \cdot (vgs - zvfb + vsb)$

$Qb = -qg \qquad Qs = 0 \qquad Qd = 0$

Subthreshold Region, vgs ≤ vtho, vgs >zvfb - vsb

$$Qg = \frac{cap \cdot zk1}{2} \cdot \left\{ [(zk1)^2 + 4(vgs - zvfb + vsb)]^{1/2} - zk1 \right\}$$

$Qb = -qg \qquad Qs = 0$

50/50 Channel-Charge Partitioning for Drain and Source, XPART=.5

Triode Region, vgs >vtho, vds ≤ vpof

$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \text{ Þ} vds + vds \cdot argx)$

$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$

$Qd = -0.5 \cdot (qg + qb) \qquad Qs = Qd$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{cap}{3} \cdot (vgs - vtho) \qquad Qs = Qd$$

40/60 Channel-Charge Partitioning for Drain and Source, XPART=0

Triode Region, vgs >vtho, vds ≤ vpof

$$Qg = cap \cdot (vgs - xvfb - zphi - 0.5 \text{ Þ} vds + argx \cdot vds)$$

$$Qb = cap \cdot [- vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho - body \text{ Þ} vds) + body \cdot argy \cdot vds])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs> vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{4 \cdot cap}{15} \cdot (vgs - vtho) \qquad Qs = \frac{3}{2} \cdot Qd$$

0/100 Channel-Charge Partitioning for Drain and Source, XPART=1

Triode Region, vgs >vtho, vds ≤ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \text{ Þ} vds + vds \cdot argx)$$

$$Qb = cap \cdot [- vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho) - body \text{ Þ} vds \text{ Þ} (0.75 - 1.5 \text{ Þ} argx)])$$

$$Qs = -(Qg + Qb + Qd)$$

Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = 0 \qquad Qs = -Qg - Qb$$

Preventing Negative Output Conductance

The LEVEL 13 model internally protects against conditions that might cause convergence problems, due to negative output conductance. The constraints imposed are:

$$ND \geq 0 \qquad MUS \geq MUZ + X3MS + VDD(M/2)$$

This model imposes these constraints after adjusting the length and width and setting the *VBS* dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

You might need to qualify BSIM1 models again, if the following occur:

1. Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This does not occur if the device characterization measurement sweeps V_{ds}.
2. Extraction produces parameters that result in negative conductance.
3. This model attempts voltage simulation outside the characterized range of the device.

Calculations Using LEVEL 13 Equations

To verify the equations, start some simple simulation and analysis tests, and check the results with a hand calculator. Check the threshold, vdsat, and ids for a very simple model with many parameters set to zero:

- series resistance, RSH=0.
- Turn off diode current, JS=JSW=IS=0.
- Turn off the LEVEL 13 subthreshold current, n0=200.
- Set the geometry parameters to zero so Leff=L=1u, Weff=W=1u.

This test returns the following TOX value:

$$cox = \frac{2.00000e-3F}{m^2}$$

The test is at vbs=-0.35 so that phi-vbs=1.0. The netlist for this test is located in the following directory:

```
$installdir/demo/hspice/mos/t1.sp
```

Simulation Results

```
ids          vth          vdsat
   1.09907e-02 7.45000e-01 3.69000e+00
```

Calculations at vgs=vds=5, vbs=-0.35

$$phi - vbs = 1$$

$$vth = -0.4 + 0.65 + (0.5 \cdot 1) - (ETA \cdot vds) = 0.75 - (0.001 \cdot vds) = 0.745$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot 1)} = 0.612463$$

$$body = 1 + \frac{g \cdot 0.5}{(2 \cdot 1)} = 1 + 0.25 \cdot g = 1.153116$$

$$vc = 0 \arg = 1$$

$$vdsat = \frac{(vgs - vth)}{body \cdot \sqrt{(arg)}} = \frac{(5 - 0.745)}{body} = 3.69000$$

At vds=VDDM (default VDDM=5), mobility=mus=700

$$ids = cox \cdot \left(\frac{Weff}{Leff}\right) \cdot 700 \cdot \frac{(vgs - vth)^2}{(2 \cdot body \cdot arg)}$$

$$ids = \left(\frac{10 \cdot 700 \cdot 4.255^2}{2 \cdot 1.15311 \cdot 1}\right) \cdot cox = 54953.36 \cdot cox$$

$$ids = 1.09907e-2$$

These calculations agree with the above simulation results.

Compatibility Notes

Model Parameter Naming

The following names are HSPICE-specific: U00, DL0, DW0, PHI0, ETA0, NB0, and ND0. A zero was added to the SPICE names to avoid conflicts with other standard parameter names. For example, you cannot use U0 because it is an alias for UB, the mobility parameter in many other levels. You cannot use DL, because it is an alias for XL, a geometry parameter available in all levels.

You can use DL0 and DW0 with this model, but you should use XL, LD, XW, and WD instead (noting the difference in units).

Watch the units of TOX. It is safest to enter a number greater than one, which simulation always interprets as Angstroms.

To avoid negative gds:

1. Set X3U1, LX3U1, and WX3U1 to zero.
2. Check that

zx3ms>=0, where zx3ms=X3MS with L, W adjustment

3. Check that

zmuz+VDDM · zx3ms<zmus

SPICE/Synopsys Model Parameter Differences

Table 86 compares the UCB BSIM1 and the Synopsys LEVEL 13 model parameters. Units in this table are in brackets. This comparison uses the model parameter name only if it differs from the SPICE name. The model specifies parameter units only if they differ from SPICE units. These aliases are in parentheses. Some parameter aliases match the SPICE names.

An asterisk (*) in front of a UCB SPICE name denotes an incompatibility between the parameter name in the Synopsys Level 13 MOSFET device model and the UCB SPICE name (that is, the parameter alias does not match or the units are different).

Even if the parameter name in this model is not the same as in SPICE, the corresponding L and W sensitivity parameter names might not differ. Table 86

lists the L and W sensitivity parameters only for the few cases where the parameters are different.

Table 86 Comparing Synopsys Model Parameters & UCB SPICE 2/3

UC Berkeley SPICE 2, 3	Synopsys Device Model
VFB [V]	VFB0 (VFB)
PHI [V]	PHI0
K1 [$V^{1/2}$]	same
K2	same
* ETA	ETA0
MUZ [$cm^2/V{\cdot}s$]	same
* DL [µm]	DL0
* DW [µm]	DW0
* U0 [1/V]	U00
* U1 [µ/V]	same
X2MZ [$cm^2/V^2{\cdot}s$]	X2M (X2MZ)
LX2MZ [$\mu m{\cdot}cm^2/V^2{\cdot}s$]	X2M (LX2MZ)
WX2MZ [$\mu m{\cdot}cm^2/V^2{\cdot}s$]	WX2M (WX2MZ)
X2E [1/V]	same
X3E [1/V]	same
X2U0 [$1/V^2$]	same
X2U1 [$\mu m/V^2$]	same
MUS [$cm^2/V{\cdot}s$]	same

Table 86 Comparing Synopsys Model Parameters & UCB SPICE 2/3 (Continued)

UC Berkeley SPICE 2, 3	Synopsys Device Model
LMUS [$\mu m \cdot cm^2/V \cdot s$]	LMS (LMUS)
WMUS [$\mu m \cdot cm^2/V \cdot s$]	WMS (WMUS)
X2MS [$cm^2/V^2 \cdot s$]	same
X3MS [$cm^2/V^2 \cdot s$]	same
X3U1 [$\mu m/V^2$]	same
* TOX [μm]	TOXM[μ] (TOX[m])
* TEMP [°C]	TREF
* VDD [V]	VDDM
CGDO [F/m]	CGDOM (CGDO)
CGSO [F/m]	CGSOM (CGSO)
CGBO [F/m]	CGBOM (CGBO)
XPART	same
N0	same
* NB	NB0
* ND	ND0
RSH [ohm/sq]	RSHM (RSH)
JS [A/m^2]	IJS (JS)
PB [V]	PJ (PB)
MJ	MJ0 (MJ)
* PBSW [V]	PJW (PHP)

Table 86 Comparing Synopsys Model Parameters & UCB SPICE 2/3 (Continued)

UC Berkeley SPICE 2, 3	Synopsys Device Model
MJSW	MJW (MJSW)
CJ [F/m^2]	CJM (CJ)
CJSW [F/m]	CCJW (CJSW)
* WDF [m]	–
* DELL [m]	–

In UCB SPICE, you must specify all BSIM model parameters. The Synopsys model provides default values for the parameters.

Parasitics

ACM >0 invokes parasitic diode models. ACM=0 (default) is SPICE style.

Temperature Compensation

The default TNOM model reference temperature is 25°C, unless you use **.OPTION** SPICE to set the default TNOM value to 27°C. This option also sets some other SPICE compatibility parameters. You set TNOM in an **.OPTION** line in the netlist, and you can always use the TREF model parameter to override it locally (that is, for a model). (The model “reference temperature” means that the model parameters were extracted at and are valid at that temperature.

UCB SPICE does not use TNOM (default 27°C) for the BSIM models. Instead, you must specify the TEMP model parameter as both the model reference temperature and the analysis temperature. Analysis at TEMP applies only to thermally-activated exponentials in the model equations. You cannot adjust model parameter values when you use TEMP. Simulation assumes that you extracted the model parameters at TEMP, because TEMP is both the reference and the analysis temperature.

In contrast to UCB SPICE’s BSIM, the Synopsys LEVEL 13 model does provide for temperature analysis. The default analysis temperature is 25°C (and 27°C in UCB SPICE for all model levels except for BSIM as explained in the

previous paragraph). Use a .TEMP statement in the netlist to change the analysis temperature.

The LEVEL 13 model provides two temperature coefficients: TCV and BEX. The following equation adjusts the threshold voltage:

$$vth(t) = vth - TCV \cdot (t - tnom)$$

This model includes two implementations of the BEX factor. To select a BEX version, use the UPDATE parameter, described in the next section. The mobility in BSIM is a combination of five quantities: MUZ, zmus, z3ms, zx2mz, and zx2ms.

BEX Usage

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx3ms(t) = zx3ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2mz(t) = zx2mz \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$zx2ms(t) = zx2ms \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

This is equivalent to multiplying the final mobility by the factor:

$$\left(\frac{t}{tnom}\right)^{BEX}$$

UPDATE Parameter

The UPDATE parameter selects between variations of the BSIM equations. UPDATE=0 (default) is consistent with UCB SPICE3. UPDATE=3 also is consistent with UCB SPICE3 and BEX usage.

Parameter	Description
UPDATE=0	UCB compatible, previous BEX usage
UPDATE=1	Special X2E equation, previous BEX usage
UPDATE=2	Remove 1/Leff in U1 equation, present BEX usage
UPDATE=3	UCB compatible, present BEX usage

Explanations

The normal X2E equation is:

$$xeta = zeta - (zx2e \cdot vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation for UPDATE=1 only, is:

$$xeta = zera + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation was developed to match a parameter extraction program. If you use a parameter extraction program, check the equations carefully.

The original U1 equation divides by Leff in microns:

$$xu1 = \frac{(zu1 - (zx2u1 \cdot vsb) + zx3u1 \cdot (vds - VDDM))}{Leff}$$

This is one of the few places where Leff explicitly enters into the BSIM equations; usually, the L-adjustment model parameters (such as LU1) handles the Leff variation.

Physically xu1 should decrease as 1/Leff at long channels, but when dealing with short-channel devices, you can turn off this variation. Set UPDATE=2 to remove the 1/Leff factor in the xu1 equation.

UPDATE=2 introduces the present BEX usage as the 1/Leff removal ability. UPDATE=3 provides the present BEX using the previous xu1 equation.

IDS and VGS Curves for PMOS and NMOS

The netlists for the IDS and VGS curves for PMOS and NMOS are located in the following directory:

`$installdir/demo/hspice/mos/ml13iv.sp`

The `ml13iv.sp` file contains examples of the following model parameter and curve descriptions:

- Two Types of Model Parameter Formats Used
- VGS Curves
- GM Test
- GM B CVN7 5 37 0
- .PROCESS PC Filename=M57R
- N-channel Devices
- First Model Parameter Format
- PMOS Model
- Wire Model for Poly and Metal Layers
- Second Model Parameter Format
- N+ Diffusion Layer
- PMOS Model
- Wire Model for Poly and Metal Layers

LEVEL 28 Modified BSIM Model

This section lists the LEVEL 28 parameters and equations for the modified BSIM model.

LEVEL 28 Features

The following are the significant features of the LEVEL 28 model.

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by the source and drain

- Nonuniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of the electrical parameters

LEVEL 28 Model Parameters

MOSFET Level 28 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 28.

Table 87 Transistor Process Parameters

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. Set this parameter to 28 for this model.
B1		0.0	Lower vdsat transition point
LB1	µm	0.0	Length sensitivity
WB1	µm	0.0	Width sensitivity
B2		1	Upper vdsat transition point
LB2	µm	0.0	Length sensitivity
WB2	µm	0.0	Width sensitivity
CGBO	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDO	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSO	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
ETA0		0.0	Linear vds threshold coefficient
LETA	µm	0.0	Length sensitivity

Table 87 Transistor Process Parameters (Continued)

Name (Alias)	Units	Default	Description
WETA	μm	0.0	Width sensitivity
ETAMN		0.0	Minimum linear vds threshold coefficient
LETAMN	μm	0.0	Length sensitivity
WETAMN	μm	0.0	Width sensitivity
GAMMN	$V^{1/2}$	0.0	Minimum root-vsb threshold coefficient
LGAMN	$V^{1/2}$·μm	0.0	Length sensitivity
WGAMN	$V^{1/2}$·μm	0.0	Width sensitivity
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
LK1	$V^{1/2}$·μm	0.0	Length sensitivity
WK1	$V^{1/2}$·μm	0.0	Width sensitivity
K2		0.0	Linear vsb threshold coefficient
LK2	μm	0.0	Length sensitivity
WK2	μm	0.0	Width sensitivity
MUZ	$cm^2/V·s$	600	Low drain field first order mobility
LMUZ	μm·$cm^2/V·s$	0.0	Length sensitivity
WMUZ	μm·$cm^{2/}V·s$	0.0	Width sensitivity
N0		200	Low field weak inversion gate drive coefficient (value of 200 for N0 disables the weak inversion calculation)
LN0	μm	0.0	Length sensitivity

Table 87 Transistor Process Parameters (Continued)

Name (Alias)	Units	Default	Description
WN0	μm	0.0	Width sensitivity
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
LNB	μm	0.0	Length sensitivity
WNB	μm	0.0	Width sensitivity
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
LND	μm	0.0	Length sensitivity
WND	μm	0.0	Width sensitivity
PHI0	V	0.7	Two times the Fermi potential
LPHI	V·μm	0.0	Length sensitivity
WPHI	V·μm	0.0	Width sensitivity
TOXM (TOX)	μm (m)	0.02	Gate oxide thickness (if TOXM or TOX >1, uses Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
LU0	μm/V	0.0	Length sensitivity
WU0	μm/V	0.0	Width sensitivity
U1	1/V	0.0	Drain field mobility reduction factor
LU1	μm/V	0.0	Length sensitivity
WU1	μm/V	0.0	Width sensitivity
VDDM	V	5.0	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage

Table 87 Transistor Process Parameters (Continued)

Name (Alias)	Units	Default	Description
LVFB	V·μm	0.0	Length sensitivity
WVFB	V·μm	0.0	Width sensitivity
WFAC		4	Weak inversion factor
LWFAC	μm	0.0	Length sensitivity
WWFAC	μm	0.0	Width sensitivity
WFACU		0.0	Second weak inversion factor
LWFACU	μm	0.0	Length sensitivity
WWFACU	μm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
LX2E	μm/V	0.0	Length sensitivity
WX2E	μm/V	0.0	Width sensitivity
X2M (X2MZ)	$cm^2/V^2 \cdot s$	0.0	Vsb correction to the low field first order mobility
LX2M (LX2MZ)	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X2U0	$1/V^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
LX2U0	$\mu m/V^2$	0.0	Length sensitivity
WX2U0	$\mu m/V^2$	0.0	Width sensitivity
X2U1	$\mu m/V^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
LX2U1	$\mu m^2/V^2$	0.0	Length sensitivity

Table 87 Transistor Process Parameters (Continued)

Name (Alias)	Units	Default	Description
WX2U1	$\mu m^2/V^2$	0.0	Width sensitivity
X33M	$cm^2/V^2 \cdot s$	0.0	Gate field reduction of X3MS
LX33M	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX33M	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X3E	1/V	0.0	Vds correction to the linear vds threshold coefficient
LX3E	$\mu m/V$	0.0	Length sensitivity
WX3E	$\mu m/V$	0.0	Width sensitivity
X3MS	$cm^2/V^2 \cdot s$	5.0	Vds correction for the high-drain field mobility
LX3MS	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Length sensitivity
WX3MS	$\mu m \cdot cm^2/V^2 \cdot s$	0.0	Width sensitivity
X3U1	$1/V^2$	0.0	Vds reduction to the drain field mobility reduction factor
LX3U1	$\mu m/V^2$	0.0	Length sensitivity
WX3U1	$\mu m/V^2$	0.0	Width sensitivity
XPART		1.0	Selects the coefficient for sharing the gate capacitance charge

Notes:

1. When you read parameter names, be careful about the difference in appearance between the capital letter O and the number zero (0).
2. Use NMOS conventions to specify all LEVEL 28 parameters, even for PMOS—for example, ETA0 = 0.02, not ETA0 = -0.02.

3. You can use the WL-product sensitivity parameter for any parameter with an L and W sensitivity. Replace the leading “L” of the L sensitivity parameter name with a “P”.

Table 88 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ, X2M, X3MS, and X33M mobility parameters
FEX		0.0	Temperature exponent for the U1 mobility reduction factor
TCV	V/°K	0.0	Flat-band voltage temperature coefficient

Sensitivity Factors of Model Parameters

For transistors, drop the 0 from the end of the parameter name, and add one of the following product sensitivity factors for a basic electrical parameter:

- L (channel length)
- W (channel width)
- WL (width and length)

For example, the VFB0 sensitivity factors are LVFB, WVFB, and PVFB. If A0 is a basic parameter, LA, WA and PA are the corresponding sensitivity factors for this parameter (you cannot use the SCALM option to scale LA, WA, and PA). Then the model uses the following general formula to obtain the parameter value.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the z character, followed by the parameter name.

$$za = A0 + LA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] + WA \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

$$+ PA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff}\right] \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff}\right]$$

Specify LA and WA in units of microns times the units of A0. Specify PA in units of square microns times the units of A0.

If you set LREF or WREF=0, you effectively set the parameter value to infinity. This is the default.

Example

$VFB0 = -0.350v$ $LVFB = -0.1v\mu$

$WVFB = 0.08v \cdot \mu$

$Leff = 1 \cdot 10^{-6}m = 1\mu$ $Weff = 2 \cdot 10^{-6}m = 2\mu$

$LREFeff = 2 \cdot 10^{-6}m = 2\mu$ $WREFeff = 1 \cdot 10^{-5}m = 10\mu$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff}\right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff}\right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu}\right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu}\right)$$

$zvfb = -0.35v - 0.05v + 0.032v$ $zvfb = -0.368v$

LEVEL 28 Model Equations

The LEVEL 28 model equations follow.

Effective Channel Length and Width

The effective channel length and width for LEVEL 28 is consistent with the LEVEL 3 model. L, W, and the M multiplier are from the **.MODEL** statement in the netlist. SCALE and SCALM are options. If you do not specify any scaling options or multipliers, then:

Leff = L+XL-2·LD Weff = W+XW-2·WD

Note: If you specify LDAC and WDAC in the **.MODEL** statement,
Leff=L+XL-2·LDAC Weff=W+XW-2·WDAC

Lscaled = L· SCALE
Wscaled = W· SCALE
XLscaled = XL· SCALM
LDscaled = LD· SCALM

XWscaled = XW· SCALM
WDscaled = WD· SCALM
Leff = Lscaled· LMLT+XLscaled-2· LDscaled
LREFeff = LREFscaled· LMLT+XLREFscaled-2· LDscaled
Weff = M· (Wscaled· WMLT+XWREFscaled-2· WDscaled)
WREFeff = M· (WREFscaled· WMLT+XWscaled-2· WDscaled)

Threshold Voltage

Effective model parameter values for the threshold voltage, after you adjust the device size, are zphi, zvfb, zk1, zk2, zeta, zx2e, zx3e, zgammn, and zetamn. Simulation calculates these values from the PHI0, VFB0, K1, K2, ETA0, X2E, X3E, GAMMN, and ETAMN model parameters, and from their respective length and width sensitivity parameters.

xbs=(zphi-vbs)1/2

xeta=zeta+zx2e·vbs+zx3e·vds

vth=zvfb + zphi + zk1·xbs - zk2·xbs2-xeta·vds

This equation is quadratic in xbs and vds. It is joined to linear equations at d(vth)/d(xbs) = zgammn and at d(vth)/d(vds) = -zetamn, which prevents the quadratics from going in the wrong direction.

Both gammn and etamn default to zero, and typically do not affect behavior in the normal operating region.

Effective Mobility

The effective model parameter values for mobility, after you adjust the device size, are zmuz, zx2m, zx3m, zx33m, zu0, and zx2u0. Simulation calculates these values from the MUZ, X2M, X3m, X33M, U00, and X2U0 model parameters, and from their respective length and width sensitivity parameters.

$$v_{gst} = v_{gs} - v_{th} \qquad m_{eff} = (zmuz + zx2m \cdot v_{bs})$$

$$cx3ms = \frac{zx3ms}{(muz + zx33m \cdot v_{gst})}$$

$$\cdot (1 + cx3ms \cdot (VDDM + v_{ds} - (VDDM \cdot VDDM + v_{ds} \cdot v_{ds})^{1/2}))$$

$$xu0 = zu0 + zx2u0 \cdot v_{bs}$$

$$u_{eff} = \frac{m_{eff}}{(1 + xu0 \cdot v_{gst})} \qquad beta = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Saturation Voltage (vdsat)

The effective model parameter values for the saturation voltage, after you adjust the device size, are zu1, zx2u1, and zx3u1. Simulation calculates these values from the U1, X2U1, and X3U1 model parameters, and from their length and width sensitivity parameters.

$$xbs = (zphi - v_{bs})^{1/2} \qquad g = 1 - \frac{1}{(1.744 + 0.8364 \cdot xbs^2)}$$

$$body = \frac{1 + g \cdot zk1}{(2 \cdot xbs)} \qquad xu1 = zu1 + vbs \cdot zx2u1$$

$$rx = (body^2 + zu1 \cdot 2 \cdot body \cdot v_{gst} + zx3u1 \cdot 4 \cdot v_{gst}^2)^{1/2}$$

$$v_{dsat} = \frac{2 \cdot v_{gst}}{(body + rx)}$$

This vds value generates the partial derivative of:

$$f(v_{ds}, v_{gst}, v_{bs}) = (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (xu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

In the preceding equation, vds=zero.

Transition Points

The effective model parameter values for the transition points, after you adjust the device size, are zb1 and zb2. Simulation calculates these values from the B1 and B2 model parameters, and from their respective length and width sensitivity parameters.

$$v1 = v_{dsat} - zb1 \cdot \frac{v_{dsat}}{1 + v_{dsat}} \qquad v2 = v_{dsat} + zb2 \cdot v_{gst}$$

Strong Inversion Current

For vds < v1:

$$I_{ds} = beta \cdot (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (zu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

The vds derivative varies approximately linearly between v1 and v2.

For vds>v2, ids is a function of beta and vgst only. If zb1 and zb2 are both positive, their main effect is to increase the saturation current.

Weak Inversion Current

The effective model parameter values for weak inversion current, after you adjust the device size, are zn0, znb, znd, zwfac, and zwfacu. Simulation calculates these values from the N0, ND0, NB0, WFAC, and WFACU model parameters, and from their respective length and width sensitivity parameters.

Simulation calculates the weak inversion current when zn0 is less than 200, and adds it to the strong inversion current:

$$Itotal = Istrong + Iweak \cdot \left(1 - exp\left(\frac{-v_{ds}}{vtherm}\right)\right)$$

In deep subthreshold:

$$xn = zn0 + znb \cdot v_{bs} + znd \cdot v_{ds}$$

$$vtherm = \frac{KT}{Q} \qquad xweak = \frac{(v_{gs} - vt)}{(xn \cdot vtherm)}$$

$$Iweak = const \cdot exp(xweak)$$

zwfac and zwfacu control the modification of this formula near the threshold. Just above threshold, the device is in saturation:

$$Istrong = const \cdot xweak^2$$

Iweak needs an xweak^2 term to cancel the kink in gm at the threshold. Then Iweak goes to zero for xweak>A0, which is at a small voltage above the threshold. Iweak has four regions:

(1) xweak < -zwfac+A0

$$Iweak = const \cdot exp(xweak)$$

(2) -zwfac+A0 < xweak < 0

$$Iweak = const \cdot exp(xweak - const \cdot wf)$$

In the preceding equation, wf is the integral with respect to the xweak value of:

$$dwf = \frac{(xweak + zwfac - A0)^2}{[(1 + xweak + zwfac - A0)(1 + zwfacu \cdot (xweak + zwfac - A0))]}$$

(3) 0 < xweak < A0

$$Iweak = (\text{same formula as in region 2}) - const \cdot xweak^2$$

(4) A0 < xweak

$$Iweak = 0$$

A0, and the constants in the preceding equations, are not model parameters. Continuity conditions, at the boundaries between regions, uniquely determine these constants.

LEVEL 39 BSIM2 Model

BSIM2 (Berkeley Short-Channel IGFET Model 2) is the LEVEL 39 MOSFET model. The Synopsys implementation of this model is based on Berkeley SPICE 3E2.

To provide input to the Level 39 device model, assign the model parameters as for other device models. You can use a tabular model entry without model parameter names in BSIM1, but *not* in BSIM2.

LEVEL 39 Model Parameters

MOSFET Level 39 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 39.

This section lists the BSIM2 parameters, their units, their defaults (if any) in the Level 39 MOSFET model, and their descriptions. Table 89 lists 47 BSIM2-specific parameters. The Synopsys model does not use three of the parameters (TEMP, DELL, and DFW). The width and length sensitivity parameters are associated with the remaining parameters, except the first six (TOX, VDD, VGG, VBB, DL, and DW). So the total parameter count is 120. (Unlike Berkeley SPICE, the Synopsys Level 39 MOSFET model has L and W

sensitivity for MU0). This count does not include the *generic* MOS parameters or the WL-product sensitivity parameters, which are Synopsys enhancements.

Table 89 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
TOX	m	0.02	Gate oxide thickness (assumes that TOX>1 is in Angstroms)
TEMP	C	-	Not used in Level 39 (see Compatibility Notes on page 366)
VDD	V	5	Drain supply voltage (NMOS convention)
VGG	V	5	Gate supply voltage (NMOS convention)
VBB	V	-5	Body supply voltage (NMOS convention)
DL	m	0	Channel length reduction
DW	m	0	Channel width reduction
VGHIGH	V	0	Upper bound of the weak-strong inversion transition region
VGLOW	V	0	Lower bound of the weak-strong inversion transition region
VFB	V	-0.3	Flat band voltage
PHI	V	0.8	Surface potential
K1	V^{-1}	0.5	Body effect coefficient
K2	-	0	Second-order body effect coefficient (for nonuniform channel doping)
ETA0	-	0	Drain-induced barrier lowering coefficient
ETAB	V^{-1}	0	Sensitivity of the drain-induced barrier lowering coefficient to V_{bs}

Table 89 BSIM2 Model Parameters (Continued)

Name (Alias)	Units	Default	Description
MU0	$cm^2/V{\cdot}s$	400	Low-field mobility
MU0B	$cm^2/V^2{\cdot}s$	0	Sensitivity of low-field mobility to V_{bs}
MUS0	$cm^2/V{\cdot}s$	600	High-drain field mobility
MUSB	$cm^2/V^2{\cdot}s$	0	Sensitivity of the high-drain field mobility to V_{bs}
MU20	-	0	Empirical parameter for the output resistance
MU2B	V^{-1}	0	Sensitivity of the empirical parameter to V_{bs}
MU2G	V^{-1}	0	Sensitivity of the empirical parameter to V_{gs}
MU30	$cm^2/V^2{\cdot}s$	0	Empirical parameter for the output resistance
MU3B	$cm^2/V^3{\cdot}s$	0	Sensitivity of the empirical parameter to V_{bs}
MU3G	$cm^2/V^3{\cdot}s$	0	Sensitivity of the empirical parameter to V_{gs}
MU40	$cm^2/V^3{\cdot}s$	0	Empirical parameter for the output resistance
MU4B	$cm^2/V^4{\cdot}s$	0	Sensitivity of the empirical parameter to V_{bs}
MU4G	$cm^2/V^4{\cdot}s$	0	Sensitivity of the empirical parameter to V_{gs}
UA0	V^{-1}	0	First-order vertical-field mobility reduction factor
UAB	V^{-2}	0	Sensitivity of the first-order factor to V_{bs}
UB0	V^{-2}	0	Second-order vertical-field mobility reduction factor
UBB	V^{-3}	0	Sensitivity of the second-order factor to V_{bs}
U10	V^{-1}	0	High-drain field (velocity saturation) mobility reduction factor

Table 89 BSIM2 Model Parameters (Continued)

Name (Alias)	Units	Default	Description
U1B	V^{-2}	0	Sensitivity of the mobility reduction factor to V_{bs}
U1D	V^{-2}	0	Sensitivity of the mobility reduction factor to V_{ds}
N0	-	0.5	Subthreshold swing coefficient
NB	$V^{1/2}$	0	Sensitivity of the subthreshold swing to V_{bs}
ND	V^{-1}	0	Sensitivity of the subthreshold swing to V_{ds}
VOF0	-	0	Threshold offset (normalized to NKT/q) for the subthreshold
VOFB	V^{-1}	0	Sensitivity of the offset to V_{bs}
VOFD	V^{-1}	0	Sensitivity of the offset to V_{ds}
AI0	-	0	Impact ionization coefficient
AIB	V^{-1}	0	Sensitivity of the impact ionization coefficient to V_{bs}
BI0	V	0	Impact ionization exponent
BIB	-	0	Sensitivity of the impact ionization exponent to V_{bs}
DELL	m	-	Length reduction of the source drain diffusion (not used in the Level 39 MOSFET model)
WDF	m	-	Default width (not used in the Level 39 MOSFET model); use “**.OPTION** DEFW=#” in the netlist instead

Specify all BSIM2 parameters according to the NMOS convention, even for a PMOS model. Examples: VDD=5, not -5; VBB=-5, not 5; and ETA0=0.02, not -0.02. See Compatibility Notes on page 366.

The Level 39 MOSFET model also includes the JSW[A/m] source/drain bulk diode sidewall reverse saturation current density.

Other Device Model Parameters that Affect BSIM2

You must specify the following MOSFET model parameters before you can use some Synopsys enhancements, such as

- LDD-compatible parasitics.
- Adjusts the model parameter geometry, relative to a reference device.
- Impact ionization modeling with bulk-source current partitioning.
- Element temperature adjustment of the key model parameters.

This is a partial list. For complete information, see the following:

- Calculating Effective Length and Width for AC Gate Capacitance on page 95
- Drain and Source Resistance Model Parameters on page 42
- Impact Ionization Model Parameters on page 61
- Temperature Parameters and Equations on page 98

.MODEL VERSION Changes to BSIM2 Models on page 368 describes how the VERSION parameter in the **.MODEL** statement changes the BSIM2 model, depending on the model version number.

LEVEL 39 Model Equations

In the following expressions, model parameters are in all upper case Roman. These expressions assume that you have already adjusted all model parameters for geometry, and that you have already adjusted parameters without a trailing 0 for the bias as appropriate. The exceptions are U1 and N for which the following equations explicitly calculate the bias dependences:

Threshold voltage, V_{th}:

$$V_{th} = V_{bi} + K1\sqrt{PHI - V_{bs}} - K2(PHI - V_{bs}) - ETA \cdot V_{ds}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$V_{bi} = VFB + PHI$$

Strong inversion ($V_{gs} > V_{th} + VGHIGH$):

Linear region ($V_{ds} < V_{dsat}$) drain-source current I_{DS}:

$$I_{DS} = \frac{\beta'\left(V_{gs} - V_{th} - \frac{a}{2}V_{ds}\right)V_{ds}}{1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2 + U1 \cdot V_{ds}}$$

The following equations calculate values used in the preceding equation:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{a\sqrt{K}},$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2},$$

$$V_c = \frac{U_{1S}(V_{gs} - V_{th})}{a[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]},$$

$$U_{1S} = U10 + U1B \cdot V_{bs},$$

$$U1 = U_{1S}\left[1 - \Theta(V_{dsat} - V_{ds})\frac{U1D(V_{ds} - V_{dsat})^2}{V_{dsat}^2}\right]$$

In the preceding equations, $\Theta(x)$ is the usual unit step function:

$$\beta' = \beta_0 + \beta_1 \tanh\left(MU2\frac{V_{ds}}{V_{dsat}}\right) + \beta_3 V_{ds} - \beta_4 V_{ds}^2$$

$$\beta_0 = \frac{W_{eff}}{L_{eff}} MU \cdot C_{ox},$$

$$\beta_1 = \beta_S - (\beta_0 + \beta_3 VDD - \beta_4 VDD^2),$$

$$\beta_i = \frac{W_{eff}}{L_{eff}} MUi \cdot C_{ox},\ i = S, 3, 4, \qquad a = 1 + \frac{gK1}{2\sqrt{PHI - V_{bs}}},$$

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - V_{bs})}$$

Saturation (V_{ds} > V_{dsat}) drain-source current, I_{DS}:

$$I_{DS} = \frac{\beta'(V_{gs} - V_{th})^2}{2aK[1 + UA(V_{gs}-V_{th}) + UB(V_{gs}-V_{th})^2]} \cdot (1 + f)$$

In the preceding equation, the *f* impact ionization term is:

$$f = AI \cdot e^{\frac{-BI}{V_{ds} - V_{dsat}}}.$$

Weak Inversion (V_{gs}<V_{th}+VGLOW; [VGLOW<0]):

Subthreshold drain-source current, I_{ds}:

$$I_{DS} = \beta' \cdot V_{tm}^2 \cdot exp\left(\frac{V_{gs} - V_{th}}{N \cdot V_{tm}} + VOFF\right) \cdot \left[1 - exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right] \cdot (1 + f)$$

The following equations calculate the V_{tm} and N values used in the preceding equation:

$$V_{tm} = \frac{kT}{q} \text{ and } N = N0 + \frac{NB}{\sqrt{PHI - V_{bs}}} + ND \cdot V_{ds}$$

Strong inversion-to-weak inversion transition region (V_{th} +VGLOW≤ V_{gs} ≤*th* +VGHIGH):

$$V_{geff}(V_{gst}) = \sum_{j=0}^{3} C_j V_{gst}^j$$

The preceding equation replaces V_{gst} = V_{gs} - V_{th} in the linear or saturation drain currents, based on V_{dsat} (V_{geff}).

At the lower boundary (V_{gs}-V_{th}=VGLOW), the saturation equation is valid for all V_{ds} (that is, V_{dsat} (V_{geff}(VGLOW)) ≈ 0) to allow a match to the above subthreshold equation.

To internally determine the Cj coefficients of the V_{geff} cubic spline, the I_{DS} and dI_{ds}/dV_{gs} conditions must both be continuous at the
V_{gs} = V_{th} + VGLOW and V_{gs} = V_{th} + VGHIGH boundaries.

Effective Length and Width

If DL is nonzero:

$$L_{eff} = L_{scaled} \cdot LMLT - DL$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL$$

Otherwise:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

If DW is nonzero:

$$W_{eff} = (W_{scaled} \cdot WMLT - DW) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT - DW) \cdot M$$

Otherwise:

$$W_{eff} = (W_{scaled} \cdot WMLT + XW - 2 \cdot WD_{scaled}) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \cdot M$$

Geometry and Bias of Model Parameters

Most of the BSIM2 parameters include width and length sensitivity parameters. You can also specify Synopsys-proprietary WL-product sensitivity parameters. If P is a parameter, then its associated width, length, and WL-product sensitivity parameters are WP, LP, and PP.

The value of the P’ parameter, adjusted for width, length, and WL-product, is:

$$P' = P + WP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) + LP \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right) + PP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}}\right) \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}}\right)$$

Berkeley SPICE does not use the WREF and LREF terms. They are effectively infinite, which is the default in the Level 39 MOSFET model.

The following BSIM2 parameters do not have associated geometry-sensitivity parameters:

TOX
TEMP (not used)
VDD
VGG
VBB
DL
DW

BSIM2 parameters ending in 0 are valid at zero bias, and they have associated bias sensitivities, listed in the BSIM2 parameter table.

If PB, PD, and PG are the geometry-adjusted v_{bs}-, v_{ds}-, and v_{gs}- sensitivity parameters, and if they are associated with the P0 geometry-adjusted zero-bias parameter, then the following equation calculates the P bias-dependent parameter:

$$P = P0 + PB \cdot V_{bs} + PD \cdot V_{ds} + PG \cdot V_{gs}$$

The exceptions are the U1 velocity saturation factor and the N subthreshold swing coefficient. Modeling Guidelines, Removing Mathematical Anomalies on page 373 shows expressions for their bias dependences.

Compatibility Notes

SPICE3 Flag

If you specify the SPICE3=0 (default) model parameter, certain Synopsys corrections to the BSIM2 equations are effective. If you set the SPICE3 value to 1, the equations are as faithful as possible to the BSIM2 equations for SPICE3E2. Even in this mode, certain numerical problems have been addressed and should not normally be noticeable.

Temperature

The default model reference temperature (TNOM) is 25°C in the Level 39 MOSFET model, unless you set **.OPTION** SPICE, which sets the TNOM default to 27° C. This option also sets some other SPICE compatibility parameters. In the Level 39 model, you set TNOM in an **.OPTION** line in the netlist; to override this locally (that is, for a model), use the TREF model

parameter. (“Reference temperature” means that the model parameters were extracted at, and are therefore valid at, that temperature.)

UCB SPICE 3 does not use TNOM (default 27° C) for the BSIM models. Instead, you must specify the TEMP model parameter as both the model reference temperature and the analysis temperature. Analysis at TEMP applies only to thermally-activated exponentials in the model equations. You cannot adjust the model parameter values if you use TEMP. Simulation assumes that you extracted the model parameters at TEMP, because TEMP is both the reference and analysis temperature.

For model levels *other than* 4 (BSIM1) and 5 (BSIM2) in UCB SPICE3, simulation adjusts the key model parameters for the difference between TEMP (default 27°C) and TNOM. To specify TEMP in the netlist, use **.TEMP #** as in the Level 39 MOSFET model.

In contrast to UCB SPICE’s BSIM models, the Synopsys Level 39 MOSFET model does provide for temperature analysis. The default analysis temperature is 25°C in the Level 39 model. Set **.TEMP #** in your netlist to change the analysis temperature (you cannot use TEMP as a model parameter). The Level 39 MOSFET model adjusts the temperature of the key model parameters as explained in Temperature Effect on page 336.

Parasitics

ACM > 0 invokes the MOS source-drain parasitics in the Level 39 MOSFET device model. ACM=0 (default) is SPICE style. See Synopsys Device Model Enhancements on page 371.

Selecting Gate Capacitance

CAPOP=39 selects the BSIM2 charge-conserving capacitance model as shipped with Berkeley SPICE 3E2. This is the default selection if you set SPICE3=1.

- XPART (charge-sharing flag) is currently not a BSIM2 model parameter, despite its specification in the sample BSIM2 input decks shipped with Berkeley SPICE 3E. It appears that its use in SPICE 3E was as a printback debug aid.
- Saturation charge sharing appears to be fixed at 60/40 (S/D) in the BSIM2 capacitance model. For the charge equations, see Charge-based Gate Capacitance Model (CAPOP=39) on page 369. See also Modeling Guidelines, Removing Mathematical Anomalies on page 373.

You can choose other CAPOP values. CAPOP=13 (recommended) selects the BSIM1-based charge-conserving capacitance model for the MOSFET LEVEL 13 (BSIM1) or LEVEL 28 (modified BSIM1) device models. This option is the default selection if SPICE3=0. If you use this capacitance model, you can use the XPART or XQC model parameters to adjust charge sharing. See LEVEL 13 BSIM Model on page 324 for more information.

Unused Parameters

The Level 39 MOSFET model does not use the DELL (S/D diode length reduction) and WDF (default device width) SPICE model parameters. SPICE 3E does not use the DELL function. You can specify a default width in the Level 39 MOSFET model, on the **.OPTION** line as DEFW (which defaults to 100µ).

.MODEL VERSION Changes to BSIM2 Models

The Level 39 MOSFET model provides a VERSION parameter to the **.MODEL** statement, which lets you move LEVEL 13 BSIM and LEVEL 39 BSIM2 models between device model versions. Use the VERSION parameter in a LEVEL 13 **.MODEL** statement. Table 90 lists the changes in the BSIM model.

Table 90 BSIM2 Model Features by Version Number

Model Version	Effect of VERSION on BSIM2 Model
92A	LEVEL 39 BSIM2 model introduced: no changes
92B	No changes
93A	Introduced gds constraints, fixed a defect in the WMU3B parameter, and introduced a defect in the MU4 parameter
93A.02	Introduced the VERSION parameter, and fixed an MU4 parameter defect
95.1	Fixed defects that caused PMUSB, LDAC, and WDAC parameter problems, fixed the GMBS defect if you used gds constraints
96.1	Limited ETA + ETAB · vb5≥0

Preventing Negative Output Conductance

The Level 39 MOSFET model internally protects against conditions in the LEVEL 13 model that cause convergence problems due to negative output conductance. This model imposes the following constraints:

$MU2 \geq 0 \quad ND \geq 0 \quad AI \geq 0$

Simulation imposes these constraints after adjusting the length and width and setting the *VBS* dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

Consequently, you might need to requalify the BSIM2 models in the following situations:

1. Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds}. This does not occur if the device characterization measurement sweeps V_{ds}.
2. The extraction technique produces parameters that result in negative conductance.
3. This model simulates the voltage outside the device's characterized range.

Charge-based Gate Capacitance Model (CAPOP=39)

The BSIM2 gate capacitance model conserves charge and has non-reciprocal attributes. Using charges as state variables guarantees charge conservation. Charge partitioning is fixed at 60/40 (S/D) in saturation and is 50/50 in the linear region. $Q_s = -(Q_g+Q_d+Q_b)$ in all regions.

Accumulation region (V_{gs}<V_{bs}+VFB):

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - VFB)$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Subthreshold region (V_{bs} + VFB<V_{gs}<V_{th} + VGLOW):

$$Q_g = C_{ox}W_{eff} \cdot L_{eff}(V_{gs} - V_{bs} - VFB)$$

$$\cdot \left[1 - \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} + \frac{1}{3}\left\{ \frac{V_{gs} - V_{bs} - VFB}{V_{gs} - V_{bs} - VFB - V_{gst}} \right\}^2 \right]$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Saturation region (V_{ds} > V_{dsat}):

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} + Q_{bulk}$$

The following equations calculate values used in the preceding equation:

$$Q_{bulk} = \frac{1}{3}C_{ox}W_{eff} \cdot L_{eff}[V_{th} - V_{bs} - VFB]$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{4}{10} \cdot \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} = \left(-\frac{4}{15}\right)C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

Linear region $(V_{ds} < V_{dsat})$:

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} \cdot \left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} \right] + Q_{bulk}$$

$$Q_b = -Q_{bulk} \qquad Q_d = -\frac{1}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

$$\cdot \left[\frac{3\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} + \frac{\frac{V_{ds}}{V_{dsat}}\left(1 - \frac{V_{ds}}{V_{dsat}}\right) + 0.2\left(\frac{V_{ds}}{V_{dsat}}\right)^2}{\left(2 - \frac{V_{ds}}{V_{dsat}}\right)^2} \right] + Q_{bulk}$$

Synopsys Device Model Enhancements

In the following expressions, model parameters are in all upper case Roman. Simulation assumes that you have already adjusted all model parameters without a trailing 0 for both geometry and bias as appropriate.

Temperature Effects

LEVEL=39 enforces TLEV=1. You cannot currently use any other TLEV value. The following equation adjusts the threshold voltage for LEVEL 39 TLEV=1:

$$V_{th}(T) = V_{bi}(T) + K1 \cdot \sqrt{\phi(T) - V_{bs}} - K2 \cdot (\phi(T) - V_{bs}) - ETA \cdot V_{ds}$$

The following equations calculate values used in the preceding equation:

$$V_{bi}(T) = V_{to}(T) - K1 \cdot \sqrt{\phi(T)} + K2 \cdot \phi(T)$$

$$V_{to}(T) = V_{to} - TCV \cdot (T - T_{nom}),$$

In the preceding equations, the nominal-temperature, zero-bias threshold voltage is:

$$V_{to} = V_{bi} + K1 \cdot \sqrt{PHI} - K2 \cdot PHI$$
$$= VFB + PHI + K1 \cdot \sqrt{PHI} - K2 \cdot PHI,$$

Simulation calculates $\phi(T)$ according to the specified TLEVC value.

The following equation adjusts the mobility:

$$\mu(T) = \mu(T_{nom}) \cdot \left(\frac{T}{T_{nom}}\right)^{BEX} \text{where } \mu = \frac{\beta'}{C_{ox}(W_{eff}/L_{eff})}.$$

UIS adjusts the velocity saturation:

$$U1S(T) = U1S \cdot \left(\frac{T}{T_{nom}}\right)^{FEX}$$

This model also includes all of the usual Synopsys model adjustments to capacitances, parasitics, diodes, and resistors.

Alternate Gate Capacitance Model

Select CAPOP=13 for the charge-conserving capacitance model, widely used with LEVEL=13 (BSIM1) and LEVEL=28 (improved BSIM1). See LEVEL 13 BSIM Model on page 324 for more details.

Impact Ionization

To select impact ionization modeling (instead of BSIM2), keep the AI0=0 value, and specify the ALPHA [ALPHA $\cdot$ (V_{ds} - V_{dsat}) replaces AI in equation for *f* in the BSIM2 equations section], VCR (replaces BI), and IIRAT (multiplies *f*) model parameters.

Synopsys impact ionization modeling differs from BSIM2 modeling in two ways:

1. A bias term (V_{ds} - V_{dsat}) multiplies the exponential and ALPHA values.
2. You can use the IIRAT model parameter to partition the impact ionization component of the drain current, between the source and the bulk. IIRAT multiplies *f* in the saturation I_{ds} equation. Thus, the IIRAT fraction of the impact ionization current goes to the source, and the 1-IIRAT fraction goes to the bulk, adding to *IDB*. IIRAT defaults to zero (that is, 100% of impact ionization current goes to the bulk).

BSIM2's impact ionization assumes that all of the impact ionization current is part of I_{ds}. In other words, it flows to the source. This assumption can lead to inaccuracies, for example, in cascode circuits. See Calculating the Impact Ionization Equations on page 61 for more details.

Parasitic Diode for Proper LDD Modeling

The Level 39 MOSFET model includes alternative MOS parasitic diodes to replace SPICE-style MOS parasitic diodes. You can use these alternatives to geometrically scale the parasitics with MOS device dimension, properly modeling the LDD parasitic resistances, shared sources and drains, and select different diode sidewall capacitances along the gate edge and field edge.

To select the MOS parasitic diode, use the ACM model parameter. ACM=0 (default) chooses SPICE style. The alternatives likely to be of most interest to the BSIM2 user are ACM=2 and 3.

ACM=2 calculates the diode area based on W, XW, and HDIF (contact to gate spacing). You can override the calculation from the element line. You can specify LDIF (spacer dimension); RS and RD (source and drain sheet resistance under the spacer) for LDD devices, and RSH (sheet resistance of

the heavily-doped diffusion). Thus, simulation properly calculates the total parasitic resistance of the LDD devices.

ACM=3 uses all features of ACM=2. Its calculations of diode parasitics take into account the sharing of source/drains, and different junction sidewall capacitances along the gate and field edges. Use the GEO parameter to specify source/drain sharing from the element line. See MOSFET Diode Models on page 39 for details.

Skewing of Model Parameters

As in any other Synopsys model, you can set up the BSIM2 model file for skewing to reflect the process variation. You can perform Worst-Case or Monte-Carlo analysis, based on fab statistics. For more information, see Chapter 12, “Statistical Analysis and Optimization.” in the *HSPICE Simulation and Analysis Manual*.

HSPICE Optimizer

You can tie the BSIM2 model, like any other HSPICE model, into the optimizer in a Synopsys circuit simulator to fit to actual device data.

For more information, see Chapter 12, “Statistical Analysis and Optimization.” in the *HSPICE Simulation and Analysis Manual*. An example fit appears at the end of this section.

Modeling Guidelines, Removing Mathematical Anomalies

Because of the somewhat arbitrary geometric and bias adjustments made in the original BSIM2 parameters, they can take on non-physical values or values that are not mathematically allowed in Berkeley SPICE 3. This can lead to illegal function arguments, program crashes, and unexpected model behavior (for example, negative conductance). You must satisfy the following guidelines and corrections at all geometries of interest, and at biases up to double the supply voltages (that is, to $V_{ds} = 2 \cdot VDD$, $V_{gs} = 2 \cdot VGG$, and $V_{bs} = 2 \cdot VBB$).

To avoid a drain current discontinuity at $V_{ds} = V_{dsat}$, be sure that BI ≠ 0 if AI0 ≠ 0.

To prevent negative g_{ds}, be sure that ETA>0, MU3>0, and MU4<MU3 / (4 * VDD). This should ensure a positive g_{ds} value at biases up to double the supply voltages. To simplify matters, set all MU4 parameters to zero. You can obtain reasonably good fits to submicron devices without using MU4[1].

In the Level 39 MOSFET model, U1S cannot become negative. A negative U1S is physically meaningless, and causes negative arguments in a square root function in one of the BSIM2 equations. The U1D value should be less than unity (between 0 and 1).

For reasonable V_{th} behavior, make sure that:

$$K1 - 2K2 \cdot \sqrt{PHI - V_{bs}} \geq 0$$

For the equations to make sense, the following must hold: N > 0, VGLOW ≤ 0, and VGHIGH ≥ 0.

The BSIM2 gate capacitance model in SPICE 3E tends to display negative C_{gs} in the subthreshold. This is due to $C_{gg'}$ 0 as $V_{gs'}$ V_{th} by construction of the gate charge equation so that $C_{gs} = C_{gg} - C_{gd} - C_{gb'} - C_{gd} - C_{gb} \approx - C_{gb}$. Therefore, use CAPOP=13 (default) until UC Berkeley releases an improved BSIM2 gate capacitance model.

Modeling Example

The following is the result of fitting data from a submicron channel-length NMOS device to BSIM2. To fit this data, this example uses the Synopsys ATEM characterization software and the Synopsys simulation optimizer.

Figure 36 I_{DS} vs.V_{ds} for V_{gs} = 1, 2, 3, 4, 5V; BSIM2 Model vs. Data

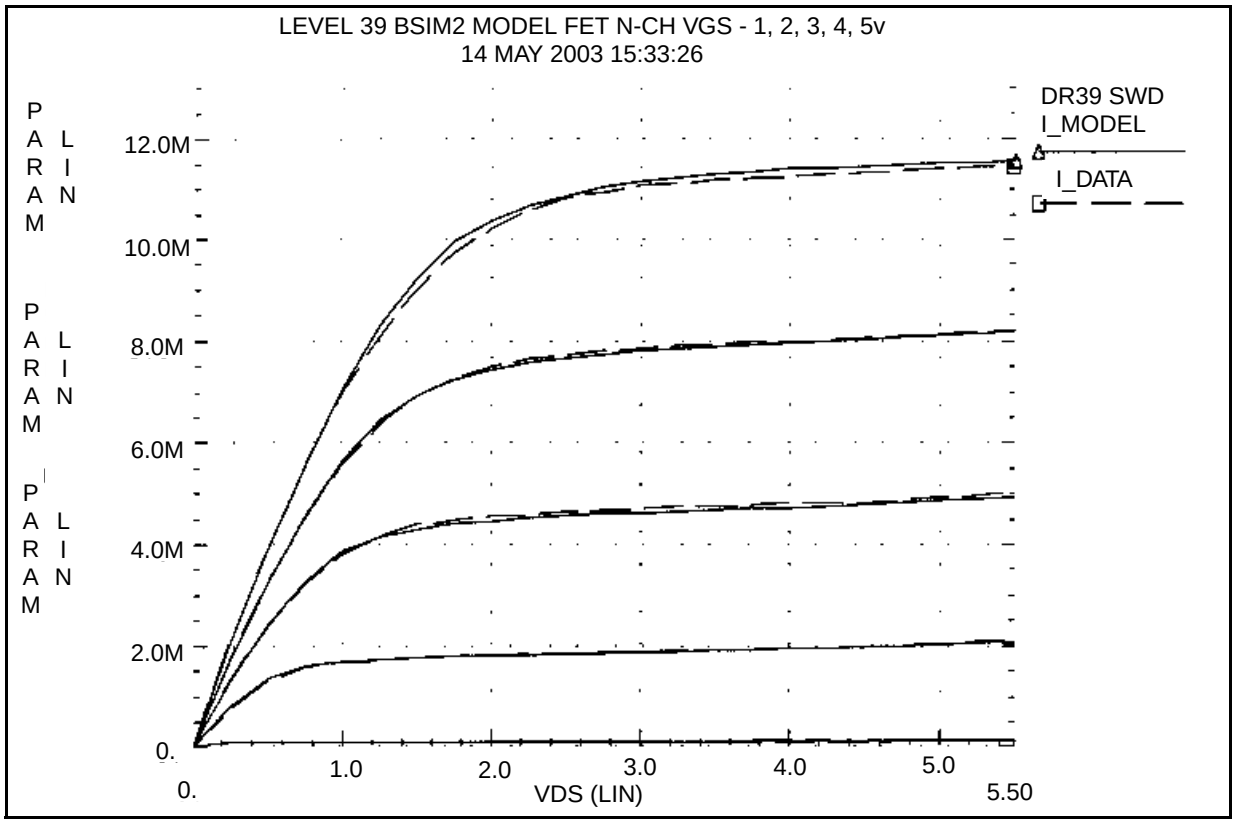


Figure 37 gds vs. Vds for Vgs = 2, 3, 4, 5V; BSIM2 Model vs. Data, LOG scale

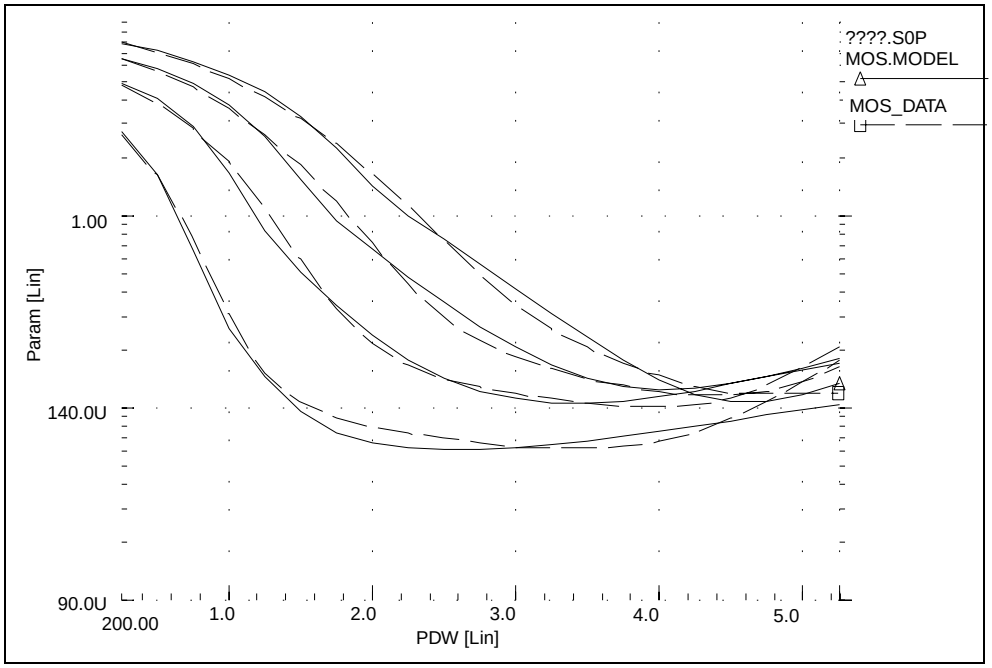


Figure 38 IDS vs. Vgs for Vds = 0.1V, Vbs = 0, -1, -2, -3, -4V, Showing Subthreshold Region; Model vs. Data

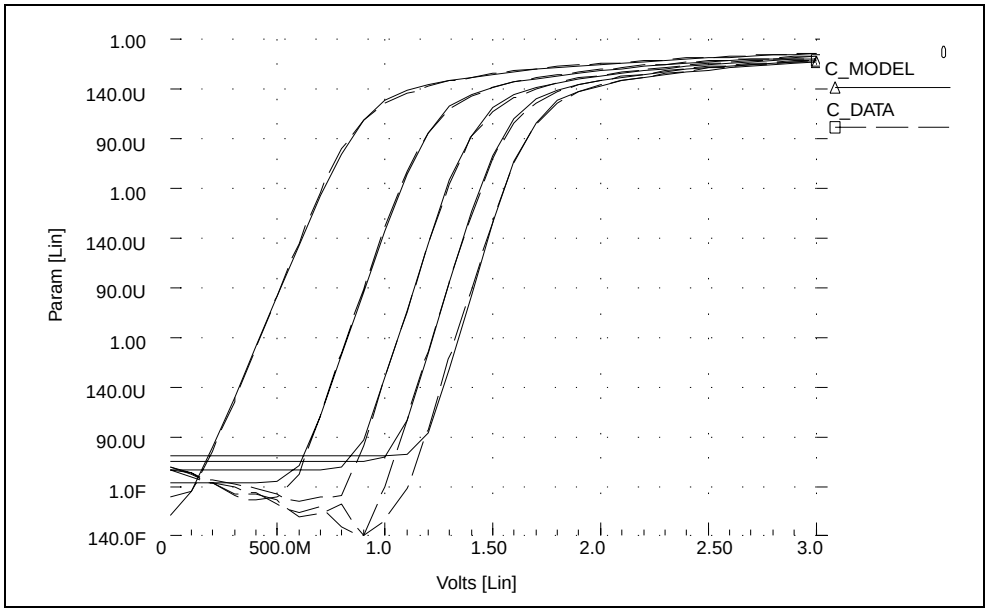
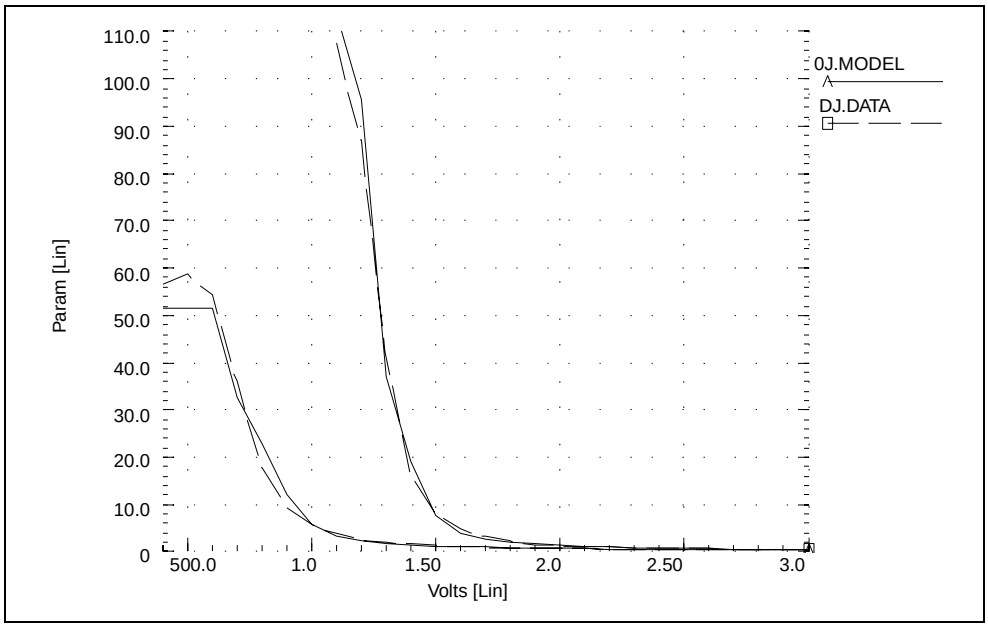


Figure 39 g_m/I_{DS} vs. V_{gs} for V_{ds} = 0.1V, V_{bs} = 0, -2V; BSIM2 Model vs. Data



Typical BSIM2 Model Listing

In this example, geometry sensitivities are set to zero because a fit at only one geometry has been performed. This example includes extra HSPICE parameters for LDD, temperature, and geometry.

```
.MODEL NCH NMOS LEVEL = 39
+ TOX = 2.000000E-02 TEMP = 2.500000E+01
+ VDD = 5.000000E+00 VGG = 5.000000E+00
+ VBB =-5.000000E+00 DL =0.000000E+00
+ DW = 0.000000E+00  VGHIGH = 1.270000E-01
+ LVGHIGH = 0.000000E+00 WVGHIGH = 0.000000E+00
+ VGLOW =-7.820000E-02 LVGLOW = 0.000000E+00
+ WVGLOW = 0.000000E+00  VFB =-5.760000E-01
+ LVFB = 0.000000E+00 WVFB = 0.000000E+00
+ PHI = 6.500000E-01 LPHI = 0.000000E+00
+ WPHI = 0.000000E+00  K1 = 9.900000E-01
+ LK1 = 0.000000E+00 WK1 = 0.000000E+00
+ K2 = 1.290000E-01 LK2 = 0.000000E+00
+ WK2 = 0.000000E+00 ETA0 = 4.840000E-03
+ LETA0 = 0.000000E+00 WETA0 = 0.000000E+00
+ ETAB =-5.560000E-03 LETAB = 0.000000E+00
+ WETAB = 0.000000E+00  MU0 = 3.000000E+02
+ MU0B = 0.000000E+00 LMU0B = 0.000000E+00
```

```
+ WMU0B = 0.000000E+00 MUS0 = 7.050000E+02
+ LMUS0 = 0.000000E+00  WMUS0 = 0.000000E+00
+ MUSB = 0.000000E+00 LMUSB = 0.000000E+00
+ WMUSB = 0.000000E+00 MU20 = 1.170000E+00
+ LMU20 = 0.000000E+00 WMU20 = 0.000000E+00
+ MU2B = 0.000000E+00 LMU2B = 0.000000E+00
+ WMU2B = 0.000000E+00  MU2G = 0.000000E+00
+ LMU2G = 0.000000E+00 WMU2G = 0.000000E+00
+ MU30 = 3.000000E+01 LMU30 = 0.000000E+00
+ WMU30 = 0.000000E+00  MU3B = 0.000000E+00
+ LMU3B = 0.000000E+00 WMU3B = 0.000000E+00
+ MU3G =-2.970000E+00 LMU3G = 0.000000E+00
+ WMU3G = 0.000000E+00  MU40 = 0.000000E+00
+ LMU40 = 0.000000E+00 WMU40 = 0.000000E+00
+ MU4B = 0.000000E+00 LMU4B = 0.000000E+00
+ WMU4B = 0.000000E+00  MU4G = 0.000000E+00
+ LMU4G = 0.000000E+00 WMU4G = 0.000000E+00
+ UA0 = 0.000000E+00 LUA0 = 0.000000E+00
+ WUA0 = 0.000000E+00  UAB = 0.000000E+00
+ LUAB = 0.000000E+00  WUAB = 0.000000E+00
+ UB0 = 7.450000E-03 LUB0 = 0.000000E+00
+ WUB0 = 0.000000E+00  UBB = 0.000000E+00
+ LUBB = 0.000000E+00 WUBB = 0.000000E+00
+ U10 = 0.000000E+00 LU10 = 7.900000E-01
+ WU10 = 0.000000E+00  U1B = 0.000000E+00
+ LU1B = 0.000000E+00 WU1B = 0.000000E+00
+ U1D = 0.000000E+00 LU1D = 0.000000E+00
+ WU1D = 0.000000E+00  N0 = 8.370000E-01
+ LN0 = 0.000000E+00  WN0 = 0.000000E+00
+ NB  = 6.660000E-01 LNB = 0.000000E+00
+ WNB = 0.000000E+00 ND = 0.000000E+00
+ LND = 0.000000E+00 WND = 0.000000E+00
+ VOF0 = 4.770000E-01 LVOF0 = 0.000000E+00
+ WVOF0 = 0.000000E+00  VOFB =-3.400000E-02
+ LVOFB = 0.000000E+00 WVOFB = 0.000000E+00
+ VOFD =-6.900000E-02 LVOFD = 0.000000E+00
+ WVOFD = 0.000000E+00  AI0 = 1.840000E+00
+ LAI0 = 0.000000E+00 WAI0 = 0.000000E+00
+ AIB = 0.000000E+00 LAIB = 0.000000E+00
+ WAIB = 0.000000E+00  BI0 = 2.000000E+01
+ LBI0 = 0.000000E+00 WBI0 = 0.000000E+00
+ BIB = 0.000000E+00 LBIB = 0.000000E+00
+ WBIB = 0.000000E+00  DELL = 0.000000E+00
+ WDF = 0.000000E+00
```

Common SPICE Parameters

```
+ CGDO = 1.000000E-09 CGSO = 1.000000E-09
```

```
+ CGBO = 2.500000E-11
+ RSH = 3.640000E+01 JS = 1.380000E-06
+ PB = 8.000000E-01 PBSW = 8.000000E-01
+ CJ = 4.310000E-04 CJSW = 3.960000E-10
+ MJ = 4.560000E-01 MJSW = 3.020000E-01
```

Synopsys Parameters

```
+ ACM = 3 LMLT = 8.500000E-01
+ WMLT = 8.500000E-01
+ XL =-5.000000E-08 LD = 5.000000E-08
+ XW = 3.000000E-07 WD = 5.000000E-07
+ CJGATE = 2.000000E-10 HDIF = 2.000000E-06
+ LDIF = 2.000000E-07
+ RS = 2.000000E+03 TRS = 2.420000E-03
+ RD = 2.000000E+03 TRD = 2.420000E-03
+ TCV = 1.420000E-03 BEX =-1.720000E+00
+ FEX =-2.820000E+00 LMU0 = 0.000000E+00
+ WMU0 = 0.000000E+00 JSW =2.400000E-12
```

References

[1] Duster, J.S., Jeng, M.C., Ko, P. K., and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.

7

BSIM MOSFET Models: Levels 47 to 65

Lists and describes seven of the newest BSIM-type MOSFET models supported by HSPICE.

This chapter describes seven of the newest Berkeley Short Channel IGFET (BSIM) type MOSFET models that HSPICE supports:

- Level 47 BSIM3 Version 2 MOS Model
- Level 49 and 53 BSIM3v3 MOS Models
- Level 54 BSIM4 Model
- Level 57 UC Berkeley BSIM3-SOI Model
- Level 59 UC Berkeley BSIM3-SOI FD Model
- Level 60 UC Berkeley BSIM3-SOI DD Model
- Level 65 SSIMSOI Model

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website:

http://www.eigroup.org/cmc/cmos/default.htm

For descriptions of older BSIM models that Synopsys supports, see Chapter 6, BSIM MOSFET Models: Levels 13 to 39.

Level 47 BSIM3 Version 2 MOS Model

The BSIM3 version 2.0 MOS model from UC Berkeley is available as the Synopsys Level 47 model.

Table 91 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
VTH0	V	0.7	Threshold voltage of the long channel at $V_{bs} = 0$ and small V_{ds} • 0.7 for n-channel. • - 0.7 for p-channel.
K1	$V^{1/2}$	0.53	First-order body effect coefficient
K2		-0.0186	Second-order body effect coefficient
K3		80.0	Narrow width effect coefficient
K3B	1/V	0	Body width coefficient of the narrow width effect
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2		0.022	Body bias coefficient of the threshold temperature effect
GAMMA1	$V^{1/2}$	See Level 47 Model Equations on page 390.	Body effect coefficient, near interface
GAMMA2	$V^{1/2}$	See Level 47 Model Equations on page 390.	Body effect coefficient in the bulk
W0	m	2.5e-6	Narrow width effect coefficient
NLX	m	1.74e-7	Lateral nonuniform doping along the channel
TOX	m	150e-10	Gate oxide thickness

Table 91 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
XJ	m	0.15e-6	Junction depth
DL	m	0.0	Channel length reduction on one side (multiplied by SCALM)
DW	m	0.0	Channel width reduction on one side (multiplied by SCALM)
NPEAK	cm^{-3} ([8])	1.7e17	Peak doping concentration near the interface
NSUB	cm^{-3}	6.0e16	Substrate doping concentration
PHI	V	See Level 47 Model Equations on page 390.	Surface potential under strong inversion
XT	m	1.55e-7	Doping depth
VBM	V	-5.0	Maximum substrate bias
VBX	V	See Level 47 Model Equations on page 390.	V_{bs} at which the depletion width equals *XT*
DVT0		2.2	Short-channel effect coefficient 0
DVT1		0.53	Short-channel effect coefficient 1
DVT2	1/V	-0.032	Short-channel effect coefficient 2
U0	m^2/Vsec ([8])	0.067	Low field mobility at T = *TREF* • 0.067 for n-channel • 0.025 for p-channel
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UA1	m/V	4.31e-9	Temperature coefficient of *UA*

Table 91 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
UB	m^2/V^2	5.87e-19	Second-order mobility degradation coefficient
UB1	m^2/V^2	-7.61e-18	Temperature coefficient of *UB*
UC	1/V	0.0465	Body bias sensitivity coefficient of mobility
UC1	1/V	-0.056	Temperature coefficient of *UC*
VSAT	cm/sec	8e6	Saturation velocity of the carrier at T = *TREF*
AT	m/sec	3.3e4	Temperature coefficient of *VSAT*
RDSW	ohm · µm	0.0	Source drain resistance per unit width
RDS0	ohm	0.0	Source drain contact resistance
LDD	m	0.0	Total length of the LDD region
ETA		0.3	Coefficient of the drain voltage reduction
ETA0		0.08	DIBL (Drain Induced Barrier Lowering) coefficient for the subthreshold region
ETAB	1/V	-0.07	Subthreshold region DIBL coefficient
EM	V/m	4.1e7	Electrical field in the channel above which the hot carrier effect dominates
NFACTOR		1.0	Subthreshold region swing
VOFF	V	-0.11	Offset voltage in the subthreshold region
LITL	m		Characteristic length. Default is: $$LITL = \left(\frac{\varepsilon_{si} T_{ox} X_j}{\varepsilon_{ox}}\right)^{1/2}$$
VGLOW	V	-0.12	Lower bound of the weak-strong inversion transition region

Table 91 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
VGHIGH	V	0.12	Upper bound of the weak-strong inversion transition region
CDSC	F/m^2	2.4e-4	Drain/source and channel coupling capacitance
CDSCB	F/Vm^2	0	Body coefficient for CDSC
CIT	F/m^2	0.0	Interface state capacitance
PCLM		1.3	Coefficient of the channel length modulation
PDIBL1		0.39	Coefficient 1 for the DIBL (Drain Induced Barrier Lowering) effect
PDIBL2		0.0086	Coefficient 2 for the DIBL effect
DROUT		0.56	Coefficient 3 for the DIBL effect
DSUB		DROUT	DIBL coefficient in the subthreshold region
PSCBE1	V/m	4.24e8	Exponent 1 for the substrate current induced body effect
PSCBE2	m/V	1.0e-5	Coefficient 2 for the substrate current induced body effect
A0		1	Bulk charge effect. Default is 4.4 for PMOS.
TNOM (TREF)	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25 °C. See 4 and 5 in Notes on page 387.
SUBTHMOD		2	Subthreshold model selector
SATMOD		2	Saturation model selector
KETA	1/V	-0.047	Body bias coefficient of the bulk charge effect
A1	1/V	0	First nonsaturation factor (0 for NMOS, 0.23 for PMOS)

Table 91 MOSFET Level 47 Model Parameters (Continued)

Name	Unit	Default	Description
A2		1.0	Second nonsaturation factor (1.0 for NMOS, 0.08 for PMOS)
UTE		-1.5	Mobility temperature exponent
KT1L	Vm	0	Channel length sensitivity of the temperature coefficient for the threshold voltage
UC0*	$(V/m)^2$		Temperature coefficient
BULKMOD		1	Bulk charge model selector
XPART		1	Charge partitioning flag
VFB	V		Flat-band voltage
PVAG		0	Gate dependence of the output resistance

* UC0 has no effect on the model

Using the BSIM3 Version 2 MOS Model

The Level 47 model uses the same model parameters for the source/drain diode current, capacitance, and resistance as used in the other supported MOS levels. The ACM model parameter controls the choice of source/drain equations.

The Level 47 model also uses the same noise equations as the other MOSFET model levels. The NLEV parameter controls the choice of noise equations.

This model, like all Synopsys simulation device models, can include parameters. You can use these parameters to model the process skew, either by worst-case corners or by Monte Carlo. For information about Worst-Case and Monte Carlo analysis, see “Performing Worst Case Analysis” and “Performing Monte Carlo Analysis” in Chapter 12, “Statistical Analysis and Optimization,” in the *HSPICE Simulation and Analysis Manual*.

Notes

1. Set Level=47 to identify the model as a BSIM3 model.
2. This model is based on BSIM3 version 2.0 from UC Berkeley. Code was received from UC Berkeley in July 1994 in the form of SPICE3e2. Changes announced in a letter from UCB September 13, 1994, have been included. DC sweeps have been checked against SPICE3e2.
3. The default setting for *CAPOP* is CAPOP=13, which is the BSIM1 charge-conserving capacitance model. This model does not use the BSIM3 capacitance model.
4. The Level 47 model supports the TNOM model parameter name as an alias for *TREF*. The conventional terminology is *TREF*, which is supported as a model parameter in all Synopsys MOS levels. Level 47 supports the TNOM alternative name for compatibility with SPICE3.
5. The default room temperature is 25°C in Synopsys simulators, but is 27°C in SPICE3. If you specify the BSIM3 model parameters at 27°C, add TREF=27 to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add **.OPTION** TNOM=27 to the netlist when you test the Synopsys model versus SPICE3.
6. The default of *DERIV* is zero, the analytical method. You can set *DERIV* to 1 for the finite difference method. Analytic derivatives in the SPICE3e2 code are not exact in some regions. Setting DERIV=1 returns more accurate derivatives (*GM*, *GDS*, and *GMBS*), but consumes more CPU time.
7. You can select one of three ways to calculate V_{th}:
   - Using *K1* and *K2* values that you specify.
   - Using *GAMMA1*, *GAMMA2*, *VBM*, and *VBX* values that you enter in the **.MODEL** statement.
   - Using *NPEAK*, *NSUB*, *XT*, and *VBM* values that you specify.
8. You can enter the *NPEAK* and *U0* model parameters in meters or centimeters. Simulation converts *NPEAK* to cm^{-3} as follows: if *NPEAK* is greater than 1e20, simulation multiplies it by 1e-6, and converts *U0* to m^2/Vsec as follows: if *U0* is greater than 1, simulation multiplies it by 1e-4. You must enter the *NSUB* parameter in cm^{-3} units.
9. The specified value of *VTH0* for p-channel in the **.MODEL** statement should be negative.

10. The default value of *KT1* is -0.11. The negative sign ensures that the absolute value of the threshold decreases with increasing temperature for NMOS and PMOS.
11. You cannot set the *LITL* model parameter below a minimum value of 1.0e-9 m to avoid a possible divide by zero error.
12. After you adjust the temperature, *VSAT* cannot go below a minimum value of 1.0e4 m/sec to assure that it is positive after temperature compensation.
13. Seven model parameters accommodate the temperature dependencies of six temperature-dependent model variables. These parameters are *KT1* and *KT2* for *VTH*, *UTE* for *U0*, *AT* for *VSAT*, *UA1* for *UA*, *UB1* for *UB*, and *UC1* for *UC*.
14. Set up the temperature conversion between this model and SPICE3 as follows:

```
SPICE3:   .OPTION TEMP=125
   .MODEL NCH NMOS Level=8
   + TNOM =27 ...
HSPICE:   .TEMP 125
   .MODEL NCH NMOS Level=47
   + TREF =27 ...
```

15. The SCALM option does not affect parameters that are unique to this model, but it does affect the common MOS parameters, such as *XL*, *LD*, *XW*, *WD*, *CJ*, *CJSW*, *JS*, and *JSW*.
16. Level 47 uses the common Synopsys MOS parasitic models, which ACM specifies.
17. Level 47 uses the common Synopsys MOS noise models, which NLEV specifies.
18. You can use *DELVTO* and *DTEMP* on the element line with MOSFET Level 47.
19. The PSCBE1 and PSCBE2 model parameters determine the impact ionization current, which contributes to the drain-source current. Impact ionization does not contribute to the bulk current.

Leff and Weff Equations for BSIM3 Version 2.0

The standard equations for Leff and Weff in the Synopsys model are:

$$L_{eff} = L + XL - (2 \cdot LD)$$

$$W_{eff} = W + XW - (2 \cdot WD)$$

BSIM3 uses the following UCB SPICE3 equations:

$$L_{eff} = L - (2 \cdot DL)$$

$$W_{eff} = W - (2 \cdot DW)$$

The units for these parameters are meters with defaults of zero.

Simulation uses the standard Synopsys model equation for both cases, and accepts DL(DW) as the value for LD(WD). If you specify both LD(WD) and DL(DW) in a **.MODEL** statement, simulation uses the LD(WD) value.

If you specify LDAC and WDAC in the **.MODEL** statement, then:

Leff = L+XL-2·LDAC, Weff = W+XW-2·WDAC

This model uses the LD(DL) and WD(DW) values to generate defaults for CGSO, CGDO, and CGBO. You can also use these values with the RS and RD parameters for ACM>0.

Example

The following two models return the same simulation results:

```
* HSPICE style:
   .MODEL n1 nmos Level=47 XL=0.1e6 LD=0.15e-6
   + SatMod=2 SubthMod=2 BulkMod=1
   + CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0

* SPICE3 style:
   .MODEL n2 nmos Level=47 LD=0.1e-6
   + SatMod=2 SubthMod=2 BulkMod=1
   + CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
```

Level 47 Model Equations

The following model equations are based on the BSIM3 source code:

Threshold Voltage

Model Parameters

V_{th0}, $K1$, $K2$, ϕ_s, N_{lx}, $K3$, W_0, T_{ox}, V_{bi}, D_{vt0}, D_{vt1},

D_{vt2}, N_{peak}, N_{sub}, Υ_1, Υ_2, V_{bx}, V_{bm}, V_{bi},X_t, $TREF$

$$V_{th} = V_{th0} + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}\sqrt{\frac{\phi_s}{\phi_s - V_{bs}}}} - 1\right)\sqrt{\phi_s}$$

$$+ (K3 + K3B \cdot V_{bs}) \cdot \left(\frac{T_{ox}}{W_{eff} + W_0}\right)\phi_s - \Delta V_{th}$$

$$T_{ratio} = \frac{(TEMP + DTEMP + 273.15)}{(TREF + 273.15)}$$

$$\Delta V_{th} = \theta_{th}(L_{eff}) \cdot (V_{bi} - \phi_s)$$

$$\theta_{th}(L_{eff}) = D_{vt0} \cdot \left[\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{2l_t}\right) + 2\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{l_t}\right)\right]$$

$$l_t = \sqrt{3 \cdot T_{ox} \cdot X_{dep}} \cdot (1 + D_{vt2} \cdot V_{bs})$$

$$X_{dep} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot (\phi_s - V_{bs})}{q \cdot N_{peak}}}$$

If you do not specify *Phi*$_S$ as a model parameter, then:

$$\phi_s = 2 \cdot V_{tm} \cdot ln\left(\frac{N_{peak}}{n_i}\right) \qquad \text{(Npeak and ni in cm-3)}$$

$$V_{tm} = K \cdot T/q$$

$$n_i = 1.45e10 \cdot \left(\frac{T}{300.15}\right)^{1.5} \cdot \exp(21.5565981 - Eg/(2 \cdot V_{tm}))$$

$$Eg = 1.16 - (7.02e-4) \cdot \dot{T^2} / (T + 1108.0)$$

If you do not specify *K1* and *K2* as model parameters, simulation calculates them as follows:

$$K_1 = \Upsilon_2 - 2 \cdot K_2 \cdot \sqrt{\phi_s - V_{bm}}$$

$$K_2 = (\Upsilon_1 - \Upsilon_2) \cdot \frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

$$\Upsilon_1 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{peak}}}{C_{ox}} \qquad \Upsilon_2 = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot N_{sub}}}{C_{ox}}$$

$$V_{bx} = \phi_s - \left(\frac{q \cdot N_{peak} \cdot X_t^2}{2 \cdot \varepsilon_{si}} \right)$$

If you do not specify V_{bi} as a model parameter, then:

$$V_{bi} = \frac{k \cdot T}{q} \cdot ln\left(\frac{1.0e22 \cdot N_{peak}}{n_i^2} \right)$$

Mobility of Carrier

Model Parameters

μ_0, U_a, U_b, U_c

$$\mu_{eff} = \frac{\mu_0}{1 + U_a \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right) + U_b \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right)^2 + U_c \cdot V_{bs}}$$

Drain Saturation Voltage

Model Parameters

A_0, v_{sat}, X_j, A_1, A_2, R_{ds0}, R_{dsw}

Rds and Pfactor:

$$R_{ds} = R_{ds0} + R_{dsw} / (1e6 \cdot W_{eff})$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$ (if Pfactor >1, simulation sets it to Pfactor = 1)

$$V_{gst} = V_{gs} - V_{th}$$

If Rds = 0 and Pfactor = 1, then:

$$V_{dsat} = \frac{E_{sat} \cdot L_{eff} \cdot V_{gst}}{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}$$

For BULKMOD = 1:

$$A_{bulk} = \left(1 + \frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot T1s \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

For BULKMOD = 2:

$$A_{bulk} = \left(\frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot \sqrt{\phi_s} \cdot 2}\right) / (1 + KETA \cdot V_{bs})$$

$$T1 = 2 \cdot \sqrt{X_j \cdot X_{dep}}$$

For $V_{bs} \leq 0$:

$$T1s = \sqrt{\phi_s - V_{bs}}$$

For $V_{bs} \geq 0$:

$$T1s = \frac{\phi_s \cdot \sqrt{\phi_s}}{\phi_s + \frac{V_{bs}}{2}} \qquad E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$$

In general, Vdsat solves Tmpa * Vdsat * Vdsat - Tmpb * Vdsat + Tmpc = 0:

$$V_{dsat} = (Tmpb - \sqrt{Tmpb^2 - 4 \cdot Tmpa \cdot Tmpc}) / (2 \cdot Tmpa)$$

$$Tmpa = A_{bulk} \cdot (A_{bulk} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds} - 1 + 1/Pfactor)$$

$$Tmpb = V_{gst} \cdot (2/Pfactor - 1) + (A_{bulk} \cdot E_{sat} \cdot L_{eff}) + (3 \cdot A_{bulk} \cdot V_{gst} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

$$Tmpc = (V_{gst} \cdot E_{sat} \cdot L_{eff}) + (V_{gst}^2 \cdot 2 \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

Linear Region

$$I_{dslin0} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{1}{1 + V_{ds}/(E_{sat} \cdot L)} \cdot \left(V_{gs} - V_{th} - A_{bulk} \cdot \frac{V_{ds}}{2}\right) \cdot V_{ds}$$

$$I_{ds} = \frac{I_{dslin0}}{1 + \frac{R_{ds} \cdot I_{dslin0}}{V_{ds}}}$$

Saturation Region

Model Parameters

$litl,\ eta,\ L_{dd},\ E_m,\ D_{rout},\ P_{clm},\ P_{dibl1},\ P_{dibl2},\ P_{scbe1},\ P_{scbe2}$

V_{asat} and F_{vag}:

$$V_{asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot \left(V_{gst} - \frac{A_{bulk} \cdot V_{dsat}}{2}\right)}{2/Pfactor - 1 + R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot A_{bulk}}$$

$$F_{vag} = 1 + \frac{P_{vag} \cdot V_{gst}}{E_{sat} \cdot L_{eff}}$$

Early Voltage, satMod = 1:

$$V_A = V_{asat} + F_{vag} \cdot \left(\frac{1 + eta \cdot \frac{L_{dd}}{litl}}{P_{clm} \cdot A_{bulk}}\right)$$

$$\cdot \left(\frac{(A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst} - \lambda \cdot (V_{ds} - V_{dsat})) \cdot (V_{ds} - V_{dsat})}{E_{sat} \cdot litl}\right)$$

$$\lambda = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + (V_{gst})}{2 \cdot litl \cdot E_m}$$

Early Voltage, satMod = 2:

$$V_A = V_{asat} + F_{vag} \cdot U_{vds} \cdot \left(\frac{1}{V_{aclm}} + \frac{1}{V_{adibl}}\right)^{-1}$$

$$U_{vds} = 1 + eta \cdot \frac{L_{dd}}{litl}$$

$$V_{aclm} = \frac{1}{P_{clm}} \cdot \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}{A_{bulk} \cdot E_{sat} \cdot litl} \cdot (V_{ds} - V_{dsat})$$

$$V_{adibl} = \frac{1}{\theta_{rout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{bulk} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right]$$

$$\theta_{rout} = P_{dibl1} \cdot \left[\exp\left(\frac{-D_{rout} \cdot L_{eff}}{2 \cdot l_t} \right) + 2\exp\left(\frac{-D_{rout} \cdot L_{eff}}{l_t} \right) \right] + P_{dibl2}$$

$$V_{ahce} = \left[\frac{P_{scbe2}}{L_{eff}} \cdot \exp\left(\frac{-P_{scbe1} \cdot litl}{V_{ds} - V_{dsat}} \right) \right]^{-1}$$

Drain Current

$$I_{dsat} = W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot (V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}) \cdot Pfactor$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

$$I_{ds} = I_{dsat} \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_A} \right) \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_{ahce}} \right)$$

Subthreshold Region

Model Parameters

$Nfactor,\ C_{dsc},\ C_{dscb}, V_{off},\ C_{it}, D_{sub}, eta_0,\ eta_b$

n and DIBL:

$$n = 1 + \frac{Nfactor \cdot 1.034e{-}10}{X_{dep} \cdot C_{ox}} + \frac{(C_{dsc} + C_{dscb} \cdot V_{bs}) \cdot \left[\exp\left(\frac{-L_{eff}}{2 \cdot l_t} \right) + 2\exp\left(\frac{-L_{eff}}{l_t} \right) \right] + C_{it}}{C_{ox}}$$

$$DIBL = (eta_0 + eta_b \cdot V_{bs}) \cdot \left[\exp\left(\frac{-D_{sub} \cdot L_{eff}}{2 \cdot l_{t0}}\right) + 2\exp\left(\frac{-D_{sub} \cdot L_{eff}}{l_{t0}}\right) \right]$$

$$l_{t0} = \sqrt{3 \cdot T_{ox} \cdot X_{dep0}} \qquad X_{dep0} = \sqrt{\frac{2 \cdot \varepsilon_{si} \cdot \phi_s}{q \cdot N_{peak}}}$$

If subthMod = 0:

$$I_{ds} = g_m = g_{ds} = g_{mb} = 0$$

If subthMod = 1:

$$I_{ds} = \frac{I_{limit} \cdot I_{exp}}{I_{limit} + I_{exp}} \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right] \qquad I_{limit} = \frac{9}{2} \cdot u0 \cdot \sqrt{\frac{q\varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2$$

$$I_{exp} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

If subthMod = 2:

$$I_{ds} = u0 \cdot \sqrt{\frac{q \cdot \varepsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right)\right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

Transition Region (for subthMod = 2 only)

Model Parameters

V_{gshigh}, V_{gslow}

$$I_{ds} = (1-t)^2 \cdot I_{dslow} + 2 \cdot (1-t) \cdot t \cdot I_p + t^2 \cdot I_{dshigh}$$

$$t = \left(\frac{V_p - V_{gslow}}{V_{gslow} - 2 \cdot V_p + V_{gshigh}}\right) \cdot \left(\sqrt{1 + \frac{(V_{gslow} - 2 \cdot V_p + V_{gshigh})(V_{gs} - V_{th} - V_{gslow})}{(V_p - V_{gslow})^2}} - 1\right)$$

$$V_p = \frac{(g_{mhigh} \cdot V_{gshigh} - g_{mlow} \cdot V_{gslow}) - (I_{dshigh} - I_{dslow})}{g_{mhigh} - g_{mlow}}$$

$$I_p = I_{dslow} + g_{mlow} \cdot (V_p - V_{gslow})$$

Temperature Compensation

Model Parameters

$A_t,\ U_{a1},\ U_{b1},\ U_{c1},\ KT1,\ KT2, UTE$

$$V_{th}(temp) = V_{th}(tref) + (KT1 + KT2 \cdot V_{bs}) \cdot (T_{ratio} - 1)$$

$$u0(temp) = u0(tref) \cdot (T_{ratio})^{UTE}$$

$$V_{sat}(temp) = V_{sat}(tref) - A_t \cdot (T_{ratio} - 1)$$

$$U_a(temp) = U_a(tref) + U_{a1} \cdot (T_{ratio} - 1)$$

$$U_b(temp) = U_b(tref) + U_{b1} \cdot (T_{ratio} - 1)$$

$$U_c(temp) = U_c(tref) + U_{c1} \cdot (T_{ratio} - 1)$$

PMOS Model

In the following example of a PMOS model for the Level 47 MOSFET, VTH0 is negative.

```
.model pch PMOS Level=47
+ Tnom=27.0
+ Npeak= 1.5E+23 Tox=7.0E-09 Xj=1.0E-07
+ dl= 0.2E-06 dw=-0.1E-06
+ SatMod= 2 SubthMod= 2 BulkMod= 1
+ Vth0= -.8 Phi= .7 K1= .5 K2=0.03 K3= 0
+ Dvt0= 48 Dvt1= .6 Dvt2=-5e-4
+ Nlx=0 W0= 0
+ Vsat= 9E6 Ua= 1E-09 Ub= 0 Uc= -3E-02
+ Rds0= 180 Rdsw= 0 U0= 7E-03
+ A0= .87
+ Voff=-.07 NFactor= 1.5 Cit=-3E-05
+ Cdsc= 6E-02 Vglow=-.12 Vghigh= .12
+ Pclm= 77 Pdibl1= 0 Pdibl2= 2E-011
+ Drout= 0 Pscbe1= 0 Pscbe2= 1E-28
+ Eta= 0 Litl= 4.5E-08
```

```
+ Em= 0 Ldd= 0
+ kt1=-.3 kt2=-.03
+ At= 33000
+ Ua1= 4E-09 Ub1= 7E-18 Uc1= 0
```

Level 49 and 53 BSIM3v3 MOS Models

The Synopsys Level 49 and Level 53 models are based on the BSIM3v3 MOS model from UC Berkeley.

- Level 49 is an HSPICE-enhanced version of BSIM3v3. Level 49 maintains compliance with the UC Berkeley release of BSIM3v3 with the following three exceptions:
  - Default parameter values—To eliminate differences in default parameter values, Level 49 explicitly assigns the CAPMOD and XPART parameters, and sets ACM=10.
  - Parameter range limits—Provides parameter range limits that are identical to that of the Berkeley release. Differences occur only in the severity of the warning for five parameters. Level 49 issues a warning that the model exceeded the parameter range, but continues with the simulation.
  - However, the Berkeley release issues a fatal error, and aborts the simulation. These five parameters are NGATE, DVT1W, DVT1, DSUB, and DROUT. (See Parameter Range Limits on page 428 for more details.)
  - Improvements in numerical stability—Provides improvements in numerical stability. In most practical situations, these improvements do not affect compliance with the Berkeley release, but improve the convergence and the simulation time.
- Level 53 maintains full compliance with the Berkeley release, including numerically-identical model equations, identical parameter default values, and identical parameter range limits.
- Level 49 and 53 both support the following instance parameters, along with the DELVTO instance parameter for local mismatch and NBTI (negative bias temperature instability) modeling:
  - MULU0, low-field mobility (U0) multiplier. Default=1.0.
  - MULUA, first-order mobility degradation coefficient (UA) multiplier.
  - MULUB, second-order mobility degradation coefficient (UB) multiplier.

Both Levels 49 and 53 support a superset of model parameters that include HSPICE-specific parameters. For Level 53, in all cases, HSPICE-specific parameters default to OFF. The single exception in Level 49 is that ACM defaults to 0. To achieve Level 49 compliance with Berkeley BSIM3v3, set ACM=10.

If you set any of the following parameter values for MOSFET Level 49 and 53, simulation reports a warning:

- Leff <= 5e-8
- Weff <= 1e-7
- LeffCV <= 5e-8
- WeffCV <= 1e-7

Simulation aborts if you set Leff or Weff <= 0.0.

Selecting Model Versions

Recommended BSIM3v3 Version

The recommended BSIM3v3 model specification is Level=49, VERSION=3.24. This version provides the most stable and up-to-date representation of the UCB BSIM3v3.2.4 model.

However, do not change the VERSION specification in existing model cards without consulting the foundry or model extraction group that created the model cards.

As of the 99.2 release, there are five official BSIM3v3 releases from Berkeley and several Level 49 releases. For additional release information from the UCB group, see the BSIM3 home page:
http://www-device.EECS.Berkeley.EDU/~bsim3/

To minimize confusion and maintain backward compatibility, you can select the VERSION and HSPVER model parameters. VERSION selects the Berkeley release version; HSPVER selects the Synopsys release version. For example, HSPVER=97.2 and VERSION=3.1 reproduce results from HSPICE 97.2 using the BSIM3 Version 3.1 model.

HSPVER defaults to the current release that you are using. The VERSION model parameter selects among the various Berkeley releases of BSIM3v3 as follows:

- *Version 3.0 Berkeley release (October 30, 1995) default for HSPICE96.1,96.2,96.3.* Simulation invokes this version if you specify VERSION=3.0 and HSPVER= 98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of October 1995, specify the VERSION=3.0 and HSPVER=98.0 parameters.
- *Version 3.1 Berkeley (December 9, 1997) default for HSPICE97.1,97.2. 97.4.* Simulation invokes this version if you specify VERSION=3.1 or 3.11 and HSPVER= 98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of December 1996, specify the VERSION=3.1 or 3.11 and HSPVER = 98.0 parameters.
- *Berkeley Version 3.0, 3.1 bug fixes.* Berkeley corrected several Version 3.0 and 3.1 bugs in the June, 1998 release. These fixes are incorporated into HSPICE98.2, which simulation uses if you specify VERSION=3.0 or VERSION=3.1 and HSPVER=98.2. As a result of bug fixes, you might notice some differences between Version 3.0/3.1 in HSPICE98.2 and previous Version 3.0/3.1 releases. Notably, differences occur if you specify PD and PS perimeter factors that are less than Weff (PD,PS < Weff no longer clamp to Weff in Version 3.1) and if DLC and LINT are not identical (LeffCV calculation bug in Versions 3.0 and 3.1).

For a complete list of bug fixes, see the BSIM3 web site:
http://www-device.eecs.berkeley.edu/~bsim3

Note: Version 3.11 was introduced in HSPICE97.4. This version represents Berkeley Version 3.1 (Dec., 1996) with HSPICE bug fixes. This model maintains backward compatibility. Starting with HSPICE98.2, Version 3.1 and 3.11 are identical, and represent Version 3.1 with Berkeley June, 1998 bug fixes.

- *Version 3.2 Berkeley release (June 16, 1998).* Simulation invokes this version if you specify VERSION=3.2 and HSPVER=98.2.
- *Version 3.2.1 Berkeley release (April 20, 1999).* Simulation invokes this version if you specify VERSION=3.21 and HSPVER=99.2.
- *Version 3.2.2 Berkeley release (April 20, 1999).* Simulation invokes this version if you specify VERSION=3.22 and HSPVER=99.2.
- For the latest HSPICE improvements, use VERSION=3.24 and HSPVER=02.2.

Note: Versions 3.2.1 and 3.2.2 are identical, except BSIM3v3.2.1 uses a bias-dependent Vfb and BSIM3v3.2.2 uses a bias-independent Vfb for the capMod = 1 and 2 capacitance models. Versions 3.23 and 3.2.4 provide various model fixes, compared to Version 3.22.

Table 92 Parameter Settings for Berkeley Releases, MOSFET Levels 49/53

Berkeley Release	VERSION	HSPVER
Version 3.0 (October 1995)	3.0	98.0
Version 3.0 with June 1998 bug fixes	3.0	98.2
Version 3.1 (December 1996)	3.1	98.0
Version 3.1 with June 1998 bug fixes	3.1	98.2
Version 3.2 (June 16,1998)	3.2	98.2
Version 3.2.1 (April 20, 1999)	3.21	99.2
Version 3.2.2 (April 20, 1999)	3.22 3.23 3.2.4	99.2 01.4 02.2

Version 3.2 Features

In June 1998, Berkeley released BSIM3 Version 3.2, which includes the following new features:

- A new intrinsic capacitance model, CAPMOD=3, includes finite charge layer thickness effects; CAPMOD now defaults to 3 (new parameters: CAPMOD=3, ACDE, and MOIN).
- Improved modeling of C-V characteristics at the weak-to-strong inversion transition (new parameters: NOFF and VOFFCV).
- Vth dependence on Tox (new parameter: TOXM).
- Flatband voltage parameter more accurately models different gate materials (new parameter: VFB).
- Improved substrate current scalability with channel length (new parameter: APLHA1).

- Restructured nonquasi-static (NQS) model includes pole-zero analysis and bug fixes. NQSMOD is a BSIM3 element parameter. HSPICE supports the model (but not the element) parameter.
- Junction diode model temperature dependence (new parameters: TCJ, TCJSW, TCJSWG, TPB, TPBSW, and TPBSWG).
- Adjustable current limiting in the junction diode current model (new parameter: IJTH).
- Use C-V inversion charge equations (CAPMOD=0,1,2,3) to calculate the thermal noise if NOIMOD=2 or 4.
- Eliminated the small negative capacitance values (Cgs and Cgd) in the accumulation-depletion regions.
- Separate set of length/width dependence parameters for the CV model (LLC, LWC, LWLC, WLC, WWC, and WWLC parameters).
- Additional parameter checking.
- Bug fixes.

Note: If you use the defaults for all new Version 3.2 parameters, Version 3.2 and Version 3.1 (with June, 1998 bug fixes) return identical DC results. However, transient and AC results generally differ. This discrepancy arises only from differences in the flatband voltage calculations used in the intrinsic charge/capacitance models. These differences occur in all CAPMOD models 1-3.

- Level 53 resets HSPVER < 98.0 to 98.0.
- HSPVER<98.2 resets to 98.2 if VERSION>=3.2 for Levels 49/53.
- Version 3.0, 3.1, and 3.11 in HSPICE do not support NQSMOD and CAPMOD=3. Only Version 3.2 supports them.
- Version 3.24 added Rds noise to the thermal noise model. Simulation smooths out the unified flicker noise, from the linear region to the saturation region. You might need to re-extract the parameters for the unified flicker noise model.

For more information about the Berkeley releases, see the BSIM3 web site:

http://www-device.eecs.berkeley.edu/~bsim3

Nonquasi-Static (NQS) Model

You can also select the Berkeley NonQuasi-Static (NQS) model for Levels 49 and 53. This model provides a first-order correction to the quasi-static charge models. See *M.Chan, K.- Y. Hui, C. Hu, and P.-K. Ko, IEEE Trans. Electron Devices, vol. ED-45, pp.834-841, 1998*. The Level 49/53 MOSFET model supports only the model parameter implementation.

To invoke the NQS model, specify the NQSMOD=1 parameter in the model card. You can use NQSMOD with any of the CAPMOD Levels (0-3) but only with Version 3.2. Version 3.0 and 3.1 do not support NQS.

HSPICE Junction Diode Model and Area Calculation Method

You can use two junction diode models with both Levels 49 and 53: the HSPICE junction model and the Berkeley junction model.

- For the HSPICE junction model, specify the ACM=0,1,2, or 3 model parameter value.
- For the Berkeley junction model, specify ACM=10,11,12, or 13.

The default ACM value is 0 for Levels 49 or 10 for Level 53. For the junction current, junction capacitance, and parasitic resistance equations corresponding to ACM=0,1,2,3 see MOSFET Diode Models on page 39.

Set ACM=10,11,12, or 13 to enable the Berkeley junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for ACM=10-13 correspond to the ACM=0-3 parasitic resistor equations. ACM=10-13 all use the Berkeley junction capacitance model equations:

```
   (Bulk-source capacitance)
if (Ps >Weff)
   Cbs = AS * Cjbs + (PS - Weff) * Cjbssw + Weff *
   Cjbsswg
else
   Cbs = AS * Cjbs + PS * Cjbsswg
```

The AS and PS area and perimeter factors default to 0, if you do not specify them on the element line.

```
if (Vbs < 0)
   Cjbs = Cj * (1 - (Vbs/Pb))^-Mj
   Cjbssw = Cjsw * (1 - (Vbs/Pbsw))^-Mjsw
   Cjbsswg = Cjswg * (1 - (Vbs/Pbswg))^-Mjswg
```

```
else
   Cjbs = Cj * (1 + Mj * (Vbs/Pb))
   Cjbssw = Cjsw * (1 + Mjsw * (Vbs/Pbsw))
   Cjbsswg = Cjswg * (1 + Mjswg * (Vbs/Pbswg))
```

Bulk-drain equations are analogous. ACM=10,11,12,13 do not use the HSPICE equations for AS, PS, AD, and PD. In accordance with the BSIM3v3 model, the default values for these area and perimeter factors are zero. To invoke the HSPICE calculations for AS, PS, AD, and PD, specify the CALCACM=1 model parameter.

Note: Simulation invokes CALCACM only if ACM=12.The calculations used in ACM=10, 11, and 13 are not consistent with the Berkeley diode calculations.

CALCACM = 1 and ACM = 12 invoke the following area and perimeter calculations:

If you do not specify AD on the element line:

```
   AD = 2 * HDIFeff * Weff
else:
   AD = AD * WMLT^2
```

If you do not specify AS on the element line:

```
   AS = 2 * HDIFeff * Weff
else:
   AS = AS * WMLT^2
```

If you do not specify PS on the element line:

```
   PS = 4 * HDIFeff + 2 * Weff
else:
   PS = PS * WMLT
```

If you do not specify PD on the element line:

```
   PD = 4 * HDIFeff + 2 * Weff
else:
   PD = PD * WMLT
```

Note: Weff is not the same Weff used in the BSIM3v3, and Levels 49 and 53 I-V, C-V model equations.

The preceding equations use the following simple forms:

```
   Weff = W * WMLT + XW
   HDIFeff = HDIF * WMLT
```

Parameter	Description
W	width specified on the element line
HDIF	heavy diffusion length specified in the model card
WMLT	shrink factor specified in the model card
XW	etch/mask effect factor specified in the model card

Note: These equations ignore the SCALM, SCALE, and M factor effects. See MOSFET Diode Models on page 39 (ACM=2) for further details.

TSMC Diode Model

Starting in HSPICE version 2003.09, HSPICE MOSFET Level 49 (ACM=12, BSIM3 version 3.2 or later) supports a TSMC diode model. You can use this TSMC diode model to simulate the breakdown effect, the resistance-induced non-ideality factor, and geometry-dependent reverse current of a diode.

Order this model directly from Taiwan Semiconductor Manufacturing Company (TSMC), not from Synopsys. See the TSMC web site: http://www.tsmc.com

BSIM3v3 STI/LOD

HSPICE BSIM3v3 (Level=49) supports UC Berkeley's STI/LOD stress effect model (see Table 93). To turn on this stress effect model in BSIM3v3, specify STIMOD=1 in your model cards.

Table 93 Supported HSPICE BSIM3v3 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given or if (<=0), the stress effect is turned off.
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given or if (<=0), the stress effect is turned off
SD (instance parameter)		0.0		Distance between neighboring fingers. For NF >1,If not given or (<=0), stress effect is turned off
STIMOD (Also instance parameter)		0.0		STI model selector, which gives priority to the instance parameter. • 0: No STI effect. • 1: UCB's STI model • 2: TSMC's STI model
SAREF	M	1e-06	No	Reference distance for SA, >0.0
SBREF	M	1e-06	No	Reference distance for SB, >0.0
WLOD	M	0.0	No	Width parameter for stress effect
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. 1.0<=kvsat<=1.0
TKU0		0.0	No	Temperature coefficient of KU0
LKU0		0.0	No	Length dependence of KU0
WKU0		0.0	No	Width dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, >0

Table 93 Supported HSPICE BSIM3v3 STI/LOD Parameters (Continued)

Parameter	Unit	Default	Bin?	Description
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
WKVTH0		0.0	No	Width dependence of KVTH0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0
STK2		0.0	No	K2 shift factor related to VTh0 change
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0

Parameter Differences

Some parameter names differ between the Synopsys model and the Berkeley junction models. The Synopsys models (ACM=0-3) do not recognize the following BSIM3v3 parameters:

- NJ (ignored, use N instead)
- CJSWG (ignored, use CJGATE instead)
- MJSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall grading coefficient = MJSW)
- PBSW (ignored, use PHP instead)
- PBSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall contact potential = PHP)

The Berkeley model (ACM=10,11,12,13) does not recognize the following parameters:

- CJGATE (ignored, use CJSWG instead)
- PHP (ignored, use PBSW instead)

Noise Model

The HSPICE NLEV parameter overrides the BSIM3v3 NOIMOD parameter. Specifying NLEV invokes the HSPICE noise model. See Noise Models on page 96 for more information. If you do not specify NLEV, simulation invokes the Berkeley noise equations.

Performance Improvements

To improve the performance of Levels 49 and 53 reduce the complexity of model equations, replacing some calculations with spline functions and compiler optimization. For Level 49, the result is a reduction in simulation time of up to 40% compared to releases before 97.4 while maintaining accuracy to 5 digits or better. To use the spline functions, set the SFVTFLAG=1 model parameter in the model card. SFVTFLAG=0, the default value, disables the spline functions. For Level 53, all BSIM3v3 non-compliant features default to off.

Reduced Parameter Set BSIM3v3 Model (BSIM3-lite)

Setting the LITE=1 model parameter in Level 49 to invoke the BSIM3v3-lite reduced parameter set model. Use it with model binning. Without binning to account for geometry effects, the full BSIM3v3 model specifies several model parameters. However, it is often difficult to extract a “global” BSIM3v3 model that is accurate over the entire geometry range.

To improve accuracy over a range of geometries, you can bin the model parameters. That is, this model divides the entire length-width geometry range into rectangular regions or bins. Simulation extracts a different set of parameters for each bin. The built-in bilinear parameter interpolation scheme maintains continuity (over length-width) at the boundaries between bins. Because many BSIM3 model parameters account for MOSFET geometry effects, these geometry-effect parameters are redundant. You can eliminate them when you use binning.

The BSIM3-lite model parameter set was created in response to the question: What BSIM3 parameters should be excluded when using a binned model? To invoke the BSIM3-lite model, specify the LITE=1 model parameter in the model card.

Simulation checks the model card to determine if it conforms to the BSIM3-lite parameter set. BSIM3-lite takes advantage of the smaller number of calculations, and reduces simulation times by up to 10% compared to the full parameter set BSIM3 model. Only Level 49 supports LITE=1.

Table 94 lists model parameters (total 49) that the BSIM3-lite model excludes. Either exclude all parameters in this list from the model card or explicitly set them to the default value specified in the list. In some cases, as noted, the BSIM3-lite default value differs from the standard BSIM3v3 default value. You should also exclude WR, ALPHA0, and CIT, but the BSIM3-lite model card does not require this exclusion.

Table 94 Parameters Excluded from BSIM3-Lite

Parameter	Comments
mobmod	Recommended default or set = 1
nqsmod	Recommended default or set = 0
toxm	default = tox
ll	default = 0
lln	default = 1
lw	default = 0
lwn	default = 1
lwl	default = 0
wl	default = 0
wln	default = 1
ww	default = 0
wwn	default = 1
wwl	default = 0
dwg	default = 0
dwb	default = 0
llc	default = 0
lwc	default = 0

Table 94 Parameters Excluded from BSIM3-Lite (Continued)

Parameter	Comments
lwlc	default = 0
wlc	default = 0
wwc	default = 0
wwlc	default = 0
b0	default = 0
b1	default = 0
vbx	do not define
vbm	do not define
xt	do not define
nsub	do not define
nlx	default = 0, std default=1.74e-7
gamma1	do not define
gamma2	do not define
ngate	Recommended default or set = 0
k3	default = 0, std default=80
k3b	default = 0
w0	no effect
dvt0	default = 0, std default=2.2
dvt1	default = 0, std default=0.53
dvt2	default = 0, std default=-0.032
dvt0w	default = 0

Table 94 Parameters Excluded from BSIM3-Lite (Continued)

Parameter	Comments
dvt1w	default = 0, std default=5.3e6
dvt2w	default = 0, std default=-0.032
dsub	default = 0
prwg	default = 0
prwb	default = 0
wr	Recommended default or set = 1
drout	default = 0, std default=0.56
pdiblc1	default = 0, std default=0.39
cit	Recommended default or set = 0
alpha0	Recommended default or set = 0 for Version 3.2
kt1l	default = 0

Parameter Binning

To support parameter binning, Berkeley BSIM3v3 specifies LWP parameters. To bilinearly interpolate a subset of model parameters over 1/Leff and 1/Weff, you specify four terms:

- Xo parameter
- X length term
- Xw width term
- Xp product term.

Simulation then interpolates the parameter value at a specified L,W:

```
X = Xo + Xl/Leff + Xw/Weff + Xp/Leff/Weff
```

See Parameter Range Limits on page 428 to determine whether you can bin a parameter. Simulation adds the LMIN, LMAX, WMIN, WMAX, LREF, and WREF parameters to allow multiple cell binning. LMIN, LMAX, WMIN, WMAX

define the cell boundary. LREF and WREF are offset values that provide a convenient interpolation scheme. Simulation uses the LREF and WREF offsets if you define both values and you specify the BINFLAG>0.9 model parameter.

Simulation then interpolates the parameter value at a specified L,W:

```
X = Xo + Xl*(1/Leff - 1/LREF) + Xw*(1/Weff - 1/WREF)
+ Xp/(1/Leff - 1/LREF)/(1/Weff - 1/WREF)
```

To select micron units for the lwp geometry parameters, set the BINUNIT = 1 model parameter. For other choices of BINUNIT, the lengths are in units of meters. Simulation handles the XL, XLREF, XW, and XWREF parameters in a manner consistent with other Synopsys MOSFET models, and they produce shifts in parameter values without disrupting the continuity across the bin boundaries.

Charge Models

In BSIM3v3, the BSIM1 capacitance model is CAPMOD=0. Simulation replaces this with a modified BSIM1 capacitance model, based on the CAPOP=13 model in Level 49. Level 53 uses the Berkeley BSIM1 capacitance model for CAPMOD=0. Table 95 lists CAPMOD defaults for the Berkeley BSIM3v3 model, and for Levels 49 and 53.

Table 95 MOSFET Charge Model Versions

Version	BSIM3v3	Level 49	Level 53
3.0	1	1	1
3.1	2	0	2
3.2	3	3	3

VFBFLAG

The CAPMOD=0 capacitance model normally calculates the threshold voltage as Vth = vfbc + phi + k1 * sqrt(phi - vbs), where vfbc is the VFBCV model parameter. This eliminates any dependence on the VTH0 parameter. To allow capacitance dependence on VTH0, set the VFBFLAG=1 model parameter. The CAPMOD=0 capacitance model calculates the threshold voltage as Vth = vth0 + k1 * sqrt(phi - vbs) - k1 * sqrt(phi). The VFBFLAG default value is 0.

Printback

You can printback all model parameters with units. The printback also indicates whether Berkeley or Synopsys model junction diodes and noise models are invoked, and which parameters are not used (for example, simulation does not use CJGATE if ACM=0-3).

Mobility Multiplier

You can define mobility multiplier parameters in the BSIM3V3 instance line.

Name	Default	Description
mulu0	1.0	Low-field mobility (U0) multiplier
mulua	1.0	First-order mobility degradation coefficient (UA) multiplier
mulub	1.0	Second-order mobility degradation coefficient (UB) multiplier

When HSPICE prints back a MOSFET element summary (**.OPTION** LIST), it identifies the BSIM3V3 MOSFET, and prints back these three additional instance parameters.

Using BSIM3v3

Note the following points when you use BSIM3v3 with a Synopsys circuit simulator:

- Use either the Level 49 or Level 53 model. Level 53 fully complies with the Berkeley BSIM3v3 release. In most cases Level 49 returns the same results as Level 53, runs as fast or faster, shows better convergence, and allows a wider range of parameter specifications.
- Explicitly set all Berkeley-specific BSIM3 model parameters in the model card. This minimizes problems resulting from version changes and compatibility with other simulators. You do not explicitly set all lwp binning parameters.

- To match results with simulations from previous HSPICE versions, use the HSPVER=YY.N model parameter, such as HSPVER=97.4. Do not use the full year specification (such as 1997.4). The patch version number format is HSPVER=YY.NN (for example, HSPVER=98.21 is release 98.2.1).
- Levels 49 and 53 support the TNOM model parameter name as an alias for TREF. The conventional terminology in HSPICE is TREF, which all Synopsys model MOS levels support as a model parameter. Both Levels 49 and 53 support the TNOM alternative name for compatibility with SPICE3.

  The default room temperature is 25^{o}C in Synopsys circuit simulators, but is 27^{o}C in SPICE3. If you specify the BSIM3 model parameters at 27^{o}C, add TNOM=27 to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add **.OPTION** TNOM=27 to the netlist when you test the Synopsys model versus SPICE3.

  You can use DELVTO and DTEMP on the element line with Levels 49 and 53. The following equation converts the temperature setup between the Synopsys model and SPICE3:

```
SPICE3:       .OPTION TEMP=125
      .MODEL NCH NMOS Level=8
      + TNOM =27 ...
Synopsys Model:       .TEMP 125
      .MODEL NCH NMOS Level=49
      + TNOM =27 ...
```

- To automatically calculate the drain, source area, and perimeter factors for Berkeley junction diode models, use ACM=12 with CALCACM=1. Normally, ACM=10-13 defaults the area and perimeter factors to 0. To override this value for ACM=12, specify CALCACM=1. Define the HSPICE-specific parameter (HDIF) in the model card. If you do not want parasitic Rs and Rd with the BSIM3v3 internal Rsd, either do not specify the RSH, RSC, RDC, RS, and RD HSPICE parameters (default is 0) or set them to 0.
- Simulation and analysis either warns or aborts with a fatal error if certain model parameter values are out of a normal range. To view all warnings, you might need to increase the **.OPTION** WARNLIMIT value (default=1). To turn on full parameter range checking, set the PARAMCHK=1 model parameter (default is 0). If you use PARAMCHK=0, simulation checks a smaller set of parameters. (See Parameter Range Limits on page 428 for more details about parameter limits.) Use the APWARN=1 model parameter (default=0) to turn off PS,PD < Weff warnings.
- Use NQSMOD only with Version 3.2, and specify it only in the model card.

Level 49, 53 Model Parameters

The following tables describe all Level 49 and Level 53 model parameters, including:

- parameter name
- units
- default value
- whether you can bin the parameter
- a description

These tables are a superset of the BSIM3v3 model parameter set, and include HSPICE parameters. These HSPICE parameters are noted in the description column, and always default (for Level 53) to maintain compliance with the BSIM3v3 standard. These parameters also apply to Level 49 with the following exceptions:

- ACM default value = 0
- XPART default value = 1
- CAPMOD default value = 0.

Table 96 Model Flags for MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VERSION	-	3.2	No	Selects from BSIM3 Versions 3.0, 3.1, 3.2. Issues a warning if you do not explicitly set it.
HSPVER	-	98.2	No	Selects from HSPICE Versions: 98.2, 97.4, 97.2, 96.4, 96.3, 96.1
PARAMCHK	-	0	No	PARAMCHK=1 checks the model parameters for range compliance
APWARN	-	0	No	When >0 turns off the warning message for PS,PD < Weff (HSPICE specific)
BINFLAG	-	0	No	Uses wref, lref if you set this flag >0.9 (HSPICE)
MOBMOD	-	1	No	Selects a mobility model

Table 96 Model Flags for MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
CAPMOD	-	3	No	Selects from the 0,1,2,3 charge models Level 49 CAPMOD defaults to 0.
CAPOP	-	-	No	Obsolete for Levels 49 and 53. HSPICE ignores it (HSPICE specific) in all versions.
NOIMOD	-	1	No	Berkeley noise model flag
NLEV	-	-(off)	No	The noise model flag (non-zero overrides NOIMOD) (HSPICE specific). See Noise Models on page 96 for more information.
NQSMOD	-	0 (off)	No	NQS Model flag
SFVTFLAG	-	0 (off)	No	Spline function for Vth (HSPICE specific)
VFBFLAG	-	0 (off)	No	VFB selector for CAPMOD=0 (HSPICE specific)

Table 97 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VGSLIM	V	0	No	Asymptotic Vgs value, The Min value is 5V. 0-value indicates an asymptote of infinity. (HSPICE and Level 49 specific)
TOX	m	150e-10	No	Gate oxide thickness
XJ	m	0.15e-6	Yes	Junction depth
NGATE	cm^{-3}	0	Yes	Poly gate doping concentration
VTH0 (VTHO)	V	0.7 NMOS -0.7 PMOS	Yes	Threshold voltage of the long channel device at V_{bs} = 0 and small V_{ds}
NSUB	cm^{-3}	6.0e16	Yes	Substrate doping concentration

Table 97 Basic Model Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
NCH	cm^{-3} See [6]	1.7e17	Yes	Peak doping concentration near the interface
NLX	m	1.74e-7	Yes	Lateral nonuniform doping along the channel
K1	$V^{1/2}$	0.50	Yes	First-order body effect coefficient
K2	-	-0.0186	Yes	Second-order body effect coefficient
K3	-	80.0	Yes	Narrow width effect coefficient
K3B	1/V	0	Yes	Body width coefficient, narrow width effect
W0	m	2.5e-6	Yes	Narrow width effect coefficient
DVT0W	1/m	0	Yes	Narrow width coefficient 0 for Vth, small L
DVT1W	1/m	5.3e6	Yes	Narrow width coefficient 1 for Vth, small L
DVT2W	1/V	-0.032	Yes	Narrow width coefficient 2 for Vth, small L
DVT0	-	2.2	Yes	Short channel effect coefficient 0 for V_{th}
DVT1	-	0.53	Yes	Short channel effect coefficient 1 for V_{th}
DVT2	1/V	-0.032	Yes	Short channel effect coefficient 2 for V_{th}
ETA0	-	0.08	Yes	DIBL (drain induced barrier lowering) coefficient for the subthreshold region
ETAB	1/V	-0.07	Yes	DIBL coefficient for the subthreshold region
DSUB	-	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
VBM	V	-3.0	Yes	Maximum substrate bias for calculating V_{th}
U0	$cm^2/V/sec$	670 nmos 250 pmos	Yes	Low field mobility at T = *TREF* = *TNOM*
UA	m/V	2.25e-9	Yes	First-order mobility degradation coefficient

Table 97 Basic Model Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
UB	m^2/V^2	5.87e-19	Yes	Second-order mobility degradation coefficient
UC	1/V	-4.65e-11 or -0.0465	Yes	Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD = 3
A0	-	1.0	Yes	Bulk charge effect coefficient, channel length
AGS	1/V	0.0	Yes	Gate bias coefficient of Abulk
B0	m	0.0	Yes	Bulk charge effect coefficient, channel width
B1	m	0.0	Yes	Bulk charge effect width offset
KETA	1/V	-0.047	Yes	Body-bias coefficient of the bulk charge effect
VOFF	V	-0.08	Yes	Offset voltage in the subthreshold region
VSAT	m/sec	8e4	Yes	Saturation velocity of the carrier at T = *TREF* = *TNOM*
A1	1/V	0	Yes	First nonsaturation factor
A2	-	1.0	Yes	Second nonsaturation factor
RDSW	ohm · μm	0.0	Yes	Parasitic source drain resistance per unit width
PRWG	1/V	0	Yes	Gate bias effect coefficient of RDSW
PRWB	$1/V^{1/2}$	0	Yes	Body effect coefficient of RDSW
WR	-	1.0	Yes	Width offset from Weff for the Rds calculation
NFACTOR	-	1.0	Yes	Subthreshold region swing
CIT	F/m^2	0.0	Yes	Interface state capacitance

Table 97 Basic Model Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
CDSC	F/m^2	2.4e-4	Yes	Drain/source and channel coupling capacitance
CDSCD	F/Vm^2	0	Yes	Drain bias sensitivity of CDSC
CDSCB	F/Vm^2	0	Yes	Body coefficient for CDSC
PCLM	-	1.3	Yes	Coefficient of the channel length modulation values ≤ 0 result in an error message and program exit.
PDIBLC1	-	0.39	Yes	Coefficient 1 for the DIBL (drain induced barrier lowering) effect
PDIBLC2	-	0.0086	Yes	Coefficient 2 for the DIBL effect
PDIBLCB	1/V	0	Yes	Body effect coefficient of the DIBL effect coefficients
DROUT	-	0.56	Yes	Length dependence coefficient of the DIBL correction parameter in R_{out}
PSCBE1	V/m	4.24e8	Yes	Exponent 1 for the substrate current induced body effect
PSCBE2	V/m	1.0e-5	Yes	Coefficient 2 for the substrate current induced body effect
PVAG	-	0	Yes	Gate dependence of Early voltage
DELTA	V	0.01	Yes	Effective Vds parameter
ALPHA0	m/V	0	Yes	First parameter of the impact ionization current
BETA0	V	30	Yes	Second parameter of the impact ionization current
RSH	0.0	ohm/square	No	Source/drain sheet resistance in ohm per square

Table 98 AC and Capacitance Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
XPART	-	0	No	Charge partitioning rate flag (default deviates from BSIM3V3=0) Level 49 XPART defaults to 1
CGSO	F/m	p1 (see [1])	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGDO	F/m	p2 (see [2])	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGBO	F/m	0	No	Gate-bulk overlap capacitance per unit channel length
CGS1	F/m	0.0	Yes	Lightly-doped source-gate overlap region capacitance
CGD1	F/m	0.0	Yes	Lightly-doped drain-gate overlap region capacitance
CKAPPA	F/m	0.6	Yes	Coefficient for the lightly-doped region overlap capacitance fringing field capacitance
CF	F/m	([3])	Yes	Fringing field capacitance
CLC	m	0.1e-6	Yes	Constant term for short channel model
CLE	-	0.6	Yes	Exponential term, short channel model
VFBCV	V	-1.0	Yes	Flat band voltage, used only in CAPMOD=0 C-V calculations

Table 99 Length and Width Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
WINT	m	0.0	No	Width offset fitting parameter from I-V without bias
WLN	-	1.0	No	Power of the length dependence of the width offset
WW	m^{WWN}	0.0	No	Coefficient of the width dependence for the width offset

Table 99 Length and Width Parameters, MOSFET 49/53 (Continued)

Name	Unit	Default	Bin	Description
WWN	-	1.0	No	Power of the width depends on the width offset.
WWL	m^{WWN} *m^{WLN}	0.0	No	Coefficient of the length and width cross term for the width offset
DWG	m/V	0.0	Yes	Coefficient of the gate dependence for Weff
DWB	$m/V^{1/2}$	0.0	Yes	Coefficient of the substrate body bias dependence for Weff
LINT	m	0.0	No	Length offset fitting the parameter from the I-V without the bias
LL	m^{LLN}	0.0	No	Coefficient of the length dependence for the length offset
LLN	-	1.0	No	Power of the length dependence of the length offset
LW	m^{LWN}	0.0	No	Coefficient of the width dependence for the length offset
LWN	-	1.0	No	Power of the width dependence of the length offset
LWL	m^{LWN} *m^{LLN}	0.0	No	Coefficient of the length and width cross term for the length offset
DLC	m	LINT	No	Length offset fitting parameter from CV
DWC	m	WINT	No	Width offset fitting parameter from CV

Table 100 Temperature Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
KT1	V	-0.11	Yes	Temperature coefficient for Vth
KT1L	m-V	0.0	Yes	Temperature coefficient for the channel length dependence of Vth
KT2	-	0.022	Yes	Body bias coefficient of the Vth temperature effect
UTE	-	-1.5	Yes	Mobility temperature exponent

Table 100 Temperature Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
UA1	m/V	4.31e-9	Yes	Temperature coefficient for UA
UB1	$(m/V)^2$	-7.61e-18	Yes	Temperature coefficient for UB
UC1	m/V^2	-5.69e-11	Yes	Temperature coefficient for UC
AT	m/sec	3.3e4	Yes	Temperature coefficient for the saturation velocity
PRT	ohm-um	0	Yes	Temperature coefficient for RDSW
XTI	-	3.0	No	Junction current temperature exponent

Table 101 Bin Description Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
LMIN	m	0.0	No	Minimum channel length
LMAX	m	1.0	No	Maximum channel length
WMIN	m	0.0	No	Minimum channel width
WMAX	m	1.0	No	Maximum channel width
BINUNIT				Assumes that weff, leff, wref, lref units are in microns if BINUNIT=1 or in meters otherwise

Table 102 Process Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
DTOXCV (capmod=3 only)				Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and finite channel charge layer thickness.
GAMMA1	$V^{1/2}$	[8]	Yes	Body effect coefficient near the surface

Table 102 Process Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
GAMMA2	$V^{1/2}$	[9]	Yes	Body effect coefficient in the bulk
VBX	V	[10]	Yes	VBX at which the depletion region width equals XT
XT	m	1.55e-7	Yes	Doping depth

Table 103 Noise Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
NIOA	-	1.0e20 nmos 9.9e18 pmos	No	Body effect coefficient near the surface
NOIB	-	5.0e4 nmos 2.4e3 pmos	No	Body effect coefficient in the bulk
NOIC	-	-1.4e-12 nmos 1.4e-12 pmos	No	VBX at which the depletion region width equals XT
EM	V/m	$4.1e^{7}$	No	Flicker noise parameter
AF	-	1.0	No	Flicker noise exponent
KF	-	0.0	No	Flicker noise coefficient
EF	-	1.0	No	Flicker noise frequency exponent

Note: See also Noise Models on page 96 for HSPICE noise model usage (the NLEV parameter for HSPICE overrides Berkeley NOIMOD parameter).

Table 104 Junction Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
ACM	-	10	No	Area calculation method selector (HSPICE specific) • ACM=0-3 uses the HSPICE junction models • ACM=10-13 uses the Berkeley junction models Level 49 ACM defaults to 0
JS	A/m^2	0.0	No	Bulk junction saturation current. (Default deviates from BSIM3v3 = $1.0e^{-4}$)
JSW	A/m	0.0	No	Sidewall bulk junction saturation current
NJ	-	1	No	Emission coefficient (use only with the Berkeley junction model: ACM=10-13)
N	-	1	No	Emission coefficient (HSPICE-specific), (use only with the HSPICE junction model,ACM=0-3)
CJ	F/m^2	$5.79e^{-4}$	No	Zero-bias bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-4}$)
CJSW	F/m	0.0	No	Zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-10}$)
CJSWG	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (use only with the Berkeley junction model, ACM=10-13)
CJGATE	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (HSPICE-specific) (use only if ACM=3)
PB, PHIB	V	1.0	No	Bulk junction contact potential
PBSW	V	1.0	No	Sidewall bulk junction contact potential
PHP	V	1.0	No	Sidewall bulk junction contact potential (HSPICE) (use only with the HSPICE junction model: ACM=0-3)

Table 104 Junction Parameters, MOSFET Levels 49/53 (Continued)

Name	Unit	Default	Bin	Description
PBSWG	V	PBSW	No	Gate-edge sidewall bulk junction contact potential (use only with the Berkeley junction model, ACM=10-13). HSPICE has no equivalent parameter. Gate-edge contact potential is always set to PHP for the HSPICE junction model.
MJ	-	0.5	No	Bulk junction grading coefficient
MJSW	-	0.33	No	Sidewall bulk junction grading coefficient
MJSWG	-	MJSW	No	Gate-edge sidewall bulk junction grading coefficient (use only with the Berkeley junction model: ACM=10-13) HSPICE has no equivalent parameter. Always set the gate-edge grading coefficient to MJSW for the HSPICE junction model.

Note: See MOSFET Diode Models on page 39 for HSPICE junction diode model usage.

Table 105 NonQuasi-Static (NQS) Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
ELM	-	5.0	Yes	Elmore constant

Table 106 MOSFET Levels 49/53 Version 3.2 Parameters

Name	Unit	Default	Bin	Description
TOXM	m	TOX	No	Reference gate oxide thickness
VFB	V	[11]	Yes	DC flatband voltage
NOFF	-	1.0	Yes	I-V parameter, weak to strong inversion transition
VOFFCV	-	0.0	Yes	C-V parameter, weak to strong inversion transition

Table 106 MOSFET Levels 49/53 Version 3.2 Parameters (Continued)

Name	Unit	Default	Bin	Description
JTH	A	0.1	No	Diode limiting current
ALPHA1	V^{-1}	0.0	Yes	Substrate current parameter
ACDE	m/V	1.0	Yes	Exponential coefficient for the charge thickness in the accumulation and depletion regions
MOIN	m/V	15.0	Yes	Coefficient, gate-bias dependent surface potential
TPB	V/K	0.0	No	Temperature coefficient of PB
TPBSW	V/K	0.0	No	Temperature coefficient of PBSW
TPBSWG	V/K	0.0	No	Temperature coefficient of PBSWG
TCJ	V/K	0.0	No	Temperature coefficient of CJ
TCJSW	V/K	0.0	No	Temperature coefficient of CJSW
TCJSWG	V/K	0.0	No	Temperature coefficient of CJSWG
LLC	m^{lln}	LL	No	Coefficient of the length dependence for the C-V channel length offset
LWC	m^{lwn}	LW	No	Coefficient of the width dependence for the C-V channel length offset
LWLC	$m^{lln+lwn}$	LWL	No	Coefficient of the length and width for the C-V channel length offset
WLC	m^{wln}	WL	No	Coefficient of the length dependence for the C-V channel width offset
WWC	m^{wwn}	WW	No	Coefficient of the width dependence for the C-V channel width offset
WWLC	$m^{wln+wwn}$	WWL	No	Coefficient of the length and width cross terms for the C-V channel width offset

Notes:

1. If you do not specify C_{gso}, simulation calculates it as follows:
   - If you specify a *dlc* value that is greater than 0.0, then,

     ```
     cgso = p1 = max(0,dlc*cox - cgs1)
     ```

   - Otherwise, *cgso = 0.6*xj*cox*
2. If you do not specify C_{gdo}, simulation calculates it as follows:
   - if you specify a *dlc* value that is greater than 0.0, then,

     ```
     cgdo = p2 = max(0,dlc*cox - cgd1)
     ```

   - Otherwise *cgdo = 0.6*xj*cox*
3. If you do not specify C_f, simulation calculates it using:

$$C_f = \frac{2\varepsilon_{ox}}{\pi}\log\left(1 + \frac{4\times10^{-7}}{T_{ox}}\right)$$

4. If you do not specify V_{th0} in the **.MODEL** statement, simulation calculates it with V_{fb} = -1, using:

$$V_{th0} = V_{fb} + \phi_s + K_1\sqrt{\phi_s}$$

5. If you do not specify K_1 and K_2, simulation calculates it using:

$$K_1 = GAMMA_2 + 2K_2\sqrt{\phi_s - V_{bs}}$$

$$K_2 = \frac{(GAMMA_2 - GAMMA_1)(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

6. If you do not specify n_{ch}, but you specify $GAMMA_1$, then simulation calculates n_{ch} from:

$$n_{ch} = \frac{GAMMA_1{}^2 C_{OX}{}^2}{2q\varepsilon_{si}}$$

   If you do not specify n_{ch} or $GAMMA_1$, then *nch* defaults to 1.7e17 per cubic meter and simulation calculates $GAMMA_1$ from n_{ch}.

7. If you do not specify *PHI*, simulation calculates it using:

$$\phi_s = 2\frac{k_B T}{q}\log\left(\frac{n_{ch}}{n_i}\right)$$

$$n_i = 1.45\times 10^{10}\left(\frac{T}{300.15}\right)^{1.5}\exp\left(21.5565981 - \frac{qE_g(T)}{2k_B T}\right)$$

$$E_g(T) = 1.16 - \frac{7.02\times 10^{-4}T^2}{T + 1108}$$

8. If you do not specify $GAMMA_1$, simulation calculates it using:

$$GAMMA_1 = \frac{\sqrt{2q\varepsilon_{si}n_{ch}}}{C_{ox}}$$

9. If you do not specify $GAMMA_2$, simulation calculates it using:

$$GAMMA_2 = \frac{\sqrt{2q\varepsilon_{si}n_{sub}}}{C_{ox}}$$

10. If you do not specify V_{bx}, simulation calculates it using:

$$V_{bx} = \phi_s - \frac{qn_{ch}X_t^2}{2\varepsilon_{si}}$$

11. The BSIM3 model can calculate V_{th} in any of three ways:
    - Using *K1* and *K2* values that you specify
    - Using *GAMMA1*, *GAMMA2*, *VBM*, and *VBX* values that you enter in the **.MODEL** statement
    - Using *NPEAK*, *NSUB*, *XT*, and *VBM* values that you specify

You can enter the U0 model parameter in meters or centimeters. Simulation converts U0 to m^2/Vsec as follows: if U0 is greater than 1, it is multiplied by 1e-4. You must enter the NSUB parameter in
cm^{-3} units.

Specify a negative value of VTH0 for the p-channel in the **.MODEL** statement.

The PSCBE1 and PSCBE2 model parameters determine the impact ionization current, which contributes to the bulk current.

Parameter Range Limits

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems. Level 53 follows exactly the BSIM3v3 range limit reporting scheme. Level 49 deviates from the BSIM3v3 scheme as noted in the comments column of Table 107.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding **.OPTION** statement, # is the maximum number of warning messages that simulation reports. The default WARNLIMIT value is 1. In some cases (as noted in Table 107), simulation checks parameters only if you set the PARMAMCHK=1 model parameter.

Table 107 Model Parameter Range Limit, Levels 49/53

Name	Limits	Comments
TOX	<= 0 Fatal < 10-9 Warn if parmchk=1	
TOXM	<= 0 Fatal < 10-9 Warn if parmchk=1	
XJ	<= 0 Fatal	
NGATE	< 0 Fatal > 10^{25} Fatal <= 10^{18} Fatal if parmchk=1	if >10^{23} simulation multiplies NGATE by 10^{-6} before the other limit checks. Level 49 returns: < 0 Fatal > 10^{25} Warn <= 10^{18} Warn if paramchk==1
NSUB	<= 0 Fatal <= 10^{14} Warn if parmchk=1 >= 10^{21} Warn if parmchk=1	Ignores NSUB if k1,k2 are defined
NLX	< -Leff Fatal < 0 Warn if parmchk=1	

Table 107 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
NCH	<= 0 Fatal <= 10^{15} Warn if parmchk=1 >= 10^{21} Warn if parmchk=1	if >10^{20} simulation multiplies NCH by 10^{-6} before the other limit checks.
DVT1W	< 0 Fatal	< 0 Level 49 reports a warning
DVT0	< 0 Warn if paramchk=1	
DVT1	< 0 Fatal	< 0 Level 49 reports a warning
ETA0	<= 0 Warn if paramchk=1	
DSUB	< 0 Fatal	< 0 Level 49 reports a warning
VBM		Ignored if you defined K1 and K2
U0	<= 0 Fatal	
B1	= -Weff Fatal B1 + Weff < 10^{-7} Warn if paramchk=1	
VSAT	<= 0 Fatal < 10^{3} Warn if paramchk==1	
A1	-	See a2 conditions on the next line
A2	• < 0.01 Warn and reset a2=0.01 if paramchk=1 • > 1 Warn and reset a2=1,a1=0 if paramchk=1	
DELTA	< 0 Fatal	
RDSW	< 0.001 Warn if paramchk=1 and reset rdsw=0	
NFACTOR	< 0 Warn if paramchk=1	
CDSC	< 0 Warn if paramchk=1	
CDSCD	< 0 Warn if paramchk=1	

Table 107 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
PCLM	<= 0 Fatal	
PDIBLC1	< 0 Warn if paramchk=1	
PDIBLC2	< 0 Warn if paramchk=1	
PS	< Weff Warn	
W0	= -Weff Fatal w0 + Weff < 10^{-7} Warn if paramchk==1	
DROUT	< 0 Fatal if paramchk=1	Level 49 reports a warning
PSCBE2	<= 0 warn if paramchk=1	
CGS0	< 0 Warn and reset to 0 if paramchk=1	
CGD0	< 0 Warn and reset to 0 if paramchk=1	
CGB0	< 0 Warn and reset to 0 if paramchk=1	
ACDE	< 0.4, >1.6 Warn	
MOIN	< 5.0, >25 Warn	
IJTH	< 0 Fatal	
NOFF	< 0.1, >4.0 Warn	

Table 108 Element Parameter Range Limit, MOSFET Levels 49/53

Name	Limits	Comments
PD	< Weff, Warn	
PS	< Weff, Warn	

Table 108 Element Parameter Range Limit, MOSFET Levels 49/53 (Continued)

Leff	< 5.0 x 10^{-8} Fatal
Weff	< 1.0 x 10^{-7} Fatal
LeffCV	< 5.0 x 10^{-8} Fatal
WeffCV	< 1.0 x 10^{-7} Fatal

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 14.

Level 49, 53 Equations

The effective channel length and width in all model equations are:

$$L_{eff} = L_{drawn} - 2dL \qquad W_{eff} = W_{drawn} - 2dW \qquad W'_{eff} = W_{drawn} - 2dW'$$

Wdrawn = W * WMULT + XW
Ldrawn = L * LMULT + XL

- The unprimed W_{eff} is bias-dependent.
- The primed quantity is bias-independent.

$$dW = dW' + dW_g V_{gsteff} + dW_b(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})$$

$$dW' = W_{int} + \frac{W_L}{L^{WLN}} + \frac{W_W}{W^{WWN}} + \frac{W_{WL}}{L^{WLN} W^{WWN}}$$

$$dL = L_{int} + \frac{L_L}{L^{LLN}} + \frac{L_W}{W^{LWN}} + \frac{L_{WL}}{L^{LLN} W^{LWN}}$$

C-V calculations replace dW’ with:

$$dW' = DWC + \frac{W_{LC}}{L^{WLN}} + \frac{W_{WC}}{W^{WWN}} + \frac{W_{WLC}}{L^{WLN} W^{WWN}}$$

C-V also replaces dL’ with:

$$dL = DLC + \frac{L_{LC}}{L^{LLN}} + \frac{L_{WC}}{W^{LWN}} + \frac{L_{WLC}}{L^{LLN}W^{LWN}}$$

Note: For details of BSIM3 Version 3 equations, see the web site:

http://www-device.eecs.berkeley.edu/~bsim3/get.html

.MODEL CARDS NMOS Model

This is an example of a NMOS model for the Level 49 MOSFET. VTH0 is positive.

```
.model nch nmos Level=49
+ Tnom=27.0
+ nch=1.024685E+17 tox=1.00000E-08 xj=1.00000E-07
+ lint=3.75860E-08 wint=-2.02101528644562E-07
+ vth0=.6094574 k1=.5341038 k2=1.703463E-03 k3=-17.24589
+ dvt0=.1767506 dvt1=.5109418 dvt2=-0.05
+ nlx=9.979638E-08 w0=1e-6
+ k3b=4.139039
+ vsat=97662.05 ua=-1.748481E-09 ub=3.178541E-18 uc=1.3623e-10
+ rdsw=298.873 u0=307.2991 prwb=-2.24e-4
+ a0=.4976366
+ keta=-2.195445E-02 a1=.0332883 a2=.9
+ voff=-9.623903E-02 nFactor=.8408191 cit=3.994609E-04
+ cdsc=1.130797E-04
+ cdscb=2.4e-5
+ eta0=.0145072 etab=-3.870303E-03
+ dsub=.4116711
+ pclm=1.813153 pdiblc1=2.003703E-02 pdiblc2=.00129051
+ pdiblcb=-1.034e-3
+ drout=.4380235 pscbe1=5.752058E+08 pscbe2=7.510319E-05
+ pvag=.6370527 prt=68.7 ngate=1.e20 alpha0=1.e-7 beta0=28.4
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=1e-8
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
```

```
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

PMOS Model

This is an example of a PMOS model for the Level 49 MOSFET. VTH0 is negative.

```
.model pch PMOS Level=49
+ Tnom=27.0
+ nch=5.73068E+16 tox=1.00000E-08 xj=1.00000E-07
+ lint=8.195860E-08 wint=-1.821562E-07
+ vth0=-.86094574 k1=.341038 k2=2.703463E-02 k3=12.24589
+ dvt0=.767506 dvt1=.65109418 dvt2=-0.145
+ nlx=1.979638E-07 w0=1.1e-6
+ k3b=-2.4139039
+ vsat=60362.05 ua=1.348481E-09 ub=3.178541E-19 uc=1.1623e-10
+ rdsw=498.873 u0=137.2991 prwb=-1.2e-5
+ a0=.3276366
+ keta=-1.8195445E-02 a1=.0232883 a2=.9
+ voff=-6.623903E-02 nFactor=1.0408191 cit=4.994609E-04
+ cdsc=1.030797E-3
+ cdscb=2.84e-4
+ eta0=.0245072 etab=-1.570303E-03
+ dsub=.24116711
+ pclm=2.6813153 pdiblc1=4.003703E-02 pdiblc2=.00329051
+ pdiblcb=-2.e-4
+ drout=.1380235 pscbe1=0 pscbe2=1.e-28
+ pvag=-.16370527
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03 prt=76.4
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=0
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

Level 54 BSIM4 Model

The UC Berkeley BSIM4 model explicitly addresses many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The Level 54 model is based on the UC Berkeley BSIM4 MOS model. BSIM4.4 is fully supported in this release. For details, see the BSIM web site:

http://www-device.eecs.berkeley.edu/

General Form

```
Mxxx nd ng ns <nb> mname <L=val> <W=val> <M=val>
 + <AD=val> <AS=val> <PD=val> <PS=val>
 + <RGATEMOD=val> <RBODYMOD=val> <TRNQSMOD=val>
 + <ACNQSMOD=val> <GEOMOD=val> <RGEOMOD=val>
 + <NRS=val> <NRD=val> <RBPB=val> <RBPD=val>
 + <RBPS=val> <RBDB=val> <RBSB=val> <NF=val>
 + <MIN=val> <RDC=val> <RSC=val> <DELVTO=val>
 + <MULU0=val> <DELK1=val> <DELNFCT=val>
 + <DELTOX=val> <OFF> <IC=Vds, Vgs, Vbs>
 + <WNFLAG=val>
```

Parameter	Description
ACNQSMOD	AC small-signal NQS model selector.
AD	Drain diffusion area.
AS	Source diffusion area.
DELK1	Shift in body bias coefficient (K1).
DELNFCT	Shift in subthreshold swing factor (NFACTOR).
DELTOX	Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/ insulator thicknesses.
DELVTO (DELVT0)	Shift in the VTH0 zero-bias threshold voltage.

Parameter	Description
GEOMOD	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect.
IC	Initial guess in the order
L	BSIM4 MOSFET channel length in meters.
MIN	Whether to minimize the number of drain or source diffusions for even-number fingered device.
mname	MOSFET model name reference.
MULU0	Low-field mobility (U0) multiplier.
nb	Bulk terminal node name.
nd	Drain terminal node name.
NF	Number of device fingers.
ng	Gate terminal node name.
NRD	Number of drain diffusion squares.
NRS	Number of source diffusion squares.
ns	Source terminal node name.
OFF	Sets the initial condition to OFF in DC analysis.
PD	Perimeter of the drain junction: • If PERMOD=0, it excludes the gate edge. • Otherwise, it includes the gate edge.
PS	Perimeter of the source junction: • If PERMOD=0, it excludes the gate edge. • Otherwise, it includes the gate edge.
RBDB	Resistance connected between dbNode and bNode.
RBODYMOD	Substrate resistance network model selector.

Parameter	Description
RBPB	Resistance connected between bNodePrime and bNode.
RBPD	Resistance connected between bNodePrime and dbNode.
RBPS	Resistance connected between bNodePrime and sbNode.
RBSB	Resistance connected between sbNode and bNode.
RDC	Drain contact resistance for per-finger device.
RGATEMOD	Gate resistance model selector.
RGEOMOD	Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance.
RSC	Source contact resistance for per-finger device.
TRNQSMOD	Transient NQS model selector.
W	BSIM4 MOSFET channel width in meters.
WNFLAG	Turn on to select bin model based on width per NF for multi-finger devices.

Improvements Over BSIM3v3

BSIM4 includes the following major improvements and additions over BSIM3v3:

- An accurate new model of the intrinsic input resistance (Rii) for both RF, high-frequency analog, and high-speed digital applications
- A flexible substrate resistance network for RF modeling
- A new accurate channel thermal noise model, and a noise partition model for the induced gate noise
- A non-quasi-static (NQS) model consistent with the Rii-based RF model, and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances
- An accurate gate direct tunneling model

- A comprehensive and versatile geometry-dependent parasitics model for source/drain connections and multi-finger devices
- An improved model for steep vertical retrograde doping profiles
- A better model for pocket-implanted devices in Vth, the bulk charge effect model, and Rout
- An asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
- Accepts either the electrical or physical gate oxide thickness as the model input in a physically accurate manner
- A quantum mechanical charge-layer-thickness model for both IV and CV
- A more accurate mobility model for predictive modeling
- A gate-induced drain leakage (GIDL) current model, not available in earlier BSIM models
- An improved unified flicker (1/f) noise model, which is smooth over all bias regions, and which considers the bulk charge effect
- Different diode IV and CV characteristics for the source and drain junctions
- A junction diode breakdown with or without current limiting
- A dielectric constant of the gate dielectric as a model parameter
- .OP now prints the total capacitances, instead of just the intrinsic capacitances for the BSIM4 (Level 54) MOSFET model

BSIM4.2.1 has the following improvements over BSIM4.2.0:

- A new GISL (Gate Induced Source Leakage) current component corresponds to the same current at the drain side (GIDL).
- The warning limits for effective channel length, channel width, and gate oxide thickness have been reduced to avoid unnecessary warnings if you use BSIM4 aggressively, beyond the desired model card application ranges.
- The DELTOX parameter in the MOS active element (M) models the relative variation on the transconductance (oxide thickness) of the MOS in Monte Carlo analysis.
- `.OPTION LIST` can now print an element summary for the MOSFET Level=54 model

TSMC Diode Model

HSPICE MOSFET Level 54 (BSIM4) supports a TSMC junction diode model. You can use this TSMC junction diode model to simulate the temperature dependence, source/body, and drain/body currents of a junction diode.

Note: For a complete description of this effect model, visit the official UCB BSIM web site:

```
http://www-device.eecs.berkeley.edu/~bsim3/
```

You can order either of these models directly from Taiwan Semiconductor Manufacturing Company (TSMC)—not from Synopsys. See the TSMC web site:

```
http://www.tsmc.com
```

BSIM4 STI/LOD

HSPICE BSIM4 supports the full STI (Shallow Trench Isolation) or LOD (Length of Diffusion) induced mechanical stress-effect model (for version 4.3 or later), which was first released in the UCB BSIM4.3.0 model version. HSPICE BSIM4 turns on the simulation of this effect when the following conditions (consistent with those of the UCB BSIM4 model) are satisfied:

```
if (VERSION >= 4.3)
{
if ((SA > 0 and SB > 0 and NF==1) or ( SA > 0 and SB > 0 and (
NF >1 and SD > 0 )))
{ UCB's STI/LOD model is turned on}
}
```

If VERSION >= 4.3, the STI model is not dependent on STIMOD=0 or 1. In this case, the STI model is applied to the model similar to the UCB STI model (see Table 109). When parameter values that satisfy SA>0, SB>0, NF>1, and SD=0 are given in model cards, no evaluation of such effect is performed.

Table 109 Supported HSPICE BSIM4 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given or if (<=0), the stress effect is turned off.
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given or if (<=0), the stress effect is turned off
SD (instance parameter)		0.0		Distance between neighboring fingers. For NF >1,If not given or (<=0), stress effect is turned off
STIMOD (Also instance parameter)		0.0 (V < 4.3) 1.0 (V >= 4.3)		STI model selector, which gives priority to the instance parameter. • 0: No STI effect. • 1: UCB's STI model • 2: TSMC's STI model
SAREF	M	1e-06	No	Reference distance for SA, >0.0
SBREF	M	1e-06	No	Reference distance for SB, >0.0
WLOD	M	0.0	No	Width parameter for stress effect
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. 1.0<=kvsat<=1.0
TKU0		0.0	No	Temperature coefficient of KU0
LKU0		0.0	No	Length dependence of KU0
WKU0		0.0	No	Width dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, >0

Table 109 Supported HSPICE BSIM4 STI/LOD Parameters (Continued)

Parameter	Unit	Default	Bin?	Description
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
WKVTH0		0.0	No	Width dependence of KVTH0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0
STK2		0.0	No	K2 shift factor related to VTh0 change
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0

LMLT and WMLT in BSIM4

You can use LMLT and WMLT to shrink the length and width in memory design. The LMLT and WMLT parameters are unitless, and are used to scale (usually scale down) MOSFET drawn length and width (specified in BSIM4 MOSFET instance lines), respectively. This makes memory design and netlist creation quite convenient because most (if not all) memory circuits use the smallest feature sizes as the process capability improves, even within the same generation of CMOS technology.

The shrunken device length and width will then be further offset (by XL and XW, respectively) to the actual device size in lithography and etching process

steps, and finally to the electrical size as a result of subsequent ion implementation and annealing steps.

Name (Alias)	Default	Description
LMLT	1.0	Channel length shrinking factor
WMLT	1.0	Device width shrinking factor

Both LMLT and WMLT must be greater than 0; if not, simulation resets them to 1.0 (default) and issues a warning message.

To use these two parameters, add them in the model cards, without any other modifications. For example:

```
.model nmos nmos
+ level=54 lmlt=0.85 wmlt=0.9
```

- The drawn channel length (L) is multiplied by LMLT.
- The drawn channel width (W) is multiplied by WMLT,

BSIM4 evaluates the effective length and width, Leff and Weff, as:

```
Leff = Lnew - 2.0 * dL
Weff = Wnew - 2.0 * dW
```

Lnew and Wnew are evaluated as:

```
Lnew = L + XL
Wnew = W + XW
```

dL and dW are evaluated with Lnew and Wnew:

```
T0 = pow(Lnew, LLN)
T1 = pow(Wnew, LWN)
dL = LINT + LL/T0 + LW / T1 + LWL / (T0*T1)
T2 = pow(Lnew, WLN)
T3 = pow(Wnew, WWN)
dw = WINT + WL / T2 + WW / T3 + WWL / (T2*T3)
```

Similarly, the preceding equations determine the Ldlc, Ldlcig, LeffCV, Wdwc, Wdwcig, WeffCV, WeffCJ, grgeltd, and Wnew model variables and quantities.

When multiplied by the LMLT and WMLT parameters, Leff and Weff become:

```
Leff = Lnew' - 2.0 * dL
Weff = Wnew' - 2.0 * dL
```

Lnew' and Wnew' are evaluated as:

```
Lnew' = L * LMLT + XL
Wnew' = W * WMLT + XW
```

Similarly dL, dW, Ldlc, Ldlcig, LeffCV, Wdwc, Wdwcig, WeffCV, WeffCJ, and grgeltd are all evaluated from Lnew' and Wnew'.

HSPICE Junction Diode Model and ACM

BSIM4 now supports Area Calculation Method (ACM) similar to BSIM3v3 for the following models and corresponding ACM values:

- For the HSPICE junction model, specify ACM=0,1,2, or 3.
- For the Berkeley BSIM4 junction model, specify ACM=10,11,12, or 13.

For the junction current, junction capacitance, and parasitic resistance equations corresponding to ACM=0,1,2,3 see MOSFET Diode Models on page 39.

Set ACM=10,11,12, or 13 to enable the Berkeley BSIM4 junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for ACM=10,11,12, or 13 correspond to the ACM=0,1,2. or 3 parasitic resistor equations. ACM=10,11,12, or 13 all use the Berkeley junction-capacitance model equations. The default ACM value is 12. For ACM=10,11,12, or 13 usage, see Level 49 and 53 BSIM3v3 MOS Models on page 397.

CALCACM still only applies to ACM=12, although it is disabled. ACM=12 uses the Berkeley BSIM4 junction diodes and parasitic resistors equations if CALCACM equals 1 or 0. The default CALCACM value is 1.

Table 110 MOSFET Level 54 Parameters

Parameter	Description
nf	Number of device figures
min	Whether to minimize the number of drain or source diffusions for even-number fingered device
rbdb	Resistance connected between the internal drain-side body node and the external body node
rbsb	Resistance connected between the internal source-side body node and the external body node

Table 110 MOSFET Level 54 Parameters (Continued)

Parameter	Description
rbpb	Resistance connected between the internal reference body node and the external body node
rbps	Resistance connected between the internal reference body node and the internal drain-side body node
rbpd	Resistance connected between the internal reference body node and the internal source-side body node
trnqsmod	Transient NQS model selector
acnqsmod	AC small-signal NQS model selector
rbodymod	Substrate resistance network model selector
rgatemod	Gate resistance model selector
geomod	Geometry-dependent parasitics model selector
rgeomod	Source/Drain diffusion resistance and contact model selector

MOSFET Level 54 uses the generic MOSFET model parameters described in Chapter 3, Common MOSFET Model Parameters. It also uses the parameters described in this section, which apply only to MOSFET Level 54.

The simulation calculates Rd and Rs as follows:

Rd(TEMP) = Rd(TNOM) * (1 + TRD * (TEMP - TNOM))
Rs(TEMP) = Rs(TNOM) * (1 + TRS * (TEMP - TNOM))

Table 111 MOSFET Level 54 Instance Parameters

Parameter	Unit	Default	Description
RDC	ohm	0.0	Drain contact resistance for the per-finger device
RSC	ohm	0.0	Source contact resistance for the per-finger device

Table 111 MOSFET Level 54 Instance Parameters (Continued)

Parameter	Unit	Default	Description
DELVTO (DELVT0)	V	0.0	Shift in the zero-bias threshold voltage (VTH0)
MULU0		1.0	Low-field mobility (U0) multiplier
DELK1	$V^{1/2}$		Shift in the body bias coefficient (K1)
DELNFCT		0.0	Shift in subthreshold swing factor (NFACTOR)

Table 112 MOSFET Level 54 Warning Messages

Parameter	Effective Value	Warning Message
RDC	RD_eff = RD_diffusion + RDC / NF;	Warning if RDC < 0.0 and reset RDC to 0.0
RSC	RS_eff = RS_diffusion + RSC / NF;	Warning if RSC < 0.0 and reset RSC to 0.0
DELVTO (DELVT0)	VTH0_eff = VTH0 + DELVTO;	N/A
MULU0	U0_eff = U0 * MULU0;	Warning if MULU0 < 0.0 and reset MULU0 to 1.0
DELK1	K1_eff = K1 + DELK1;	Warning if DELK1 < -K1 and reset DELK1 to 0.0
DELNFCT	NFACTOR_eff = NFACTOR + DELNFCT;	N/A

Table 113 Model Selectors/Controllers, MOSFET Level 54

Parameter	Default	Binnable	Description
VERSION	4.10	NA	Model version number
BINUNIT	1	NA	Binning unit selector
PARAMCHK	1	NA	Switch for the parameter value check

Table 113 Model Selectors/Controllers, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
MOBMOD	1	NA	Mobility model selector
RDSMOD	0	NA	Bias-dependent source/drain resistance model selector
IGCMOD	0	NA	Gate-to-channel tunneling current model selector
IGBMOD	0	NA	Gate-to-substrate tunneling current model selector
CAPMOD	2	NA	Capacitance model selector
RGATEMOD	0 (no gate resistance)		Gate resistance model selector
RBODYMOD	0 (network off)	NA	Substrate resistance network model selector
TRNQSMOD	0	NA	Transient NQS model selector
ACNQSMOD	0	NA	AC small-signal NQS model selector
FNOIMOD	1	NA	Flicker noise model selector
TNOIMOD	0	NA	Thermal noise model selector
DIOMOD	1	NA	Source/drain junction diode IV model selector
PERMOD	1	NA	PS/PD includes/excludes the gate-edge perimeter
GEOMOD	0 (isolated)	NA	Geometry-dependent parasitics model selector
RGEOMOD	1	NA	Source/drain diffusion resistance and contact model selector

Table 114 MOSFET Level 54 Process Parameters

Parameter	Default	Binnable	Description
EPSROX	3.9 (SiO_2)	No	Gate dielectric constant relative to vacuum
TOXE	3.0e-9m	No	Electrical gate equivalent oxide thickness
TOXP	TOXE	No	Physical gate equivalent oxide thickness
TOXM	TOXE	No	Tox at which simulation extracts parameters
DTOX	0.0m	No	Defined as (TOXE-TOXP)
XJ	1.5e-7m	Yes	S/D junction depth
GAMMA1 (γ_1 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient near the surface
GAMMA2 (γ_2 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient in the bulk
NDEP	$1.7e17cm^{-3}$	Yes	Channel doping concentration at the depletion edge for the zero body bias
NSUB	$6.0e16cm^{-3}$	Yes	Substrate doping concentration
NGATE	$0.0cm^{-3}$	Yes	Poly Si gate doping concentration
NSD	$1.0e20cm^{-3}$	Yes	Source/drain doping concentration
VBX	calculated (v)	No	V_{bs} at which the depletion region width equals XT
XT	1.55e-7m	Yes	Doping depth
RSH	0.0ohm/square	No	Source/drain sheet resistance
RSHG	0.1ohm/square	No	Gate electrode sheet resistance

Table 115 Basic Model Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
VTH0 or VTHO	0.7V (NMOS) -0.7V (PMOS)	Yes	Long-channel threshold voltage at V_{bs}=0
VFB	-1.0V	Yes	Flat-band voltage (PHIN)
PHIN	0.0V	Yes	Non-uniform vertical doping effect on the surface potential
K1	$0.5V^{1/2}$	Yes	First-order body bias coefficient
K2	0.0	Yes	Second-order body bias coefficient
K3	80.0	Yes	Narrow width coefficient
K3B	$0.0V^{-1}$	Yes	Body effect coefficient of K3
W0	2.5e-6m	Yes	Narrow width parameter
LPE0	1.74e-7m	Yes	Lateral non-uniform doping parameter
LPEB	0.0m	Yes	Lateral non-uniform doping effect on K1
VBM	-3.0V	Yes	Maximum applied body bias in the VTH0 calculation
DVT0	2.2	Yes	First coefficient of the short-channel effect on V_{th}
DVT1	0.53	Yes	Second coefficient of the short-channel effect on V_{th}
DVT2	$-0.032V^{-1}$	Yes	Body-bias coefficient of the short-channel effect on V_{th}
DVTP0	0.0m	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices
DVTP1	$0.0V^{-1}$	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices

Table 115 Basic Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
DVT0W	0.0	Yes	First coefficient of the narrow width effect on V_{th} for a small channel length
DVT1W	$5.3e6m^{-1}$	Yes	Second coefficient of the narrow width effect on V_{th} for a small channel length
DVT2W	$-0.032V^{-1}$	Yes	Body-bias coefficient of narrow width effect for small channel length
U0	$0.067m^2/(Vs)$ (NMOS); $0.025 m^2/(Vs)$ (PMOS)	Yes	Low-field mobility
UA	1.0e-9m/V for MOBMOD=0 and 1; 1.0e-15m/V for MOBMOD=2	Yes	Coefficient of the first-order mobility degradation due to the vertical field
UB	$1.0e-19m^2/V^2$	Yes	Coefficient of the second-order mobility degradation due to the vertical field
UC	$-0.0465V^{-1}$ for MOB-MOD=1; $-0.0465e-9 m/V^2$ for MOBMOD=0 and 2	Yes	Coefficient of the mobility degradation due to the body-bias effect
EU	1.67 (NMOS); 1.0 (PMOS)	No	Exponent for the mobility degradation of MOBMOD=2
VSAT	8.0e4m/s	Yes	Saturation velocity
A0	1.0	Yes	Coefficient of the channel-length dependence of the bulk charge effect
AGS	$0.0V^{-1}$	Yes	Coefficient of the V_{gs} dependence of the bulk charge effect

Table 115 Basic Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
B0	0.0m	Yes	Bulk charge effect coefficient for the channel width
B1	0.0m	Yes	Bulk charge effect width offset
KETA	$-0.047V^{-1}$	Yes	Body-bias coefficient of the bulk charge effect
A1	$0.0V^{-1}$	Yes	First non-saturation effect parameter
A2	1.0	Yes	Second non-saturation factor
WINT	0.0m	No	Channel-width offset parameter
LINT	0.0m	No	Channel-length offset parameter
DWG	0.0m/V	Yes	Coefficient of gate bias dependence of W_{eff}
DWB	$0.0m/V^{1/2}$	Yes	Coefficient of the body bias dependence of the W_{eff} bias dependence
VOFF	-0.08V	Yes	Offset voltage in subthreshold region for large *W* and *L* values
VOFFL	0.0mV	No	Channel-length dependence of VOFF
MINV	0.0	Yes	V_{gsteff} fitting parameter for the moderate inversion condition
NFACTOR	1.0	Yes	Subthreshold swing factor
ETA0	0.08	Yes	DIBL coefficient in the subthreshold region
ETAB	$-0.07V^{-1}$	Yes	Body-bias coefficient for the DIBL effect for the subthreshold
DSUB	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
CIT	$0.0F/m^2$	Yes	Interface trap capacitance

Table 115 Basic Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
CDSC	2.4e-4F/m^2	Yes	Coupling capacitance between the source/drain and the channel
CDSCB	0.0F/(Vm^2)	Yes	Body-bias sensitivity of CDSC
CDSCD	0.0(F/Vm^2)	Yes	Drain-bias sensitivity of DCSC
PCLM	1.3	Yes	Channel-length modulation parameter
PDIBLC1	0.39	Yes	Parameter for the DIBL effect on Rout
PDIBLC2	0.0086	Yes	Parameter for the DIBL effect on Rout
PDIBLCB	0.0V^{-1}	Yes	Body bias coefficient of the DIBL effect on Rout
DROUT	0.56	Yes	Channel-length dependence of the DIBL effect on Rout
PSCBE1	4.24e8V/m	Yes	First substrate current induced body-effect parameter
PSCBE2	1.0e-5m/V	Yes	Second substrate current induced body-effect parameter
PVAG	0.0	Yes	Gate-bias dependence of Early voltage
DELTA δ (in equation)	0.01V	Yes	Parameter for DC V_{dseff}
FPROUT	0.0V/$m^{0.5}$	Yes	Effect of the pocket implant on Rout degradation
PDITS	0.0V^{-1}	Yes	Impact of the drain-induced V_{th} shift on Rout
PDITSL	0.0m^{-1}	No	Channel-length dependence of the drain-induced V_{th} shift for Rout
PDITSD	0.0V^{-1}	Yes	Vds dependence of the drain-induced V_{th}shift for Rout

Table 116 Parameters for Asymmetric and Bias-Dependent Rds Model, MOSFET Level 54

Parameter	Default	Binnable	Description
RDSW	200.0 ohm(μm)^{WR}	Yes	Zero bias LLD resistance per unit width for RDSMOD=0
RDSWMIN	0.0 ohm(μm)^{WR}	No	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0
RDW	100.0 ohm(μm)^{WR}	Yes	Zero bias lightly-doped drain resistance $R_d(v)$ per unit width for RDSMOD=1
RDWMIN	0.0 ohm(μm)^{WR}	No	Lightly-doped drain resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
RSW	100.0 ohm(μm)^{WR}	Yes	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDSMOD=1
RSWMIN	0.0 ohm(μm)^{WR}	No	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
PRWG	1.0V^{-1}	Yes	Gate-bias dependence of the LDD resistance
PRWB	0.0V$^{-0.5}$	Yes	Body-bias dependence of the LDD resistance
WR	1.0	Yes	Channel-width dependence of the LDD resistance
NRS	1.0	No	Number of source diffusion squares
NRD	1.0	No	Number of drain diffusion squares

Table 117 Impact Ionization Current Model Parameters, MOSFET 54

Parameter	Default	Binnable	Description
ALPHA0	0.0Am/V	Yes	First parameter of the impact ionization current
ALPHA1	0.0A/V	Yes	Isub parameter for length scaling
BETA0	30.0V	Yes	Second parameter for the impact ionization current

Table 118 Gate-Induced Drain Leakage Model Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
AGIDL	0.0ohm	Yes	Pre-exponential coefficient for GIDL
BGIDL	2.3e9V/m	Yes	Exponential coefficient for GIDL
CGIDL	$0.5V^3$	Yes	Parameter for the body-bias effect on GIDL
DGIDL	0.8V	Yes	Fitting parameter for band bending for GIDL

Table 119 Gate Dielectric Tunneling Current Model Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
AIGBACC	$0.43\ (F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in the accumulation
BIGBACC	$0.054\ (F_s^2/_g)^{0.5}\ m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in the accumulation
CIGBACC	$0.075V^{-1}$	Yes	Parameter for I_{gb}in the accumulation
NIGBACC	1.0	Yes	Parameter for I_{gb} in the accumulation
AIGBINV	$0.35\ (F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gb} in the inversion
BIGBINV	$0.03\ (F_s^2/_g)^{0.5}m^{-1}V^{-1}$	Yes	Parameter for I_{gb} in the inversion
CIGBINV	$0.0006V^{-1}$	Yes	Parameter for I_{gb} in the inversion
EIGBINV	1.1V	Yes	Parameter for I_{gb} in the inversion
NIGBINV	3.0	Yes	Parameter for I_{gb} in the inversion
AIGC	0.054 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}m^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}

Table 119 Gate Dielectric Tunneling Current Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
BIGC	0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
CIGC	0.075 (NMOS) and 0.03(PMOS) V^{-1}	Yes	Parameter for I_{gcs} and I_{gcd}
AIGSD	0.43 (NMOS) and 0.31 (PMOS) $(F_s^2/_g)^{0.5}$ m^{-1}	Yes	Parameter for I_{gs} and I_{gd}
BIGSD	0.054 (NMOS) 0.024 (PMOS) $(F_s^2/_g)^{0.5}$ $m^{-1}V^{-1}$	Yes	Parameter for I_{gs} and I_{gd}
CIGSD	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	Parameter for I_{gs} and I_{gd}
DLCIG	LINT	Yes	Source/drain overlap length for Igs and Igd
NIGC	1.0	Yes	Parameter for I_{gcs}, I_{gcd}, I_{gs} and I_{gd}
POXEDGE	1.0	Yes	Factor for the gate oxide thickness in the source/drain overlap regions
PIGCD	1.0	Yes	v_{ds}dependence of I_{gcs} and I_{gcd}
NTOX	1.0	Yes	Exponent for the gate oxide ratio
TOXREF	3.0e-9m	No	Nominal gate oxide thickness for the gate dielectric tunneling current model only

Table 120 Charge/Capacitance Model Parameters MOS 54

Parameter	Default	Binnable	Description
XPART	0.0	No	Charge partition parameter
CGSO	calculated (F/m)	No	Non LDD region source-gate overlap capacitance per unit channel width
CGDO	calculated (F/m)	No	Non LDD region drain-gate overlap capacitance per unit channel width
CGBO	0.0 (F/m)	No	Gate-bulk overlap capacitance per unit channel length
CGSL	0.0F/m	Yes	Overlap capacitance between the gate and the lightly-doped source region
CGDL	0.0F/m	Yes	Overlap capacitance between gate and lightly-doped source region
CKAPPAS	0.6V	Yes	Coefficient of the bias-dependent overlap capacitance for the source side
CKAPPAD	CKAPPAS	Yes	Coefficient of bias-dependent overlap capacitance for the drain side
CF	calculated (F/m)	Yes	Fringing field capacitance
CLC	1.0e-7m	Yes	Constant term for the short channel model
CLE	0.6	Yes	Exponential term for the short channel model
DLC	LINT (m)	No	Channel-length offset parameter for the CV model
DWC	WINT (m)	No	Channel-width offset parameter for the CV model
VFBCV	-1.0V	Yes	Flat-band voltage parameter (for CAPMOD=0 only)
NOFF	1.0	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion
VOFFCV	0.0V	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion

Table 120 Charge/Capacitance Model Parameters MOS 54 (Continued)

Parameter	Default	Binnable	Description
ACDE	1.0m/V	Yes	Exponential coefficient for the charge thickness in CAPMOD=2 for the accumulation and depletion regions
MOIN	15.0	Yes	Coefficient for the gate-bias dependent surface potential

Table 121 High-Speed/RF Model Parameters, MOS Level 54

Parameter	Default	Binnable	Description
XRCRG1	12.0	Yes	Parameter for the distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models
XRCRG2	1.0	Yes	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models
RBPB	50.0ohm	No	Resistance between bNodePrime and bNode
RBPD	50.0ohm	No	Resistance between bNodePrime and dbNode
RBPS	50.0ohm	No	Resistance between bNodePrime and sbNode
RBDB	50.0ohm	No	Resistance between dbNode and dbNode
RBSB	50.0ohm	No	Resistance between sbNode and bNode
GBMIN	1.0e-12mho	No	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to an unreasonably large substrate resistance

Table 122 Flicker and Thermal Noise Model Parameters, MOS Level 54

Parameter	Default	Binnable	Description
NOIA	6.25e41 $(eV)^{-1}s^{1-EF}m^{-3}$ for NMOS; 6.188e40 $(eV)^{-1}s^{1-EF}m^{-3}$ for PMOS	No	Flicker noise parameter A
NOIB	3.125e26 $(eV)^{-1}s^{1-EF}m^{-1}$ for NMOS; 1.5e25 $(eV)^{-1}s^{1-EF}m^{-1}$ for PMOS	No	Flicker noise parameter B
NOIC	8.75 $(eV)^{-1}S^{1-EF}m$	No	Flicker noise parameter C
EM	4.1e7V/m	No	Saturation field
AF	1.0	No	Flicker noise exponent
EF	1.0	No	Flicker noise frequency exponent
KF	0.0 $A^{2-EF}s^{1-EF}F$	No	Flicker noise coefficient
NTNOI	1.0	No	Noise factor for short-channel devices for TNOIMOD=0 only
TNOIA	1.5	No	Coefficient of the channel-length dependence of the total channel thermal noise
TNOIB	3.5	No	Channel-length dependence parameter for partitioning the channel thermal noise

Table 123 Layout-Dependent Parasitics Model Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
DMCG	0.0m	No	Distance from the S/D contact center to the gate edge
DMCI	DMCG	No	Distance from the S/D contact center to the isolation edge in the channel-length direction
DMDG	0.0m	No	Same as DMCG, but for merged devices only
DMCGT	0.0m	No	DMCG of the test structures
NF	1	No	Number of device figures
DWJ	DWC (in CVmodel)	No	Offset of the S/D junction width
MIN	0	No	Minimize the number of drain or source diffusions for even-number fingered device
XGW	0.0m	No	Distance from the gate contact to the channel edge
XGL	0.0m	No	Gate length offset due to patterning variations
NGCON	1	No	Number of gate contacts

Table 124 Asymmetric Source/Drain Junction Diode Model Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
IJTHSREV	IJTHSREV=0.1A	No	Limiting current in the reverse bias region
IJTHDREV	IJTHDREV= IJTHSREV	No	Limiting current in the reverse bias region
IJTHSFWD	IJTHSFWD=0.1A	No	Limiting current in the forward bias region
IJTHDFWD	IJTHDFWD= IJTHSFWD	No	Limiting current in the forward bias region

Table 124 Asymmetric Source/Drain Junction Diode Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
XJBVS	XJBVS=1.0	No	Fitting parameter for the diode breakdown
XJBVD	XJBVD=XJBVS	No	Fitting parameter for the diode breakdown
BVS	BVS=10.0V	No	Breakdown voltage
BVD	BVD=BVS	No	Breakdown voltage
JSS	JSS=1.0e-4A/m^2	No	Bottom junction reverse saturation current density
JSD	JSD=JSS	No	Bottom junction reverse saturation current density
JSWS	JSWS=0.0A/m	No	Isolation-edge sidewall reverse saturation current density
JSWD	JSWD=JSWS	No	Isolation-edge sidewall reverse saturation current density
JSWGS	JSWGS=0.0A/m	No	Gate-edge sidewall reverse saturation current density
JSWGD	JSWGD=JSWGS	No	Gate-edge sidewall reverse saturation current density
CJS	CJS=5.0e-4 F/m^2	No	Bottom junction capacitance per unit area at zero bias
CJD	CJD=CJS	No	Bottom junction capacitance per unit area at zero bias
MJS	MJS=0.5	No	Bottom junction capacitance grading coefficient
MJD	MJD=MJS	No	Bottom junction capacitance grading coefficient
MJSWS	MJSWS=0.33	No	Isolation-edge sidewall junction capacitance grading coefficient

Table 124 Asymmetric Source/Drain Junction Diode Model Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
MJSWD	MJSWD=MJSWS	No	Isolation-edge sidewall junction capacitance grading coefficient
CJSWS	CJSWS=5.0e-10 F/m	No	Isolation-edge sidewall junction capacitance per unit area
CJSWD	CJSWD=CJSWS	No	Isolation-edge sidewall junction capacitance per unit area
CJSWGS	CJSWGS=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
CJSWGD	CJSWGD=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
MJSWGS	MJSWGS=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
MJSWGD	MJSWGD=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
PBS	PBS=1.0V	No	Bottom junction built-in potential
PBD	PBD=PBS	No	Bottom junction built-in potential
PBSWS	PBSWS=1.0V	No	Isolation-edge sidewall junction built-in potential
PBSWD	PBSWD=PBSWS	No	Isolation-edge sidewall junction built-in potential
PBSWGS	PBSWGS=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWGD	PBSWGD=PBSWS	No	Gate-edge sidewall junction built-in potential

Table 125 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
TNOM	27°X	No	Temperature at which simulation extracts parameters
UTE	-1.5	Yes	Mobility temperature exponent
KT1	-0.11V	Yes	Temperature coefficient for the threshold voltage
KT1L	0.0Vm	Yes	Channel length dependence of the temperature coefficient for the threshold voltage
KT2	0.022	Yes	Body-bias coefficient of the V_{th} temperature effect
UA1	1.0e-9m/V	Yes	Temperature coefficient for UA
UB1	-1.0e-18 (m/V^2)	Yes	Temperature coefficient for UB
UC1	0.056/V for MOBMOD=1: 0.056e-9m/V^2 for MOBMOD=0 and 2	Yes	Temperature coefficient for UC
AT	3.3e4m/s	Yes	Temperature coefficient for the saturation velocity
PRT	0.0ohm-m	Yes	Temperature coefficient for Rdsw
NJS, NJD	NJS=1.0; NJD=NJS	No	Emission coefficients of junction for the source and drain junctions
XTIS, XTID	XTIS=3.0; XTID=XTIS	No	Junction current temperature exponents for the source and drain junctions
TPB	0.0V/K	No	Temperature coefficient of PB
TPBSW	0.0V/K	No	Temperature coefficient of PBSW
TPBSWG	0.0V/K	No	Temperature coefficient of PBSWG
TCJ	$0.0K^{-1}$	No	Temperature coefficient of CJ

Table 125 Temperature Dependence Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
TCJSW	$0.0K^{-1}$	No	Temperature coefficient of CJSW
TCJSWG	$0.0K^{-1}$	No	Temperature coefficient of CJSWG
TRD	0.0 1K-1		Temperature coefficient for the drain diffusion and the Rd contact resistances.
TRS	0.0 1/K		Temperature coefficient for the source diffusion and the Rs contact resistances.

Table 126 dW and dL Parameters, MOSFET Level 54

Parameter	Default	Binnable	Description
WL	$0.0\mu^{\Omega\Lambda N}$	No	Coefficient of the length dependence of the width offset
WLN	1.0	No	Power of the length dependence of the width offset
WW	$0.0m^{WWN}$	No	Coefficient of the width dependence of the width offset
WWN	1.0	No	Power of the width dependence of the width offset
WWL	$0.0\ m^{WWN+WLN}$	No	Coefficient of the length and width cross term dependence for the width offset
LL	$0.0m^{LLN}$	No	Coefficient of the length dependence for the length offset
LLN	1.0	No	Power of the length dependence for the length offset
LW	$0.0m^{LWN}$	No	Coefficient of the width dependence for the length offset
LWN	1.0	No	Power of the width dependence, length offset
LWL	$0.0\ m^{LWN+LLN}$	No	Coefficient of the length and width cross term dependence for the length offset

Table 126 dW and dL Parameters, MOSFET Level 54 (Continued)

Parameter	Default	Binnable	Description
LLC	LL	No	Coefficient of the length dependence for the CV channel length offset
LWC	LW	No	Coefficient of the width dependence for the CV channel length offset
LWLC	LWL	No	Coefficient of the length and width cross-term dependence for the CV channel length offset
WLC	WL	No	Coefficient of the length dependence for the CV channel width offset
WWC	WW	No	Coefficient of the width dependence for the CV channel width offset
WWLC	WWL	No	Coefficient of the length and width cross-term dependence for the CV channel width offset

Table 127 Range Parameters for Model Application, MOSFET Level 54

Parameter	Default	Binnable	Description
LMIN	0.0µ	No	Minimum channel length
LMAX	1.0m	No	Maximum channel length
WMIN	0.0m	No	Minimum channel width
WMAX	1.0m	No	Maximum channel width

Level 54 BSIM4 Template Output List

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 14.

Level 57 UC Berkeley BSIM3-SOI Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices of which BSIM3PD2.0.1 for PD SOI devices is Synopsys MOSFET Level 57. For a description of this model, see the *BSIM3PD2.0 MOSFET MODEL User's Manual* at:

`http://www-device.eecs.berkeley.edu/~bsim3soi`

Level 57 uses the UCB Version 2.2.3 model, which includes a separate set of the geometry-dependence parameters (LLC, LWC, LWLC, WLC, WWC, and WWLC) to calculate *LeffCV* and *WeffCV*.

Level 57 also includes a new Full-Depletion (FD) module (soiMod=1). This module provides a better fit to FD SOI devices. As soiMod=0 (default), the model is identical to previous BSIMSOI PD models. This module also includes gate to channel/drain/source tunneling currents and overlap components.

The following enhancements to the BSIMSOI PD version were made starting in the BSIMSOI 3.0 version:

- If the self-heating model is on, simulation calculates the channel surface potential.
- NDIF includes parameter value checking.
- Simulation calculates the Vgsteff derivatives.
- The default value of CTH0 changed from 0 to 1E-5
- The DELTOX parameter in the MOS active element (M) models the relative variation on the transconductance (oxide thickness) of the MOS in Monte Carlo analysis.

You can download the BSIMSOI3.0 source code, equation/parameter list, and bug report from:

http://www-device.eecs.berkeley.edu/~bsimsoi

General Syntax for BSIM3/SOI

```
Mxxx nd ng ns ne <np> <nb> <nT> mname <L=val> <W=val>
+ <M=val> <AD=val> <AS=val> <PD=val> <PS=val> <NRD=val>
+ <NRS=val> <NRB=val> <RTH0=val> <CTH0=val> <NBC=val>
+ <NSEG=val> <PDBCP=val> <PSBCP=val> <AGBCP=val>
+ <AEBCP=val> <VBSUSR=val> <DELTOX=val> <TNODEOUT>
+ <off> <FRBODY> <BJToff=val> <IC=Vds, Vgs, Vbs, Ves, Vps>
```

In this syntax, the angle brackets indicate optional parameters.

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	External body contact node name or number.
nb	Internal body node name or number.
nT	Temperature node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.

Parameter	Description
AD	Drain diffusion area. Overrides **.OPTION DEFAD** statement. Default=DEFAD.
AS	Source diffusion area. Overrides **.OPTION DEFAS** statement. Default=DEFAS.
PD	Drain junction perimeter, including channel edge. Overrides **.OPTION DEFPD**.
PS	Source junction perimeter including channel edge. Overrides **.OPTION DEFPS**.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides **.OPTION DEFNRD**.
NRS	Number of squares of source diffusion for the source series resistance. Overrides **.OPTION DEFNRS**.
NRB	Number of squares for the body series resistance.
FRBODY	Coefficient of the distributed body resistance effects. Default = 1.0
RTH0	Thermal resistance per unit width: • If you do not specify RTH0, simulation extracts it from the model card. • If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width: • If you do not specify CTH0, simulation extracts it from the model card. • If you specify CTH0, it overrides CTH0 in the model card.
NBC	Number of body contact isolation edge.
NSEG	Number of segments for partitioning the channel width.
PDBCP	Parasitic perimeter length for the body contact a the drain side.
PSBCP	Parasitic perimeter length for the body contact at the source side.
AGBCP	Parasitic gate-to-body overlap area for the body contact.
AEBCP	Parasitic body-to-substrate overlap area for the body contact.

Parameter	Description
VBSUSR	Optional initial value of Vbs that you specify for transient analysis.
DELTOX	Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
TNODEOUT	Temperature node flag indicating the use of the T node.
OFF	Sets the initial condition of the element to OFF in DC analysis.
BJTOFF	Turning off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it.

- If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
- If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

Level 57 Model Parameters

Table 128 MOSFET Level 57 Model Control Parameters

Parameter	Unit	Default	Description
capmod	-	2	Flag for the short channel capacitance model
MOBMOD	-	1	Mobility model selector

Table 128 MOSFET Level 57 Model Control Parameters (Continued)

Parameter	Unit	Default	Description
noimod	-	1	Flag for the noise model
SHMOD	-	0	Flag for self-heating: 0 - no self-heating 1 - self-heating

Table 129 MOSFET Level 57 Process Parameters

Parameter	Unit	Default	Description
DTOXCV (capmod=3 only)			Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and the finite channel charge layer thickness.
Nch	$1/cm^3$	1.7e17	Channel doping concentration
Ngate	$1/cm^3$	0	Poly gate doping concentration
Nsub	$1/cm^3$	6.0e16	Substrate doping concentration
Tbox	m	3.0e-7	Buried oxide thickness
Tox	m	1.0e-8	Gate oxide thickness
Tsi	m	1.0e-7	Silicon film thickness
Xj	m	-	S/D junction depth

Table 130 MOSFET Level 57 DC Parameters

Parameter	Unit	Default	Description
a0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter

Table 130 MOSFET Level 57 DC Parameters (Continued)

Parameter	Unit	Default	Description
Aely	V/m	0	Channel length dependency of the Early voltage for the bipolar current
Agidl	1/W	0.0	GIDL constant
ags	1/V	0.0	Gate bias coefficient of A_{bulk}
Ahli	-	0	High-level injection parameter for the bipolar current
alpha0	m/V	0.0	First parameter of the impact ionization current
b0	m	0.0	Bulk charge effect coefficient for the channel width
b1	m	0.0	Bulk charge effect width offset
beta0	1/V	0.0	First V_{ds} dependence parameter of the impact ionization current
beta1	-	0.0	Second V_{ds} dependence parameter of the impact ionization current
beta2	V	0.1	Third V_{ds} dependence parameter of the impact ionization current
Bgidl	V/m	0.0	GIDL exponential coefficient
cdsc	F/m^2	2.4e-4	Drain/source to the channel coupling capacitance
cdscb	F/m^2	0	Body-bias sensitivity of cdsc
cdscd	F/m^2	0	Drain-bias sensitivity of cdsc
cit	F/m^2	0.0	Interface trap capacitance
delta	-	0.01	Effective V_{ds} parameter
drout	-	0.56	L dependence coefficient of the DIBL correction parameter in Rout
dsub	-	0.56	DIBL coefficient exponent

Table 130 MOSFET Level 57 DC Parameters (Continued)

Parameter	Unit	Default	Description
Dvt0	-	2.2	First coefficient of the short-channel effect on Vth
dvt0w	-	0	First coefficient of the narrow width effect on Vth for a small channel length
dvt1	-	0.53	Second coefficient of the short-channel effect on Vth
dvt1w	-	5.3e6	Second coefficient of the narrow width effect on Vth for a small channel length
dvt2	1/V	-0.032	Body-bias coefficient of the short-channel effect on Vth
dvt2w	1/V	-0.032	Body-bias coefficient of the narrow width effect on Vth for a small channel length
dwb	$m/V^{1/2}$	0.0	Coefficient of the substrate body bias dependence of Weff
dwbc	m	0.0	Width offset for the body contact isolation edge
dwg	m/V	0.0	Coefficient of the gate dependence of Weff
esati	V/m	1.e7	Saturation channel electric field for the impact ionization current
eta0	-	0.08	DIBL coefficient in the subthreshold region
etab	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
fbjtii	-	0.0	Fraction of the bipolar current affecting the impact ionization
Isbjt	A/m^2	1.0e-6	BJT injection saturation current
Isdif	A/m^2	0	Body to source/drain injection saturation current
Isrec	A/m^2	1.0e-5	Recombination in the depletion saturation current
Istun	A/m^2	0.0	Reverse tunneling saturation current

Table 130 MOSFET Level 57 DC Parameters (Continued)

Parameter	Unit	Default	Description
k1	$V^{1/2}$	0.6	First-order body effect coefficient
k1w1	m	0	First-order effect width dependent parameter
k1w2	m	0	Second-order effect width dependent parameter
k2	-	0	Second-order body effect coefficient
k3	-	0	Narrow coefficient
k3b	1/V	0	Body effect coefficient of k3
kb1	-	1	Backgate body charge coefficient
keta	1/V	-0.6	Body-bias coefficient of the bulk charge effect
Ketas	V	0.0	Surface potential adjustment for the bulk charge effect
Lbjt0	m	0.2e-6	Reference channel length for the bipolar current
lii	-	0	Channel length dependence parameter for the impact ionization current
lint	m	0.0	Length offset fitting parameter from I-V without bias
Ln	m	2.0e-6	Electron/hole diffusion length
Nbjt	-	1	Power coefficient of the channel length dependency for the bipolar current
NdioDE	-	1.0	Diode non-ideality factor
nfactor	-	1	Subthreshold swing factor
Ngidl	V	1.2	GIDL V_{ds} enhancement coefficient
nlx	m	1.74e-7	Lateral non-uniform doping parameter
Nrecf0	-	2.0	Recombination non-ideality factor at the forward bias

Table 130 MOSFET Level 57 DC Parameters (Continued)

Parameter	Unit	Default	Description
Nrecr0	-	10	Recombination non-ideality factor at the reversed bias
Ntun	-	10.0	Reverse tunneling non-ideality factor
pclm	-	1.3	Channel length modulation parameter
PDIBLC1	-	0.39	Correction parameter for the DIBL effect of the first output resistance
pdiblc2	-	0.0086	Correction parameter for the DIBL effect of the second output resistance
prwb	$1/V^{1}$	0	Body effect coefficient of Rdsw
prwg	$1/V^{1/2}$	0	Gate-bias effect coefficient of Rdsw
pvag	-	0.0	Gate dependence of the Early voltage
Rbody	ohm/m^2	0.0	Intrinsic body contact sheet resistance
Rbsh	ohm/m^2	0.0	Extrinsic body contact sheet resistance
rdsw	$\Omega*\mu m^{wr}$	100	Parasitic resistance per unit width
rsh	ohm/square	0.0	Source/drain sheet resistance in ohm per square
sii0	1/V	0.5	First V_{gs} dependence parameter for the impact ionization current
sii1	1/V	0.1	Second V_{gs} dependence parameter for the impact ionization current
sii2	1/V	0	Third V_{gs} dependence parameter for the impact ionization current
siid	1/V	0	V_{ds} dependence parameter of the drain saturation voltage for the impact ionization current

Table 130 MOSFET Level 57 DC Parameters (Continued)

Parameter	Unit	Default	Description
tii	-	0	Temperature dependence parameter for the impact ionization current
u0	$cm^2/(V\text{-}sec)$	NMOS-670 PMOS-250	Mobility at Temp=Tnom
ua	m/V	2.25e-9	First-order mobility degradation coefficient
ub	$(m/V)^2$	5.87e-19	Second-order mobility degradation coefficient
uc	1/V	-0.0465	Body-effect of the mobility degradation coefficient
Vabjt	V	10	Early voltage for the bipolar current
vdsatii0	V	0.9	Nominal drain saturation voltage at threshold for the impact ionization current
VECB	v	0.026v	Electron tunneling from the conduction band
VEVB	v	0.075v	Electron tunneling from the valence band
voff	v	-0.08	Offset voltage in the subthreshold region for large W and L values
Vrec0	V	0.0	Voltage dependent parameter for the recombination current
vsat	m/sec	8e4	Saturation velocity at Temp=Tnom
vth0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
Vtun0	V	0.0	Voltage dependent parameter for the tunneling current
w0	m	0	Narrow width parameter
wint	m	0.0	Width offset fitting parameter from I-V without bias
wr	-	1	Width offset from Weff for the Rds calculation

Table 131 MOSFET Level 57 AC & Capacitance Parameters

Parameter	Unit	Default	Description
acde	m/V	1.0	Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions
asd	V	0.3	Smoothing parameter for the source/drain bottom diffusion
cf	F/m	cal.	Fringing field capacitance of the gate-to-source/drain
cgdl	F/m	0.0	Overlap capacitance for the lightly-doped drain-gate region
cgdo	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0	Gate substrate overlap capacitance per unit channel length
cgsl	F/m	0.0	Overlap capacitance for the lightly-doped source-gate region
cgso	F/m	calculated	Non LDD region source-gate overlap capacitance per channel length
cjswg	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
ckappa	F/m	0.6	Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region
clc	m	0.1e-7	Constant term for the short-channel model
cle	-	0.0	Exponential term for the short-channel model
csdesw	F/m	0.0	Fringing capacitance per unit length for the source/drain sidewall
csdmin	V	cal.	Minimum capacitance for the source/drain bottom diffusion
delvt	V	0.0	Threshold voltage adjustment for C-V
dlbg	m	0	Length offset fitting parameter for the backgate charge

Table 131 MOSFET Level 57 AC & Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
dlc	m	lint	Length offset fitting parameter for the gate charge
dlcb	m	lint	Length offset fitting parameter for the body charge
dwc	m	wint	Width offset fitting parameter from C-V
fbody	-	1.0	Scaling factor for the body charge
Ldif0	-	1	Channel length dependency coefficient of the diffusion cap.
mjswg	V	0.5	Grading coefficient of the source/drain (gate side) sidewall junction capacitance
moin	$V^{1/2}$	15.0	Coefficient for the gate-bias dependent surface potential
Ndif	-	-1	Power coefficient of the channel length dependency for the diffusion capacitance
pbswg	V	0.7	Built-in potential of the source/drain (gate side) sidewall junction capacitance
tt	second	1ps	Diffusion capacitance transit time coefficient
vsdfb	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
vsdth	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
xpart	-	0	Charge partitioning rate flag

Table 132 MOSFET Level 57 Temperature Parameters

Parameter	Unit	Default	Description
at	m/sec	3.3e4	Temperature coefficient for U_a
cth0	$m^oC/(W*s)$	0	Normalized thermal capacity

Table 132 MOSFET Level 57 Temperature Parameters (Continued)

Parameter	Unit	Default	Description
kt1	V	-0.11	Temperature coefficient for the threshold voltage
kt2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
ktil	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
Ntrecf	-	0	Temperature coefficient for N_{recf}
Ntrecr	-	0	Temperature coefficient for N_{recr}
prt	Ω-um	0	Temperature coefficient for Rdsw
rth0	m^oC/W	0	Normalized thermal resistance
tcjswg	1/K	0	Temperature coefficient of C_{jswg}
tnom	^oC	25	Temperature at which simulation expects parameters
tpbswg	V/K	0	Temperature coefficient of P_{bswg}
ua1	m/V	4.31e-9	Temperature coefficient for U_a
ub1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
uc1	1/V	-0.056	Temperature coefficient for U_c
ute	-	-1.5	Mobility temperature exponent
xbjt	-	1	Power dependence of j_{bjt} on the temperature
xdif	-	XBJT	Power dependence of j_{dif} on the temperature
xrec	-	1	Power dependence of j_{rec} on the temperature
xtun	-	0	Power dependence of j_{tun} on the temperature

Notes:

- BSIMPD2.01 supports capmod=2 and 3 only. It does not support capmod=0 and 1.
- Modern SOI technology commonly uses source/drain extension or LDD. The source/drain junction depth (Xj) can be different from the silicon film thickness (Tsi). By default, if you do not specify Xj, simulation sets it to Tsi. Xj cannot be greater than Tsi.
- BSIMPD refers the substrate to the silicon below the buried oxide (not to the well region in BSIM3) to calculate the backgate flatband voltage (Vfbb) and the parameters related to the source/drain diffusion bottom capacitance (Vsdth, Vsdfb, Csdmin).
  - Positive nsub means the same type of doping as the body.
  - Negative nsub means the opposite type of doping.
- New W0FLK Parameter:

  The following equation models the SPICE2 flicker noise current density, used in both UCB SOI code and the Synopsys Level=57 MOSFET model for noiMod=1 and 4:

  ```
  Sid,f[I2/Hz]=KF*Ids^AF/(Cox*Leff^2*f^EF) -- (1)
  ```

  However, if AF is not equal to unity, it does not scale properly with Weff, because Ids is approximately proportional to Weff. Also, without the HSPICE multiplicity factor (M factor) in equation (1), this model cannot simulate multiple transistors in parallel.

  To solve these problems, HSPICE 2002.2 added a W0FLK (width normalizing) parameter, and corrects equation (1) as:

  ```
  M*KF*[(Weff/W0FLK)(1-AF)]*Ids^AF/(Cox*Leff^2*f^EF) -- (2)
  ```

  The default value of W0FLK is -1.0 to switch off the new width-scaling model. The unit is in meters.

  The next equation handles the flicker noise model (noimod=1 & 4), depending on whether you specify W0FLK.

  If W0FLK <= 0.0 (the default case), then the flicker noise model of noiMod=1 and 4 uses this equation for backward compatibility.

  ```
     M*KF*Ids^AF/(Cox*LeffA2*f^EF) -- (3)
  ELSE
     M*KF*[(Weff/W0FLK)^(1-AF)]*Ids^AF/(Cox*Leff^2*f^EF)
  ```

Level 57 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 14.

Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22

- BSIM PD version 2.2 enhances the model flexibility and accuracy from PD version 2.0, and the following are its major features.
  - Gate-body tunneling (substrate current) enhances the model accuracy.
  - Body contact resistance improves the modeling accuracy.
  - Binning enhances the model flexibility.
- BSIM PD version 2.21 updates the PD version 2.2 for bug fixes and S/D swapping for the gate current components.
- BSIM PD version 2.22 updates the 2.21 version for bug fixes and enhancements. The major features are:
  - FRBODY instance parameter
  - Improved temperature dependence of the gate direct tunneling model
  - Two new model parameters, VEVB and VECB
  - UC Berkeley code no longer supports the NECB and NEVB model parameters. Version 2.22 accepts these parameters for backwards compatibility, but they have no effect.
- **.OPTION** LIST prints an element summary for the MOSFET Level=57 model.

bjtoff	BJT on/off flag (Turn off BJT if equal to 1)
rth0	Thermal Resistance per unit width
cth0	Thermal Capacitance per unit width
nrb	Number of squares for the body series resistance
frbody	Coefficient of the distributed body resistance effects
nbc	Number of body contact isolation edge
nseg	Number of segments for channel width partitioning
pdbcp	Parasitic perimeter length for the body contact at the drain side
psbcp	Parasitic perimeter length for the body contact at the source side
agbcp	Parasitic gate-to-body overlap area for the body contact

aebcp Parasitic body-to-substrate overlap area for the body contact
vbsusr Optional initial value of Vbs, which you specify for transient analysis

- BSIM PD version 2.23 includes several bug fixes and enhancements from version 2.2.
  - Adds geometric dependency in CV delta L and delta W.
  - Fixes a gate-body-tunneling residue problem in the low-bias region.
  - Provides an additional parameter (dtoxcv) in capMod=3 for flexibility
  - Other bug fixes

Using BSIM3-SOI PD

To use BSIM3-SOI PD versions 2.0, 2.2, 2.21, or 2.22 in simulation, apply the VERSION model parameter. For example:

- Invokes PD2.0 if VERSION=2.0
- Invokes PD2.2 and PD2.21 if VERSION=2.2
- Invokes PD2.22 if VERSION=2.22
- Invokes PD2.23 if VERSION=2.23.

For gate-body tunneling, set the IGMOD model parameter to 1.

Example

```
mckt drain gate source bulk nch L=10e-6 W=10e-6
.model nch   nmos Level=57   igmod=1   version=2.2
+ tnom=27   tox=4.5e-09   tsi=.0000001   tbox=8e-08
+ mobmod=0   capmod=2   shmod=0   paramchk=0
+ wint=0   lint=-2e-08   vth0=.42   k1=.49
+ k2=.1   k3=0   k3b=2.2   nlx=2e-7
+ dvt0=10   dvt1=.55   dvt2=-1.4   dvt0w=0
+ dvt1w=0   dvt2w=0   nch=4.7e+17   nsub=-1e+15
+ ngate=1e+20   agidl=1E-15   bgidl=1E9   ngidl=1.1
+ ndiode=1.13   ntun=14.0   nrecf0=2.5   nrecr0=4
+ vrec0=1.2   ntrecf=.1   ntrecr=.2   isbjt=1E-4
+ isdif=1E-5   istun=2E-5   isrec=4E-2   xbjt=.9
+ xdif=.9    xrec=.9   xtun=0.01   ahli=1e-9
+ lbjt0=0.2e-6   ln=2e-6   nbjt=.8   ndif=-1
+ aely=1e8   vabjt=0   u0=352   ua=1.3e-11
+ ub=1.7e-18   uc=-4e-10   w0=1.16e-06   ags=.25
+ A1=0   A2=1   b0=.01   b1=10
+ rdsw=0   prwg=0   prwb=-.2   wr=1
+ rbody=1E0   rbsh=0.0   a0=1.4   keta=0.1
```

```
+ ketas=0.2   vsat=135000   dwg=0   dwb=0
+ alpha0=1e-8   beta0=0   beta1=0.05   beta2=0.07
+ vdsatii0=.8   esatii=1e7   voff=-.14   nfactor=.7
+ cdsc=.00002   cdscb=0   cdscd=0   cit=0
+ pclm=2.9   pvag=12   pdiblc1=.18   pdiblc2=.004
+ pdiblcb=-.234   drout=.2   delta=.01   eta0=.05
+ etab=0   dsub=.2   rth0=.005   clc=.0000001
+ cle=.6   cf=1e-20   ckappa=.6   cgdl=1e-20
+ cgsl=1e-20   kt1=-.3   kt1l=0   kt2=.022
+ ute=-1.5   ua1=4.31e-09   ub1=-7.61e-18   uc1=-5.6e-11
+ prt=760   at=22400   cgso=1e-10   cgdo=1e-10
+ cjswg=1e-12   tt=3e-10   asd=0.3   csdesw=1e-12
+ tcjswg=1e-4   mjswg=.5   pbswg=1
```

UCB BSIMSOI3.1

In addition to BSIMSOI3.0, the MOSFET Level 57 model also supports the UCB BSIMSOI3.1 model version, which includes the following new features that are not available in BSMISOI3.0.

Ideal Full-Depletion (FD) Modeling

BSIMSOI3.0 supports the modeling of these two families of SOI MOSFETs with a SOIMOD switching model flag.

- SOIMOD = 0 for partially depleted devices (PD).
- SOIMOD = 1 for devices that tend to operate in a mixed mode of PD and FD.

V3.1 also provides an ideal full-depletion (FD) module (SOIMOD=2), not available in V3.0 to model FD SOI devices that literally exhibit no floating-body behavior. As in BSIMSOI3.0, the default SOIMOD value is 0 for BSIMSOI3.1.

The following physical modeling components, related to the internal SOI body node, are critical for accurately modeling PD SOI devices, but are not needed for the ideal FD module. Thus, for the ideal FD module, HSPICE ignores these components, which makes SOI MOSFET modeling much easier than for PD devices, or non-ideal FD devices.

- Source/Drain to body diode currents
- Source-Body-Drain parasitic BJT currents
- Impact ionization currents
- Gate-body direct currents
- Body-related capacitances.

Gate Resistance Modeling

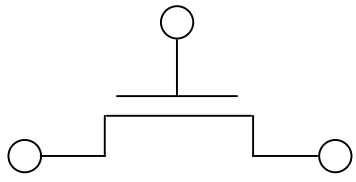
BSIMSOI3.1 uses the same gate resistance models as in the BSIM4 model with four options for various gate-resistance modeling topologies.

Table 133 BSIMSOI3.1 Gate Resistance Modeling Topologies

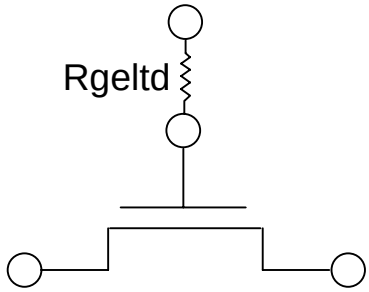
Name	Unit	Default	Bin	Description
NGCON	-	-	N	Number of gate contacts
RGATEMOD	-	0	N	Gate resistance model selector • RGATEMOD = 0: No gate resistance • RGATEMOD = 1: Constant gate resistance • RGATEMOD = 2: Rii model with variable resistance • RGATEMOD = 3: Rii model with two nodes
RSHG	Ohm/Sq	0.1	N	Gate electrode sheet resistance
XGL	m	0	N	Offset of the gate length due to variations in patterning
XGW	m	0	N	Distance from the gate contact to the channel edge in the W direction
XRCRG1	-	12	Y	Parameter for distributed channel-resistance effect for intrinsic input resistance
XRCRG2	-	1	Y	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance

Gate Resistance Equivalent Circuit

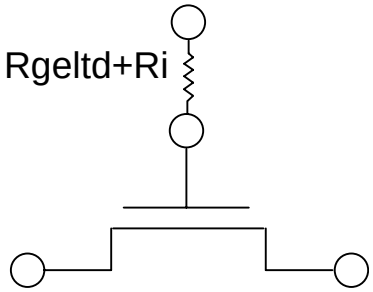
- RGATEMOD = 0: No gate resistance (default)



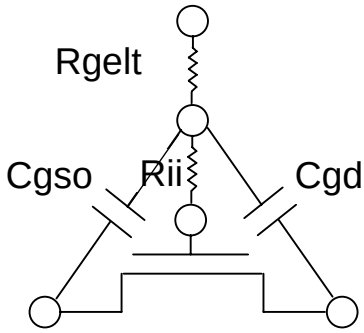
- RGATEMOD = 1: Constant gate resistance



- RGATEMOD = 2: Variable resistance with Rii model



- RGATEMOD = 3: Rii model with two nodes



- Rgeltd: (Poly) gate electrode resistance, bias independent.
- Rii: Intrinsic input gate resistance, reflected to the gate from the intrinsic channel region. It is bias dependent and a first-order non-quasi static model for RF and rapid transient MOSFET operations.

Enhanced Binning Capability

Model parameters for the following components are now binnable for better accuracy and scalability:

- Junction depth
- Gate-tunneling current
- Temperature dependence of threshold voltage, mobility, saturation velocity, parasitic resistance, and diode currents.

Bug Fixes

The BSIMSOI3.1 from UC Berkeley fixes the following bugs in the BSIMSOI3.0 model:

- The model now takes NSEG into account when calculating the gate-channel tunneling current.
- The GMIN connecting gate and drain is now multiplied by 1e-6 to reduce false leakage current.
- A swapping error in the source/drain overlap capacitance stamping.
- The bulk charge effect coefficient (A_{bulkCV}) is now corrected for Q_{inv} and its derivatives in CAPMOD=2

Level 59 UC Berkeley BSIM3-SOI FD Model

The UC Berkeley SOI (BSIM3-SOI) Fully Depleted (FD) model is Level 59 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3SOI FD2.1 MOSFET MODEL User Manual*, at:

http://www-device.eecs.berkeley.edu/~bsim3soi

The general syntax for including a BSIM3-SOI FD MOSFET element in a netlist is:

```
Mxxx nd ng ns ne <np> mname <L=val>
+ <W=val> <M=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <NRD=val> <NRS=val> <NRB=val> <RTH0=val> <CTH0=val>
+ <off> <BJToff=val> <IC=Vds, Vgs, Vbs, Ves, Vps>
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	Optional external body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD.
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS.
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides DEFNRD in the OPTIONS statement.

Parameter	Description
NRS	Number of squares of source diffusion for the source series resistance. Overrides DEFNRS in the OPTIONS statement.
NRB	Number of squares for the body series resistance.
RTH0	Thermal resistance per unit width: • If you do not specify RTH0, simulation extracts it from the model card. • If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width • If you do not specify CTH0, simulation extracts it from the model card. • If you specify CTH0, it overrides CTH0 in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps in a 4-terminal device) Simulation uses these settings if you specify UIC in the .TRAN statement. The .IC statement overrides them.

Level 59 Model Parameters

Table 134 MOSFET Level 59 Model Control Parameters

Parameter	Unit	Default	Description
CAPMOD	-	2	Flag for the short channel capacitance model
Level	-	-	Level 59 for BSIM3SOI
MOBMOD	-	1	Mobility model selector

Table 134 MOSFET Level 59 Model Control Parameters (Continued)

Parameter	Unit	Default	Description
NOIMOD	-	1	Flag for the Noise model
SHMOD	-	0	Flag for self-heating: • 0 = no self-heating • 1 = self-heating

Table 135 MOSFET Level 59 Process Parameters

Parameter	Unit	Default	Description
NCH	$1/cm^3$	1.7e17	Channel doping concentration
NGATE	$1/cm^3$	0	Poly gate doping concentration
NSUB	$1/cm^3$	6.0e16	Substrate doping concentration
TBOX	m	3.0e-7	Buried oxide thickness
TOX	m	1.0e-8	Gate oxide thickness
TSI	m	1.0e-17	Silicon film thickness

Table 136 MOSFET Level 59 DC Parameters

Parameter	Unit	Default	Description
A0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
ABP	-	1.0	Coefficient of A_{beff} dependency on V_{gst}
ADICE0	-	1	DICE bulk charge factor
AGIDL	1/W	0.0	GIDL constant

Table 136 MOSFET Level 59 DC Parameters (Continued)

Parameter	Unit	Default	Description
AGS	1/V	0.0	Gate bias coefficient of A_{bulk}
AII	1/V	0.0	First Vdsatii parameter for the Leff dependence
ALPHA0	m/V	0.0	First parameter of the impact ionization current
ALPHA1	1/V	1.0	Second parameter of the impact ionization current
B0	m	0.0	Bulk charge effect coefficient for the channel width
B1	m	0.0	Width offset for the bulk charge effect
BGIDL	V/m	0.0	GIDL exponential coefficient
BII	m/V	0.0	Second Vdsatii parameter for the Leff dependence
CDSC	F/m^2	2.4e-4	Drain/source to the channel coupling capacitance
CDSCB	F/m^2	0	Body-bias sensitivity of cdsc
CDSCD	F/m^2	0	Drain-bias sensitivity of cdsc
CII	-	0.0	First Vdsatii parameter for the V_{ds} dependence
CIT	F/m^2	0.0	Interface trap capacitance
DELP	V	0.02	Constant for limiting V_{bseff} to the surface potential
DELTA	-	0.01	Effective V_{ds} parameter
DII	V	-1.0	Second Vdsatii parameter for the V_{ds} dependence
DROUT	-	0.56	L dependence coefficient of the DIBL correction parameter in R_{out}
DSUB	-	0.56	DIBL coefficient exponent
DVBD0	V	0	First coefficient of the V_{ds} 0 dependency on Leff
DVBD1	V	0	Second coefficient of the V_{ds} 0 dependency on Leff

Table 136 MOSFET Level 59 DC Parameters (Continued)

Parameter	Unit	Default	Description
DVT0	-	2.2	First coefficient of the short-channel effect on V_{th}
DVT0W	-	0	First coefficient of the narrow-width effect on V_{th} for a small channel length
DVT1	-	0.53	Second coefficient of the short-channel effect on V_{th}
DVT1W	-	5.3e6	Second coefficient of the narrow-width effect on V_{th} for a small channel length
DVT2	1/V	-0.032	Body-bias coefficient of the short-channel effect on V_{th}
DVT2W	1/V	-0.032	Body-bias coefficient of the narrow width effect on V_{th} for small channel length
DWB	$m/V^{1/2}$	0.0	Coefficient of the substrate body bias dependence for Weff
DWG	m/V	0.0	Coefficient of the gate dependence for Weff
EDL	m	2e-6	Electron diffusion length
ETA0	-	0.08	DIBL coefficient in the subthreshold region
ETAB	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
ISBJT	A/m^2	1.0e-6	BJT injection saturation current
ISDIF	A/m^2	0	Body to source/drain injection saturation current
ISREC	A/m^2	1.0e-5	Recombination in the depletion saturation current
ISTUN	A/m^2	0.0	Reverse tunneling saturation current
K1	$V^{1/2}$	0.6	Coefficient for the first-order body effect
K2	-	0	Coefficient for the second-order body effect

Table 136 MOSFET Level 59 DC Parameters (Continued)

Parameter	Unit	Default	Description
K3	-	0	Narrow coefficient
K3B	1/V	0	Body-effect coefficient of k3
KB1	-	1	Coefficient of the V_{bs} 0 dependency on V_{gbs}
KB3	-	1	Coefficient of the V_{bs}0 dependency on V_{gs} at subthreshold region
KBJT1	m/V	0	Parasitic bipolar Early effect coefficient
KETA	m	-0.6	Body-bias coefficient of the bulk charge effect
LINT	m	0.0	Length-offset fitting parameter from I-V without bias
MXC	-	-0.9	Fitting parameter for calculating A_{beff}
NDIODE	-	1.0	Diode non-ideality factor
NFACTOR	-	1	Subthreshold swing factor
NGIDL	V	1.2	GIDL V_{ds} enhancement coefficient
NLX	m	1.74e-7	Lateral non-uniform doping parameter
NTUN	-	10.0	Reverse tunneling non-ideality factor
PCLM	-	1.3	Channel length modulation parameter
PDIBL1	-	0.39	First correction parameter for the DIBL effect of the output resistance
PDIBL2	-	0.0086	Second correction parameter for the DIBL effect of the output resistance
PRWB	$1/V^{1}$	0	Body effect coefficient of Rdsw
PRWG	$1/V^{1/2}$	0	Gate bias effect coefficient of Rdsw
PVAG		0.0	Gate dependence of the Early voltage

Table 136 MOSFET Level 59 DC Parameters (Continued)

Parameter	Unit	Default	Description
RBODY	ohm/m^2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/m^2	0.0	Extrinsic body contact sheet resistance
RDSW	$\Omega*\mu m^{wr}$	100	Parasitic resistance per unit width
RSH	ohm/square	0.0	Source/drain sheet resistance in ohm per square
U0	cm^2/(V-sec)	NMOS-670 PMOS-250	Mobility at Temp=Tnom
UA	m/V	2.25e-9	First-order coefficient for mobility degradation
UB	$(m/V)^2$	5.87e-19	Second-order coefficient for mobility degradation
UC	1/V	-0.0465	Body-effect coefficient for mobility degradation
VBSA	V	0	Transition body voltage offset
VOFF	v	-0.08	Offset voltage in the subthreshold region for large W and L values
VSAT	m/sec	8e4	Saturation velocity at Temp=Tnom
VTH0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
W0	m	0	Narrow width parameter
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WR	-	1	Width offset from Weff for calculating R_{ds}

Table 137 MOSFET Level 59 AC/Capacitance Parameters

Parameter	Unit	Default	Description
ASD	V	0.3	Smoothing parameter for the source/drain bottom diffusion
CF	F/m	cal.	Gate to source/drain fringing field capacitance
CGDL	F/m	0.0	Lightly-doped drain-gate region overlap capacitance
CGDO	F/m	calculated	Non-LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0.0	Gate-substrate overlap capacitance per channel length
CGSL	F/m	0.0	Lightly-doped source-gate region overlap capacitance
CGSO	F/m	calculated	Non-LDD region source-gate overlap capacitance per channel length
CJSWG	F/m^2	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for lightly-doped region overlap capacitance fringing field capacitance
CLC	m	0.1e-7	Constant term for the short channel model
CLE	-	0.0	Exponential term for the short channel model
CSDESW	F/m	0.0	Source/drain sidewall fringing capacitance per unit length
CSDMIN	V	cal.	Source/drain bottom diffusion minimum capacitance
DLC	m	lint	Length offset fitting parameter for the gate charge
DWC	m	wint	Width offset fitting parameter from C-V
MJSWG	V	0.5	Source/drain (gate side) sidewall junction capacitance grading coefficient
PBSWG	V	0.7	Built-in potential for the source/drain (gate side) sidewall junction capacitance
TT	second	1ps	Diffusion capacitance transit time coefficient

Table 137 MOSFET Level 59 AC/Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
VSDFB	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
VSDTH	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
XPART	-	0	Charge partitioning rate flag

Table 138 MOSFET Level 59 Temperature Parameters

Parameter	Unit	Default	Description
AT	m/sec	3.3e4	Temperature coefficient for U_a
CTH0	$m^oC/(W*s)$	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient for the temperature effect of the threshold voltage
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
PRT	Ω-um	0	Temperature coefficient for R_{dsw}
RTH0	m^oC/W	0	Normalized thermal resistance
TNOM	^oC	25	Temperature at which simulation expects parameters
UA1	m/V	4.31e-9	Temperature coefficient for U_a
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
UC1	1/V	-0.056	Temperature coefficient for U_c
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of j_{bjt} on the temperature

Table 138 MOSFET Level 59 Temperature Parameters (Continued)

Parameter	Unit	Default	Description
XDIF	-	XBJT	Power dependence of j_{dif} on the temperature
XREC	-	1	Power dependence of j_{rec} on the temperature
XTUN	-	0	Power dependence of j_{tun} on the temperature

Note: BSIMFD refers the substrate to the silicon below the buried oxide, not to the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the bottom capacitance of the source/drain diffusion (V_{sdth}, V_{sdfb}, C_{sdmin}).

- Positive nsub means the same type of doping as the body.
- Negative nsub means opposite type of doping.

Level 59 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see Table 4 on page 14.

Level 60 UC Berkeley BSIM3-SOI DD Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices. BSIM3DD2.2 for DD SOI devices is Level 60 in the Synopsys MOSFET models.

For a description of this model, see the *BSIM3DD2.1 MOSFET MODEL User's Manual*, at

`http://www-device.eecs.berkeley.edu/~bsim3soi`

BSIM3DD2.1 includes many advanced concepts for dynamic and continuous transition between PD and FD operation. These concepts are collectively named Dynamic Depletion.

Model Features

- Simulation applies dynamic depletion to both I-V and C-V. Tbox and Tsi continuously scale the charge and drain current.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Diode and C-V formulation properly bind the body potential.
- Improved self-heating.
- Improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current.
- Depletion charge model (EBCI) for better accuracy in predicting capacitive coupling. The BSIM3v3 based model is also improved.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3v3.1 to assure continuities of Ids, Gds, Gm and their derivatives for all bias conditions.

Syntax

The general syntax for a BSIM3SOI MOSFET element in a netlist is:

```
Mxxx nd ng ns ne <np> mname <L=val> <W=val> <M=val>
+ <AD=val> <AS=val> <PD=val> <PS=val> <NRD=val> <NRS=val>
+ <NRB=val> <RTHO=val> <CTHO=val> <off> <BJToff=val>
+ <IC=Vds, Vgs, Vbs, Ves, Vps>
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.

Parameter	Description
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an **.OPTION** statement. Default=DEFL with a maximum of 0.1m.
W	SOI MOSFET channel width in meters. This parameter overrides DEFW in an **.OPTION** statement. Default=DEFW with a maximum of 0.1m.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the **.OPTION** statement: Default=DEFAD
AS	Source diffusion area. Overrides DEFAS in the **.OPTION** statement: Default=DEFAS
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the **.OPTION** statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the **.OPTION** statement.
NRD	Number of squares of the drain diffusion for the drain series resistance. Overrides DEFNRD in the **.OPTION** statement.
NRS	Number of squares of the source diffusion for the source series resistance. Overrides DEFNRS in the**.OPTION** statement.
NRB	Number of squares for the body series resistance.
RDC	Additional drain resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default =0.0.

Parameter	Description
RSC	Additional source resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0.
RTHO	Thermal resistance per unit width: • If you do not specify RTHO, simulation extracts it from the model card. • If you specify RTHO, it overrides RTHO in the model card.
CTHO	Thermal capacitance per unit width: • If you do not specify CTHO, simulation extracts it from the model card. • If you specify CTHO, it overrides CTHO in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the **.TRAN** statement. The .IC statement overrides it.

Level 60 Model Parameters

Table 139 MOSFET Level 60 BSIMSOI Model Control Parameters

SPICE Symbol	Description	Unit	Default	See Table 144
shMod	Flag for self-heating • 0 = no self-heating • 1 = self-heating	-	0	
mobmod	Mobility model selector	-	1	-
capmod	Flag for the short channel capacitance model	-	2	nI-1
noimod	Flag for the noise model	-	1	-

Table 140 MOSFET Level 60 Process Parameters

SPICE Symbol	Description	Unit	Default	See Table 144
Tsi	Silicon film thickness	m	10-7	-
Tbox	Buried oxide thickness	m	$3x10^{-7}$	-
Tox	Gate oxide thickness	m	$1x10^{-8}$	-
Nch	Channel doping concentration	$1/cm^3$	$1.7x10^{17}$	-
Nsub	Substrate doping concentration	$1/cm^3$	$6x10^{16}$	nI-2
ngate	Poly gate doping concentration	$1/cm^3$	0	-

Table 141 MOSFET Level 60 DC Parameters

SPICE Symbol	Description	Unit	Default	See Table 144
vth0	Threshold voltage @ V_{bs} =0 for the long and wide device	-	0.7	nI-3
k1	First order body effect coefficient	$V^{1/2}$	0.6	-
k2	Second order body-effect coefficient	-	0	-
k3	Narrow width coefficient	-	0	-
k3b	Body-effect coefficient of k3	1/V	0	-
Vbsa	Transition body voltage offset	V	0	-
delp	Constant for limiting Vbseff to fs	V	0.02	-
Kb1	Coefficient of Vbs0 dependency on Ves	-	1	-
Kb3	Coefficient of Vbs0 dependency on V_{gs} at the subthreshold region	-	1	-

Table 141 MOSFET Level 60 DC Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
Dvbd0	First coefficient of Vbs0, Leff dependency	V	0	-
Dvbd1	Second coefficient of Vbs0, Leff dependency	V	0	-
w0	Narrow width parameter	m	0	-
nlx	Lateral non-uniform doping parameter	m	1.74e-7	-
dvt0	First coefficient of the short-channel effect on Vth	-	2.2	-
dvt1	Second coefficient of the short-channel Vth effect	-	0.53	-
dvt2	Body-bias coefficient of the short-channel Vth effect	1/V	-0.032	-
dvt0w	First coefficient of the narrow-width effect on Vth for a small channel length	-	0	-
dvt1w	Second coefficient of the narrow-width effect on Vth for a small channel length	-	5.3e6	-
dvt2w	Body-bias coefficient of the narrow-width effect on Vth for a small channel length	1/V	-0.032	-
u0	Mobility at Temp = Tnom • NMOSFET • PMOSFET	$cm^2/(V\text{-}sec)$	 670 250	-
ua	First-order mobility degradation coefficient	m/V	2.25e-9	-
ub	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	-
uc	Body-effect of the mobility degradation coefficient	1/V	-.0465	-
vsat	Saturation velocity at Temp = Tnom	m/sec	8e4	-

Table 141 MOSFET Level 60 DC Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
a0	Bulk charge effect coefficient for the channel length	-	1.0	-
ags	Gate bias coefficient of A_{bulk}	1/V	0.0	-
b0	Bulk charge effect coefficient for the channel width	m	0.0	-
b1	Bulk charge effect width offset	m	0.0	-
keta	Body-bias coefficient of the bulk charge effect	m	-0.6	-
Abp	Coefficient of the Abeff dependency on Vgst	-	1.0	-
mxc	Fitting parameter for calculating Abeff	-	-0.9	-
adice0	DICE bulk charge factor	-	1	-
A1	First non-saturation effect parameter	1/V	0.0	-
A2	Second non-saturation effect parameter	0	1.0	-
rdsw	Parasitic resistance per unit width	W-mmWr	100	-
prwb	Body-effect coefficient of Rdsw	1/V	0	-
prwg	Gate bias effect coefficient of Rdsw	$1/V^{1/2}$	0	-
wr	Width offset from Weff for calculating Rds	-	1	-
wint	Width offset fitting parameter of I-V without bias	m	0.0	-
lint	Length offset fitting parameter of I-V without bias	m	0.0	-
dwg	Coefficient of the gate dependence of W_{eff}	m/V	0.0	
dwb	Coefficient, substrate body bias dependence, W_{eff}	$m/V^{1/2}$	0.0	

Table 141 MOSFET Level 60 DC Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
voff	Offset voltage in the subthreshold region for large W and L values	V	-0.08	-
nfactor	Subthreshold swing factor	-	1	-
eta0	DIBL coefficient in the subthreshold region	-	0.08	-
etab	Body-bias coefficient for subthreshold DIBL effect	1/V	-0.07	-
dsub	DIBL coefficient exponent	-	0.56	-
cit	Interface trap capacitance	F/m^2	0.0	-
cdsc	Drain/Source to the channel coupling capacitance	F/m^2	2.4e-4	-
cdscb	Body-bias sensitivity of C_{dsc}	F/m^2	0	-
cdscd	Drain-bias sensitivity of C_{dsc}	F/m^2	0	-
pclm	Channel length modulation parameter	-	1.3	-
pdibl1	Correction parameter for the DIBL effect of the first output resistance	-	.39	-
pdibl2	Correction parameter for the DIBL effect of the second output resistance	-	0.086	-
drout	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	-
pvag	Gate dependence of the Early voltage	-	0.0	-
delta	Effective V_{ds} parameter	-	0.01	-
aii	First Vdsatii parameter for the Leff dependence	1/V	0.0	-
bii	Second Vdsatii parameter for the Leff dependence	m/V	0.0	-

Table 141 MOSFET Level 60 DC Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
cii	First Vdsatii parameter for the Vds dependence	-	0.0	-
dii	Second Vdsatii parameter for the Vds dependence	V	-1.0	-
alpha0	First parameter of the impact ionization current	m/V	0.0	-
alpha1	Second parameter of the impact ionization current	1/V	1.0	-
beta0	Third parameter of the impact ionization current	V	30	-
Agidl	GIDL constant	W-1	0.0	-
Bgidl	GIDL exponential coefficient	V/m	0.0	-
Ngidl	GIDL Vds enhancement coefficient	V	1.2	-
ntun	Reverse tunneling non-ideality factor	-	10.0	-
Ndiode	Diode non-ideality factor	-	1.0	-
Isbjt	BJT injection saturation current	A/m2	1e-6	-
Isdif	Body to source/drain injection saturation current	A/m2	0.0	-
Isrec	Recombination in the depletion saturation current	A/m2	1e-5	-
Istun	Reverse tunneling saturation current	A/m2	0.0	-
Edl	Electron diffusion length	m	2e-6	-
Kbjt1	Parasitic bipolar early effect coefficient	m/V	0	-
Rbody	Intrinsic body contact sheet resistance	ohm/m2	0.0	-
Rbsh	Extrinsic body contact sheet resistance	ohm/m2	0.0	-
rsh	Source drain sheet resistance in ohm per square	Ω/square	0.0	-

Table 142 MOSFET 60 AC and Capacitance Parameters

SPICE Symbol	Description	Unit	Default	See Table 144
xpart	Charge partitioning rate flag	-	0	
cgso	Non-LDD region source-gate overlap capacitance per channel length	F/m	calculated	nC-1
cgdo	Non-LDD region drain-gate overlap capacitance per channel length	F/m	calculated	nC-2
cgeo	Gate substrate overlap capacitance per unit channel length	F/m	0.0	-
cjswg	Source/Drain (gate side) sidewall junction Capacitance per unit width (normalized to 100nm T_{si})	F/m^2	1e-10	-
pbswg	Built-in potential for the Source/Drain (gate side) sidewall junction capacitance	V	.7	-
mjswg	Grading coefficient for the Source/Drain (gate side) sidewall junction capacitance	V	0.5	-
tt	Coefficient for the diffusion capacitance transit time	second	1ps	-
vsdfb	Flatband voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-3
vsdth	Threshold voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-4
csdmin	Minimum capacitance of the source/drain bottom diffusion	V	calculated	nC-5
asd	Smoothing parameter for the source/drain bottom diffusion	-	0.3	-
csdesw	Source/drain sidewall fringing capacitance per unit length	F/m	0.0	-

Table 142 MOSFET 60 AC and Capacitance Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
cgs1	Overlap capacitance for the lightly-doped source-gate region	F/m	0.0	-
cgd1	Overlap capacitance for the lightly-doped drain-gate region	F/m	0.0	-
ckappa	Coefficient of the fringing field capacitance for the overlap capacitance in the lightly-doped region	F/m	0.6	-
cf	Fringing field capacitance for the gate-to-source/drain	F/m	calculated	nC-6
clc	Constant term for the short-channel mode	m	$0.1x10^{-7}$	-
cle	Exponential term for the short-channel mode	none	0.0	-
dlc	Length offset fitting parameter from C-V	m	lint	-
dwc	Width offset fitting parameter from C-V	m	wint	-

Table 143 MOSFET Level 60 Temperature Parameters

SPICE Symbol	Description	Unit	Default	See Table 144
tnom	Temperature at which simulation expects parameters	^oC	27	-
ute	Mobility temperature exponent	none	-1.5	-
kt1	Temperature coefficient for the threshold voltage	V	-0.11	-
kt11	Channel length dependence of the temperature coefficient for the threshold voltage	V*m	0.0	
kt2	Body-bias coefficient of the Vth temperature effect	none	0.022	-

Table 143 MOSFET Level 60 Temperature Parameters (Continued)

SPICE Symbol	Description	Unit	Default	See Table 144
ua1	Temperature coefficient for U_a	m/V	4.31e-9	-
ub1	Temperature coefficient for U_b	$(m/V)^2$	-7.61e-18	-
uc1	Temperature coefficient for U_c	1/V	-.056	nT-1
at	Temperature coefficient for the saturation velocity	m/sec	3.3e4	-
cth0	Normalized thermal capacity	moC/(W*sec)	0	-
prt	Temperature coefficient for Rdsw	Ω-μm	0	-
rth0	Normalized thermal resistance	moC/W	0	-
xbjt	Power dependence of jbjt on the temperature	none	2	-
xdif	Power dependence of jdif on the temperature	none	2	-
xrec	Power dependence of jrec on the temperature	none	20	-
xtun	Power dependence of j_{tun} on the temperature	none	0	-

Table 144 MOSFET Level 60 Model Parameter Notes

Note	Explanation
nI-1	*Capmod* 0 and 1 do not calculate the dynamic depletion. Therefore, ddMod does not work with *capmod*.
nI-2	BSIMSOI refers to a substrate of the silicon below the buried oxide, not the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, C_{sdmin}). • Positive n_{sub} is the same type of doping as the body. • Negative n_{sub} is the opposite type of doping.
nC-1	If you do not specify *cgso*, simulation calculates it: • if you specify *dlc* greater than 0, then cgso=pl=(dlc*cox)-cgs1 • if the previously-calculated cgso<0, then cgso=0 • else cgso=0.6*Tsi*cox
nC-2	Calculates *Cgdo* similar to *Csdo*
nC-3	If nsub is positive, then: $V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}\cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3$ else: $V_{sdfb} = -\frac{kT}{q}\log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$
nC-4	If nsub is positive, then: $\phi_{sd} = 2\frac{kT}{q}\log\left(\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753x10^{-12}\sqrt{n_{sub}}}{C_{box}}$ $V_{sdth} = V_{sdfb} + \phi_{sd} + \Upsilon_{sd}\sqrt{\phi_{sd}}$ else: $\phi_{sd} = 2\frac{kT}{q}\log\left(-\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753x10^{-12}\sqrt{-n_{sub}}}{C_{box}}$ $V_{sdth} = V_{sdfb} - \phi_{sd} + -\Upsilon_{sd}\sqrt{\phi_{sd}}$

Table 144 MOSFET Level 60 Model Parameter Notes (Continued)

Note	Explanation
nC-5	$X_{sddep} = \sqrt{\frac{2\varepsilon_{si}\phi_{sd}}{q\left\|n_{sub}\cdot 10^{6}\right\|}}, C_{sddep} = \frac{\varepsilon_{si}}{X_{sddep}}, C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep}+C_{box}}$
nC-6	If you do not specify cf, then simulation calculates it: $CF = \frac{2\varepsilon_{ox}}{\pi} 1n\left(1+\frac{4x10^{-7}}{T_{ox}}\right)$
nT-1	For mobmod=1 and 2, the unit is m/V^2. Default is -5.6E-11. For mobmod=3, the unit is 1/V and the default is -0.056.

Level 65 SSIMSOI Model

Level 65 is a surface-potential, charge-based, and partially depleted SOI MOSFET model developed by Motorola semiconductor.

Model Feature

The SSIMSOI model includes the following features:

- A simple linear body resistance- and body-tie parasitic for body-contacted SOI devices for several capacitances and conductances are added.
- A lateral bipolar model used to account for both the BJT current and the associated diffusion capacitance.
- Additional components of the channel-edge diode generation and recombination current. Side-wall and areal components of diode currents are removed.
- Shot noise sources associated with the parasitic currents used to model the observed Lorentzian noise spectra in SOI.
- The body-bias dependence for DIBL is removed to prevent convergence difficulties for typical forward body-bias operation in floating-body MOSFETs.
- Side-wall and areal junction (depletion) capacitances are removed and replaced with the appropriate SOI back-oxide capacitances.

- The SSIM HCI degradation, oxide reliability, and electromigration models are removed.
- Additional parameters are added to account for parasitics related to device contacts.
- Additional parameters are added to account for asymmetric S/D parasitics (diode current and capacitance, gate overlap tunneling currents, GIDL/GISL currents, and S/D resistances). Asymmetry can dramatically impact PDSOI floating-body effects.

Using Level 65 with Synopsys Simulators

To simulate using the SSIMSOI model:

1. Set Level=65 to identify the model as the SSIMSOI model.
2. Set the correct simulator room temperature.

   The default room temperature is 25C in Synopsys circuit simulators, but is 27 oC in most other simulators. When comparing to other simulators, use **TEMP** 27 or **.OPTION** TNOM=27 to set the simulation temperature to 27 in the netlist.
3. Set DTEMP on the element line.

   You can use DTEMP with this model to increase the temperature of individual elements, relative to the circuit temperature. If you do not specify DTEMP, simulation extracts TRISE from the model card. If you do specify DTEMP, it overrides TRISE in the model card.

General Syntax for SSIMSOI

```
Mxxx nd ng ns ne <np> mname <L=val> <W=val>
+ <M=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <BODYTYPE=val> <IGATE=val> <AB=val> <PB=val> <LXB=val>
+ <WXB=val> <LPE=val> <DTEMP=val>
```

Parameter	Description
Mxxx	SSIMSOI element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	SSIMSOI model name reference.
L	SSIMSOI channel length in meters. Default is 5.0 um.
W	SSIMSOI channel width in meters. Default is 5.0 um.
M	Multiplier to simulate multiple SSIMSOIs in parallel. Default=1.
AD	Drain diffusion area. Default=0.
AS	Source diffusion area. Default=0.
PD	Drain diffusion perimeter. Default=0.
PS	Source diffusion perimeter. Default=0.
BODYTYPE	Flag to choose floating(0) or Tgate(2). Default=0.
IGATE	Flag to turn on/off(0/1) gate current calculations. Default=1.
AB	Body diffusion area. Default = 0.
PB	Body diffusion perimeter (Body Contacted). Default = 0.
LXB	Extrinsic Gate Length (Body Contacted). Default = 0.
WXB	Extrinsic Gate Width (Body Contacted). Default = 0.

Parameter	Description
LPE	Flag to turn on/off lpe-related parasitics.
DTEMP	Increases the temperature.

Table 145 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

Name	Parameter	Units	Default
tox	Gate oxide thickness.	Angstrom	250
tbox	Back oxide thickness.	Angstrom	250
tsi	Silicon film thickness.	cm	0.2e-4
vth0	Linear region vth, reference (large) MOSFET, Vbs=0	v	0.8 (nmos) -0.8 (pmos)
tcv	Temperature coefficient of threshold voltage.	1/K	0
vfb	Reference (large) MOSFET flatband voltage	v	calc
tcvfb	Temperature coefficient of flatband voltage	1/K	
ng	Poly gate doping density	1/cm^3	
ngf	Gate oxide fixed charge density	1/cm^2	0
pbias	Length modifier (use with odif)	micron	0
dlivcv	Length modified for capacitance model	micron	0
odif	Outdiffusion of s/d under gate	micron	0
odifs	Outdiffusion of s under gate (asymmetric)	micron	oidf
abias	Width modifier	micron	0
lldd	Ldd spacer width	micron	0

Table 145 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage) (Continued)

Name	Parameter	Units	Default
lg2ct	Distance from contact to poly edge	micron	1.0
dbias	Diffusion resistor processing bias	micron	0
nfs	Fast surface state density	1/V-cm^2	0
n1	Surface region doping density	1/cm^3	5.0e16
n2	Bulk region doping density	1/cm^3	2.0e16
wbrk	Depth of surface region	micron	0.2
vfbll	Length dependence parameter of vth0		0
vfble	Exponent for length dependence of vth0		-1
vfbwl	Width dependence parameter of vth0		0
vfbwe	Exponent for width dependence of vth0		-1
dphii	Norm. error in phi at extro. Vth0		0
cs1ll	I-dependence parameter of n1		0
cs1le	Exponent for I-dependence of n1		-1
cs2ll	I-dependence parameter of n2		0
cs2le	Exponent for I-dependence of n2		-1
cs1wl	W-dependence parameter of n1		0
cs1we	Exponent for w-dependence of n1		-1
cs2wl	W-dependence parameter of n2		0
cs2we	Exponent for w-dependence of n2		-1
dibll	I-dependence parameter of dibl		0
dible	Exponent for I-dependence of dibl		-2

Table 145 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage) (Continued)

Name	Parameter	Units	Default
gp1	Bulk charge coefficient		1.744
gp2	Bulk charge coefficient	1/V	0.8364
shrink	Linear size reduction	%	0
shrink2	Modified areal size reduction	%	0

Table 146 SSIMSOI Model Intrinsic Parameters (Mobility and Saturation, Output Conductance)

Name	Parameter	Units	Default
ubref	Mobility parameter	cm^2/V-s	700 (nmos) 300 (pmos)
ubred	Mobility filed reduction factor	(cm/V)^egvexp	100
eavfac	Effective field coefficient		0.5
eavfwl	Width dependence of eavfac		0.0
eavfwe	Exponent of width dependence of eavfac		-2.0
eavexp	Exponent of mobility field function		1.0
ubvds	Drain dependence of eff. field		0.5
vsat	Channel carrier saturation velocity	cm/sec	1.0e-7
esat0	Vsat divisor, velocity field model		2
esat1	Divisor, carrier velocity at sat.		1
lc00	Mult. For channel length modulation		0.2
lc01	Length dependence of lc00	1/micron	0
lc1	Bias dependence of channel length modulation	1/V	0

Table 146 SSIMSOI Model Intrinsic Parameters (Mobility and Saturation, Output Conductance) (Continued)

Name	Parameter	Units	Default
wlmod	Mult. for channel width modulation		0
dv2	Par. for lin/sat transition region		0.05
dv3	Length dependence of dv2		0
exb	Temperature exponent of ubref		1.5

Table 147 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
aimp0	Impact ionization parameter		0
aimpl	Length dependence of aimp0	micron	0
aimpw	Width dependence of aimp0	micron	0
aimpt	Temperature dependence of aimp0	1/K	0
bimp0	Exponent for impact ionization	1/V	28.0
bimpl	Length dependence of bimp0	micron	0
bimp2	Width dependence of bimp0	micron	0
fsat1	Bias dependence of impact ionization	1/V	0
onkink	Voltage adjustment for onset of the kink	V	0
gtundeltox	Intrinsic region delta tox (electrical vs physical)	angstrom	(off)
gtundtoxovl	S/D overlap region delta tox (electrical vs physical)	angstrom	(off)
gtunstoxovl	S overlap region delta tox (asymmetric)	angstrom	gundtoxovl
gtunwdep	Accumulation 2-D fringing parameter	micron	0
gtunecbm	ECB effective mass		0.4

Table 147 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
gtunecba	ECB fitting parameter		0.6
gtunecbb	ECB barrier height	V	3.1
gtunecbbo	ECB barrier height	V	3.1
gtunhvbm	HWB effective mass		0.3
gtunhvba	HVB fitting parameter		1.0
gtunhvbb	HVB barrier height	V	4.5
gtunhvbbo	HVB barrier height	V	4.5
gtunevbeg	EVB energy bandgap	V	1.12
gtunevbm	EVB effective mass		0.32
gtunevba	EVB fitting parameter		0.4
gtunevbb	EVB barrier height	V	4.2
gtunevbbo	EVB barrier height	V	3.1
nbit	Effective doping parameter for I-bit		1.0
ndif	Effective doping parameter for Q-diffusion		1.0
cjch	S/D zero-bias junction channel-side capacitance	F/m	0.0
mich	S/D junction channel-side grading coefficient		0.5
pbch	S/D junction channel-side built-in pot.	V	0.8
tcppbch	S/D temperature coefficient for pbch	V/K	calculated
seff	S/D diode QNR recombination velocity	cm/s	1e5
seffl	I-dependence parameter for seff		0
seffle	Exponent for I-dependence for seff		0

Table 147 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
seffwl	W-dependence parameter for seff		0
seffwe	Exponent for w-dependence for seff		0
sefft	Temperature adjustment coefficient for seff		0
jro	S/D diode SCR recombination coef	A/cm^2	1e6
jroll	I-dependence parameter for jro		0
jrole	Exponent for I-dependence for jro		0
jrowl	W-dependence parameter for jro		0
jrowe	Exponent for w-dependence for jro		0
jrot	Temperature adjustment coefficient for jro		calculated
m	S/D diode recombination slope factor		2.0
jgo	S/D diode SCR generation coefficient	A/cm^2	0
jgoll	I-dependence parameter for jgo		0
jgole	Exponent for I-dependence for jgo		0
jgowl	Exponent for I-dependence for jgo		0
jgowe	Exponent for w-dependence for jgo		0
jgot	Temperature adjustment coefficient for jgo		0
mg	S/D diode generation slope factor		2.0
seffs	S diode QNR recombination velocity (asymmetrical)	cm/s	seff
seffsll	I-dependence parameter for seffs		seffll
seffsle	Exponent for dependence for seffs		seffle
seffswl	W-dependence parameter for seffs		seffwl

Table 147 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
seffswe	Exponent for w-dependence for seffs		seffwe
seffst	Temperature adjustment coefficient for seffs		sefft
jros	S diode SCT recombination coefficient (asymmetrical)	A/cm^2	jro
jrosll	I-dependence parameter for jro		jroll
jrosle	Exponent for I-dependence for jro		jrole
jroswl	W-dependence parameter for jro		jrowl
jroswe	Exponent for w-dependence for jro		jrowe
jrost	Temperature adjustment coefficient for jro		jrot
ms	S diode recombination slope factor (asymmetrical)		m
jgos	S diode SCR generation coefficient (asymmetrical)	A/cm^2	jgo
jgosll	I-dependence parameter for jgo		jgoll
jgosle	Exponent for I-dependence for jgo		jgole
jgoswl	W-dependence parameter for jgo		jgowl
jgoswe	Exponent for w-dependence for jgo		jgowe
jgost	Temperature adjustment coefficient for jgo		jgot
mgs	S diode generation slope factor		mg
gidla	GIDL pre-exponential parameter	A/m	(off)
gidlb	GIDL exponential parameter	m/V	3.0e9
gidlc	GIDL bulk-dependence parameter	V^3	8.0
gidle	GIDL bandgap	V	calculated
gidlt	GIDL temperature-dependence parameter		calculated

Table 147 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
gisla	GISL pre-exponential parameter	A/m	gidla
gislb	GISL exponential parameter	m/V	gidlb
gislc	GISL bulk-dependence parameter	V^3	gidlc
gisle	GISL bandgap	V	gidle
gislt	GISL temperature-dependence parameter		gidlt
rshmin	Sheet res. of s/d-gate overlap	ohm/sq	0
tcmin	Temperature coefficient for rshmin	1/K	0
rshmins	Sheet res. of s-gate overlap (asymmetrical)	ohm/sq	rshmin
tcmins	Temperature coefficient for rshims (asymmetrical)	1/K	tcmin
rshpls	Sheet res. of heavily doped S/D	ohm/sq	0
tcpls	Temperature coefficient for rshpls	1/K	0
rshbody	Sheet res. of intrinsic body	ohm/sq	3000
rshbodyext	Sheet res. of extrinsic body	ohm/sq	3000
tcbody	Temperature coefficient for rshbody and rshbodyext	1/K	0
cfr	Gate to S/D fringing capacitance	F/micron	0
cfrs	Gate to s-fringing capacitance (asymmetrical)	F/micron	cfr
foc	Bias dependence of overlap capacitance		1.0
voc	Bias dependence of overlap capacitance	V	0
cfrb	Gate to body overlap capacitance	F/micron	0
cfrbox	Back-gate to S/D fringing capacitance	F/micron	0
odifact	S/D active diffusion	micron	0

Table 147 SSIMSOI Model Parasitic Parameters (Continued)

Name	Parameter	Units	Default
odifbc	Body contact diffusion	micron	0
ccp	Contact-to-poly capacitance	F/micron	0
ccpr	Ccp error in RCE netlist	F/micron	0
ccc	Contact-to-contact capacitance	F/micron	0
cccr	Ccc error in RCE netlists	F/micron	0
ccx	Contact-to-soisub capacitance	F/micron	0
cpx	Poly-to-soisub capacitance	F/micron	0
wfr	Additional contact width	micron	0
nlev	Flicker noise equation level		0
kf	Flicker noise coefficient		0.0
af	Flicker noise exponent		1.0
cexp	Flicker noise cox exponent		1.0
fexp	Flicker noise frequency exponent		1.0

8

Customer Common Model Interface

Describes a Synopsys program interface you can use to add your own proprietary MOSFET models into the HSPICE or HSPICE RF simulator.

The Customer Common Model Interface (CMI) is a Synopsys program interface that you can use to add your own proprietary MOSFET models into the Synopsys HSPICE or HSPICE RF simulator.

HSPICE RF supports the external CMI, including the BTA-SOI model.

This chapter describes the following topics:

Overview of Customer CMI

HSPICE or HSPICE RF uses a dynamically-linked shared library to integrate models with the Customer CMI. Add the cmiflag global option to load the dynamically linked Customer CMI library (libCMImodel). Simulation searches for the libCMImodel shared library in the $hspice_lib_models path. If the simulator does not find the library, it searches in the $installdir/$ARCH/lib/ models directory.

Dynamic loading shares resources more efficiently than static binding does. If you run several simulations concurrently, HSPICE or HSPICE RF needs only one copy of the dynamically-linked Customer CMI model in memory, which speeds-up the process. Theoretically, the static-linking version is always slightly faster, if you run only one simulation at a time. However, the performance difference between dynamic loading and static binding is usually less than 5%.

The Customer CMI includes several source code examples, for integration of MOS, JFET, and MESFET models in simulation. They are standard Berkeley SPICE MOSFET models (LEVEL 1, 2, 3, BSIM1, 2, 3) and JFET/MESFET models. To minimize the effort required for adding models, Synopsys provides installation scripts, which automate the shared-library generation process.

If you derive your proprietary models from SPICE models, the integration process is similar to the examples, with minimal modifications.

Note: HSPICE or HSPICE RF includes equations and programs for bias calculation, numerical integration, convergence checking, and matrix loading. You do not need to use these programs to complete a new model integration so the source code examples do not include them.

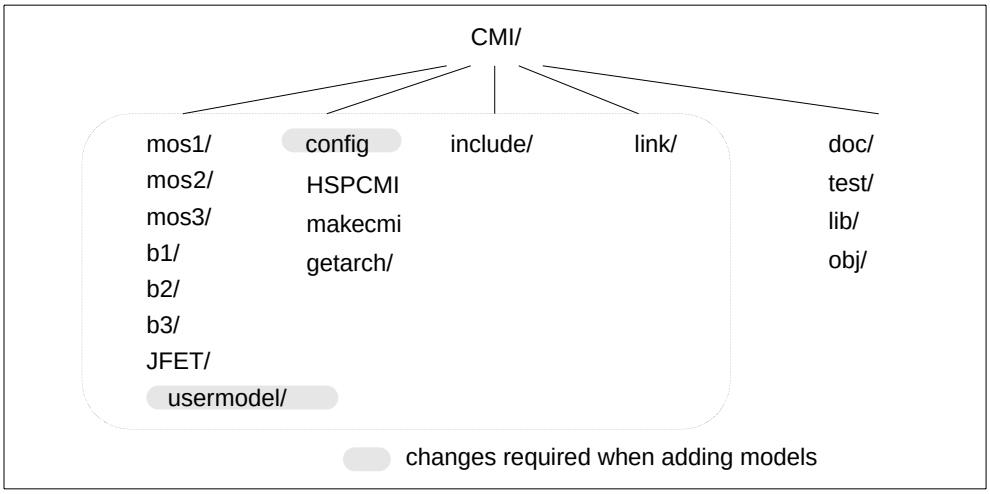
The Customer CMI supports the following platforms:

- Sun Solaris 2.5, 2.7, 2.8
- HP-UX 10.20, 11.0
- RedHat Linux6.2, Linux7.0, Linux7.1
- Windows2000, Windows NT, and Windows XP.

Directory Structure

Figure 40 shows the structure of the Customer CMI distribution for Unix (Sun and HP) and Linux platforms. Figure 41 on page 520 shows the structure of the Customer CMI distribution for the PC (Windows 95, Win98,Win2000, Windows NT, and Windows XP) platforms. You must modify the shaded files, or add new ones, for new models.

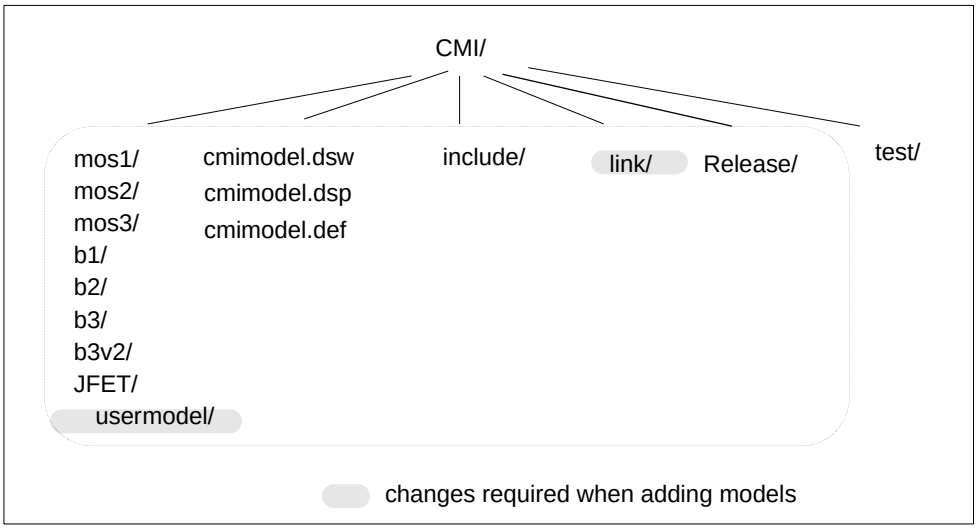
Figure 40 Customer CMI Directory Structure, Unix/Linux Platforms.



Directory	Description
HSPCMI	Subdirectory, containing the utility that processes the configuration files and the makefiles
get_arch	C shell script, for identifying platforms
config	Configuration file
doc	Customer CMI documentation
link	Main Customer CMI routines
include	Customer CMI header files
makecmi	Master makefile
test	Model testing example

Directory	Description
lib	Shared library directory
obj	Object code
mos1 mos2 mos3 b1 b2 b3 JFET	Model directories

Figure 41 Customer CMI Directory Structure, PC Platforms.



Directory	Description
cmimodel.dsw	Project workspace file
cmimodel.dsp	Project file
cmimodel.def	Definition file
include	Customer CMI header files

Directory	Description
link	Main Customer CMI routines
test	Model testing example
Release	Shared library directory
mos1 mos2 mos3 b1 b2 b3 b3v2 JFET	Model directories

Running Simulations Using Customer CMI Models

To specify Customer CMI models, use the *level* model parameter. Levels used in the example models are the same as in Berkeley Spice-3:

- LEVEL 1 (mos1/) LEVEL 1 MOS model
- LEVEL 2 (mos2/) LEVEL 2 MOS model
- LEVEL 3 (mos3/) LEVEL 3 MOS model
- LEVEL 4 (b1/) BSIM model
- LEVEL 5 (b2/) BSIM2 model
- LEVEL 8 (b3/) BSIM3v3 model
- LEVEL 9 (JFET) JFET & MESFET model

To simulate a Customer CMI model, add the following line in the input netlist:

.OPTION cmiflag

The LEVEL 8 example code (located in the *b3* directory) and the Level 49 MOSFET device model, are both based on BSIM3, version 3. However, the speed of LEVEL 8 is sometimes 20 percent slower than LEVEL 49 in the Synopsys MOSFET models. This occurs because LEVEL 49 is carefully implemented, to ensure high accuracy and performance. In contrast, LEVEL 8 in the example code is only an example of using the Customer CMI interface.

Therefore, the slower performance of the example code, compared to the MOSFET Level 49 model, is expected.

The Level 9 example code is located in the JFET directory, and is based on the JFET/MESFET Level 3 model (Statz model) and Spice3. This is example code, only for using the Customer CMI interface.

Adding Proprietary MOS Models

You can use the Customer CMI interface to enter proprietary models into HSPICE or HSPICE RF. This section describes how to use Customer CMI, to both add a new MOS model and simplify integration.

MOS Models on Unix Platforms

In the following examples, the percent sign (%) is the UNIX shell prompt, and $(installdir) points to the directory where you installed HSPICE or HSPICE RF. $ARCH is the OS type for the computer. The Customer CMI supports Sun4, Solaris, and HP platforms.

To create a Customer CMI shared library and add a new model:

1. Create a directory environment.
2. Modify the configuration file.
3. Prepare and modify the model routines.
4. Compile the shared library.
5. Set up the runtime shared-library path.

Creating the Directory Environment

To create the Customer CMI directory environment:

1. Copy the Customer CMI directory from the HSPICE or HSPICE RF release directory, to a new location, as shown in the following example:

   ```
   % cp -r $(installdir)/cmi   /home/user1/userx/model
   ```

   The new Customer CMI directory (/home/*user1*/*userx*/model/cmi) is your working directory. You must have read and write access to this directory.

2. Copy an existing model subdirectory to a new model directory.

3. Create a subdirectory for the new model under the working Customer CMI directory.

   For example, if your MOSFET model is LEVEL 222, copy the subdirectory from the existing MOS model LEVEL 3, as follows:

   ```
   %cp -r mos3 mos222
   ```

4. Add the following line in the *config* configuration file:

   ```
   mos222      222      "my own MOSFET model"
   ```

Table 148 Configuration File MOS Syntax

Parameter	Description
mos222	model name
222	model LEVEL
my own MOSFET model	descriptive comment for the model

The model name and level must be unique, within the configuration file. For more information, see the in-line comment in the configuration file.

Preparing Model Routine Files

In the new mos222 model subdirectory, rename *mos3* in all filenames to *mos222*. For example:

```
% mv CMImos3defs.h CMImos222defs.h
```

After you rename all files, the new model subdirectory should contain the following group of files:

- CMImos222defs.h
- CMImos222.c
- CMImos222GetIpar.c
- CMImos222SetIpar.c
- CMImos222GetMpar.c
- CMImos222SetMpar.c

- CMImos222eval.c
- CMImos222set.c
- CMImos222temp.c

For a detailed description of each routine, see Model Interface Routines on page 529. Modify the functions as necessary. To add a new model, most of the work required is modifying these files.

Compiling the Shared Library

1. Follow the steps in the preceding section, to modify the model routine files and the configuration file.
2. Manually set the HSPICE_CMI environment variable to the working Customer CMI directory (see Creating the Directory Environment on page 522):

   ```
   % setenv HSPICE_CMI /home/user1/userx/model/cmi
   ```

3. Use a single make operation, to compile both the model routines and the shared library.
4. To check the syntax of your C functions before you launch the compilation process, enter the following command:

   ```
   % make -f makecmi lint
   ```

   This command lists any syntax errors in your model routines.
5. To invoke the compilation process, enter the following:

   ```
   % make -f makecmi
   ```

   The simulator creates the new libCMImodel shared library in the lib/ subdirectory. It also generates all object files in the obj/ subdirectory.

Note: During compilation, Customer CMI creates files (makefile.SUN on SUN, makefile.HP on HP), and subdirectories (obj/ and lib/) in the Customer CMI working directory. Do not modify these generated files.

Choosing a Compiler

To use any functional compiler, set the CC environment variable to the location of the compiler (the auto-generated makefile, makefile.SUN or makefile.HP, uses CC). Set the appropriate compiler and link flags properly so the final

Customer CMI library build is in the position-independent code (PIC). Dynamic linking uses PIC.

For SUNOS 5.4 platforms or later, -KPIC (the automatically-generated compiler flag), and the -G -z link flag, are for the Sun workshop compiler (cc or acc). You typically install these compilers in a directory, such as /usr1/opt/SUNWspro/SC4.2/bin.

For HP9000/700 platforms, install cc in /opt/ansic/bin. For more information, type man cc or man acc, to display the on-line manual page for these commands.

You can use any optimization flags for the Customer CMI library. However, for best results, use the -fast flag for the cc or acc Sun compiler, and use the -O flag for the cc HP compiler.

Using the gcc Compiler If you use the gcc compiler, modify the makefile (makefile.SUN or makefile.HP) to set the compiler flags correctly.

For gcc, set the CC environment variable to gcc. Modify the makefile to use the -fPIC flag to compile, and the -r flag to link. For example:

```
gcc -c -I. ./include -fPIC CMImain.c ...
gcc -r -o ./lib/libCMImodel obj/*.o
```

Using the /usr/ucb/cc Compiler If you use the /usr/ucb/cc compiler, modify the makefile (makefile.SUN or makefile.HP) to set the compiler flags correctly.

The /usr/ucb/cc compiler cannot compile C source files, until you install the Language Optional Source Package. Verify that this source package is installed, then set the CC environment variable to /usr/ucb/cc.

Note: The Language Optional Source Package is not installed in Solaris by default, but it is installed in SUNOS 4.1.x by default. You must either install the optional language software, or use a workable compiler (such as cc or acc in the Sun workshop). You can also use the gcc compiler, with some minor modifications to the makefile.

Runtime Shared Library Path

The shared library is now ready to use. You must update the shared model search path (defined in the hspice_lib_models environment variable) so that the system dynamic loader can find the new Customer CMI shared library. Enter the following:

```
setenv hspice_lib_models $HSPICE_CMI/lib
```

Troubleshooting

Sometimes, even if you successfully build the Customer CMI dynamic library, HSPICE or HSPICE RF returns an error message when you run simulation:

```
**error**: Unable to load
/home/ant/lib/models/libCMImodel and /home/ant/lib/
   models/libCMImodel.so
```

If this problem occurs, it is usually because one or more symbols are undefined when you run the simulation.

Note: Different compilers usually generate nm output in different formats.

The following is an example output for undefined symbols, using the Sun workshop cc compiler on a SUNOS 5.5 machine.

```
nm libCMImodel | grep UNDEF
[  35]   |   0|   0|NOTY   |LOCL |0   |UNDEF   |
[  34]   |   0|   0|NOTY   |LOCL |0   |UNDEF   |
[1779]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |.mul
[1853]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |__dtou
[1810]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |__iob
[1822]   |   0|   0|NOTY   |WEAK |0   |UNDEF   |_ex_deregister
[1749]   |   0|   0|NOTY   |WEAK |0   |UNDEF   |_ex_register
[1857]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |atan
[1878]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |cos
[1820]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |exp
[1777]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |fabs
[1872]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |fprintf
[1764]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |log
[1767]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |malloc
[1842]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |memset
[1772]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |pow
[1869]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |sin
[1790]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |sqrt
[1758]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |strcasecmp
[1848]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |strcpy
[1858]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |strlen
[1800]   |   0|   0|NOTY   |GLOB |0   |UNDEF   |strncpy
```

To satisfy the above undefined symbols when you run simulation, use libraries such as libc or libm. However, any unsatisfied symbols (other than those shown in the example) can cause an “Unable to load” problem.

MOS Models on PC Platforms

To add proprietary MOS models on a PC platform, follow the steps below. These steps create a Dynamic Link Library.

1. Copy the Customer CMI directory from the HSPICE or HSPICE RF release directory, to a new location. For example:

```
D:/xcopy d:\synopsys\cmimodel project\cmimodel /e
```

2. Use Microsoft Visual C++ to open the cmimodel/cmimodel.dsw file.
3. In the cmimodel/project directory, create a new subdirectory named mos222.
4. To copy all files from the MOS LEVEL 3 model to the new mos222 subdirectory:

   ```
   D: project\cmimodel> xcopy mos3 mos222 /e
   ```

5. In the source files, globally replace mos3 with mos222.
6. In all file names, replace mos3 with mos222. For example:

   ```
   D: project\cmimodel rename CMImos3defs.h CMImos222defs.h
   ```

   After you rename all files, the new model subdirectory contains the following files:

   CMImos222defs.h
   CMImos222.c
   CMImos222GetIpar.c
   CMImos222SetIpar.c
   CMImos222GetMpar.c
   CMImos222SetMpar.c
   CMImos222eval.c
   CMImos222set.c
   CMImos222temp.c

7. Load all of the above files from the mos222 subdirectory into the project directory.

8. Add the following declaration to the cmimodel/link/CMImdlDec.h file:

   ```
   extern CMI_MOSDEF* pCMI_mos222def;
   ```

9. Add the following branch to the switch clause in the cmimodel/link/CMImdlLevel.h file:

   ```
   case222:
   pCMIDevice = (char *)pCMI_mos222def;
   break;
   ```

10. Rebuild the libCMImodel.dll file.
11. Put the dynamic link library into the same directory as the hspice.exe, hspicext.exe, or hspice_mt.exe executable.

Testing Customer CMI Models

To test a new model in the shared library, run a simulation on the mos3.sp input file in the test subdirectory. This file contains a simple CMOS inverter, using MOS LEVEL-3 models. Modify the transistor sizes and the model cards as necessary.

```
%hspice mos3.sp >mos3.lis
```

You can then use Avanwaves to inspect the I-V and C-V characteristics at different biasing conditions.

Use AvanWaves to carefully check the following aspects:

- Sign and value of the channel current (`ids`).
- Monotone characteristics of the channel current, versus `vgs` and `vds`.
- Sign and value of the capacitance (`cgs`, `cgs`, `cgb`, `csb`, `cdb`).

Refer to the *AvanWaves User Guide* for more information.

To verify the Customer CMI integration of your new model, run both a DC sweep analysis and a transient analysis on the test netlist.

Note: LEVELs from 100 to 200 are reserved for Customer CMI customer models. Choose levels from this range so your custom models do not conflict with existing Synopsys model levels. Also, add a special prefix or suffix for some of the auxiliary functions used in Customer CMI, especially those from the public domain (such as the `modchk` function, or `dc3p1` from Berkeley Spice3). This ensures that the function names are different from those used in the simulator's core code.

After testing, if you are satisfied with your Customer CMI library, put it in the default Customer CMI library directory ($installdir/$ARCH/lib/models). In this syntax, `$ARCH` can be `sun4`, `sol4`, or `pa`, depending on the platform you use to compile your Customer CMI library.

Model interface routines accept input parameters from Customer CMI. For each set of input conditions, the model routines must return the transistor characteristics to Customer CMI.

Model Interface Routines

Model interface routines accept the following input parameters from Customer CMI:

- Circuit and nominal model temperatures (`CKTtemp`, `CKTnomtemp`).
- Input biases (`vds`, `vgs`, `vbs`).
- Model parameters (`level`, `vto`, `tox`, `uo` ...).
- Instance parameters (`w`, `l`, `as`, `ad` ....).
- Mode of the transistor (mode: `1` for normal, `-1` for reverse).
- AC frequency (`freq` passes from the simulator to the model code).
- Integration order (`intorder`) for transient simulation. HSPICE or HSPICE RF returns the following codes:
  - `0` = Trapezoidal
  - `1` = 1st order Gear
  - `2` = 2nd order Gear
- Transient time step (`timestep`).
- Transient time point (`timepoint`).

For each set of input conditions, the model routines must return the following transistor characteristics to Customer CMI:

- Flag for computing the charge and capacitance (`1` for computation, `0` for no computation, `qflag`).
- Selector for the charge or capacitance model (`0` for Meyer capacitance model*, `13` for the capop charge-based model).
- Channel current (`ids`).
- Channel conductance (`gds`).

- Trans-conductance (gm).
- Substrate trans-conductance (gmbs).
- Turn-on voltage (von).
- Saturation voltage (vsat).
- Gate-overlap capacitances (cgso, cgdo, cgbo).
- Intrinsic MOSFET charges (qg, qd, qs).
- Intrinsic MOSFET capacitances, referenced to bulk (cggb, cgdb, cgsb, cbgb, cbdb, cbsb, cdgb, cddb, cdsb).
- Parasitic source and drain conductances (gs, gd).
- Substrate diode current (ibd, ibs).
- Substrate diode conductance (gbd, gbs).
- Substrate diode charge (qbd, qbs).
- Substrate diode junction capacitance (capbd, capbs).
- Substrate impact ionization current (isub).
- Substrate impact ionization trans-conductances (gbgs=dIsub/dVgs, gbds=dIsub/dVds, gbbs=dIsub/dVbs).
- Current for the source resistance noise, squared (nois_irs).
- Current for the drain resistance noise, squared (nois_ird).
- Current for the noise from the Thermal or Shot channel, squared (nois_idsth).
- Current for the source resistance noise, squared (nois_idsfl).

You cannot use Meyer capacitance models in HSPICE or HSPICE RF.

The CMI_VAR variable type (in the include/CMIdef.h file) transfers the transistor biases and the output characteristics, between the Customer CMI and the model interface routines.

The vds, vgs, and vbs entries provide bias conditions. The other entries carry the results from evaluating the model equations.

```
/* must be consistent with its counterpart in HSPICE */
typedef struct CMI_var {
/* device input formation */
int    mode;       /* device mode */
int    qflag;      /* flag for charge/cap computing */
double vds;        /* vds bias */
```

```
double vgs;        /* vgs bias */
double vbs;        /* vbs bias */
/* device DC information */
double gd;         /* drain conductance */
double gs;         /* source conductance */
double cgso;       /* gate-source overlap capacitance */
double cgdo;       /* gate-drain overlap capacitance */
double cgbo;       /* gate-bulk overlap capacitance */
double von;        /* turn-on voltage */
double vdsat;      /* saturation voltage */
double ids;        /* drain dc current */
double gds;        /* output conductance (dIds/dVds) */
double gm;         /* trans-conductance (dIds/dVgs) */
double gmbs;       /* substrate trans-conductance
(dIds/dVbs)        */
’   /* MOSFET capacitance model selection */
/* capop can have following values
* 13          charge model
* 0 or else   Meyer's model
```

Note: HSPICE or HSPICE RF does not support Meyer’s model.

```
int    capop;      /* capacitor selector */
/* Meyer's capacitances: intrinsic capacitance + overlap
capacitance. HSPICE or HSPICE RF ignores these 3 capacitances. A
charge-based model formulation is required. */
double capgs; /* Meyer's gate capacitance (dQg/dVgs + cgso) */
double capgd; /* Meyer's gate capacitance (dQg/dVds + cgdo) */
double capgb; /* Meyer's gate capacitance (dQg/dVbs + cgbo) */
/* substrate-junction information */
double ibs;   /* substrate source-junction leakage current */
double ibd;   /* substrate drain-junction leakage current */
double gbs;   /* substrate source-junction conductance */
double gbd;   /* substrate drain-junction conductance */
double capbs;   /* substrate source-junction capacitance */
double capbd;   /* substrate drain-junction capacitance */
double qbs;   /* substrate source-junction charge */
double qbd;   /* substrate drain-junction charge */
/* substrate impact ionization current */
double isub;   /* substrate current */
double gbgs;   /* substrate trans-conductance (dIsub/dVgs) */
double gbds;   /* substrate trans-conductance (dIsub/dVds) */
double gbbs;   /* substrate trans-conductance (dIsub/dVbs) */
/* charge-based model intrinsic terminal charges */
/* NOTE: these are intrinsic charges ONLY */
double qg;   /* gate charge */
double qd;   /* drain charge */
```

```
double qs;   /* source charge */
/* charge-based model intrinsic trans-capacitances*/
/* NOTE: these are intrinsic capacitances ONLY */
double cggb;
double cgdb;
double cgsb;
double cbgb;
double cbdb;
double cbsb;
double cdgb;
double cddb;
double cdsb;
/* noise parameters */
double nois_irs;   /* Source noise current^2 */
double nois_ird;   /* Drain noise current^2 */
double nois_idsth;   /* channel thermal/shot noise current^2 */
double nois_idsfl; /* 1/f channel noise current^2 *
double freq;   /* ac frequency */
/* extended model topology */
char *topovar;   /* topology variables */
double leff;   /* effective channel length */
double weff;   /* effective channel width */
} CMI_VAR;
```

The CMIenv global variable defines the nominal and device temperature. The pCMIenv (pointer to the global CMIenv structure) global variable accesses the CMIenv structure. The CMI_ENV type in the include/CMIdef.h file, defines the structure for CMIenv:

```
/* environment variables */
typedef struct CMI_env {
double CKTtemp;   /* simulation temperature */
double CKTnomTemp;   /* nominal temperature */
double CKTgmin;   /* GMIN for the circuit *
int    CKTtempGiven;   /* temp setting flag */
/* hspice-specific options follow */
double aspec;
double spice;
double scalm;
} CMI_ENV;
/* model parameters for JFET&MESFET */
/* JFET&MESFET model parameter for CMI_VAR in CMIdef.h */
double gg;   /* gate conductance */
double cigs;   /* gate-to-source current */
double gigs;   /* gate-to-source conductance */
double cigd;   /* gate-to-drain current */
double gigd;   /* gate-to-drain conductance */
double csat;   /* diode saturation current */
```

```
double capds;   /* drain-to-source capacitance */
double nois_irg;   /* Gate noise current^2 */
double qgso;   /* gate-to-source old charge */
double qgdo;   /* gate-to-drain old charge */
double qgs;   /* gate-to-source charge */
double qgd;   /* gate-to-drain charge */
double vgsold;   /* gate-to-source old voltage */
double vgdold;   /* gate-to-drain old voltage */
```

Interface Variables

To assign the model/instance parameter values, and to evaluate the I-V, C-V response, you need fifteen interface routines. For each new model, an interface variable (in the CMI_MOSDEF type) defines pointers to these routines, and to the model/instance variables. The include/CMIdef.h file includes this variable.

```
typedef struct CMI_MosDef {
char     ModelName[100];
char     InstanceName[100];
char     *pModel;
char     *pInstance;
int      modelSize;
int      instSize;
int      (*CMI_ResetModel)(char*,int,int);
int      (*CMI_ResetInstance)(char*);
int    (*CMI_AssignModelParm)(char*,char*,double);
int    (*CMI_AssignInstanceParm)(char*,char*,double);
int      (*CMI_SetupModel)(char*);
int      (*CMI_SetupInstance)(char*,char*);
int      (*CMI_Evaluate)(CMI_VAR*,char*,char*);
int      (*CMI_DiodeEval)(CMI_VAR*,char*,char*);
int      (*CMI_Noise)(CMI_VAR *,char*,char*);
int      (*CMI_PrintModel)(char*);
int      (*CMI_FreeModel)(char*);
int      (*CMI_FreeInstance)(char*,char*);
int      (*CMI_WriteError)(int, char*);
int      (*CMI_Start)(void);
int      (*CMI_Conclude)(void);
/* extended model topology,0 is normal mos, 1 is
   berkeley SOI, etc. */
int     topoid;
} CMI_MOSDEF;
```

All routines return 0 if they succeed, or a non-zero integer (an error code that you define) for a warning or error. The following sections describe each entry.

HSPICE or HSPICE RF extracts examples for the first seven functions, from the MOS3 implementation. Examples for the remaining eight functions are not part of the actual MOS3 code, but the code includes them for demonstration. The MOS3 implementation example contains one header file and eight C files. All routines are based on SPICE-3 code.

pModel, pInstance

When you compile, HSPICE or HSPICE RF initializes structures for an interface variable. For example:

```
/* function declaration */
int CMImos3ResetModel(char*,int,int);
int CMImos3ResetInstance(char*);
int CMImos3AssignMP(char*,char*,double);
int CMImos3AssignIP(char*,char*,double);
int CMImos3SetupModel(char*);
int CMImos3SetupInstance(char*,char*);
int CMImos3Evaluate(CMI_VAR*,char*,char*);
int CMImos3DiodeEval(CMI_VAR*,char*,char*);
int CMImos3Noise(CMI_VAR *,char*,char*);
int CMImos3PrintModel(char*);
int CMImos3FreeModel(char*);
int CMImos3FreeInstance(char*,char*);
int CMImos3WriteError(int, char*);
int CMImos3Start(void);
int CMImos3Conclude(void);
/* extended model topology, 0=normal mos, 1=berkeley SOI */
/* local */
static MOS3model    _Mos3Model;
static MOS3instance _Mos3Instance;
static CMI_MOSDEF CMI_mos3def = {
(char*)&_Mos3Model,
(char*)&_Mos3Instance,
CMImos3ResetModel,
CMImos3ResetInstance,
CMImos3AssignMP,
CMImos3AssignIP,
CMImos3SetupModel,
CMImos3SetupInstance,
CMImos3Evaluate,
CMImos3DiodeEval,
CMImos3Noise,
CMImos3PrintModel,
CMImos3FreeModel,
CMImos3FreeInstance,
```

```
CMImos3,
CMImos3Start,
CMImos3Conclude
};
/* export */
CMI_MOSDEF *pCMI_mos3def = &CMI_mos3def;
```

Note: The last 8 functions are optional. If you do not define a function, replace it with NULL.

CMI_ResetModel

This routine initializes all parameters of a model. After initialization, all model parameters become undefined in a netlist model card. The pmos flag sets the transistor type after initialization.

Syntax

`int CMI_ResetModel(char* pmodel, int pmos, int level)`

Parameter	Description
pmodel	Pointer to the model instance
pmos	1 if PMOS, or 0 if NMOS
level	Model level value, passed from the parser

Example

```
int
#ifdef __STDC__
   CMImos3ResetModel(
   char *pmodel,
   int   pmos)
#else
   CMImos3ResetModel(pmodel,pmos)
   char *pmodel;
   int   pmos;
#endif
   {
   /* reset all flags to undefined */
   (void)memset(pmodel, 0, sizeof(MOS3model));
```

```
/* Note: contains a model value passed from the parser */
   if(pmos)
   {
      ((MOS3model*)pmodel)->MOS3type = PMOS;
      ((MOS3model*)pmodel)->MOS3typeGiven = 1;
   }
   return 0;
   } /* int CMImos3ResetModel() */
```

CMI_ResetInstance

This routine initializes all parameter s in an instance. After initialization, all instance parameters become undefined in the netlist MOS instance.

Syntax

`int CMI_ResetInstance(char* pinst)`

In the preceding syntax, pinst points to the instance.

Example

```
int
#ifdef __STDC__
   CMImos3ResetInstance(
   char *ptran)
#else
   CMImos3ResetInstance(ptran)
   char *ptran;
#endif
   {
   (void)memset(ptran, 0, sizeof(MOS3instance));
   ((MOS3instance*)ptran)->MOS3w = 1.0e-4;
   ((MOS3instance*)ptran)->MOS3l = 1.0e-4;
   return 0;
   } /* int CMImos3ResetInstance() */
```

CMI_AssignModelParm

This routine sets the value of a model parameter.

Syntax

```
int CMI_AssignModelParm(char* pmodel, char* pname,double value)
```

Parameter	Description
pmodel	Pointer to the model instance.
pname	String of the parameter name. You cannot use character strings as parameter values in HSPICE RF.
value	Parameter value.

Example

```
int
#ifdef __STDC__
   CMImos3AssignMP(
   char   *pmodel,
   char   *pname,
   double value)
#else
   CMImos3AssignMP(pmodel,pname,value)
   char   *pmodel;
   char   *pname;
   double value;
#endif
   {
   int param;
   CMImos3GetMpar(pname, &param);
   CMImos3SetMpar(param, value, (MOS3model*)pmodel);
   return 0;
   } /* int CMImos3AssignMP() */
```

CMI_AssignInstanceParm

This routine sets the value of an instance parameter.

Syntax

```
int CMI_AssignInstanceParm(char *pinst,char* pname,double value)
```

Parameter	Description
pinst	Pointer to the instance.
pname	String of the parameter name. You cannot use character strings as parameter values in HSPICE RF.
value	Parameter value.

Example

```
int
#ifdef __STDC__
   CMImos3AssignIP(
   char   *ptran,
   char   *pname,
   double value)
#else
   CMImos3AssignIP(ptran,pname,value)
   char   *ptran;
   char   *pname;
   double value;
#endif
   {
   int param;
   CMImos3GetIpar(pname, &param);
   CMImos3SetIpar(param, value, (MOS3instance*)ptran);
   return 0;
   } /* int CMImos3AssignIP() */
```

CMI_SetupModel

After you specify all model parameters, where pmodel is a pointer to the model, this routine sets up a model.

Syntax

```
int CMI_SetupModel(char* pmodel)
```

In the preceding syntax, pmodel points to the model.

Example

```
int
#ifdef __STDC__
   CMImos3SetupModel(
   char *pmodel)
#else
   CMImos3SetupModel(pmodel)
   char *pmodel;
#endif
   {
   CMImos3setupModel((MOS3model*)pmodel);
   return 0;
   } /* int CMImos3SetupModel() */
```

CMI_SetupInstance

After you specify all instance parameters, this routine sets up an instance. HSPICE or HSPICE RF typically processes the temperature and the geometry.

Syntax

```
int CMI_SetupInstance(char* pinst)
```

In the preceding syntax, pinst points to the instance.

Example

```
int
#ifdef __STDC__
   CMImos3SetupInstance(
   char    *pmodel,
   char    *ptran)
#else
   CMImos3SetupInstance(pmodel,ptran)
   char    *pmodel;
   char    *ptran;
#endif
```

```
   {
   /* temperature modified parameters */
CMImos3temp((MOS3model*)pmodel,(MOS3instance*)ptran);
   return 0;
   } /* int CMImos3SetupInstance() */
```

CMI_Evaluate

Based on the bias conditions and the model/instance parameter values, this routine evaluates the model equations. It then passes all transistor characteristics via the CMI_VAR variable.

Syntax

```
int CMI_Evaluate(CMI_VAR *pvar,char *pmodel. char *pinst)
```

Parameter	Description
pvar	Pointer to the *CMI_VAR* variable
pmodel	Pointer to the model
pinst	Pointer to the instance

Example

```
int
#ifdef __STDC__
   CMImos3Evaluate(
   CMI_VAR   *pslot,
   char   *pmodel,
   char   *ptr)
#else
   CMImos3Evaluate(pslot,pmodel,ptr)
   CMI_VAR   *pslot;
   char   *pmodel;
   char   *ptr;
#endif
   {
   CMI_ENV   *penv;
   MOS3instance   *ptran;
   penv = pCMIenv;   /* pCMIenv is global */
   ptran = (MOS3instance*)ptr;
   /* call model evaluation */
```

```
(void)CMImos3evaluate(penv,(MOS3model*)pmodel,ptran,
pslot->vgs,pslot->vds,pslot->vbs);
pslot->gd      = ptran->MOS3drainConductance;
pslot->gs      = ptran->MOS3sourceConductance;
pslot->von      = ptran->MOS3von;
pslot->ids      = ptran->MOS3cd;
pslot->gds      = ptran->MOS3gds;
pslot->gm      = ptran->MOS3gm;
pslot->gmbs      = ptran->MOS3gmbs;
pslot->gbd      = ptran->MOS3gbd;
pslot->gbs      = ptran->MOS3gbs;
pslot->cgs      = ptran->MOS3capgs;
pslot->cgd      = ptran->MOS3capgd;
pslot->cgb      = ptran->MOS3capgb;
pslot->capdb      = ptran->MOS3capbd;
pslot->capsb      = ptran->MOS3capbs;
pslot->cbso      = ptran->MOS3cbs;
pslot->cbdo      = ptran->MOS3cbd;
...Assign additional CMI_VAR elements here, for the substrate
model and the overlap capacitances.
return 0;
} /* int CMImos3Evaluate() */
```

CMI_DiodeEval

Based on the bias conditions and the model/instance parameter values, this routine evaluates the MOS junction diode model equations. It then passes all transistor characteristics via the CMI_VAR variable.

Syntax

```
int CMI_DiodeEval(CMI_VAR *pvar,char *pmodel. char *pinst)
```

Parameter	Description
pvar	Pointer to the CMI_VAR variable
pmodel	Pointer to the model
pinst	Pointer to the instance

Example

```
int
#ifdef __STDC__
   CMImos3DiodeEval(
   CMI_VAR *pslot,
   char    *pmodel,
   char    *ptr)
#else
   CMImos3Diode(pslot,pmodel,ptr)
   CMI_VAR *pslot;
   char    *pmodel;
   char    *ptr;
#endif
   {
   CMI_ENV      *penv;
   MOS3instance *ptran;
   penv   = pCMIenv; /* pCMIenv is global */
   ptran   = (MOS3instance*)ptr; /* call model evaluation */
   (void)CMImos3diode(penv,(MOS3model*)pmodel,ptran,
   pslot->vgs,pslot->vds,pslot->vbs);
   pslot->ibs      = ptran->MOS3ibs;
   pslot->ibd      = ptran->MOS3ibd;
   pslot->gbs      = ptran->MOS3gbs;
   pslot->gbd      = ptran->MOS3gbd;
   pslot->capbs      = ptran->MOS3capbs;
   pslot->capbd      = ptran->MOS3capbd;
   pslot->qbs      = ptran->MOS3qbs;
   pslot->qdb      = ptran->MOS3qbd;
return 0;
   } /* int CMImos3DiodeEval() */
```

CMI_Noise

Based on the bias conditions, temperature, and model/instance parameter values, this routine evaluates the noise model equations. It then returns the noise characteristics via the `CMI_VAR` variable.

HSPICE or HSPICE RF passes values to:

- `pslot->nois_irs`. Thermal noise associated with the parasitic source resistance, expressed as a mean square noise current (in parallel with `Rs`).
- `pslot->nois_ird`. Thermal noise associated with the parasitic drain resistance, expressed as a mean square noise current (in parallel with `Rd`).

- `pslot->nois_idsth`. Thermal noise associated with a MOSFET, expressed as a mean square noise current, referenced across the MOSFET channel.
- `pslot->nois_idsfl`. Flicker noise associated with a MOSFET, expressed as a mean square noise current, referenced across the MOSFET channel.

HSPICE or HSPICE RF also passes the frequency into `CMI_Noise()` via `pslot->freq`.

Syntax

`int CMI_Noise(CMI_VAR *`*`pvar`*`,char *`*`pmodel`*`. char *`*`pinst`*`)`

Parameter	Description
pvar	Pointer to the *CMI_VAR* variable
pmodel	Pointer to the model
pinst	Pointer to the instance

Example

```
int
#ifdef __STDC__
   CMImos3Noise(
   CMI_VAR *pslot,
   char    *pmodel,
   char    *ptr)
#else
   CMImos3Noise(pslot,pmodel,ptr)
   CMI_VAR *pslot;
   char    *pmodel;
   char    *ptr;
#endif
   {double freq,fourkt;
   CMI_ENV      *penv
MOS3instance *ptran;
   penv   = pCMIenv; /* pCMIenv is a global */
   ptran   = (MOS3instance*)ptr;
   fourkt   = 4.0 * BOLTZMAN * ptran->temp; /* 4kT */
   freq   = pslot->freq;
/* Drain resistor thermal noise as current^2 source*/
pslot->nois_ird = fourkt * ptran->gdpr;
```

```
/* Source resistor thermal noise as current^2 source */
pslot->nois_irs = fourkt * ptran->gspr;
/* Assumes that the thermal noise is the current^2 source
   referenced to the channel. The source code for
   the thermalnoise() is not shown here*/
pslot->nois_idsth = thermalnoise(model, here, fourkt);
/* Assumes that the flicker (1/f) noise is the current^2
   source referenced to the channel. The source code for
   the flickernoise() is not shown here */
pslot->nois_idsfl = flickernoise(model, here, freq);
return 0;
} /* int CMImos3Noise() */
```

CMI_PrintModel

This routine prints all model parameter names, values, and units to the standard output. HSPICE or HSPICE RF calls this routine for each model after the `CMI_SetupModel`, where pmodel points to the model.

Syntax

`int CMI_PrintModel(char *`*`pmodel`*`)`

Example

```
int
#ifdef __STDC__
   CMImos3PrintModel(
   char   *pmodel)
#else
   CMImos3PrintModel(pmodel)
   char   *pmodel;
#endif
   {
   CMI_ENV   *penv
/* Note: The source for CMImos3printmodel() is not shown*/
   (void)CMImos3printmodel((MOS3model*)pmodel);
   return 0;
   } /* int CMImos3PrintModel() */
```

CMI_FreeModel

This routine frees memory that HSPICE or HSPICE RF previously allocated for model-related data. After simulation, HSPICE or HSPICE RF calls this routine during a loop over all models.

Syntax

`int CMI_FreeModel(char *pmodel)`

In the preceding syntax, `pmodel` points to the model.

Example

```
int
#ifdef __STDC__
   CMImos3FreeModel(
   char    *pmodel)
#else
   CMImos3FreeModel(pmodel)
   char    *pmodel;
#endif
   { /* free memory allocated for model data. Note
   CMImos3freemodel() source code not shown. */
(void)CMImos3freemodel((MOS3model*)pmodel);
   return 0;
   } /* int CMImos3FreeModel() */
```

CMI_FreeInstance

This routine frees memory that HSPICE or HSPICE RF previously allocated to store instance-related data. After simulation, HSPICE or HSPICE RF calls this routine during both an outer loop over all models, and an inner loop over all instances that are associated with each model.

Syntax

`int CMI_FreeInstance(char *pmodel. char *pinst)`

Parameter	Description
pmodel	Pointer to the model
pinst	Pointer to the instance

Example

```
int
#ifdef __STDC__
   CMImos3FreeInstance(
   char   *pmodel,
   char   *ptr)
#else
   CMImos3FreeInstance(pmodel,ptr)
   char   *pmodel;
   char   *ptr;
#endif
   {
   CMI_ENV   *penv
   MOS3instance   *ptran;
   ptran = (MOS3instance*)ptr;
/* free memory allocated for the model data. The
CMImos3freeinstance()source code is not shown.
*/
(void)CMImos3freeinstance((MOS3model*)pmodel,ptran);
   return 0;
   } /* int CMImos3FreeInstance() */
```

CMI_WriteError

If model evaluation detects an error, then this routine writes error messages that you define, to standard output. You define these error messages. All Customer CMI functions return an error code and pass it to `CMI_WriteError()`.

- In `CMI_WriteError()`, you define an error statement and copy it to `err_str` (based on the error code value).
- `CMI_WriteError()` returns the error status:
  - If `err_status>0`, then HSPICE or HSPICE RF issues an error and aborts.
  - If `err_status=0`, then HSPICE or HSPICE RF issues a warning and continues.

HSPICE calls `CMI_WriteError()` after every Customer CMI function call.

Syntax

```
int CMI_WriteError(int err_code, char *err_str)
```

Parameter	Description
err_code	Error code
err_str	Points to the error message

Example

```
int
#ifdef __STDC__
   CMImos3WriteError(
   void err_code,
   char *err_str)
#else
   CMImos3WriteError(err_code,err_str)
   int err_code;
   char *err_str;
#endif
   {
/* */
int err_status=0;
switch err_code
   {
case 1:
   strcpyn(err_str,”User Err: Eval()”,CMI_ERR_STR_LEN);
   err_status=1;
case 2:
   strcpyn(err_str,”User Warn: Eval()”,CMI_ERR_STR_LEN);
   err_status=1;
default:
   strcpyn(err_str,”User Err:Generic”,CMI_ERR_STR_LEN);
   err_status=1;
return err_status;
   } /* int CMImos3WriteError() */
```

CMI_Start

Before simulation, this routine runs startup functions that you define.

Syntax

```
int CMI_Start(void)
```

Example

```
int
#ifdef __STDC__
   CMImos3Start(void)
#else
   CMImos3Start(void)
#endif
   {
(void)CMImos3start();
   return 0;
   } /* int CMImos3Start() */
```

CMI_Conclude

After simulation, this routine runs the conclude functions that you define.

Syntax

```
int CMI_Conclude(void)
```

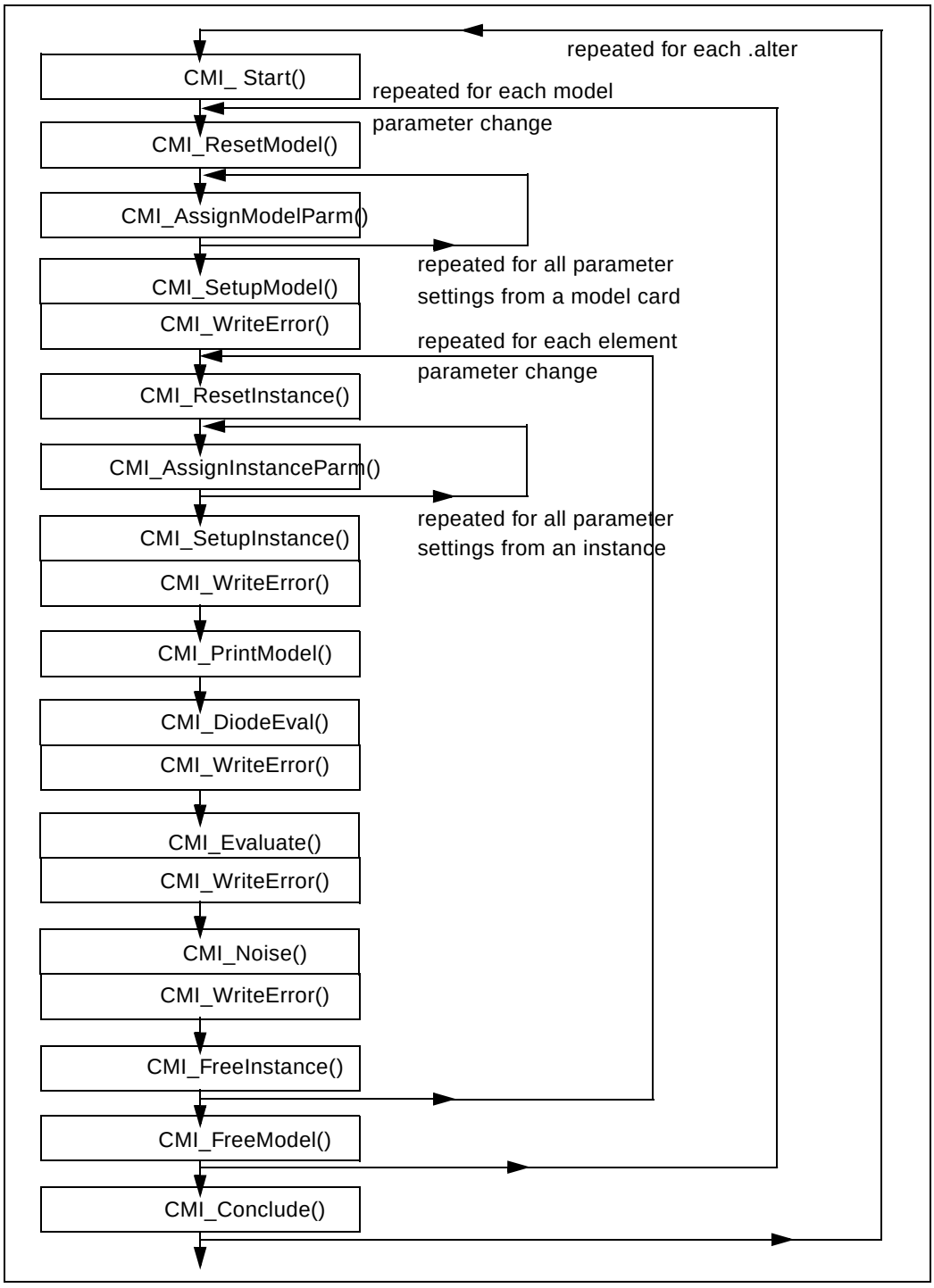
Example

```
int
#ifdef __STDC__
   CMImos3Conclude(void)
#else
   CMImos3Conclude(void)
#endif
   {
(void)CMImos3conclude();
   return 0;
   } /* int CMImos3Conclude() */Internal Routines */
```

Customer CMI Function Calling Protocol

Figure 42 illustrates the calling sequence for the interface routines.

Figure 42 Calling Sequence for the Interface Routines



Internal Routines

In the MOS3 implementation example, the interface routines in CMImos3.c also call the internal routines in Table 149:

Table 149 Common Model Interface Internal Routines

Routine	Description
CMImos3GetIpar.c	Get instance parameter index
CMImos3SetIpar.c	Set instance parameter
CMImos3GetMpar.c	Get model parameter index
CMImos3SetMpar.c	Set model parameter
CMImos3eval.c	Evaluate model equations
CMImos3set.c	Setup a model
CMImos3temp.c	Setup an instance, including the temperature effect

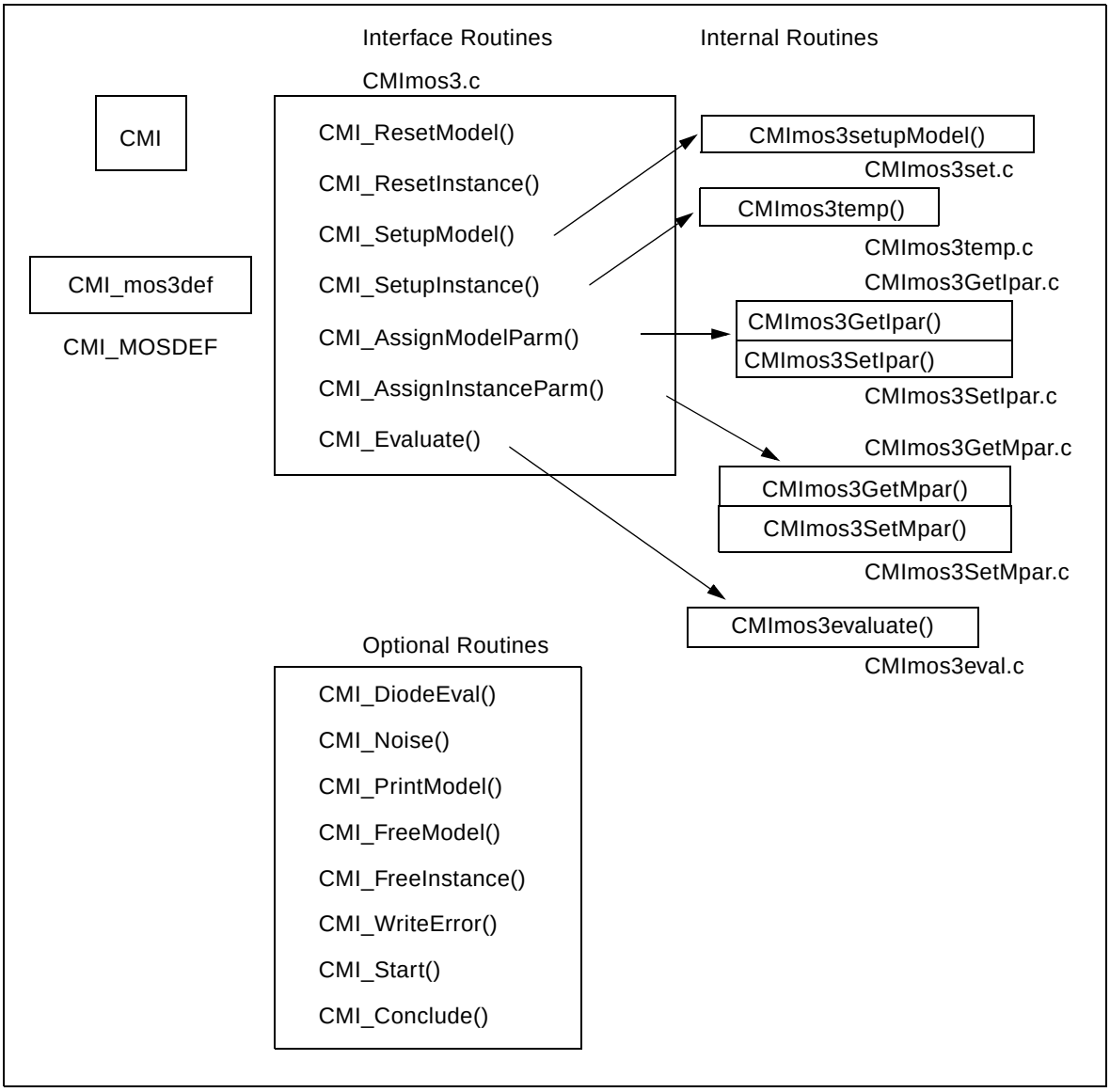
Figure 43 shows the hierarchical relationship between the interface routines and the internal routines.

For the automatic script to work, the name of the interface variable (and all routine files) must follow this naming convention:

pCMI_xxxdef
CMIxxx.c CMIxxxGetIpar.c
CMIxxxSetIpar.c CMIxxxGetMpar.c
CMIxxxSetMpar.c CMIxxxeval.c

In the preceding syntax, *xxx* is the model name.

Figure 43 Hierarchy of Interface and Internal Routines



Extended Topology

In addition to conventional four terminal (`topoid = 0`) MOSFET topology, HSPICE or HSPICE RF can support other topologies. You must assign a unique topoid for each topology.

To implement BSIM SOI topology, Customer CMI assigns `topoid=1`.

- If you create your own model named “topovar”, and it is the same as the BSIM SOI model, you can specify `topoid=1`, and use the HSPICE topology structure for stamping information.
- If your model topology is different from either the conventional 4-terminal model or the BSIM SOI, then you must specify the topovar structure. HSPICE or HSPICE RF assigns a unique topoid for your topology.

The naming convention for the structure fields is the same as in the BSIM SOI model. For detailed information about fields in the structure, see the *BSIM3PD2.0 MOSFET MODEL User Manual* at:

`http://www-device.eecs.berkeley.edu/~bsim3soi`

For example, the following is the topovar structure for the BSIM SOI model in the Customer CMI.

```
struct TOPO1 {
   double vps;
   double ves;
   double delTemp;      /* T node */
   double selfheat;
   double qsub;
   double qth;
   double cbodcon;
   double gbps;
   double gbpr;
   double gcde;
   double gcse;
   double gjdg;
   double gjdd;
   double gjdb;
   double gjdT;
   double gjsg;
   double gjsd;
   double gjsb;
   double gjsT;
   double cdeb;
   double cbeb;
   double ceeb;
```

```
   double cgeo;

/* add 4 for T */
   double cgT;
   double cdT;
   double cbT;
   double ceT;
   double rth;
   double cth;
   double gmT;
   double gbT;
   double gbpT;
   double gTtg;
   double gTtd;
   double gTtb;
   double gTtt;
};
```

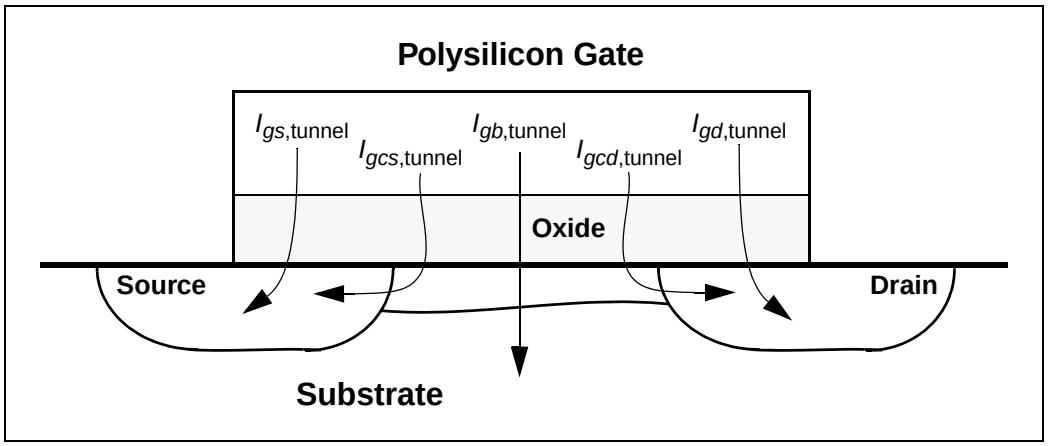
Enhancemnets for Customer CMI

This section describes several modeling capabilities for Customer CMI, which covers gate direct tunneling current modeling, additional instance parameter support as well as so called Generalized Customer CMI with BSIM4-like topology .

Gate Direct Tunneling Current

Gate direct tunneling currents, as shown in Figure 44, are supported in the Customer CMI. The tunneling process takes place in the thin gate oxide MOSFETs. The current magnitudes become increasingly more significant as the oxide thickness scales down rapidly. The HSPICE Customer CMI (MOSFET) topology meets such modeling requirements.

Figure 44 Gate Tunneling Current Components



In this figure,

- $I_{gd,tunnel}$ ($I_{gs,tunnel}$) is the tunneling current between gate and drain (source) through overlaps
- $I_{gcd,tunnel}$ ($I_{gcs,tunnel}$) represents the tunneling current from gate to channel and then to drain (source)
- $I_{gb,tunnel}$ is the tunneling current component that takes place between gate and bulk.

Generalized Customer CMI modeling capability assumes that the above current components each have bias dependence similar to those in BSIM4:

- $I_{gd,tunnel}$ depends only on vgd
- $I_{gs,tunnel}$ depends only on vgs
- $I_{gcd,tunnel}$, $I_{gcs,tunnel}$, and $I_{gb,tunnel}$ can be a function in vds, vgs, or vbs.

You can use the Customer CMI option custcmi for backward compatibility. To activate gate tunneling current modeling, include an `.OPTIONS custcmi=1` statement in the netlist. To turn off gate tunneling current modeling, include an `.OPTIONS custcmi=0` statement in the netlist.

The following is the list of variables being added into headfile CMIdef.h to support gate direct tunneling current modeling.

```
double Igbmod; /* flag to control gate-to-bulk tunneling current,
   IGBMOD=1 for ON and 0 for OFF */
double Igcmod; /* flag to control gate-to-drain and gate-to-source
   currents, IGCMOD=1 for ON and 0 for OFF */
double Igso; /* gate-to-source tunneling current through G-S
```

```
   overlap */
double Igdo; /* gate-to-drain tunneling current through G-D
   overlap */
double Igb; /* gate-to-bulk tunneling current */
double Igcs; /* gate-to-source tunneling current through channel */
double Igcd; /* gate-to-drain tunneling current through channel */
double gigsos; /* Igso-transconductance (dIgso/dVs = - dIgso/dVg) */
double gigsog; /* Igso-transconductance (dIgso/dVg) */
double gigcsg; /* Igcs-transconductance (dIgcs/dVg) */
double gigcsd; /* Igcs-transconductance (dIgcs/dVd) */
double gigcsb; /* Igcs-transconductance (dIgcs/dVb) */
double gigcss; /* Igcs-transconductance (dIgcs/dVs = - (dIgcs/dVg
   + dIgcs/dVd + dIgcs/dVb)) */
double gigdod; /* Igdo-transconductance (dIgdo/dVd = - dIgdo/dVg) */
double gigdog; /* Igdo-transconductance (dIgdo/dVg) */
double gigcdg; /* Igcd-transconductance (dIgcd/dVg) */
double gigcdd; /* Igcd-transconductance (dIgcd/dVd) */
double gigcdb; /* Igcd-transconductance (dIgcd/dVb) */
double gigcds; /* Igcd-transconductance (dIgcd/dVs = - (dIgcd/dVg
   + dIgcd/dVd +dIgcd/dVb)) */
double gigbg; /* Igb-transconductance (dIgb/dVg) */
double gigbd; /* Igb-transconductance (dIgb/dVd) */
double gigbb; /* Igb-transconductance (dIgb/dVb) */
double gigbs; /* Igb-transconductance (dIgb/dVs = - (dIgb/dVg
   + dIgb/dVd + dIgb/dVb)) */
```

Refer to /extcmi/enhancements/DE52897 for testcode and testcases.

Additional Instance Parameter support

Customer CMI supports the following instance parameter namings (to activate this, use `.OPTION CUSTCMI=1`):

- Existing HSPICE BSIM4-like instance parameters—

acnqsmod	delk1	delnfct	deltox	geomod	min
mulu0	nf	rbdb	rbodymod,	rbpb	rbpd
rbps	rbsb	rgatemod	sa	sa1	sa10
sa2	sa3	sa4	sa5	sa6	sa7
sa8	sa9	sb	sb1	sb10	sb2
sb3	sb4	sb5	sb6	sb7	sb8

sb9	sd	stimod	sw1	sw10	sw2
sw3	sw4	sw5	sw6	sw7	sw8
sw9	trnqsmod				

Among these instance parameters, `trnqsmod`, `acnqsmod`, `rbodymod`, `rgatemod`, `geomod`, and `stimod` are type integer.

- Six instance model flags of integer type with the following fixed names: `insflg1`, `insflg2`, `insflg3`, `insflg4`, `insflg5`, and `insflg6`
- Ten instance parameters of double type with the following fixed names: `insprm1`, `insprm2`, `insprm3`, ..., `insprm10`
- The syntax and namings look like this

```
m1 d g s b ...
+ <geomod=val> <nf=val> ...
+ <insflg1=val>  <insflg2=val> <insflg3=val>  ...
+ <insprm1=val>  <insprm2=val>  <insprm3=val>  ...
```

Refer to /extcmi/enhancements/STARTKS0078251 for testcode and testcases.

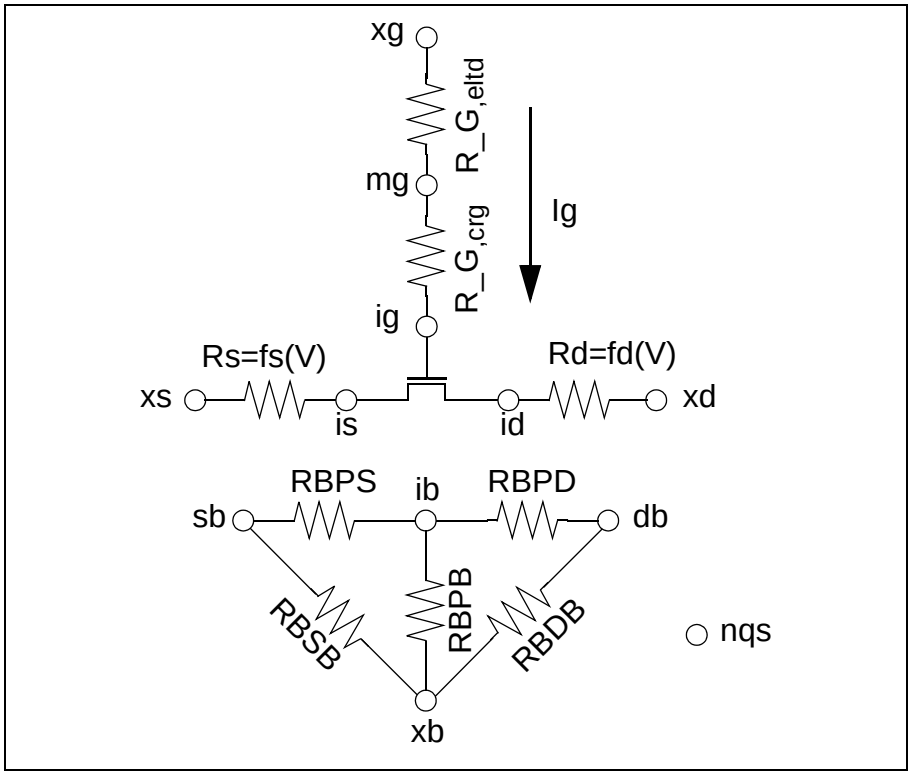
An Extension to Support BSIM4 Topology

HSPICE provides device modeling capability for MOSFET models with BSIM4 topology through a Generalized Customer CMI. To use this capability, add the `cmiflag` option to the netlist to load the dynamically-linked CMI library.

The topology ID number 101 is assigned internally for MOSFET models developed through this Generalized Customer CMI. This differs from the existing Customer CMI, which uses topology ID number 0. Therefore, you must assign the topology ID number `topoid` to `101` in the `CMI_MOSDEF` structure located in your CMI###.c file (where ### is the model name).

To better understand BSIM4 topology, Figure 45 illustrates that with settings of `RGATEMOD=3`, `RBODYMOD=1`, and `TRNQSMOD=1`, virtually every circuit can be modeled.

Figure 45 High-level Equivalent Circuits for BSIM4 Model



In this figure,

- RBPB, RBPD, RBPS, RBDB, and RBSB constitute the substrate resistance network
- $R\_G_{,eltd}$ is gate electrode resistance
- $R\_G_{,crg}$ is channel reflected gate resistance
- Rd (Rs) consists of both electrode diffusion drain (source) resistance and drain (source) bias dependent resistance LDD
- gate nodes are xg (external), mg (middle), and ig (internal)
- drain nodes are xd (external) and id (internal)
- source nodes are xs (external) and is (internal)
- bulk nodes are xb (external), ib (internal), db (internal at the drain side), and sb (internal at the source side)
- nqs is a non-quasi-static model node for modeling all intrinsic and extrinsic effects found in ultra small MOSFETs.

In addition to the gate current components in CMI_VAR of CMIdef.h, a pre-determined header file named topo101.h is provided (located in the /extcmi/mos101 directory), in which a data structure TOPO101 has been defined. This structure is accessible through a topovar pointer in CMI_VAR of the CMIdef.h file. In addition to those existing in Customer CMI data structure CMI_VAR, the other necessary calculated quantities such as

- current, charge
- conductance or transconductance
- capacitance of transcapacitance
- noise
- biases
- derivatives of bias dependent source and drain conductance

are passed to the HSPICE engine using TOPO101. Remember that header file topo101.h is shared internally in HSPICE so you must not modify it.

Additional member variables introduced in TOPO101 of topo101.h (see Figure 44 for node reference) are listed as follows:

```
double bsim4_ver; /* BSIM4 version number, up to 4.50 compatible */
double mult; /* instance multiplier (M factor) - to handle template
   output only */
double vges; /* eletrical external gate to internal source bias
   (vges=v(xg)-v(is)) */
double vgms; /* eletrical internal mid gate to source bias
   (vgms=v(mg)-v(is)) */
double vdbs; /* eletrical body nody at the drain side to source
   bias (vdbs=v(db)-v(is)) */
double vsbs; /* eletrical body nody at the source side to source
   bias (vsbs=v(sb)-v(is)) */
double vdes; /* electrical external drain to source bias
   (vdes=v(xd)-v(is)) */
double vses; /* electrical external source to source bias
   (vses=v(xs)-v(is)) */
double qdef; /* internal NQS "bias" (qdef=v(nqs)) */
double gstoto; /* electrical source conductance */
double gstotod; /* dgstoto/dvd * vses */
double gstotog; /* dgstoto/dvg * vses */
double gstotob; /* dgstoto/dvb * vses */
double gstotos; /* - (gstotod + gstotog + gstotob) */
double gdtoto; /* electrical drain conductance */
double gdtotod /* dgdtoto/dvd * (vdes - vds) */
```

```
double gdtotog; /* dgdtoto/dvg * (vdes - vds) */
double gdtotob; /* dgdtoto/dvb * (vdes - vds) */
double gdtotos; /* - (gdtotod + gdtotog + gdtotob) */
double Igidlo; /* electrical GIDL current */
double ggidlob; /* dIgidlo/dvb */
double ggidlog; /* dIgidlo/dvg */
double ggidlod; /* dIgidlo/dvd */
double Igislo; /* electrical GISL current */
double ggislob; /* dIgislo/dvb */
double ggislog; /* dIgislo/dvg */
double ggislos; /* dIgislo/dvs */
double gcrgo; /* channel-reflected gate conductance */
double gcrgod; /* dgcrgo/dVd */
double gcrgog; /* dgcrgo/dVg */
double gcrgob; /* dgcrgo/dVb */
double gcrgos; /* dgcrgo/dVs = - (dgcrgo/dVd + dgcrgo/dVg +
   dgcrgo/dVb) */
double xparto; /* charge partition flag - used for NQS modeling */
double gtau; /* NQS term to model finite channel time constant */
double grgeltd; /* gate electrode conductance */
double CoxWL; /* gate oxide capacitance for NQS */
double grbpd; /* conductance between ib and db */
double grbdb; /* conductance between xb and db */
double grbpb; /* conductance between ib and xb */
double grbps; /* conductance between ib and sb */
double grbsb; /* conductance between xb and sb */
double rgatemod; /* flag to control gate resistance model,
   rgatemod=0, 1, 2, 3 */
double rbodymod; /* flag to control substrate resistance model,
   rbodymod=0, 1, 2 */
double rdsmod; /* flag to control the use of source-drain resistance
   model, rdsmod=0 (internal), 1 (external) */
double rgeomod; /* flag to control the type of contacts */
double tnoimod; /* flag to select thermal noise model,
   tnoimod=0, 1 */
double trnqsmod; /* flag to select NQS model for transient
   analysis */
double acnqsmod; /* flag to select NQS model for AC analysis */
double qgmid; /* mid gate charge for rgatemod=3 */
double qcheq; /* channel charge under quasi-static */
double qcdump; /* channel charge deficit/surplus */
double cqdb; /* transcapacitance dqcheq/dVd */
double cqgb; /* transcapacitance dqcheq/dVg */
double cqsb; /* transcapacitance dqcheq/dVs */
double cqbb; /* transcapacitance dqcheq/dVb = - (cqdb + cqgb +
```

```
   cqsb) */
double nois_irg; /* thermal noise contributed by gate electrode
   resistance current^2 */
double nois_irbps; /* thermal noise contributed by resistance
   between ib and sb current^2 */
double nois_irbpd; /* thermal noise contributed by resistance
   between ib and db current^2 */
double nois_irbpb; /* thermal noise contributed by resistance
   between ib and xb current^2 */
double nois_irbsb; /* thermal noise contributed by resistance
   between xb and sb current^2 */
double nois_irbdb; /* thermal noise contributed by resistance
   between xb and db current^2 */
double nois_igs; /* shot noise associated with (Igso + Igcs)
   current^2 */
double nois_igd; /* shot noise associated with (Igdo + Igcd)
   current^2 */
double nois_igb; /* shot noise associated with Igb current^2 */
/* for circiut element summary */
double cdsat; /* drain-to-bulk saturation current */
double cssat; /* source-to-bulk saturation current */
double capbd; /* zero-biased junction capacitance on the drain side */
double capbs; /* zero-biased junction capacitcance on the source side */
double nf; /* number of device figures */
double min; /* flag to determine the number of drain or source diffusions
for even-number fingered device */
double rbpd; /* resistance between ib and db */
double rbdb; /* resistance between xb and db */
double rbpb; /* resistance between ib and xb */
double rbps; /* resistance between ib and sb */
double rbsb; /* resistance between xb and db */
double geomod; /* geometry-dependent parasitics model selector */
double delvto; /* zero-bias threshold voltage shift */
double mulu0; /* low-field mobility multipler */
double delk1; /* first-order body bias coefficient shift */
double delnfct; /* subthreshold swing factor shift */

/* for template output */
double templt1; /* output template #1 */
double templt2; /* output template #2 */
double templt3; /* output template #3 */
double templt4; /* output template #4 */
double templt5; /* output template #5 */
double templt6; /* output template #6 */
double templt7; /* output template #7 */
```

```
double templt8; /* output template #8 */
double templt9; /* output template #9 */
double templt10; /* output template #10 */
double templt11; /* output template #11 */
double templt12; /* output template #12 */
double templt13; /* output template #13 */
double templt14; /* output template #14 */
double templt15; /* output template #15 */
double templt16; /* output template #16 */
double templt17; /* output template #17 */
double templt18; /* output template #18 */
double templt19; /* output template #19 */
double templt20; /* output template #20 */
double templt21; /* output template #21 */
double templt22; /* output template #22 */
double templt23; /* output template #23 */
double templt24; /* output template #24 */
double templt25; /* output template #25 */
double templt26; /* output template #26 */
double templt27; /* output template #27 */
double templt28; /* output template #28 */
double templt29; /* output template #29 */
double templt30; /* output template #30 */
double templt31; /* output template #31 */
double templt32; /* output template #32 */
double templt33; /* output template #33 */
double templt34; /* output template #34 */
double templt35; /* output template #35 */
double templt36; /* output template #36 */
double templt37; /* output template #37 */
double templt38; /* output template #38 */
double templt39; /* output template #39 */
double templt40; /* output template #40 */
```

Among the above member variables: `vges`, `vgms`, `vdbs`, `vdes`, `vses`, and `qdef` are biases passed in from the HSPICE engine. While all the other components should be calculated through `CMI_Evaluate()` and `CMI_Noise()` routines, among which there are circuit element summary components (from `cdsat` to `delnfct` in the above list) and components for template output (from `templt1` to `templt40` in the above list). Taking gate tunneling current modeling as an example, and assuming that `LEVEL = 101` is to be used (for example, as in the example code in /extcmi/mos101), model evaluations are carried out within the function CMImos101evaluate(), and the

results (here I and G) are transferred to the HSPICE engine by the gate current related variables using the following pointers:

```
pslot->Igbmod = (MOS101model *)pmodel->MOS101igbMod;
pslot->Igcmod = (MOS101model *)pmodel->MOS101igcMod;
pslot->Igso = ptran->MOS101Igs;
pslot->Igdo = ptran->MOS101Igd;
pslot->Igb = ptran->MOS101Igb;
pslot->Igcs = ptran->MOS101Igcs;
pslot->Igcd = ptran->MOS101Igcd;
pslot->gigsos = ptran->MOS101gIgss;
pslot->gigsog = ptran->MOS101gIgsg;
pslot->gigcsg = ptran->MOS101gIgcsg;
pslot->gigcsd = ptran->MOS101gIgcsd;
pslot->gigcsb = ptran->MOS101gIgcsb;
pslot->gigcss = ptran->MOS101gIgcss;
pslot->gigdod = ptran->MOS101gIgdd;
pslot->gigdog = ptran->MOS101gIgdg;
pslot->gigcdg = ptran->MOS101gIgcdg;
pslot->gigcdd = ptran->MOS101gIgcdd;
pslot->gigcdb = ptran->MOS101gIgcdb;
pslot->gigcds = ptran->MOS101gIgcds;
pslot->gigbg = ptran->MOS101gIgbg;
pslot->gigbd = ptran->MOS101gIgbd;
pslot->gigbb = ptran->MOS101gIgbb;
pslot->gigbs = ptran->MOS101gIgbs;
```

`TOPO101` of topo101.h is accessible through a pointer to topvar in `CMI_VAR` of CMIdef.h; for example, in file /extcmi/mos101/CMImos101eval.c,

```
struct TOPO101 *topo101 = (struct TOPO101 *) pslot->topovar;
```

By doing this, additional eletrical biases can be accessed using `TOPO101` member variables: `vgms`, `vdbs`, `vsbs`, `vdes`, `vses`, `qdef`, and so forth.

All quantities of `TOPO101` are calculated and assigned within the evaluation function. For a detailed application, see CMIl101evaluate() and MOS101EvalNoise() in example file /extcmi/mos101/CMImos101eval.c.

On the HSPICE engine side, these quantities are used for convergence checks, Jacobian stamping, circuit element summary printout, template output, and so on. They are hard-coded and are not accessible by you.

Generalized Customer CMI only supports the following forty template namings, that is, `templt1` (or equivalently, `LX1`), `templt2` (or equivalently, `LX2`), ..., `templt40` (or equivalently, `LX40`).

These namings are case-insensitive. You should specify them in the evaluation function according to your need. For example, see the /extcmi/mos101/CMImos101eval.c file.

Activating These Enhancements

Customer CMI evolved in three phases. Here's how to activate the different enhancements:

- Original Customer CMI—
  a. Include `.OPTION CMIFLAG` in the netlist.
  b. Assign `topoid` of `CMI_MOSFET` structure to `0` in the code.
- Original Customer CMI with gate tunneling modeling and additional instance parameter support—
  a. Include `.OPTION CMIFLAG CUSTCMI=1` in the netlist.
  b. Assign `topoid` of `CMI_MOSFET` structure to `0` in the code.
- Generalized Customer CMI with BSIM4-like topologies and additional instance parameter support—
  a. Include `.OPTION CMIFLAG` in the netlist.
  b. Assign `topoid` of CMI_MOSFET structure to `101` in the code.

Conventions

This section describes model conventions in the Customer CMI.

Bias Polarity, for N- and P-channel Devices

The `vds`, `vgs`, and `vbs` input biases in CMI_VAR are:

```
vds = vd - vs
vgs = vg - vs
vbs = vb - vs
```

If your model code does not distinguish between the n-channel and p-channel bias, then you must negate these biases for the P-channel device. The example routines multiply the biases by the *type* model parameter, which is 1 for the N-device, or -1 for the P-device.

For example, the following is the MOS3 model code:

```
if (model->MOS3type < 0) { /* P-channel */
   vgs = -VgsExt;
   vds = -VdsExt;
   vbs = -VbsExt;
   }
else { /* N-channel */
   vgs = VgsExt;
   vds = VdsExt;
   vbs = VbsExt;
}
```

Use this code in both the `CMI_Evaluate()` and the `CMI_DiodeEval()` functions.

Figure 46 on page 564 shows the convention to output current components.

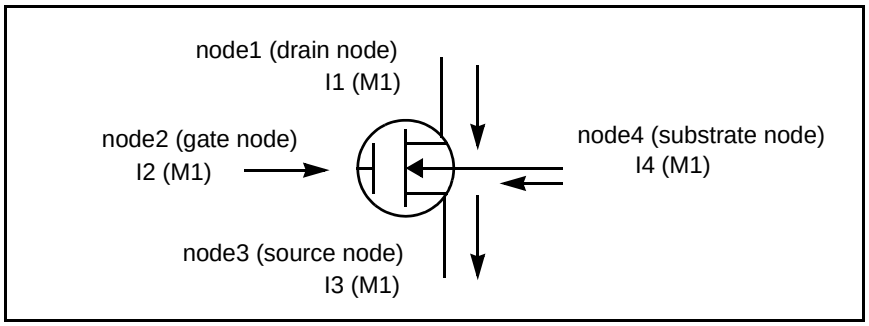
- For the channel current, drain-to-source is the positive direction.
- For substrate diodes, bulk-to-source and bulk-to-drain are the positive directions.

These conventions are the same for both N-channel devices and P-channel devices.

The conventions for von are:

- N-channel device is on, if vgs > von.
- P-channel device is on, if vgs < von.

Figure 46 MOSFET (node1, node2, node3, node4) - N-channel



Base the derivatives (conductances and capacitances) on the polarity conventions for the bias and current.

The following code demonstrates the required polarity reversal for currents, *Von,* and *Vdsat* for PMOS devices.

```
if (model->type < 0)
   {
   pslot->ids   = -pslot->ids;
   pslot->ibs   = -pslot->ibs;
   pslot->ibd   = -pslot->ibd;
   pslot->von   = -pslot->von;
   pslot->vdsat   = -pslot->vdsat;
}
```

Source-Drain Reversal Conventions

If you operate the MOSFET in the reverse mode (when Vds < 0 for N-channel, or Vds > 0 for P-channel), then HSPICE or HSPICE RF performs the appropriate computations. This includes a variable transformation (Vds -> -Vds, Vgs -> Vgd, Vbs->Vbd), and an interchange of the source and drain terminals. You do not see this transformation, but it simplifies the model coding task.

Thread-Safe Model Code

HSPICE or HSPICE RF uses shared-memory, multithreading algorithms to evaluate the model. To ensure thread-safe model code, adhere to the following rules:

- Do not use static variables in `CMI_Evaluate()`, `CMIDiodeEval()`, `CMIWriteError()`, or `CMI_Noise()`, or in functions that these routines call.
- Never write to a global variable when you execute `CMI_Evaluate()`, `CMIDiodeEval()`, `CMIWriteError()`, or `CMI_Noise()`.

A

Finding Device Libraries

Describes how to use the HSPICE automatic model selector to find the proper model for each transistor size.

For libraries with multiple models of a specific element, you can use an automatic model selector in HSPICE to automatically find the proper model for each transistor size. This chapter describes how to use the model selector.

The model selector uses the following criteria:

$$LMIN + XLREF \leq L + XL < LMAX + XLREF$$

$$WMIN + XWREF \leq W + XW < WMAX + XWREF$$

If you do not specify XLREF, simulation sets it to XL. If you do not specify XWREF, simulation sets it to XW.

The model selector syntax is based on a common model root name, with a unique extension for each model.

The following is an example of HSPICE syntax for MOSFET models:

```
M1 drain gate source bulk NJ W=2u L=1u
   .MODEL NJ4 NJF WMIN=1.5u WMAX=3u LMIN=.8u LMAX=2u
   .MODEL NJ5 NJF WMIN=1.5u WMAX=3u LMIN=2u LMAX=6u
```

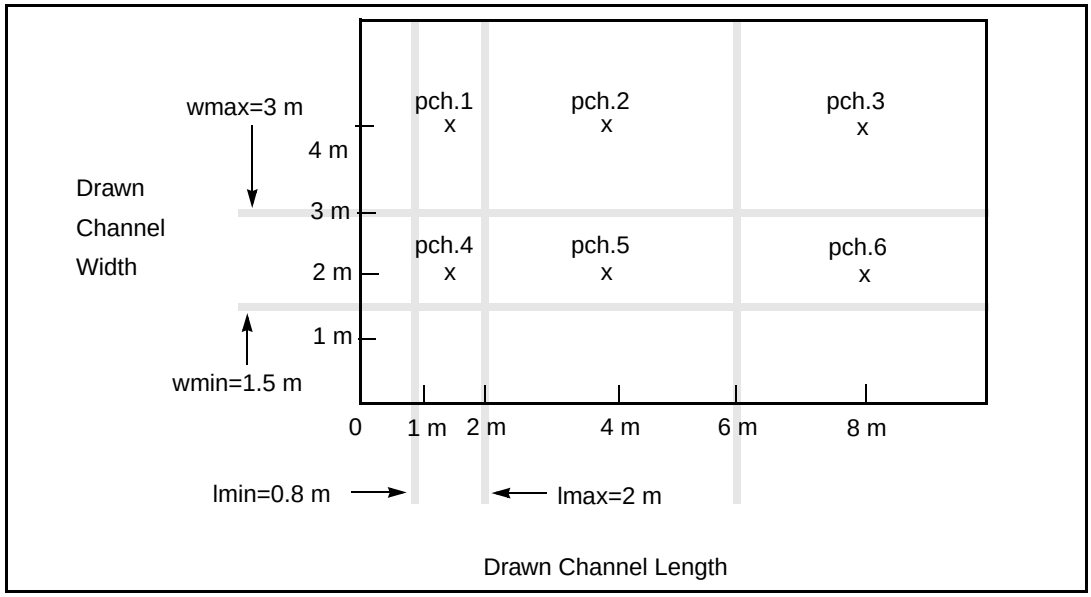
Figure 47 on page 568 illustrates the MOSFET model selection method.

This example illustrates several pch.*x* models, with varying drawn channel lengths and widths, in the model library. The model root name is pch, and the extensions are 1, 2, ..., 6. The NJ4 instance of the NJ Element (W=2 μ, L=1 μ) requires a model for which 1.5 μ ≤ channel width ≤ 3 μ, and 0.8 μ ≤ channel length ≤ 2 μ.

The automatic model selector chooses the pch.4 model because that model satisfies these requirements. Similarly, the NJ5 transistor requires a model with 1.5 μ ≤ channel width ≤ 3 μ, and 2 μ ≤ channel length ≤ 6 μ. The pch.5 model

satisfies these requirements. If a device size is out of range for all models, the automatic model selector issues an error message.

Figure 47 Automatic Model Selector Method



If the automatic model selector cannot find a model within a subcircuit, the automatic model selector searches the top level. If the automatic model selector fails to find a model, simulation terminates.

The following combination of conditions causes the automatic model selector to fail and terminates the simulation:

- The element statement uses a model name that contains a period (.).
- The model library was not designed for use with the automatic model selector.
- The simulation input includes either a multisweep specification or a **.TEMP** temperature analysis statement.

The following example illustrates how a period in a model name can cause problems in automatic model selection.

Example 1

```
M1 d g s b N.CHN W=10u L=5u* Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Example 2

```
.TEMP 25
.M1 d g s b N.CHN W=10u L=5u* Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Because Example 1 does not specify multisweep or temperature analysis, simulation does not invoke the model selector feature, so simulation uses the N.CHN model with no problems.

In Example 2, however, the .**TEMP** statement invokes the model selector feature. The model selector tries to find a model named N.*nnn* that fits within the length and width ranges specified in the element statement.

Because the length in the element statement (5 μm) is not within the 1 to 4 μm range specified in the **.MODEL** statement, the model selector cannot find a model that matches the element statement, and simulation issues a “device ‘N’ not found” error message.

B

Comparing MOS Models

Compares and reviews the most commonly used MOSFET models.

This appendix reviews the history, strengths, and weaknesses of the following commonly used MOSFET models.

MOSFET Level	Description
LEVEL 2	SPICE Level 2
LEVEL 3	SPICE Level 3
LEVEL 13	BSIM1
LEVEL 28	Synopsys proprietary model, based on BSIM1
LEVEL 39	SIM2

History and Motivation

This section describes the history and the motivation for using the Synopsys MOSFET models.

Synopsys Device Model Enhancements

Synopsys modified the standard SPICE models to satisfy the needs of customers. The modifications are in the areas of:

- Drawn dimensions, corrected for photolithography and diffusion
- Corrections for optical shrink

- Model-independent process variation parameters
- Uniform subthreshold equations
- Charge-conserving capacitance equations
- Impact ionization with selectable source/bulk partitioning of the excess drain current
- Enhanced temperature relationships

LEVEL 2

The LEVEL 2 model is an enhanced Grove equation. It is the most common MOS equations in all simulators.

The basic current equation with the 3/2-power terms was developed by Ihantola and Moll in 1964. Reddi and Sah added channel length modulation in 1965. Crawford added vertical field reduction in 1967. Klassen added the ECRIT parameter in 1978.

LEVEL 3

The LEVEL 3 model was developed by Liu in 1981. It is computationally more efficient, replacing the 3/2-power terms with a first-order Taylor expansion. It includes the drain-induced barrier lowering effect (ETA parameter).

The LEVEL 3 models is impressively physical, modeling two-dimensional effects based on junction depth and depletion depths.

LEVEL 13 (BSIM)

The BSIM1 model was developed by Sheu, Scharfetter, Poon and Hu at Berkeley in 1984, for higher accuracy modeling of short-channel devices. The approach is empirical rather than physical. It frequently uses polynomials. This makes it easier to write a parameter extraction program, but the polynomials often behave poorly. For example, this model uses a VDS quadratic function for mobility. Parameters specify the values at VDS=0 and 5 and the slope at VDS=5; unfortunately, values that look reasonable can produce a quadratic that is non-monotonic, causing a GDS<0 problem.

The Synopsys implementation of BSIM1 as the Level 13 MOSFET device model removed discontinuities in the current function, added temperature

parameters, and added diode and capacitance models consistent with other models. The Berkeley version did not include temperature parameters.

LEVEL 28

LEVEL 28 is a proprietary Synopsys device model for submicron devices, designed to fix the following problems in BSIM1:

- Negative GDS
- Poor behavior of some polynomial expressions
- A kink in GM at threshold

LEVEL 28 is based on BSIM1, but some parameters are quite different. You cannot use a BSIM1 parameter set as a LEVEL 28 model. The LEVEL 28 model is designed for optimization; it does not include a simple extraction program. It is stable for automatically generating model parameters. The LEVEL 28 model routinely optimizes IDS, GDS, and GM data.

LEVEL 39

The BSIM2 model was developed by Duster, Jeng, Ko, and Hu, and was released in SPICE3 in 1991. It is designed to model deep submicron devices. It uses a cubic spline to produce a smooth weak inversion transition, and has many additional parameters for improved accuracy. The GDS transition at VDSAT is markedly smoother than in BSIM1.

Future for Model Developments

This sequence of models shows a trend towards empirical rather than physical models, and an increasing number of parameters. It is unfortunate to lose contact with the physics, but it can be unavoidable, because the physics have become less universal. Short-channel devices are much more sensitive to the detail of the process. I-V curves from different manufacturers show qualitative differences in the shape of the curves. Therefore, the models need to be very flexible, requiring a large number of empirical parameters.

Model Equation Evaluation Criteria

This section describes the following aspects of the model equations:

- Potential for good fit to data
- Ease of fitting to data
- Robustness and convergence properties
- Behavior follows actual devices in all circuit conditions
- Ability to simulate process variation
- Gate capacitance modeling

Some of these aspects depend on general features of the Synopsys MOSFET models that are the same for all levels. Others result in simple objective measures for comparing the levels.

Potential for Good Fit to Data

Generally, the model with the largest number of parameters has the best potential fit. For the purpose of comparing the models, simulation counts the number of parameters in two ways.

Measure: Number of Parameters

Simulation counts only the drain current parameters, not the diode or series resistance, nor gate capacitance and impact ionization parameters, because these are almost the same for all levels.

```
LEVEL 2: VTO, PHI, GAMMA, XJ, DELTA, UO, ECRIT, UCRIT, UTRA,
   UEXP, NSUB, LAMBDA, NFS (total=13).

LEVEL 3: VTO, PHI, GAMMA, XJ, DELTA, ETA, UO, THETA, VMAX,
   NSUB, KAPPA, NFS (total=12).

LEVEL 13: VFB0, PHI0, K1, K2, ETA0, X2E, X3E, MUZ, X2M, X3MS,
   MUS, X2MS, U00, X2U0, U1, X2U1, X3U1, N0, ND0, NB0, plus
   L- and W- variation parameters (total = 20*3 = 60).

LEVEL 28: similar to LEVEL 13, minus MUS, X2MS, plus X33M,
   WFAC, WFACU (total = 21*3 = 63).
```

```
LEVEL 39: VGHIGH, VGLOW, VFB, K1, K2, ETA0, ETAB, MU0, MU0B,
   MUS0, MUSB, MU20, MU2B, MU2G, MU30, MU3B, MU40, MU4B,
   MU4G, UA0, UAB, UB0, UBB, U10, U1B, U1D, N0, NB, ND, plus
   L- and W- parameters (total = 33*3=99).
```

Measure: Minimal Number of Parameters

The minimal number of parameters is a subset of the above parameters, which you use to fit a specific W/L device.

- LEVEL 2 and 3 drop DELTA, which is a W-effect parameter.
- LEVEL 13 and 28 drop the L and W terms and the X2E, X3E, and ND0 second-order effects.
- LEVEL 39 drops ETAB, MU40, MU4B, MU4G, and ND.

The resulting minimal parameter counts for the five models are:

- LEVEL 2=12
- LEVEL 3=11
- LEVEL 13=17
- LEVEL 28=18
- LEVEL 39=28

Ease of Fit to Data

Generally, the larger the *minimal number of parameters*, the more time you spend fitting the data. Systematic L and W effect parameters of LEVEL 13, 28, and 39 make fitting easier, because you can optimize individual W/L devices. Then the individual models can calculate the final model parameters, with L and W terms. On the other hand, the more physical parameters of LEVEL 2 and 3 are helpful because you can more easily predict the value from a knowledge of the process, before fitting to I-V data. Examples of physical parameters are junction depths and doping concentrations.

Measure: Physical Percentage of Parameters

Starting with the minimal set of parameters, MOSFET models calculate the percentage that are physical.

- For LEVEL 2:
  - PHI, XJ, UO, ECRIT, NSUB, and NFS are physical
  - VTO, GAMMA, UCRIT, UTRA, UEXP, and LAMBDA are empirical, which is 50% physical parameters.
- For LEVEL 3, PHI, XJ, UO, VMAX, NSUB, and NFS are physical, which is 55%.
- For LEVEL 13, only PHI0 and MUZ are physical, returning 12% physical parameters.
- For LEVEL 28, only PHI0 and MUZ are physical, returning 11% physical parameters.
- For LEVEL 39, only PHI0 and MUZ are physical, returning 7% physical parameters.

Robustness and Convergence Properties

A discontinuity in the GM, GDS, and GMBS derivatives can cause convergence problems. Also, because real devices have continuous derivatives, a discontinuity leads to a large inaccuracy in the derivatives near that region. This can be annoying to an analog designer looking at a plot of gain versus bias for example. The most common important discontinuities are GDS at vds=vdsat, and GM at vgs=vth. The LEVEL 2 and 3 models contain these discontinuities, but the LEVEL 13, 28, and 39 models do not.

However, the LEVEL 13 model (BSIM1) often produces a negative GDS, which is obviously inaccurate, and causes oscillation, which can lead to convergence failure or a *timestep too small* error. A LEVEL 13 model can avoid negative GDS, but it depends on complex relationships between the MUZ, X2M, MUS, X2MS, X3MS, U1, X2U1, and X3U1 parameters. Usually, you can set X3MS=0 to remove a negative GDS, but this lowers the accuracy of the model in the linear region.

- The LEVEL 39 (BSIM2) model can also produce negative GDS, unless you select parameters carefully.
- The LEVEL 28 model does not create a negative GDS.

The BSIM1 model has a continuous GM at vgs=vth, but a plot of GM/IDS versus VGS shows a kink when data from real devices is monotonic. This kink is annoying to analog designers working with devices in the weak and medium

inversion region. LEVEL 28 and 39 have solved this problem, but they require additional parameters.

Three other important measures are:

Continuous Derivatives

Levels 2 and 3 fail. Levels 13, 28, and 39 pass.

Positive GDS

Levels 13 and 39 fail. Levels 2, 3, and 28 pass.

Monotonic GM/IDS in weak inversion

Levels 2, 3, and 13 fail. Levels 28 and 39 pass.

Behavior Follows Devices in All Circuit Conditions

A model can be a very good fit to IDS data in the normal operating region, but it still might not be useful for simulating some circuits.

The first criterion is that the model should have good temperature dependence. The MOSFET models provide temperature-dependence parameters for threshold voltage and mobility for all levels. The LEVEL 13, 28, and 39 models also include an FEX parameter that controls VDSAT variation with temperature.

The next most important criterion is that the model should include subthreshold current to provide accurate analog simulation. Even for digital circuits, this aids in convergence. All MOSFET models include a subthreshold current.

Impact ionization causes a drain-to-bulk current that has a strong effect on cascode circuits. MOSFET models provide ALPHA and VCR parameters for this current, which you can use for all levels.

The BSIM2 model includes a complex impact ionization model, with AI0, AIB, BI0, and BIB parameters. In the Berkeley SPICE3 release, this current was all assigned to the IDS drain-to-source current. Using the ALPHA and VCR parameters in the MOSFET models, simulation assigns the impact ionization

current to IDB, which is essential for cascode simulation. The IIRAT parameter allows the model to divide the current between IDS and IDB, if needed.

Ability to Simulate Process Variation

Usually, simulation performs full model parameter extraction or optimization only on a small number of test wafers. For a large number of wafers, in-fabrication measurements gather statistical data about process variation (for example, TOX) and simple electrical measurements (for example, VT). This statistical data uses a worst-case, Monte-Carlo, or Taguchi methodology to represent the process variation.

Before you run this simulation, you must modify models to account for variations in TOX, thresholds, line widths, and sheet resistance. Different MOSFET model levels use these parameters in similar ways. All of the models discussed here accept the following parameters: TOX, DELVTO, XL, XW, and RSH. The DELVTO model parameter shifts the threshold.

- For the LEVEL 2 and 3 models, setting DELVTO=0.1 is equivalent to adding 0.1 to VTO.
- For the LEVEL 13, 28, 39 models, DELVTO=0.1 is equivalent to adding 0.1 to VFB0.
- The XL and XW parameters represent the line width variation.

The equation for effective channel length is $Leff = L + XL - 2 \cdot LD$.

The Berkeley BSIM1 and BSIM2 models use Leff = L - DL. The MOSFET models support the DL and DW parameters (DL0, DW0 for BSIM1) for compatibility; use XL, LD, XW, and WD instead. In the MOSFET models, the geometry parameters (XL, LD, XW, and WD) and the parasitic parameters (CJ, MJ, CJSW, MJSW, and RSH) remain simple and level-independent, to consistently use process variation information.

Gate Capacitance Modeling

LEVEL 2 and 3 were released in Berkeley SPICE with the Meyer model for gate capacitance. This model is non-charge-conserving and sets dQG/dVD = dQD/dVG. Although it is not valid in a real device, it provides an adequate response for most digital simulations. Berkeley BSIM1 and BSIM2 models are charge-conserving, non-symmetric capacitance models.

The range of capacitance model choices and the default values depend on which model you choose. The default for LEVELs 2 and 3 is still the Meyer model, but you can also select a charge-conserving Ward-Dutton model.

Table 150 Comparison of Parameters for MOSFET Model Levels

LEVEL	2	3	13	28	39
Number of parameters	13	12	60	63	99
Minimal number of parameters	12	11	17	18	28
Physical parameters	50%	55%	12%	11%	7%
Continuous derivatives	no	no	yes	yes	yes
Positive GDS	yes	yes	no	yes	no
Monotonic GM/IDS	no	no	no	yes	yes

Outline of Optimization Procedure

1. Extract XL, LD, XW, WD, TOX, RSH, CGSO, CGDO, CGBO, CJ, MJ, CJSW, and MJSW from resistor and capacitor data, and plots of Beta versus W and L.
2. For each W/L device:
   - Extract VT versus VBS from IDS versus VGS data.
   - Calculate ETA from log(IDS) versus VGS plots at VDS=0.1, 5.0.
   - Fit VT parameters to the VT versus VBS data.
   - Optimize other parameters, except L and W sensitivity, to IDS, GDS, and GM versus VGS, VDS, and VBS data.
3. For each W/L device, calculate L and W sensitivity parameters from the optimized parameters of nearby devices.
4. Fit the models together into one model using the Lmin, Lmax, Wmin, Wmax feature of the MOSFET models.

Examples of Data Fitting

The following plots fit Levels 2, 3, 13, 28, and 39 to data from a submicron device, fabricated using a modern CMOS process. All models were optimized to the same data. Similar optimization files were used, optimizing different parameters. All models except LEVEL 39 use the impact ionization model, with ALPHA and VCR parameters. Level 39 has its own impact ionization parameters.

To avoid negative GDS, LEVEL 13 uses improved optimization of the parameter values. However, Level 13 does not eliminate the GDS discontinuity in LEVEL 3 or the GM discontinuity in LEVEL 2.

The next section provides model versus data plots for drain and gate sweeps, followed by close-up plots of the models, using a small step size to show GM and GDS problems in the individual levels.

LEVEL 28, 2, 3—Ids Model vs. Data

- Ids versus Vds at Vgs=1, 2, 3, 4, 5, Vbs=0
- Fits to IDS only (not GDS and GM) might look better for these plots, but would not be acceptable for analog design.

Figure 48 LEVEL 2 Ids Model versus Data Curves

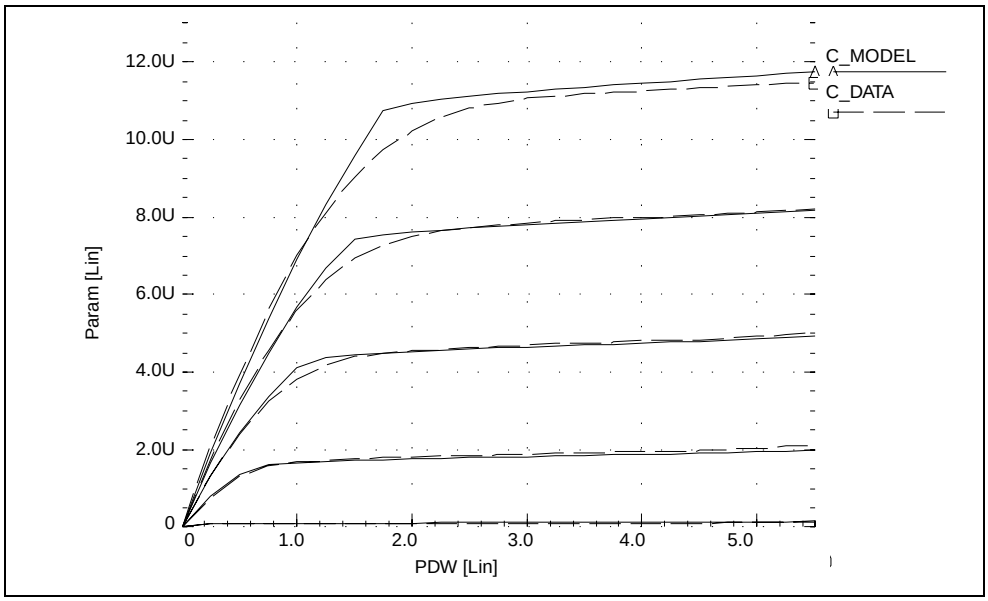


Figure 49 LEVEL 28 Ids Model versus Data Curves

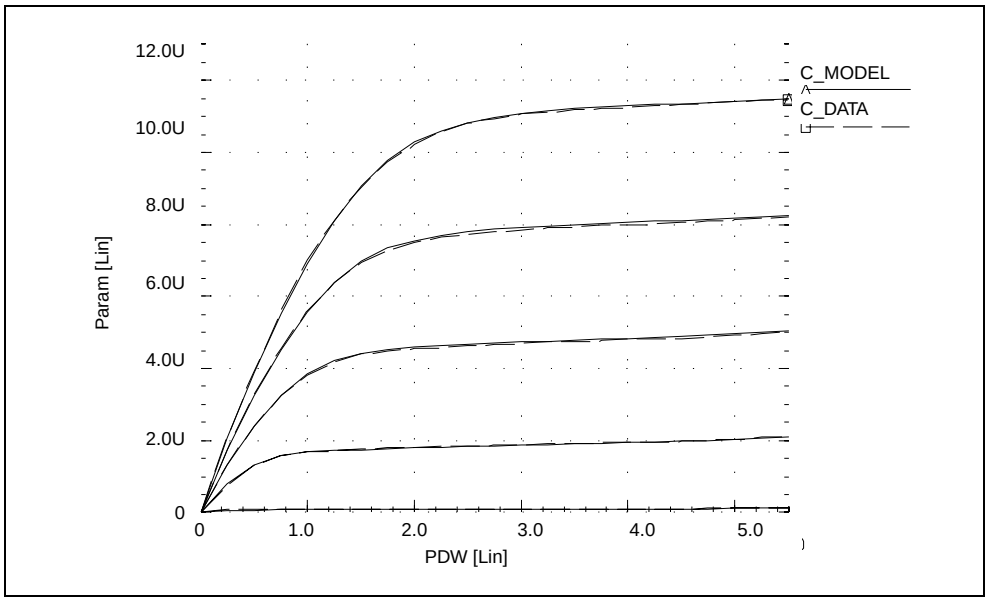
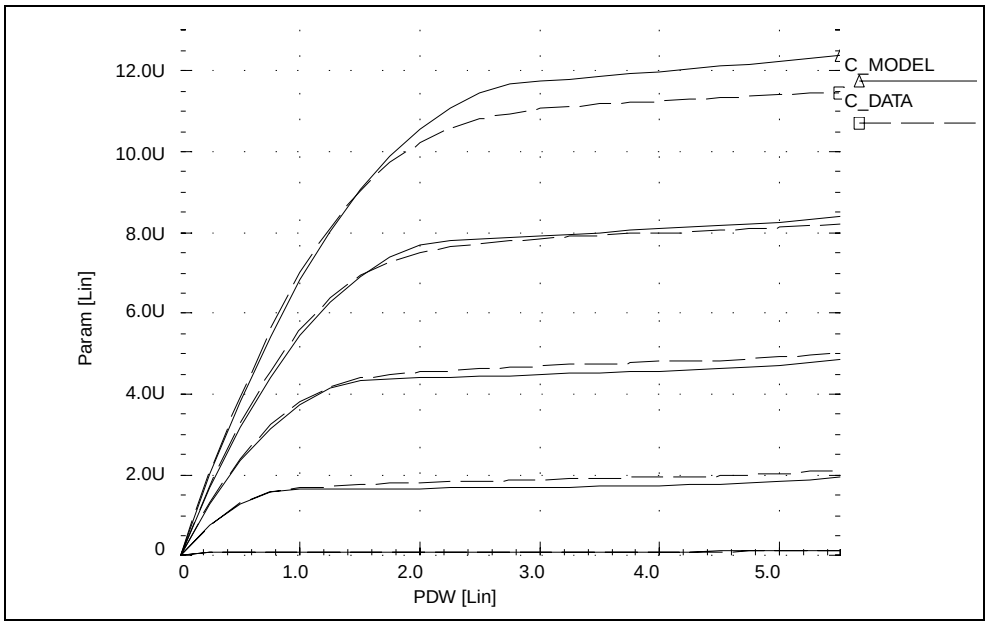


Figure 50 LEVEL 3 Ids Model versus Data Curves



LEVEL 13, 28, 39 - Ids Model vs. Data

Ids versus Vds at Vgs= 1, 2, 3, 4, 5, Vbs=0

Figure 51 LEVEL 13 Ids versus Vds Curves

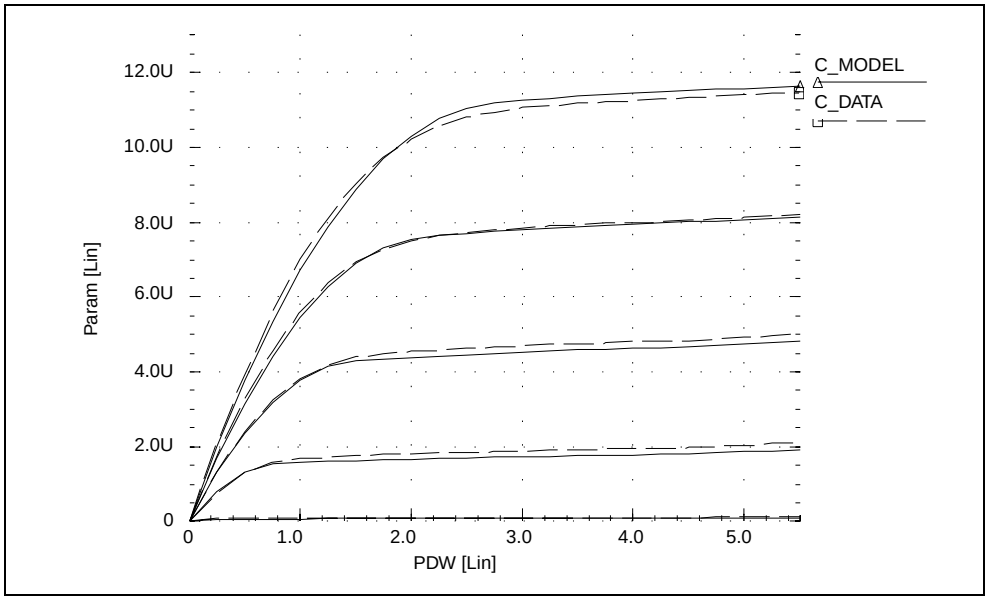


Figure 52 LEVEL 28 Ids versus Vds Curves

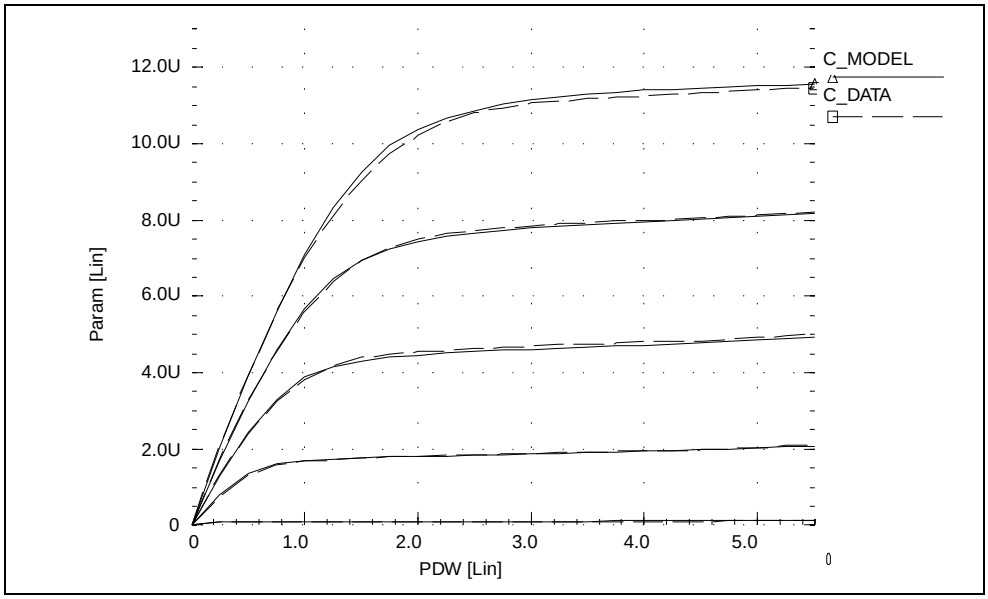
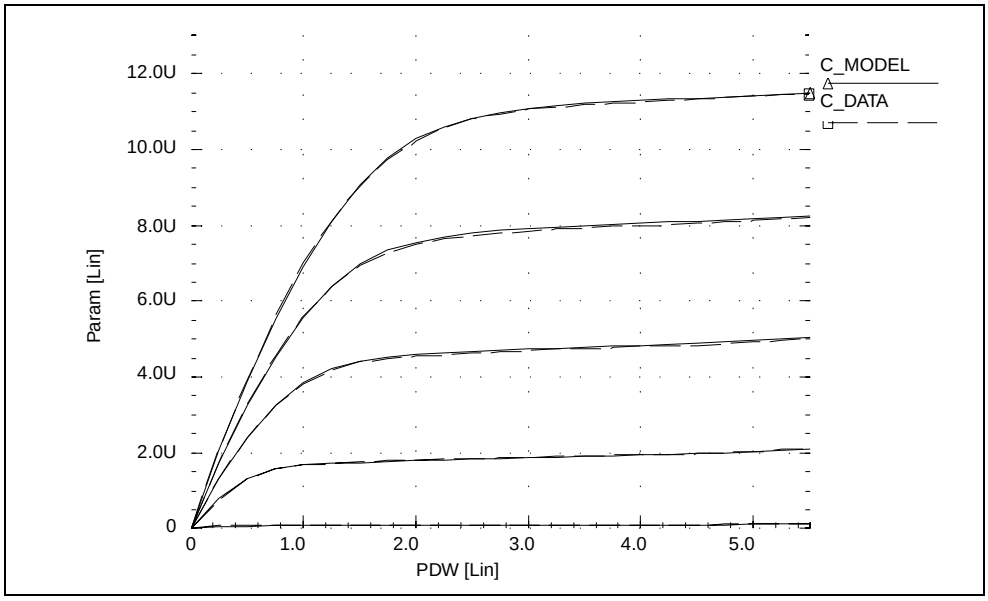


Figure 53 LEVEL 39 Ids versus Vds Curves



LEVEL 2, 3, 28—Gds Model vs. Data

- gds -vs.- Vds at Vgs=2, 3, 4, 5, Vbs=0
- The plot shows that Level 2 and 3 cannot model GDS accurately.

Figure 54 LEVEL 2 gds versus Vds Curves

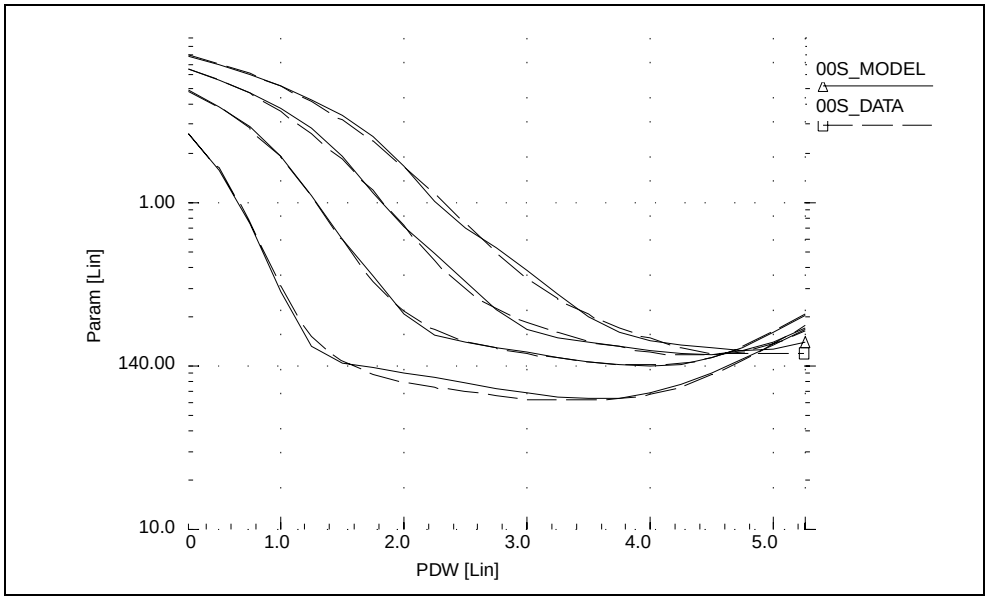


Figure 55 LEVEL 28 gds versus Vds Curves

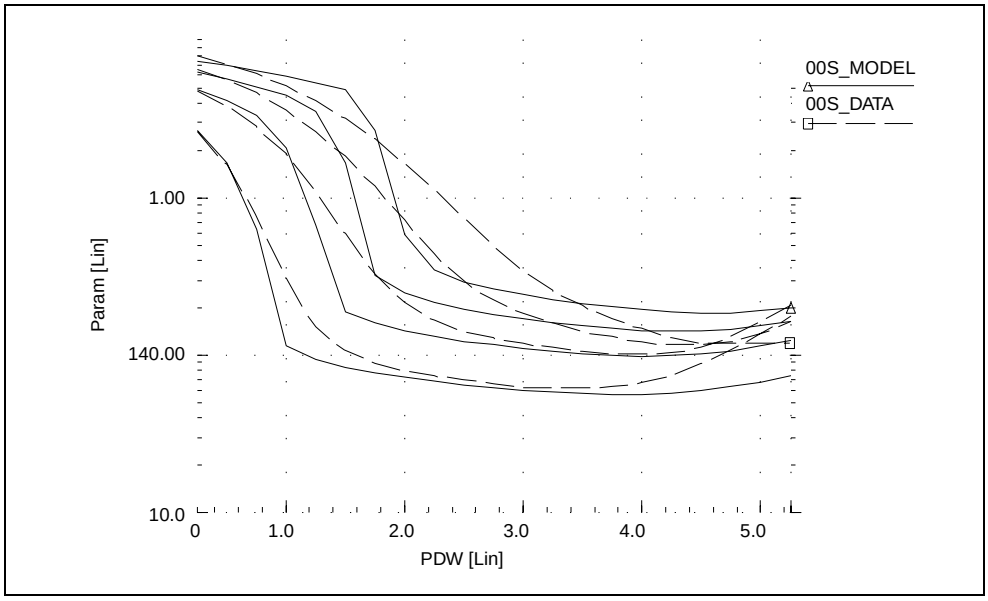
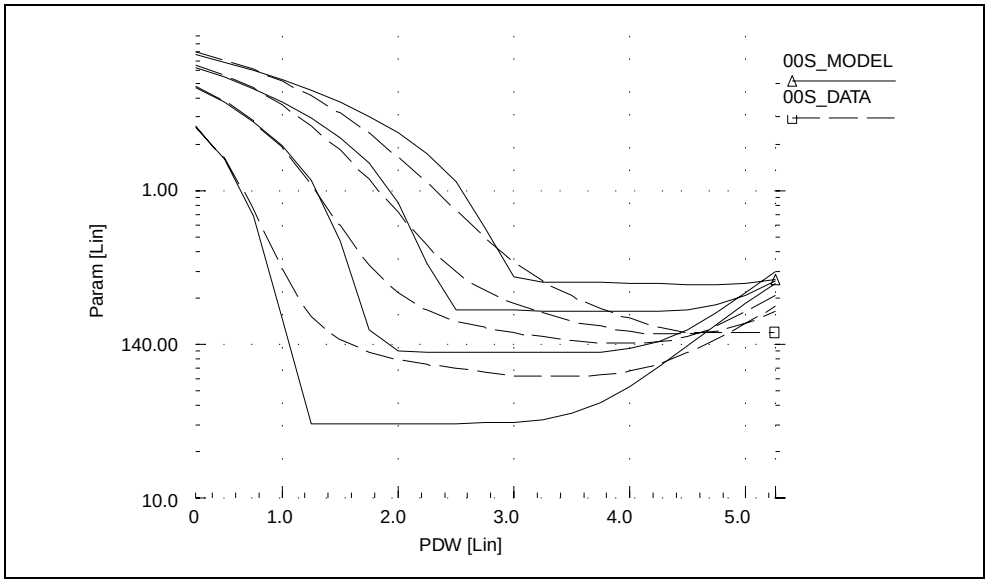


Figure 56 LEVEL 3 gds versus Vds Curves



LEVEL 13, 28, 39—Gds Model versus Data

- gds = vs. Vds at Vgs=2, 3, 4, 5, Vbs=0
- These models still have a small change in slope of Gds at Vdsat, more visible for the Level 13 model than for Level 28 or Level 39.

Figure 57 LEVEL 13 gds versus Vds Curves

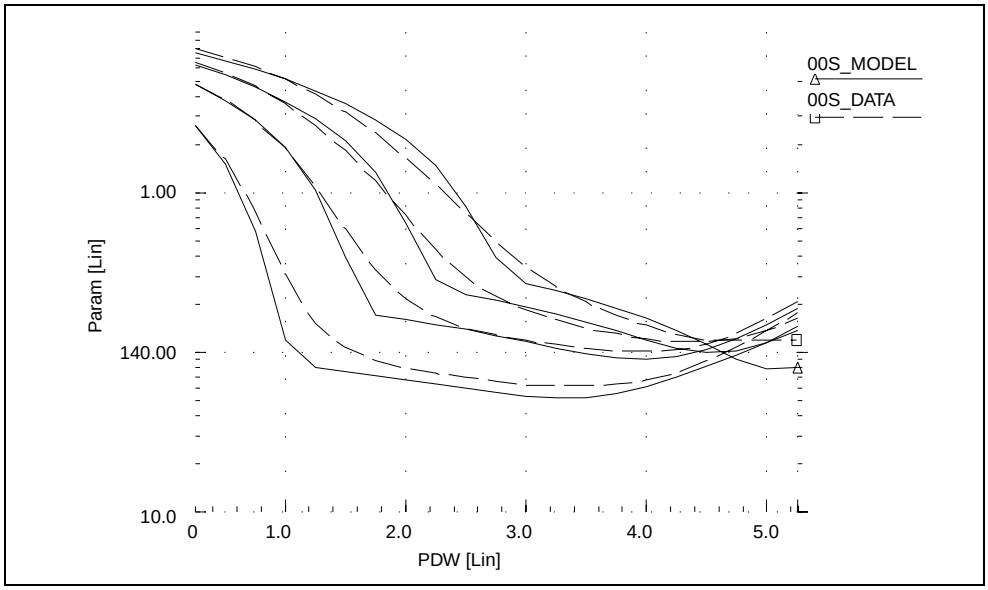


Figure 58 LEVEL 28 gds versus Vds Curves

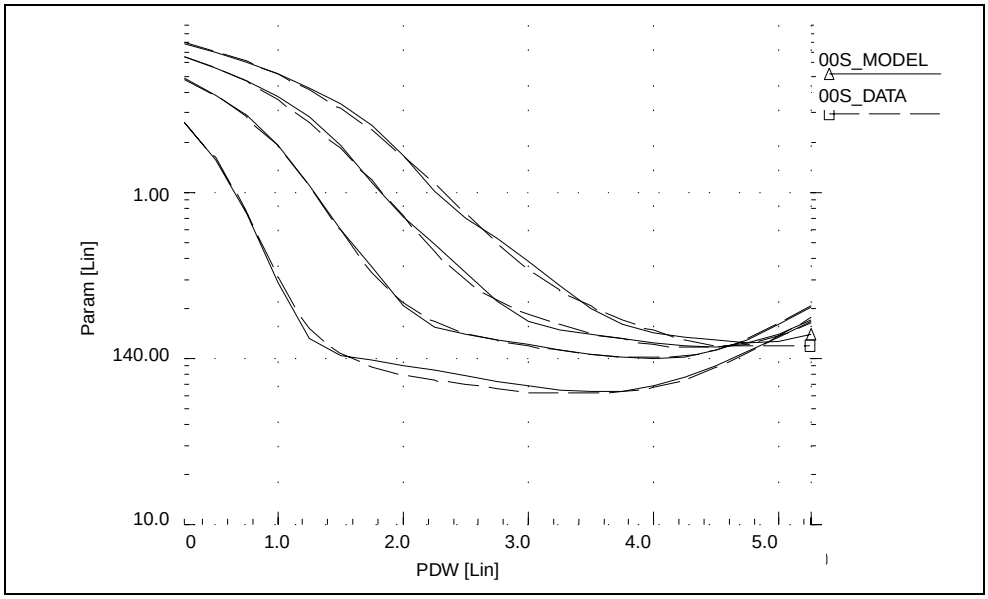
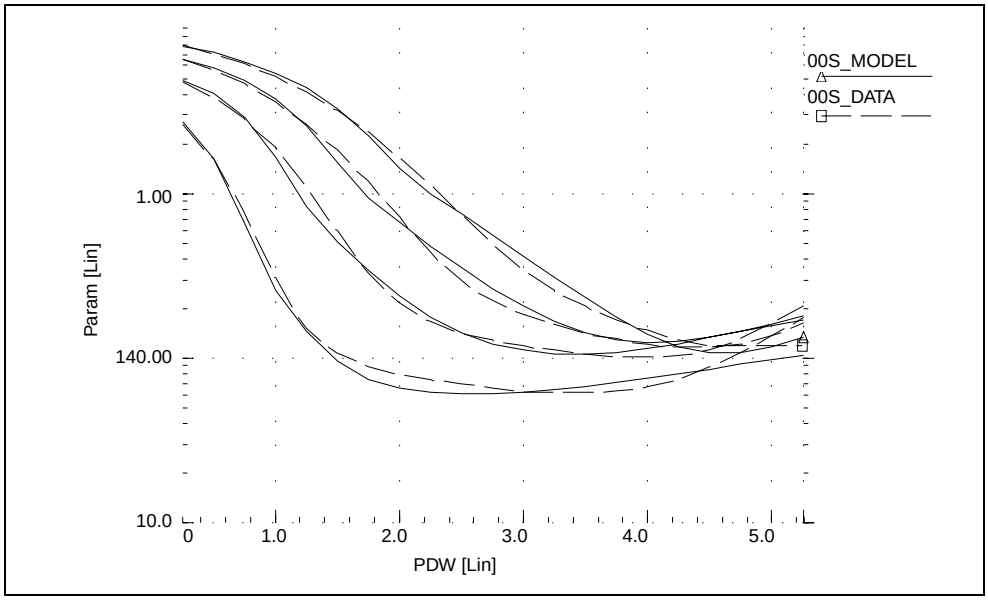


Figure 59 LEVEL 39 gds versus Vds Curves



LEVEL 2, 3, 28— Ids Model versus Data

Ids -vs.- Vgs at Vds=0.1, Vgs =0, -1, -2, -3, -4

Figure 60 LEVEL 2 Ids versus Vgs Curves

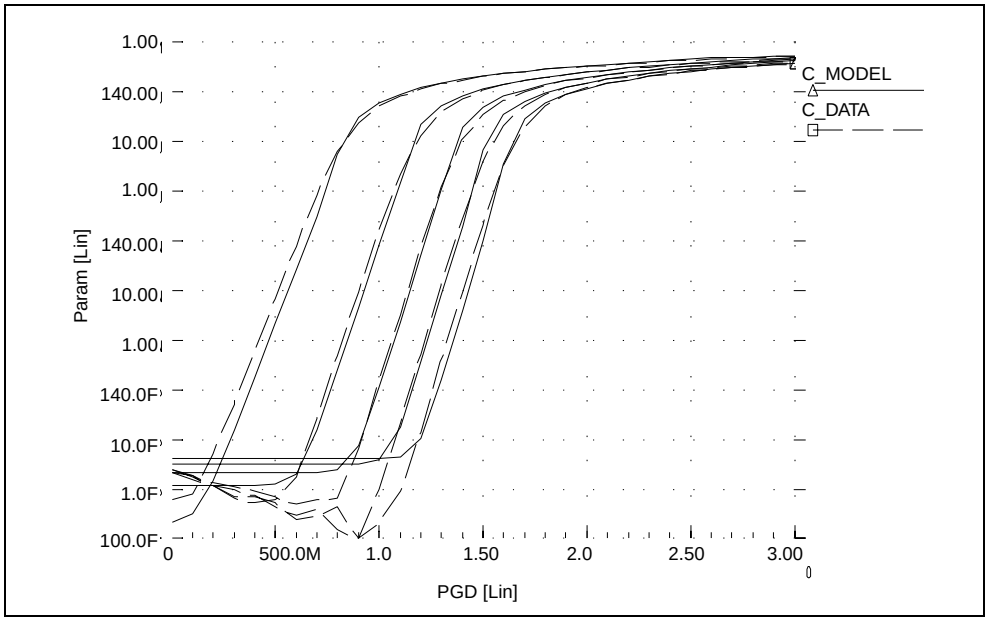


Figure 61 LEVEL 28 Ids versus Vgs Curves

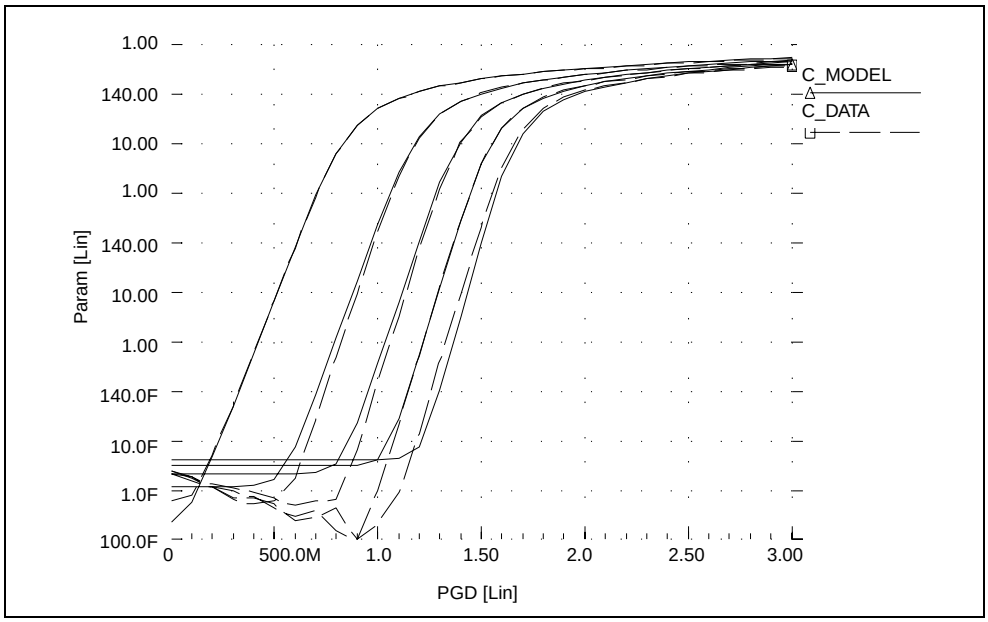
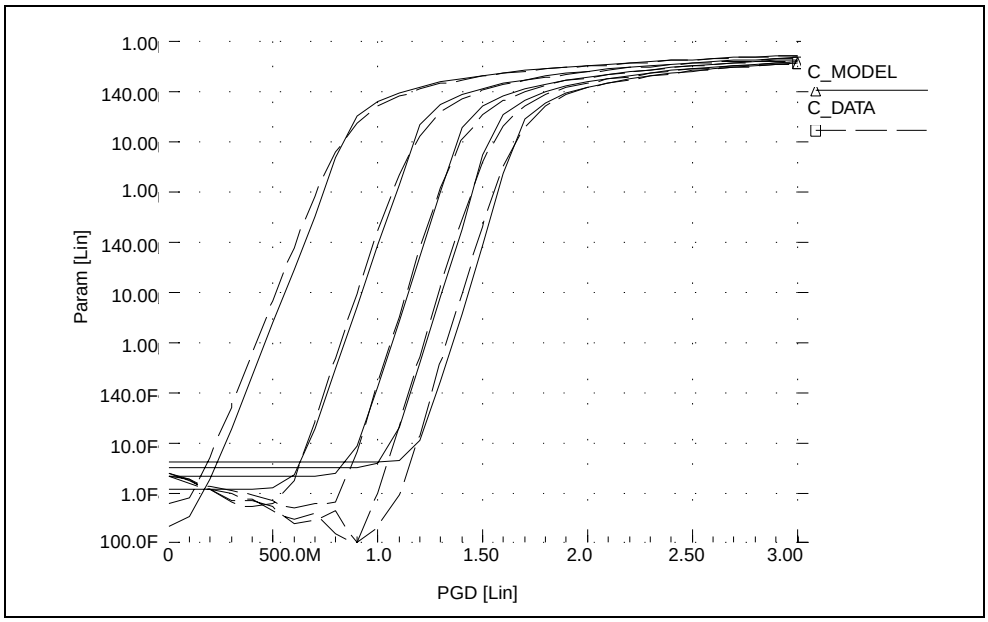


Figure 62 LEVEL 3 Ids versus Vgs Curves



LEVEL 13, 28, 39—Ids Model versus Data

Ids -vs.- Vgs at Vds=0.1, Vbs =0, -1, -2, -3, -4

Figure 63 LEVEL 13 Ids versus Vgs Curves

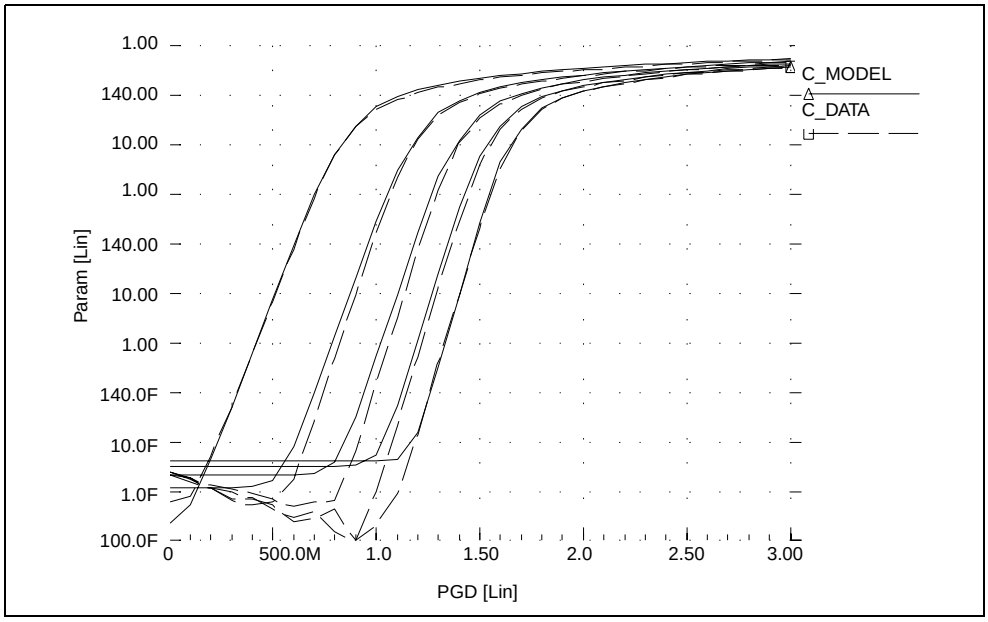


Figure 64 LEVEL 28 Ids versus Vgs Curves

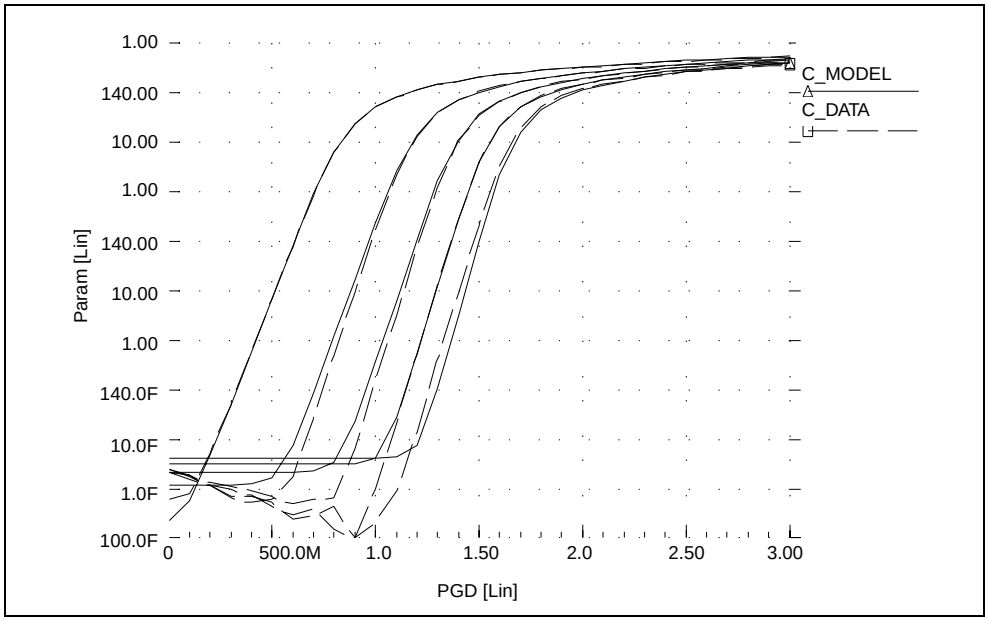
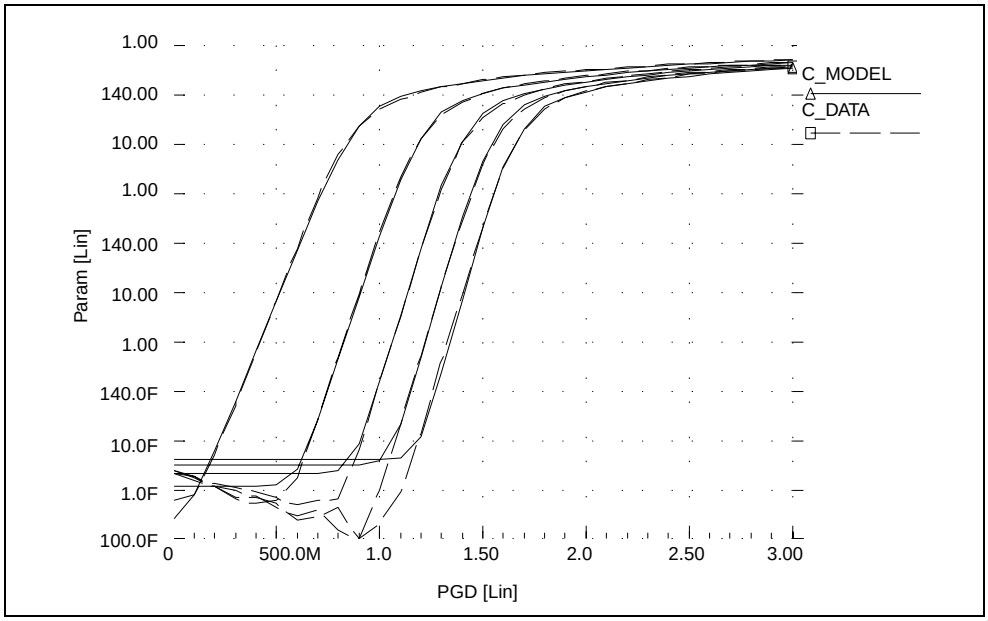


Figure 65 LEVEL 39 Ids versus Vgs Curves



LEVEL 2, 3, 28—Gm/Ids Model versus Data

- gm/Ids -vs.- Vgs at Vds=0.1, Vbs =0, -2
- The LEVEL 2 and 3 models have spikes at Vgs=Vth. The data, and the LEVEL 28 model, is monotonic decreasing.

Figure 66 LEVEL 2 gm/Ids versus Vgs Curves

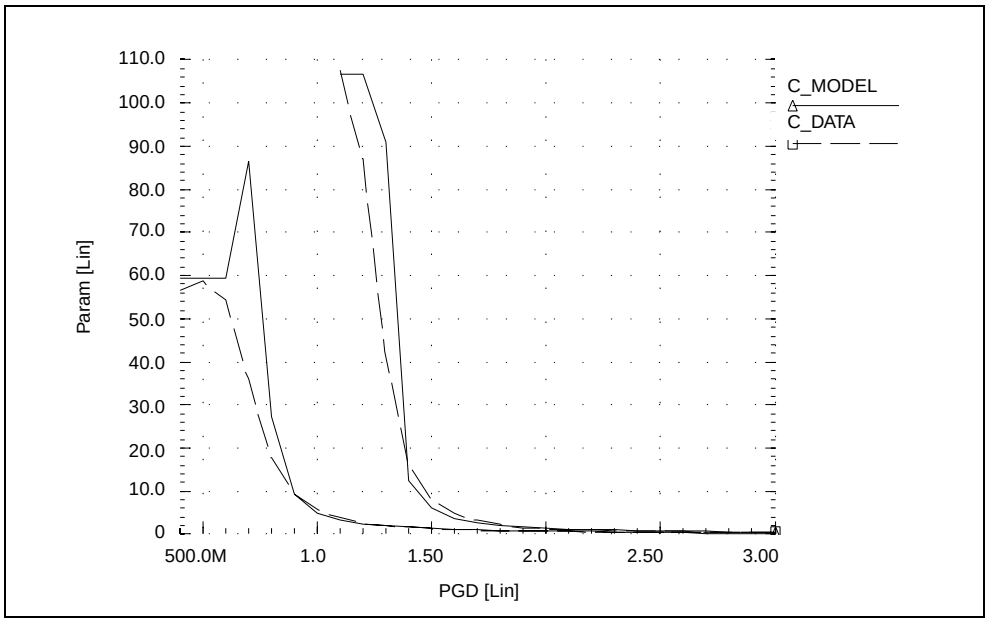


Figure 67 LEVEL 28 gm/Ids versus Vgs Curves

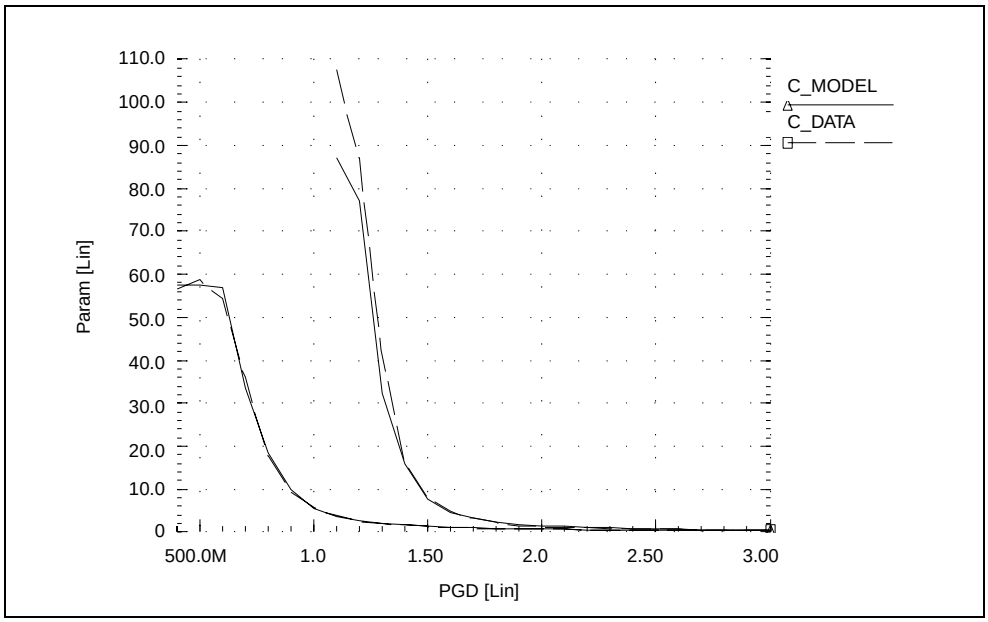
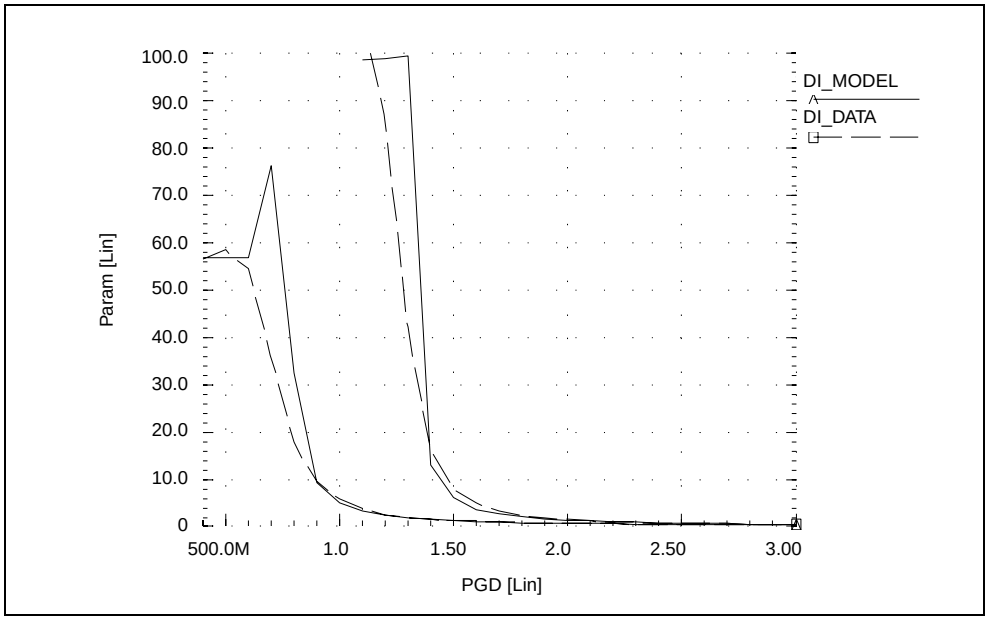


Figure 68 LEVEL 3 gm/Ids versus Vgs Curves



LEVEL 13, 28, 39—Gm/Ids Model versus Data

- gm/Ids -vs.- Vgs at Vds=0.1, Vbs =0, -2
- LEVEL 13 has a kink at Vth, which is not visible at this resolution. LEVEL 28 and 39 are monotonic.

Figure 69 LEVEL 13 gm/Ids versus Vgs Curves

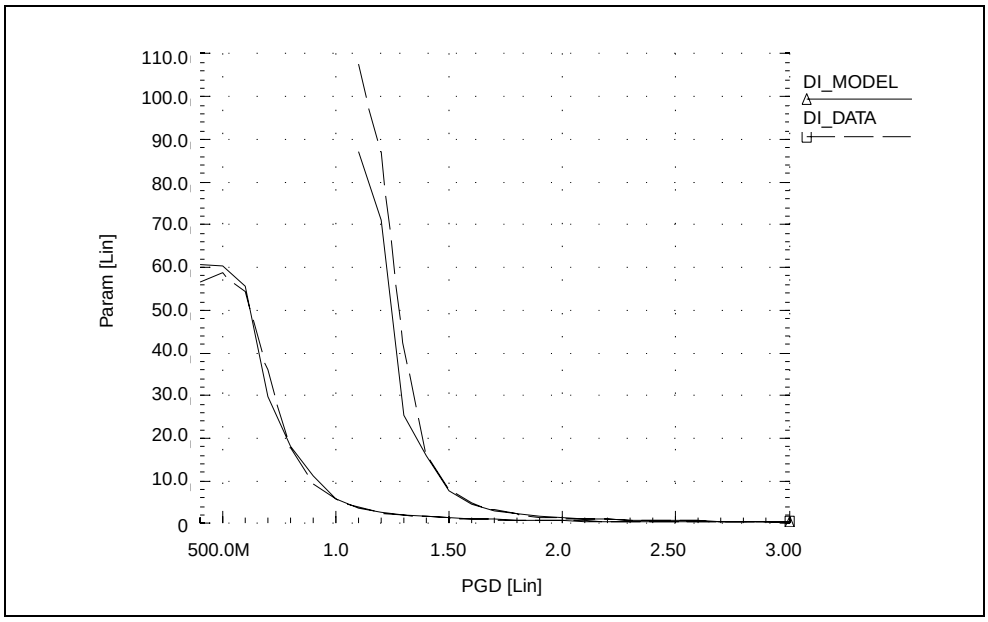


Figure 70 LEVEL 28 gm/Ids versus Vgs Curves

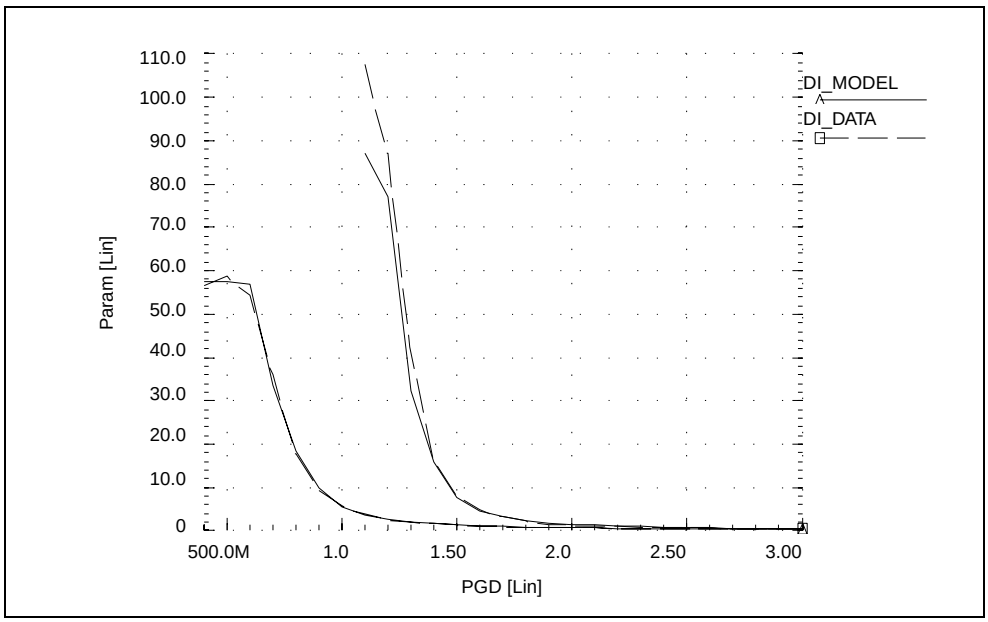
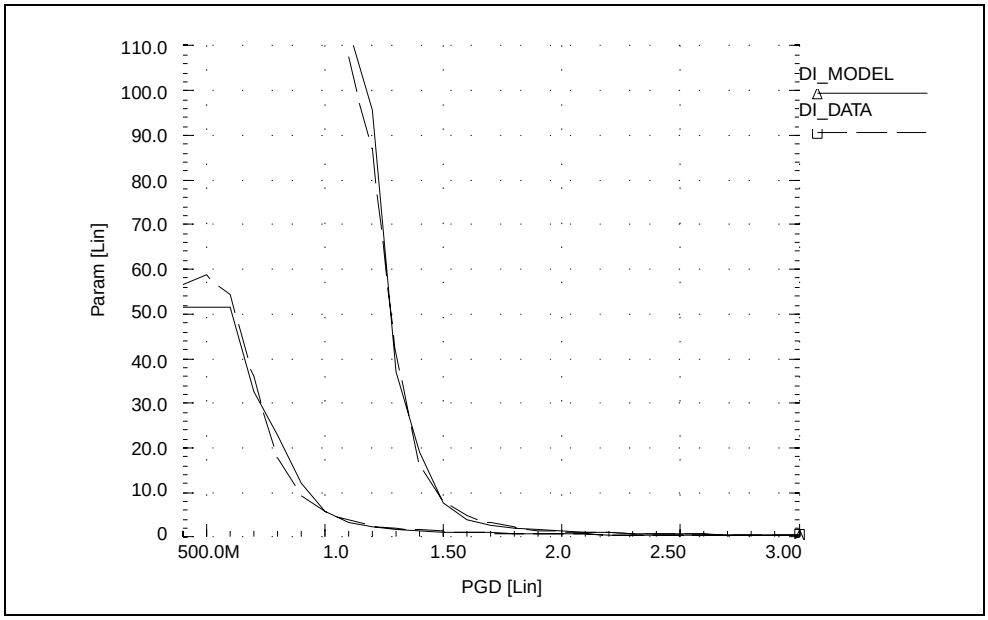


Figure 71 LEVEL 39 gm/Ids versus Vgs Curves



Gds versus Vds at Vgs=4, Vbs=0

This plot shows the behavior of gds at the linear to saturation transition. The LEVEL 3 model has a gds discontinuity.

Figure 72 LEVELs 2, 3, 28 gds versus Vds Curves

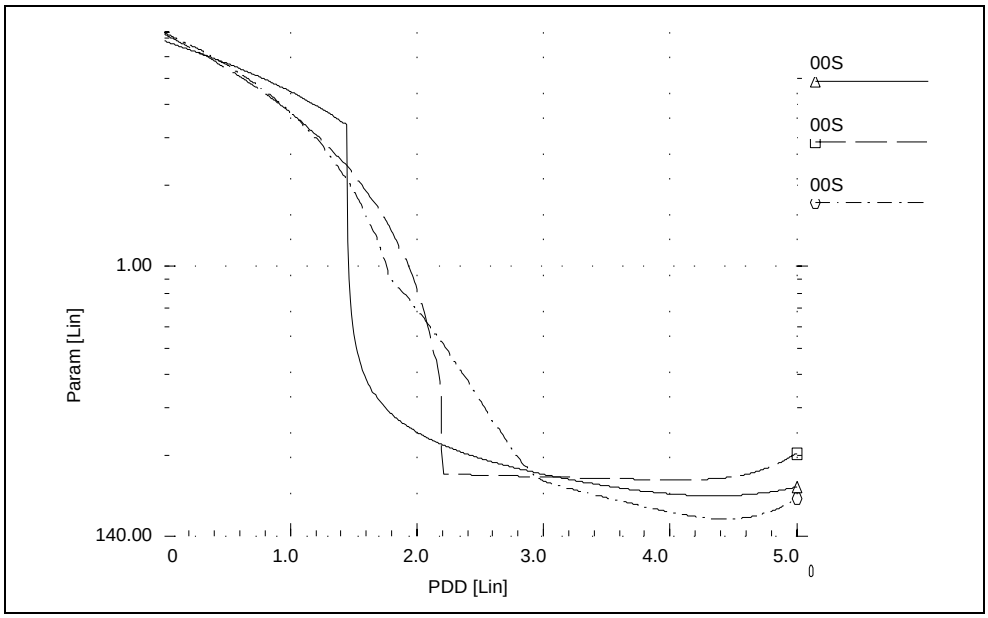
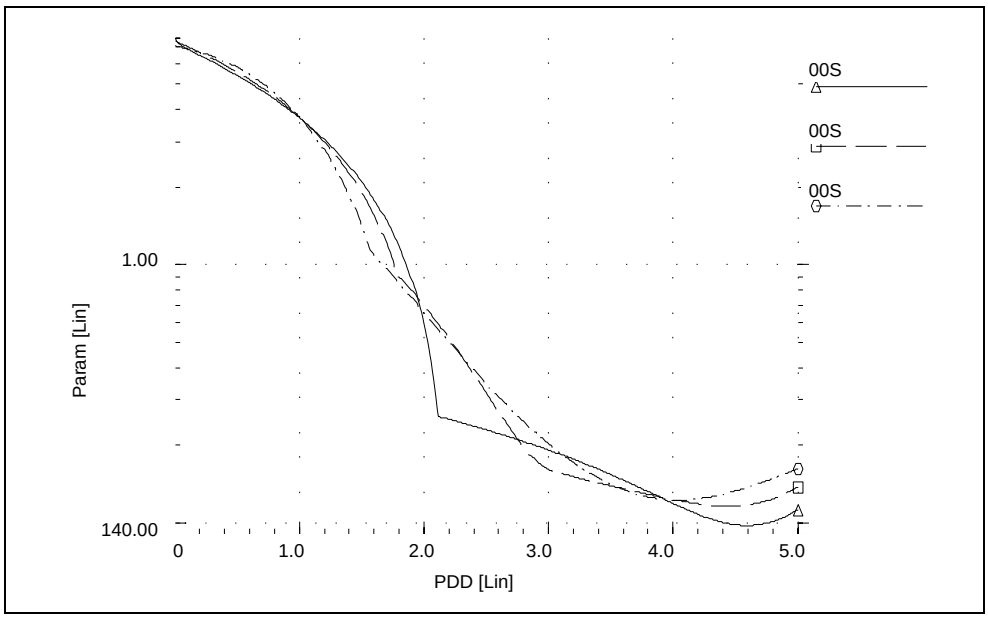


Figure 73 LEVELs 13, 28, 39 gds versus Vds Curves



Gm/Ids vs. Vgs at Vds=0.1, Vbs=0, 2

This plot shows a gm discontinuity in the LEVEL 2 model, related to the UCRIT and UEXP parameters.

Figure 74 LEVEL 2 gm/Ids versus Vgs Curves

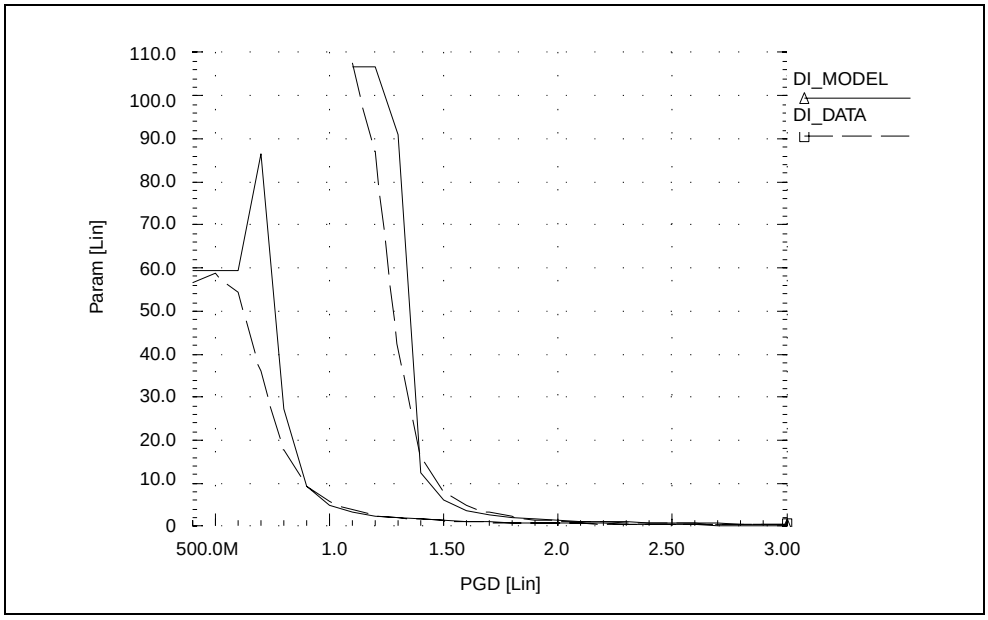
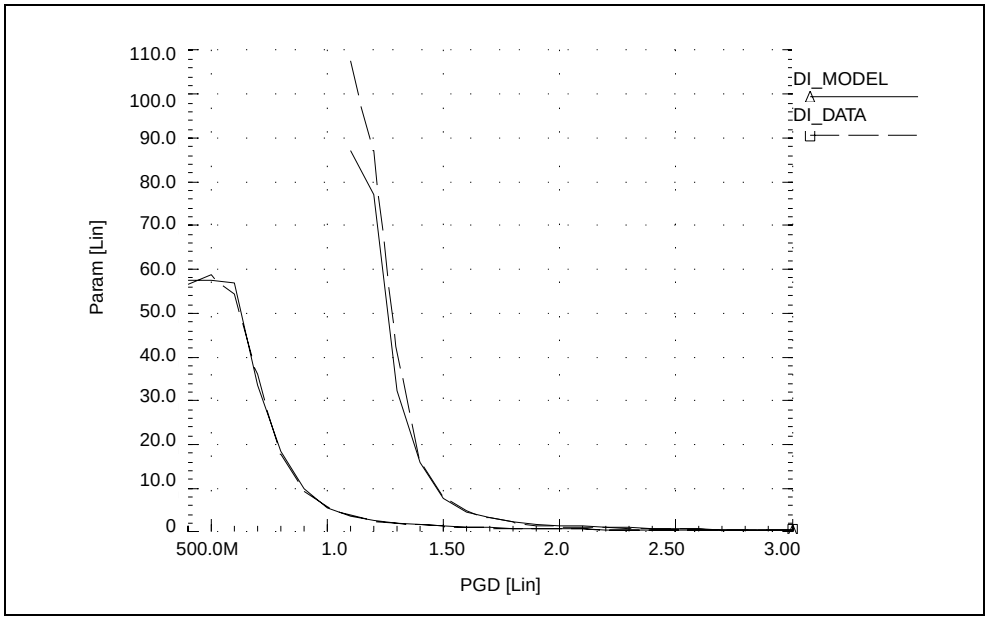


Figure 75 LEVEL 28 gm/Ids versus Vgs Curves



Gm/Ids versus Vgs at Vds=0.1, Vbs=0

This plot shows the gm/Ids ratio in the weak inversion transition region. The Level 2, 3, and 13 models have kinks near the threshold, while Level 28 and Level 39 are monotonic.

Figure 76 LEVELs 2, 3, 28 gm/Ids versus Vgs Curves

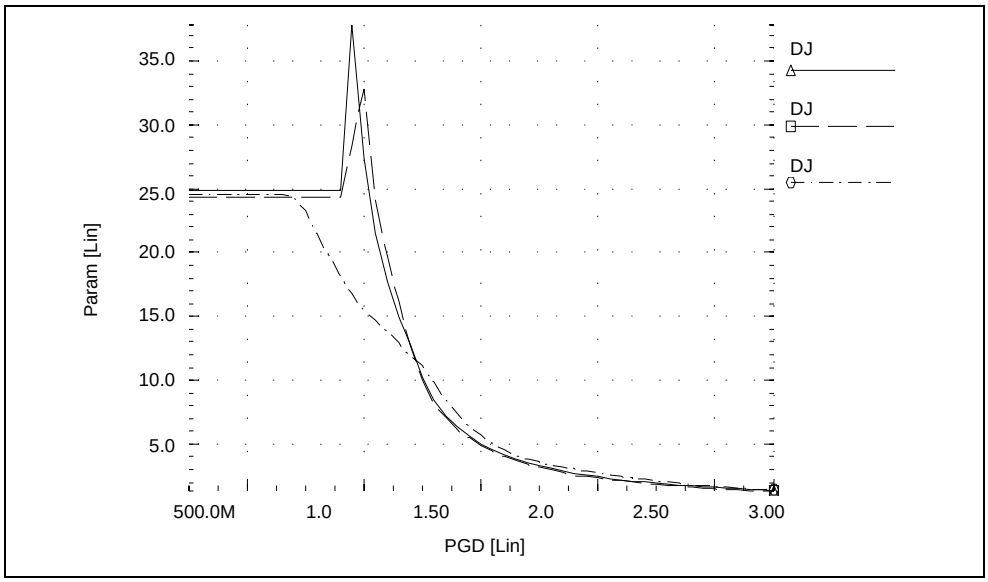
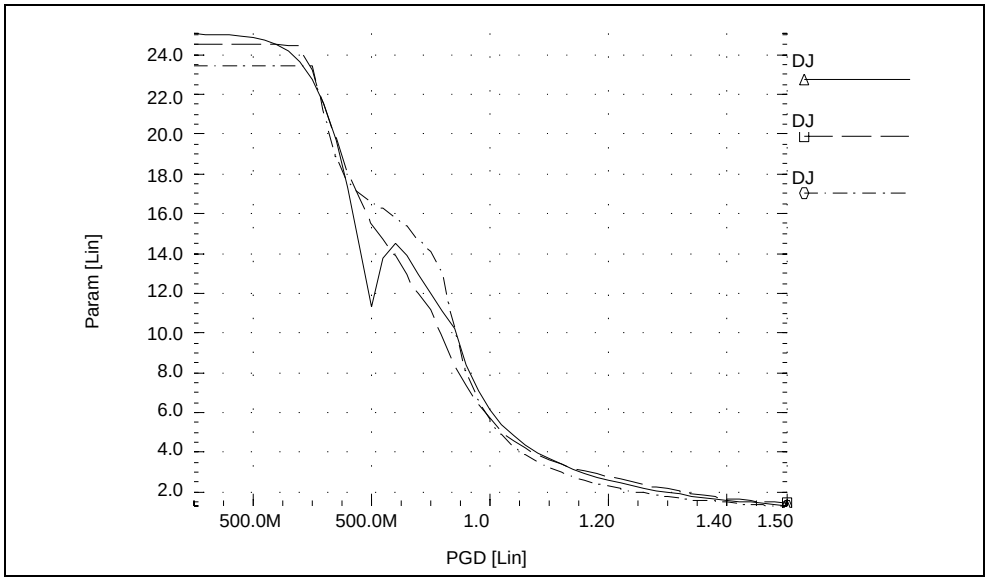


Figure 77 LEVELs 13, 28, 39 gm/Ids versus Vgs Curves



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