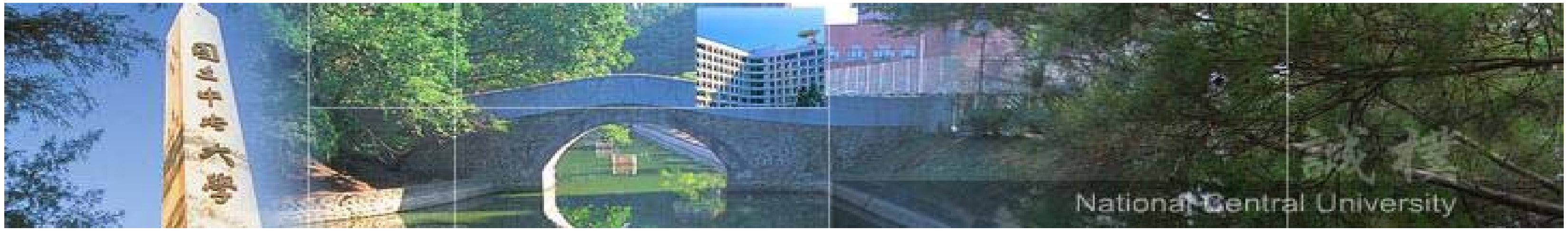

Hspice Tutorial

2008

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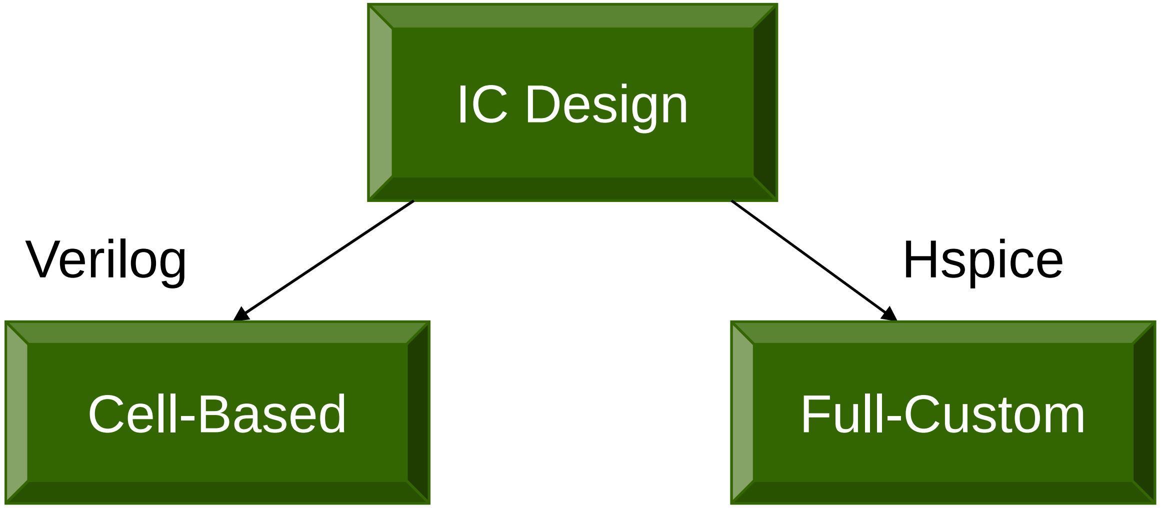
TAs:

陳詠孝 & 陳亭如

Contents

Introduction(1/2)



DSD

VLSI Design

…

VLSI Design

AIC

…

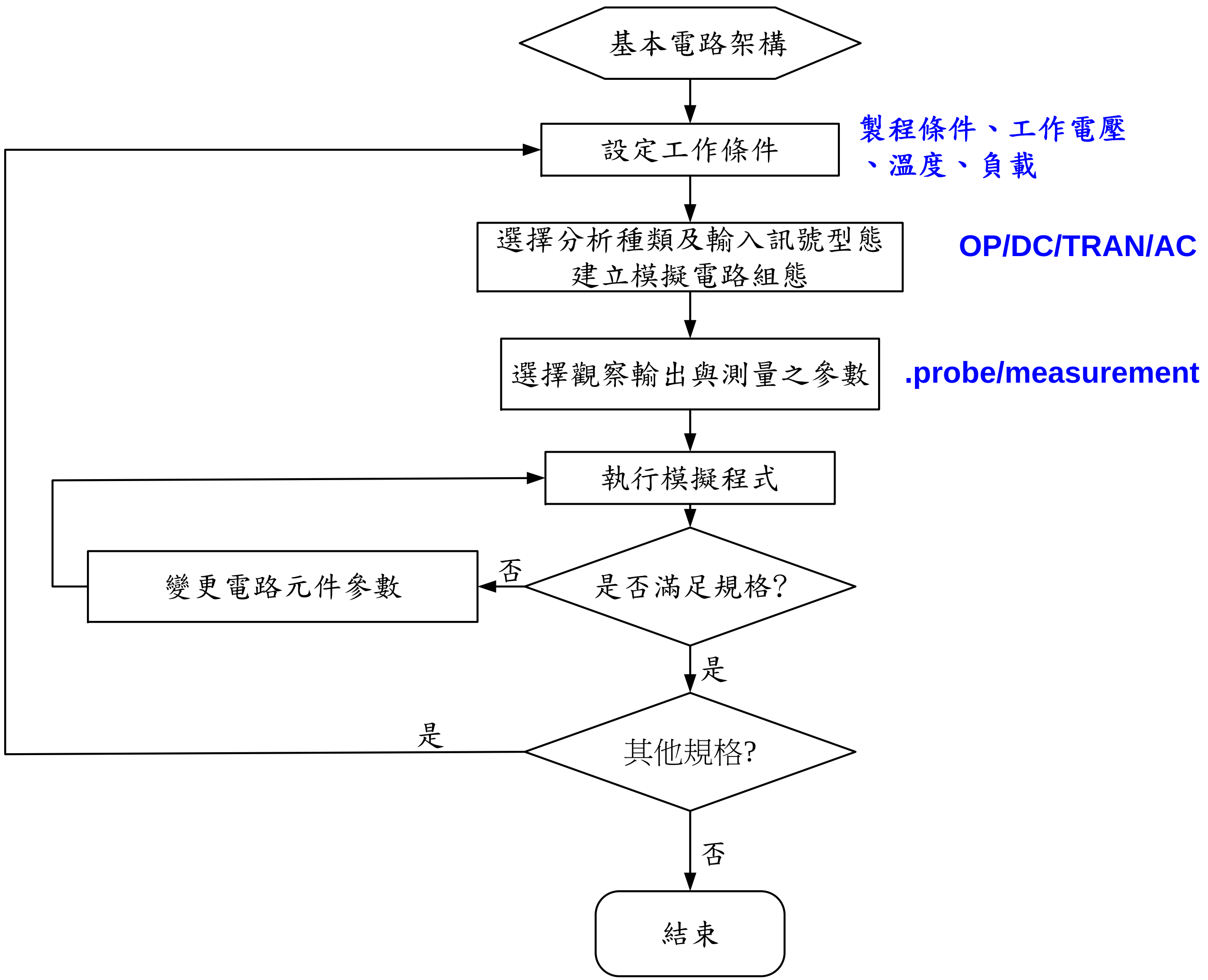
Introduction(2/2)

- **SPICE :**

  Simulation Program with Integrated Circuit Emphasis

- Hspice 是一個電路模擬軟體，用來模擬所設計電路的行為及功能特性。
- Hspice 係以電晶體、二極體、電阻及電容等各種元件模型為基礎，透過數值方法來計算電路各節點的 電壓、電流變化。
- 對於非線性的電路系統，Hspice 是在計算近似解， 所得結果的正確性和元件模型、演算法則有密切關係。
- Hspice 主要提供穩態、暫態及小信號頻率響應模擬 ，使用者需依所設計的電路種類自行規劃分析的指令及相關的輸入。

Basic Flow for SPICE



Basics for Using SPICE Tools

SPICE 之外所需的基本概念

- 了解元件的基本特性
- 熟悉所設計電路的功能
- 了解電路的輸入信號特性
- 了解電路各項規格的相依性及優先程度
- 了解需要驗證的電路規格及對應的模擬種類及電路組態
- 了解電路元件參數與架構對各項電路特性的相關性，以利模擬結果的改進

Contents

- Introduction
- **Simulation Input and Controls**
- Waveform Instructions
- Simulation Output
- Appendix

Instance and Element Names

C	Capacitor
I	Current
L	Inductor
★ M	MOSFET
R	Resistor
V	Voltage Source
X	Subcircuit Call

Unit and Scale Factor

- **Units:**

R	Ohm	(e.g. R1 node1 node2 1K)
L	Henry	(e.g. L1 node1 node2 1n)
C	Farad	(e.g. C1 node1 node2 1p)

- **Scale Factors:**

F	1e-15	T	1e12
P	1e-12	K	1e3
N	1e-9	Meg	1e6
U	1e-6	G	1e9
M	1e-3	DB	$20\log_{10}$

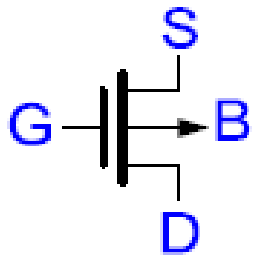
Examples:

1pF
1nH
10Meg Hz
vdb(v3)

Instance and Element Descriptions

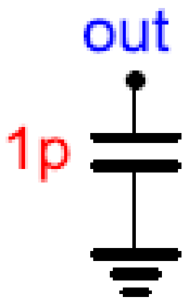
Mname D G S B N/PMOS W=?u L=?u

Mp out in vdd vdd pch W=3u L=1u



R1 A B 1K

C1 out gnd 1p



Subcircuit

.SUBCKT <Subname> <node1> <node2>……

次電路區塊描述

.ENDS <Subname>

```
.subckt inv out in Wn=0.22u Wp=0.22u Lmin=0.18u
mp0 out in vdd vdd pch w=Wp l=Lmin
mn0 out in vss vss nch w=Wn l=Lmin
.ends inv
```

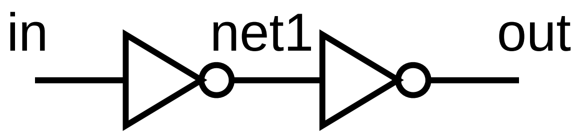
如果要在SPICE檔案中呼叫次電路時，格式如下：

Xname <node1> <node2>…… <Subname>

```
xinv dout0 d0 inv Wn=0.22u Wp=0.22u Lmin=0.18u
```

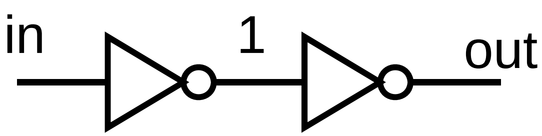
Example

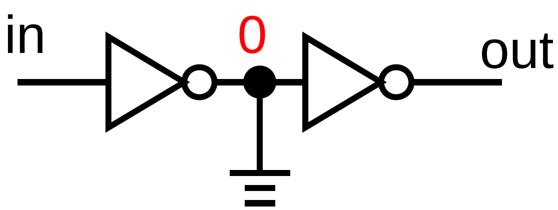
```
***** inv *****
.global vdd vss
.subckt inv in out
MM0 out in vdd vdd pch w=3u l=350n
MM1 out in vss vss nch w=1u l=350n
.ENDS
x1  in    net1  inv
x2  net1  out   inv
```




```
x1  in  1    inv
x2  1   out  inv
```

```
x1  in  0    inv
x2  0   out  inv
```





Input Control Statement

- **GLOBAL**
  - ALL nodes are assumed to be local
  - Node names can across all subcircuits by .GLOBAL

```
.GLOBAL VDD VSS
```

Netlist Structure

Title →	.Title inv
	.GLOBAL gnd!
	+ vdd!
Model →	.protect
	.lib 'C:\VLSI\mm0355v.l' TT
	.unprotect
Controls →	.op
	.options post
	.tran 0.05n 25n
	.temp 25
Sources →	v1 vdd! 0 3.3v
	v2 gnd! 0 0v
	v3 Vin 0 pulse(0v 3.3v 0.1n 0.1n 0.1n 0.5n 1.2n)
Components →	MM1 Vout Vin vdd! vdd! Pch W=3u L=350.00n
	MM0 Vout Vin gnd! gnd! Nch W=1u L=350.00n
END file →	.end

Control Statements

.AC	電路之交流分析(頻率響應)
.DC	電路之直流分析
.OP	靜態點分析
.NOISE	雜訊分析
★ .TRAN	暫態分析
.SUBCKT	定義次電路
.ENDS	次電路之結束
.OPTIONS	可設定參數及其他功能
.PRINT	指定輸出的內容
.PLOT	圖形式輸出
.TEMP	指定模擬環境的溫度
.END	檔案結束

Example

```
Inverter

.prot
.lib      'mm0355v.l' tt
.unprot
.options captab probe accurate
.temp     25
.global             VDD!     VSS!
Vdd                 VDD!     0         dc        3.3
Vss                 VSS!     0         dc        0

.op
.tran     50p       100n
.probe    v(in) v(out)

Mp                  out      in        VDD!      VDD!     pch      l= 0.35u   w= 20u
Mn                  out      in        VSS!      VSS!     nch      l= 0.35u   w= 4u

.end
```

Example

Inverter

Title. To note what circuit is described in this file. It will be skipped when SPICE is running.

.prot
.lib'mm0355v.l' tt
.unprot
.options captab probe accurate
.temp 25

The content between .prot and .unprot will not display in the .lis file. Usually, it was used when you have some circuit secrets or you don't want the useless information, such as the library, show up in the list file.

.lib command is used to specify the location of the technology library and the corner used in this simulation.

Simulation temperature

Display the node capacitance in the .lis file.

Only the node or element specified with .probe command will be displayed in the output file.

Increase the simulation accuracy and the simulation time as well.

Example

```
.global     VDD!   VSS!
Vdd         VDD!   0      dc     3.3
Vss         VSS!   0      dc     0
```

.global: Specify the global argument. All nodes with the same name will be treated as the same one.

Global ground.

.op: DC operating point analysis.

.tran: transient analysis. Time step is 50ps and stop time is 100ns

```
.op
.tran    50p    100n
.probe   v(in) v(out)
```

.probe: Record the node waveform while the option 'probe' is added in the .opstions statement.

```
Mp   out   in   VDD!   VDD!   pch   l= 0.35u   w= 20u
Mn   out   in   VSS!   VSS!   nch   l= 0.35u   w= 4u
```

Describe a PMOS and an NMOS.

```
.end
□
```

.end: EOF.

Additional space is need. Or the .end statement will be ignored.

.dc Statement

```
Inverter

.prot
.lib 'mm0355v.l' tt
.unprot
.options captab probe accurate
.temp      25
.global              VDD!      VSS!
Vdd                  VDD!      0         dc        3.3
Vss        VSS!      0         dc        0

.op
.dc        sweep     vin       0         3.3       0.1
.probe     v(out)

Vin        in        0         dc        1.65
Mp         out       in         VDD!      VDD!     pch      l= 0.35u   w= 20u
Mn         out       in         VSS!      VSS!     nch      l= 0.35u   w= 4u
.end
```

.dc: dc voltage sweep.
The voltage source Vin will change its voltage from 0V to 3.3V with a step of 0.1V.

You must specify a certain dc value for the voltage source while performing dc sweep.

.ac Statement

```
Inverter

.prot
.lib  'mm0355v.l' tt
.unprot
.options captab probe accurate
.temp       25
.global                 VDD!      VSS!
Vdd         VDD!        0         dc        3.3
Vss         VSS!        0         dc        0

.op
.ac         dec         100       1         100Meg
.probe      vdb(out)    vp(out)
Vin         in          0         dc        1.65      ac        1
Mp          out         in        VDD!      VDD!      pch       l= 0.35u    w= 20u
Mn          out         in        VSS!      VSS!      nch       l= 0.35u    w= 4u
.end
```

.ac: ac frequency sweep. Simulate 100 times/decade from 1Hz to 100MHz. The 'dec' statement can be replaced by 'lin' for linear scale.

vp(out): Display the node phase.

vdb(out): Display the node voltage in dB.

An ac voltage source is needed for ac simulation. If the amplitude of the ac voltage is 1, the output voltage will equals to the voltage gain.

Contents

Transient Sources

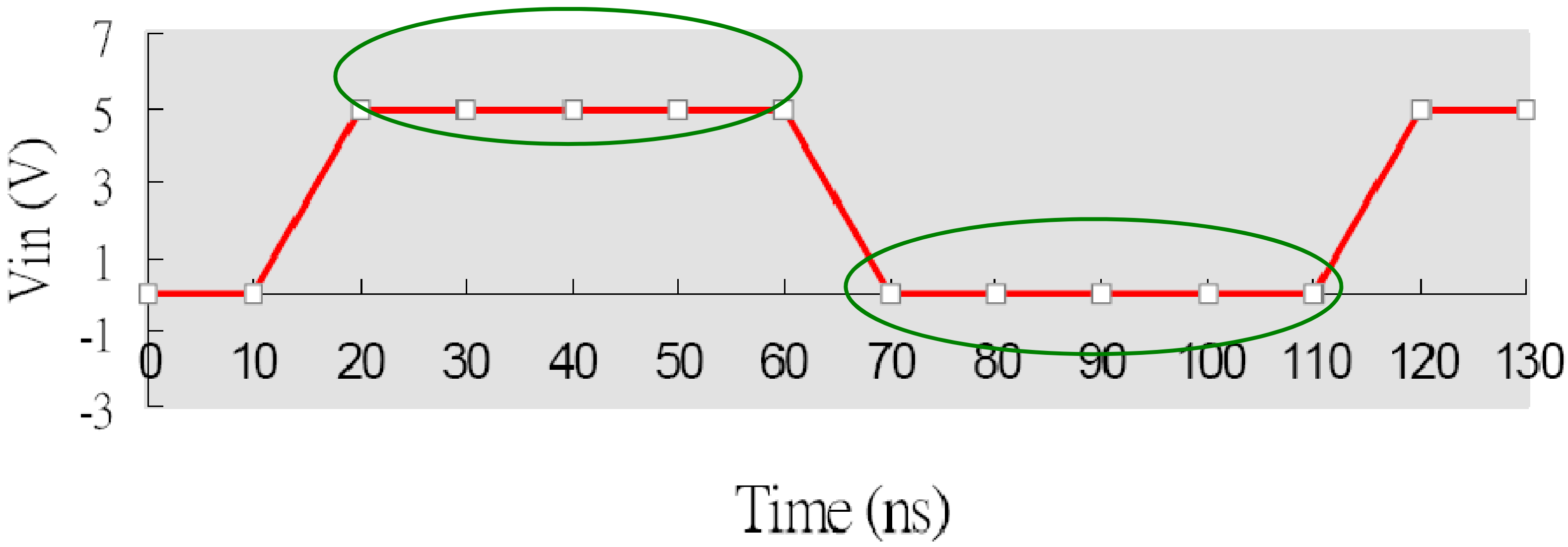
- ★ **Pulse (PULSE Function)**
- ★ **Sinusoidal (SIN Function)**
- **Exponential (EXP Function)**
- ★ **Piecewise Linear (PWL Function)**
- **Single-Frequency FM (SFFM Function)**
- **Single-Frequency AM (AM Function)**

PULSE

- **PULSE** (Periodic Waveform)

  PULSE (V1 V2 td tr tf pw per)

PULSE (0V 5V 10ns 10ns10ns 40ns 100ns)

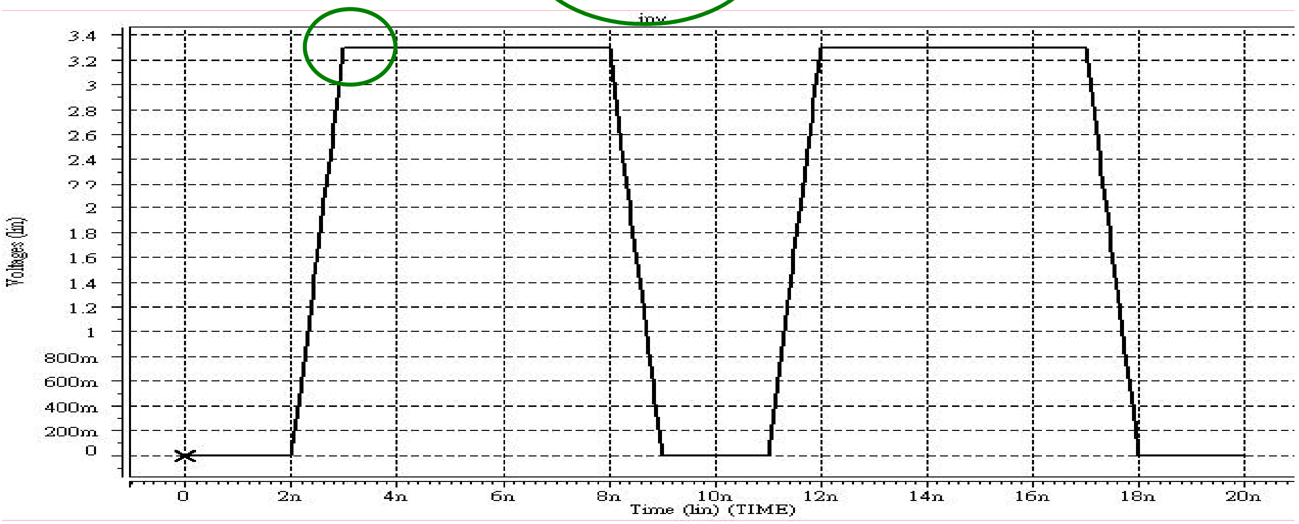


PWL

- **PWL** (Piece Wise Linear Waveform)

PWL (t1 V1 t2 V2 t3 V3 … R)

PWL (1n 0v 2n 0v 3n 3.3v 8n 3.3v 9n 0v R 0)

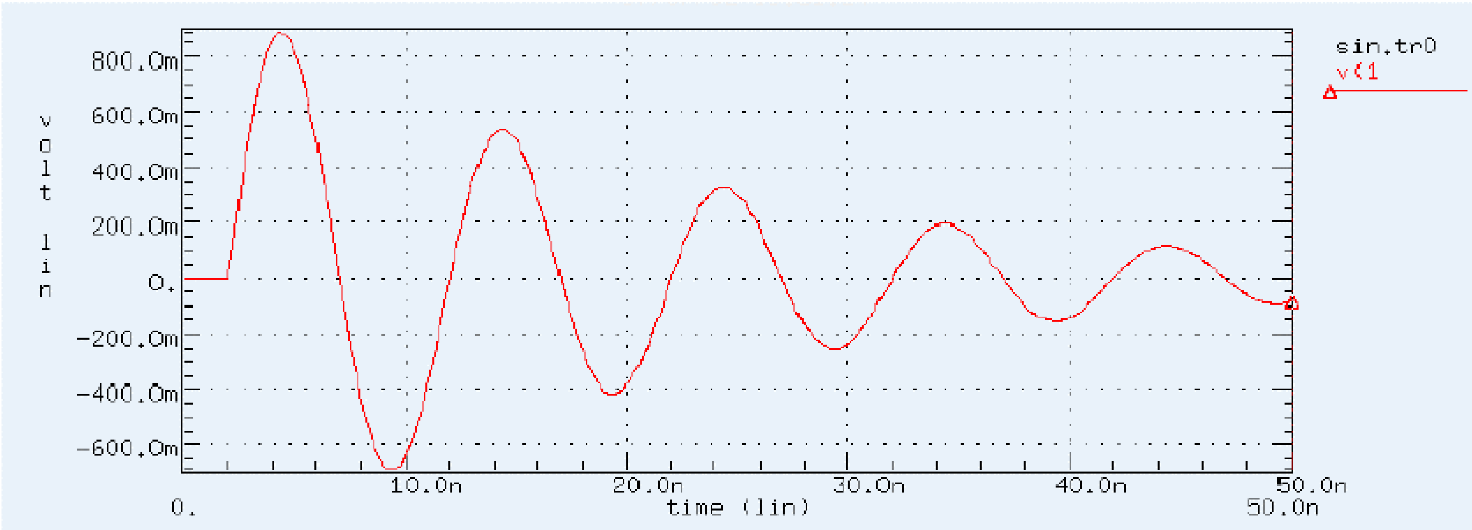


SIN

- **SIN** (Sinusoidal Waveform)

SIN (Voffset Vacmag < Freq Tdelay Dfactor >)

Vin 3 0 SIN (0V 1V 100Meg 2ns 5e7)



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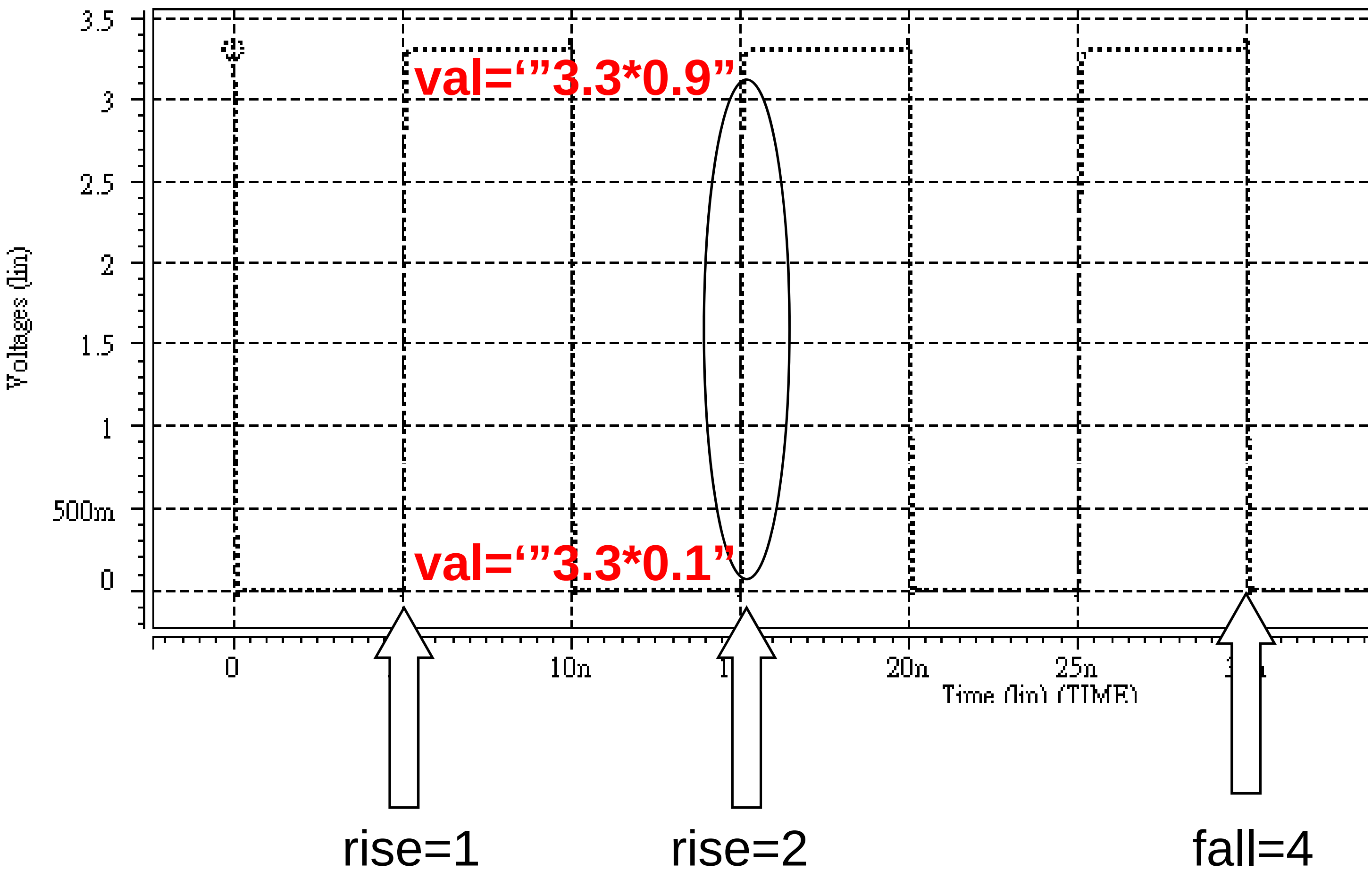
Timing Measurement

.meas tran Tr trig v(out) val="3.3*0.1" rise=2 targ v(out) val='"3.3*0.9" rise=2



Example

SP檔

inv - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
***** inv *****
.global vdd vss
.subckt inv in out
MM0 out in vdd vdd pch w=3u l=350n
MM1 out in vss vss nch w=1u l=350n
.ENDS
.protect
.lib 'mm0355v.l' TT
.unprotect
vdd vdd 0 3.3
vss vss 0 0
vin in 0 pulse(0 3.3 0n .1n .1n 4.9n 10n)
x1 in out inv
.op
.options post
.tran 0.1n 50n
.meas tran Tr trig v(out) val="3.3*0.1" rise=2
+ targ v(out) val="3.3*0.9" rise=2
.end
```

Simulate

mt0檔

inv - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)

```
$DATA1 SOURCE='HSPICE' VERSION='X-2005.09       '
.TITLE '***** inv *****'
tr               temper          alter#
 6.738e-11        25.0000          1.0000
```

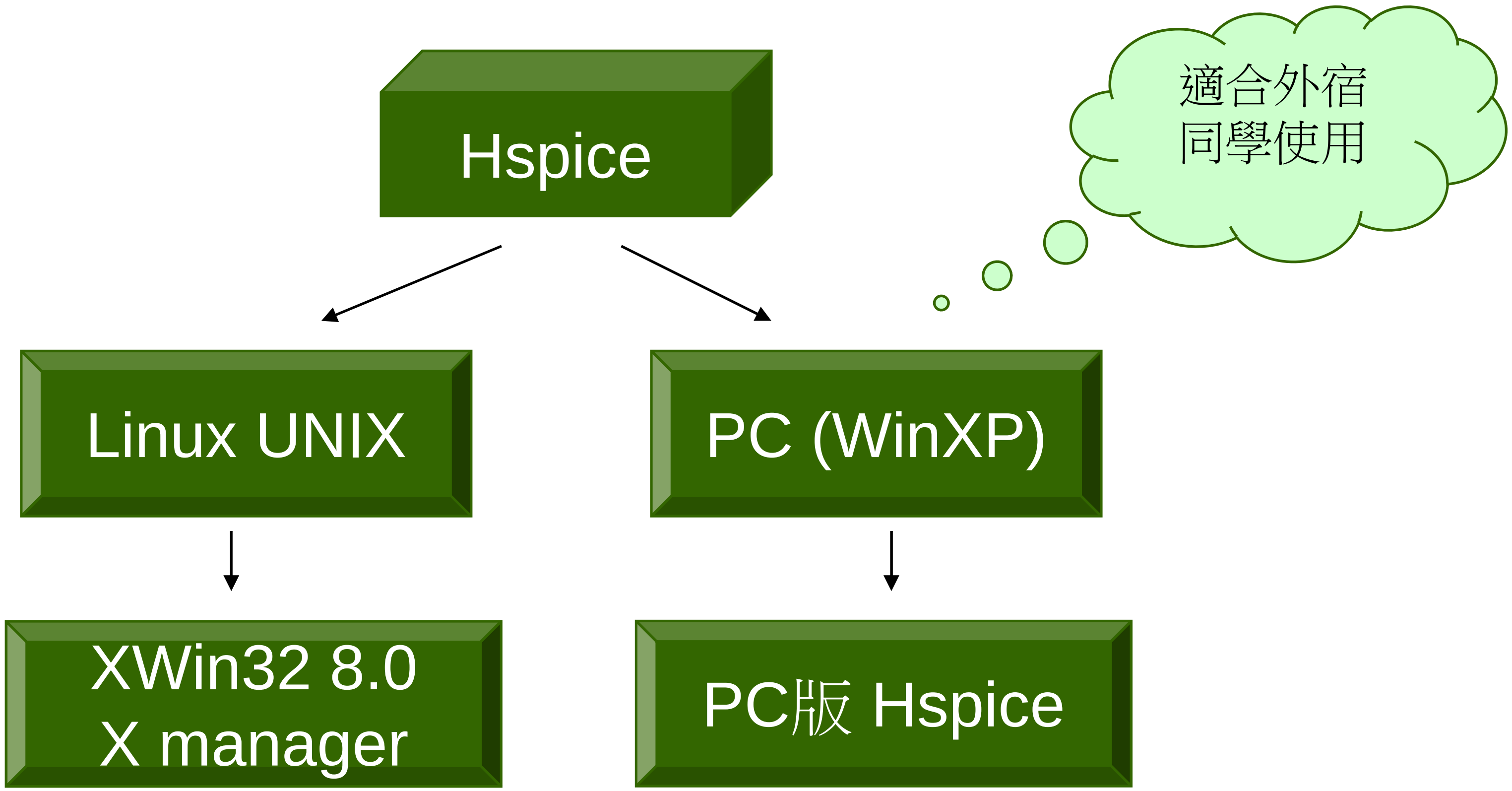
Tr=6.738e-11 s

Power

- Command :
- .meas tran pwr avg power
  - 在暫態分析中，量測整個電路的平均功率消耗
  - 結果顯示在*.mt0檔

Contents

Appendix


Hspice
適合外宿
同學使用
Linux UNIX
PC (WinXP)
XWin32 8.0
X manager
PC版 Hspice