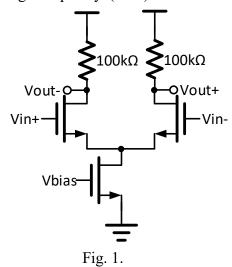
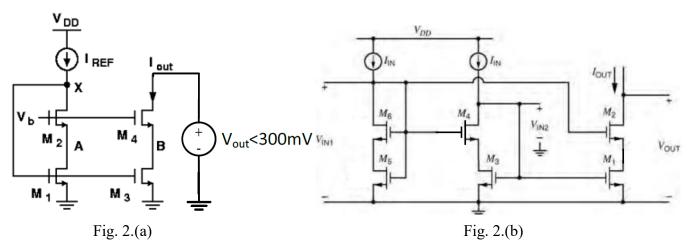
- 1. Use composer and hsipce to simulate the differential pair as shown at Fig. 1 with Vdd=1.8V. (40%)
  - (a) Design a differential pair with gain  $A_{DM(differential\ to\ differential)} > 4$  and  $A_{CM(in\ common\ -\ out\ common)} < 0.05$  for both input common mode voltage = 0.6 and 1.8. (20%)

due date: 05/08/2017

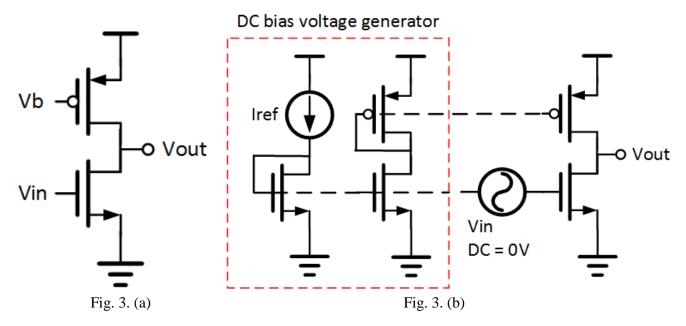
- (b) Simulate the frequency response of A<sub>DM</sub> when input common mode voltage=0.9, and base on the simulation parameter of .lis file to calculate dominant pole. (10%)
- (c) Simulate the frequency response of  $A_{CM}$  when input common mode voltage=0.9, and identify what makes the  $A_{cm}$  deteriorate at the high frequency. (10%)



- 2. Design a 1:6 wide-swing cascade current source as shown in Fig. 2(a). (40%)
  - (a) With  $I_{ref}$ =20uA ( $I_{out}$ =120uA), design the W/L sizes of  $M_1$ ~ $M_4$ , and the dc bias  $V_b$  to get Rout>500k $\Omega$  when Vout=300mV. (20%)
  - (b) Use the circuit structure as shown in Fig. 2(b) as a reference to design a bias generation circuit of Vb with I<sub>in</sub>=20uA(I<sub>out</sub>=120uA). State the M5's and M6's (Fig. 2. (b)) design strategy and show in hand calculation. And express Vin1, Vin2, and Vout in terms of Vov and Vth. (20%)



- 3. Design a common-source amplifier with Vdd=1.5V as shown in Fig. 3. (20%)
  - (a) Design the W/L sizes and Vb as shown in Fig. 3.(a) to get voltage gain Av=Vout/Vin>80. (5%)
  - (b) Keep everything the same and simulate the gain under the SF and FS corner.
  - (c) Design the W/L sizes and Iref as shown in Fig. 3.(b) to get voltage gain Av=Vout/Vin>80 for all corners. (5%)
  - (d) Comment on the differences between (b) and (c). (10%)



The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.