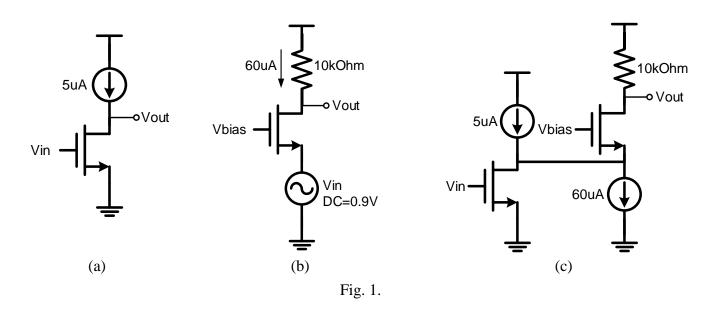
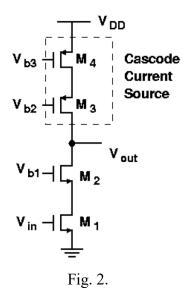
2018 Analog IC Design Homework 2

- 1. Use composer and HSPICE to simulate the circuits in Fig. 1 (ideal current source) with $V_{DD}=1.8V$ and do the calculation. (40%)
 - (a) Design a common source stage with gain A1 >100 and **output DC voltage=0.9 (static current=5uA)** as shown at Fig. 1(a). (5%)
 - (b) Base on the simulation parameter of .lis file to calculate gain of (a) and comment. (5%)
 - (c) Design a common gate stage with gain A2>8 and input DC voltage=0.9 (static current=60uA) as shown at Fig. 1(b). (5%)
 - (d) Base on the simulation parameter of .lis file to calculate gain of (c) and comment. (5%)
 - (e) Connect two stage and add additional 60uA current source as shown in Fig. 1(c). Does the DC bias stay the same? The overall gain equals to A1×A2 or not? If not, why? (20%)

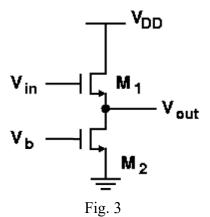


- 2. Design a common-source amplifier with cascaded loading as shown in Fig. 2. (30%)
 - (a) With V_{DD}=1.8V and Ibias=15uA, design the W/L sizes of M1~M4, the DC bias to get voltage gain Av=Vout/Vin>45dB and Vout-swing>1V. (20%)
 - (b) Keep W/L as the same and double all of m (finger) in (a), check the differences of bias current, voltage gain and output swing and make a comment. (10%)



- 3. Design a source-follower amplifier with $V_{DD}=1.8V$ as shown in Fig. 3. (30%)
 - (a) Design the W/L sizes and Vb (body-source M1 CANNOT be connected together) to get voltage gain Av=Vout/Vin>0.8 for Vin DC voltage from 0.5V to 1.8V. (10%)
 - (b) Assume that the deep-N-well is available (body-source M1 can be connected together.) Design the W/L sizes and Vb to get voltage gain Av=Vout/Vin>0.96 for Vin DC voltage from 0.5V to 1.8V. (10%)
 - (c) Comment on the differences between (a) and (b). (10%)

3.



The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file
(c) waveform with cursor values (d) comments.

by CCHsieh

source-follower amplifier的gain<1, 所以這題是要調控Vb和W/L使得Vin在0.5V~1.8V時都能產生>0.96的gain。 方法:由於Vin在低壓時易使M2進入triode region,所以要使M2的over-drive voltage調小 -->Vb壓低,使Vov變小,調整W/L(size)