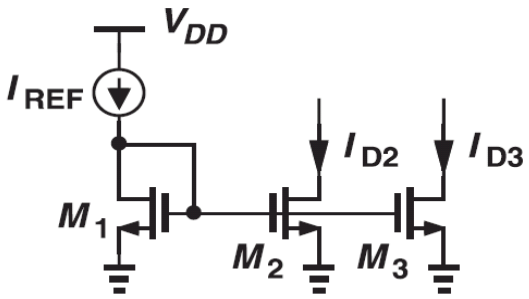
CHAPTER 11

Bandgap References

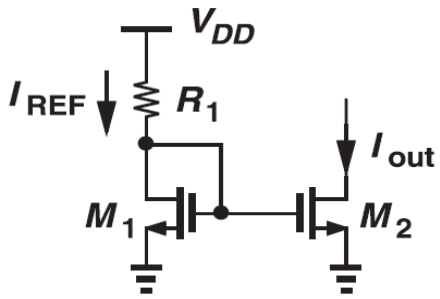
Outline

1. **General Consideration**
2. Supply-Independent Biasing
3. Temperature-Independent Reference
4. PTAT Current Generation / Constant-Gm Biasing
5. Speed and Noise Issue / Case Study

Reference Generator



(a)



(b)

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$

- To establish a DC voltage or current that is ***independent of the supply and process*** and has a well-defined behavior with ***temperature***.
- The required temperature dependence assumes one of three forms
  - Proportional to absolute temperature (PTAT)
  - Constant - G_m behavior
  - Temperature Independent.
- The output current of the circuit is quite sensitive to V_{DD}.

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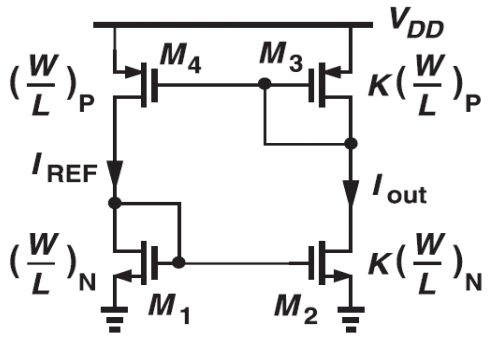
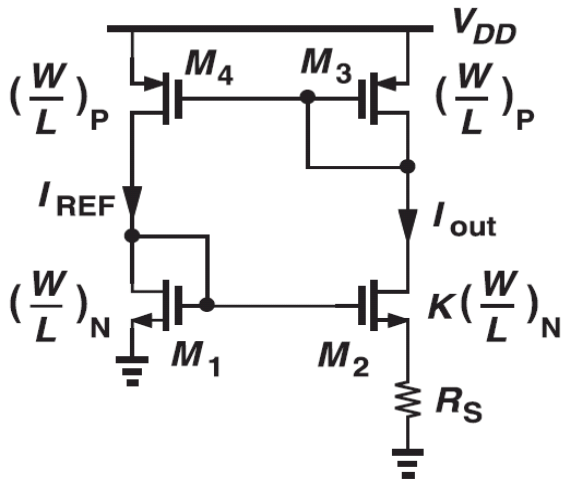
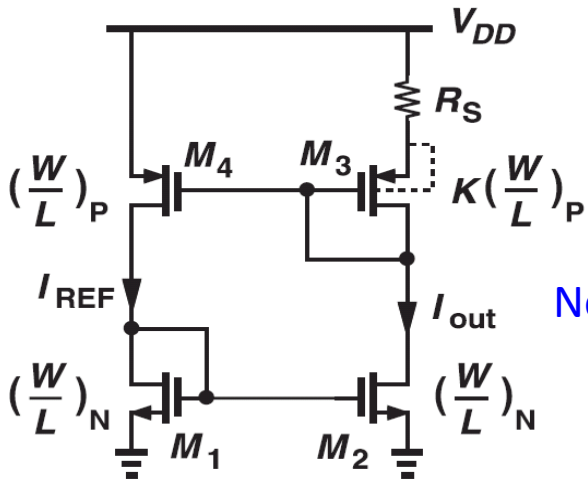
Self-biased Circuit

- **Self-biased circuit** : Supply Independent Biasing
- If M_1-M_4 operate in saturation and $\lambda = 0$, then $I_{out} = K I_{REF}$
- The current levels in the left and right branches become indefinitely.



Supply Independent Current Generator





No body effect

$$I_{out} = I_{REF}, \quad V_{GS1} = V_{GS2} + I_{D2}R_S, \quad \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K (W/L)_N}} + V_{TH2} + I_{out}R_S$$

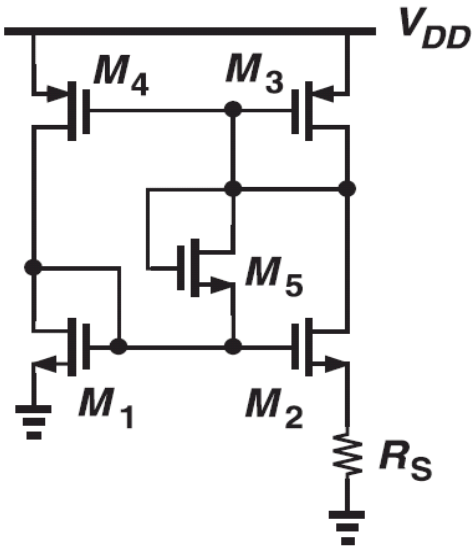
$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1-\frac{1}{\sqrt{K}}\right) = I_{out}R_S, \quad I_{out} = \frac{2}{\mu_n C_{ox} K (W/L)_N}\cdot\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \Longrightarrow \text{independent of } V_{DD}$$

- Use R_S to determine the output current.
- The current is independent of the supply voltage, but still a function of process and temperature.
- The corresponding G_m **is a constant (depending on** R_s **and** K **)**.
- Long channels are used for all of the transistors in the circuit.

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_D} = \frac{2}{R_S}\left(1-\frac{1}{\sqrt{K}}\right)$$

Start-Up Circuit

- If all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely.
  - The circuit can settle in one of two different operation conditions.



- A start-up circuit is required.
  - A mechanism that drives the circuit out of the degenerate bias point when the supply is turned on.
  - M_3 and M_1, and hence M_2 and M_4 cannot remain off.
  - M5 remains off after start up.
  - This technique is practical only if

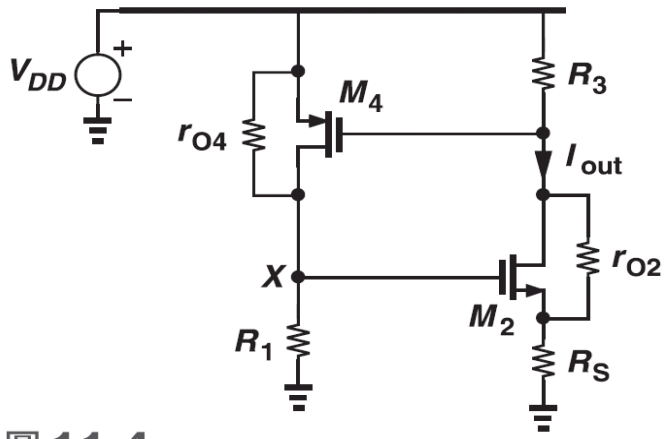
$$V_{TH1} + V_{TH5} + V_{TH3} < V_{DD} \Longrightarrow M_5 \text{ "ON" at start up}$$
$$V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD} \Longrightarrow M_5 \text{ "OFF" after start up}$$

dI_{out}/dV_{DD} with $\lambda \neq 0$

- Assume, $\lambda \neq 0$, estimate the change in I_{out} for a small change ΔV_{DD} in the supply voltage
- Let $R_1 = r_{O1} || (1/g_{m1})$, $R_3 = r_{O3} || (1/g_{m3})$, we have

$$\frac{V_{DD} - V_X}{r_{O4}} + I_{out} R_3 g_{m4} = \frac{V_X}{R_1}, \quad G_{m2} = \frac{I_{out}}{V_X}$$

$$\frac{I_{out}}{V_{DD}} = \frac{1}{r_{O4}} \left[\frac{1}{G_{m2}(r_{O4} \| R_1)} - g_{m4} R_3 \right]^{-1}$$



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- Where $G_{m2} = \dfrac{g_{m2} r_{O2}}{R_S + r_{O2} + (g_{m2} + g_{mb2}) R_S r_{O2}}$
- *If* $r_{O4} = \infty$ $\quad \dfrac{\Delta I_{out}}{\Delta V_{DD}} \approx 0$

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Temperature Independent References

- If a reference is temperature independent, then it is usually process-independent as well.
- If two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a zero TC.
- To obtain a reference voltage V_{REF} with zero TC: $V_{REF} = \alpha_1 V_1 + \alpha_2 V_2 \Rightarrow \alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0$
- Negative TC voltage
  - The forward voltage of a PN-junction diode exhibits a negative TC.

$$I_C = I_S \exp\frac{V_{BE}}{V_T},\ V_T = \frac{kT}{q},\ \mu \propto \mu_0 T^m,\ m \approx -3/2,\ n_i^2 \propto T^3 \exp\left[-E_g/(kT)\right]$$

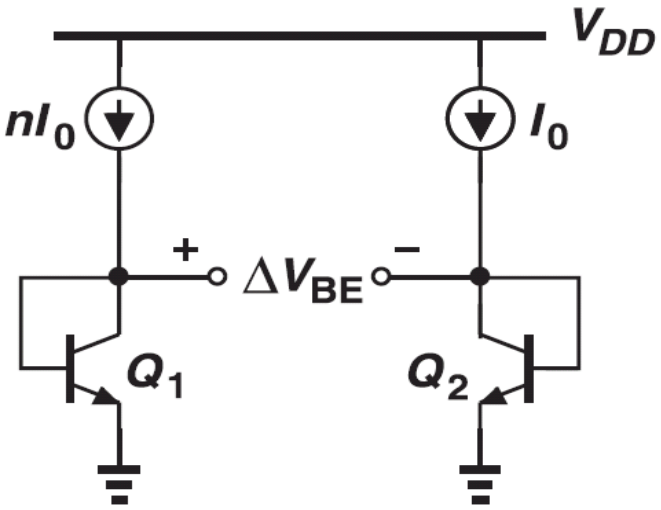
$$E_g \approx 1.12eV \quad \text{Bandgap energy},\ I_S \propto \mu kT n_i^2 = bT^{4+m}\exp\frac{-E_g}{kT},\ \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m}\exp\frac{-E_g}{kT} + bT^{4+m}\left(\exp\frac{-E_g}{kT}\right)\left(\frac{E_g}{kT^2}\right),\ \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

  - For $V_{BE} \approx 750mV, \partial V_{BE}/\partial T \approx -1.5mV/^oK$

Generation of Positive-TC Voltage



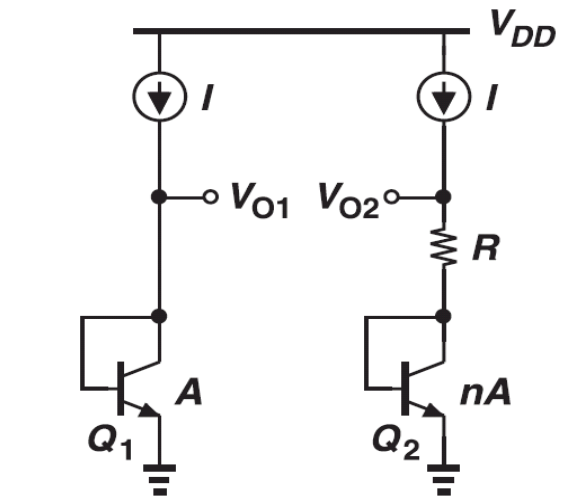
- If two identical transistors ($I_{S1} = I_{S2}$) are biased at collector currents of $nI_o = I_o$, and their base current are negligible

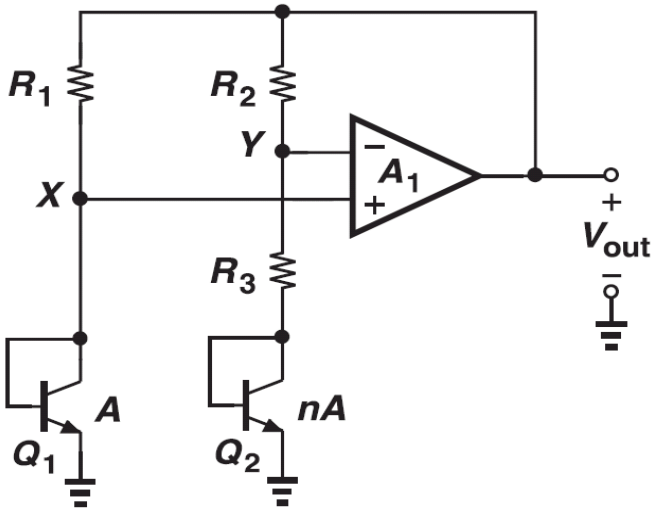
$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} = V_T \ln n$$

- Thus, V_{BE} difference exhibits a positive temperature coefficient (*Proportional To Absolute Temperature : PTAT*)

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n$$

Bandgap Reference





$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$$

$$\frac{\partial \Delta V_{BE}}{\partial T} \approx -1.5mV / {}^oK, \quad \frac{\partial V_T}{\partial T} \approx 0.087mV / {}^oK$$

$$\alpha_1 = 1, \qquad \alpha_2 \ln n (0.087mV / {}^oK) = 1.5mV / {}^oK$$

- We have

$$\alpha_2 \ln n \approx 17.2, \qquad V_{REF} \approx V_{BE} + 17.2 V_T \approx 1.25V$$

- Force V_{o1} and V_{o2} to be equal

$$V_{BE1} = RI + V_{BE2}, \qquad RI = V_{BE1} - V_{BE2} = V_T \ln n$$

$$RI = V_{BE1} - V_{BE2} = V_T \ln n, \qquad V_{O2} = V_{BE2} + V_T \ln n$$

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) = V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right)$$

- For a zero TC, we must have

$$\left(1 + \frac{R_2}{R_3}\right) \ln n \approx 17.2, \quad \text{e.g., we may choose } n = 31 \text{ and } \frac{R_2}{R_3} = 4$$

Collector Current Variation

$$\frac{\partial V_{BE}}{\partial T} \approx -1.5mV/^{o}K \quad \text{for a constant current}$$

But, the collector currents of Q_1 and Q_2 are proportional to V_T

$$I_{C1} = I_{C2} \approx (V_T \ln n)/R_3, \quad \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + V_T\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}\right)$$

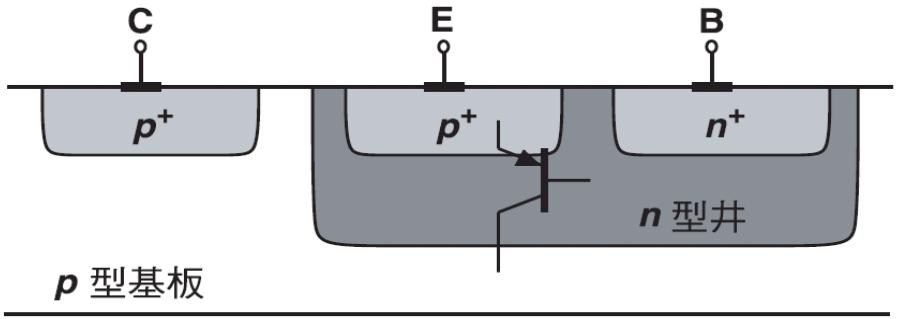
Since $\partial I_C/\partial T \approx (V_T \ln n)/(R_3 T) = I_C/T$, we have

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + V_T\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}\right) \Rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + \frac{V_T}{T} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

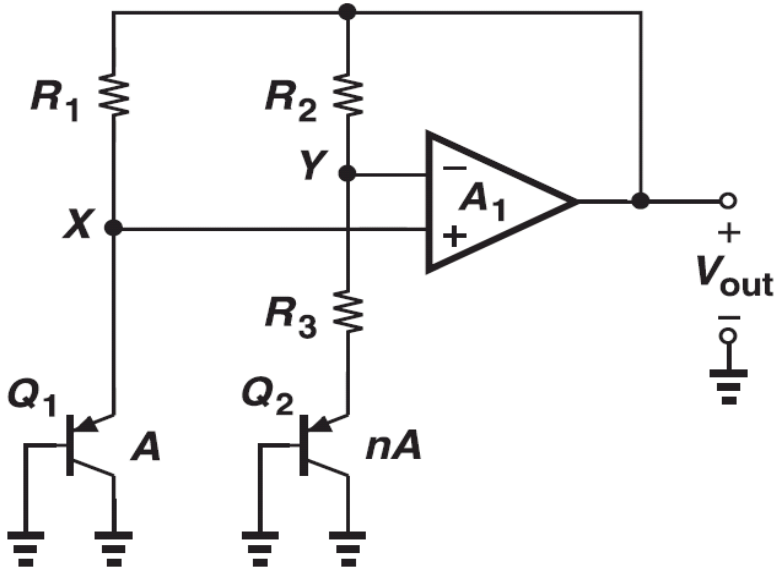
$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T} \quad \textit{compared to} \quad \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Thus the TC is slightly less negative than $-1.5mV/^{o}K$

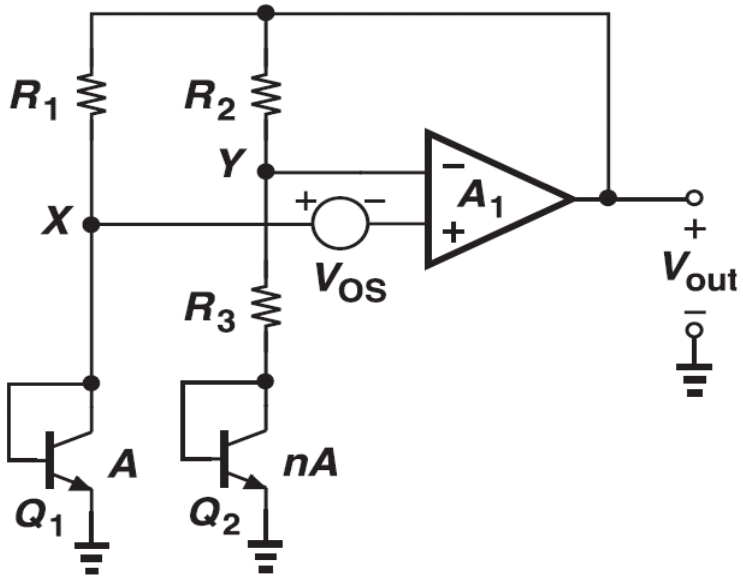
Compatibility with CMOS Technology



A *pnp* transistor can be formed as p+/n-well/p-sub



Op Amp Offset and Output Impedance



$$V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_{C2}$$

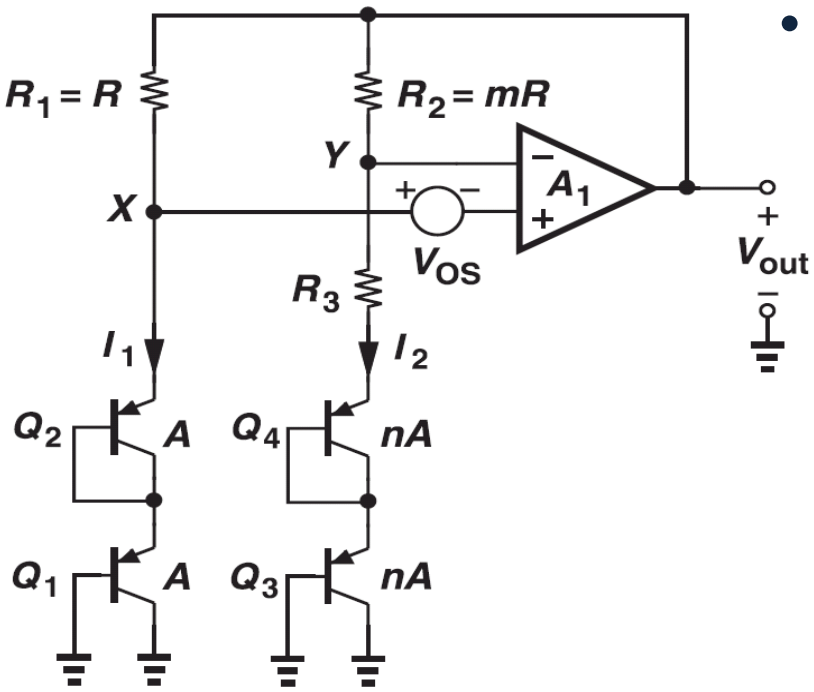
$$V_{out} = V_{BE2} + (R_3 + R_2) I_{C2}$$

$$V_{out} = V_{BE2} + (R_3 + R_2)\frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3}$$

$$= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln n - V_{OS})$$

- V_{os} is amplified by $1+R_2/R_3$
- V_{os} itself varies with temperature, raising the temperature coefficient of the output voltage.

Reduce Effect of OP AMP Offset



- To lower the effect of V_{os}
  - Large devices in a carefully chosen topology so as to minimize the offset.
  - The collector currents of Q1 and Q2 can be ratioed by a factor of *m* such that (by R_1 and R_2)

$$\Delta V_{BE} = V_T \ln(mn)$$

  - Use two pn junction in series to double ΔV_{BE}

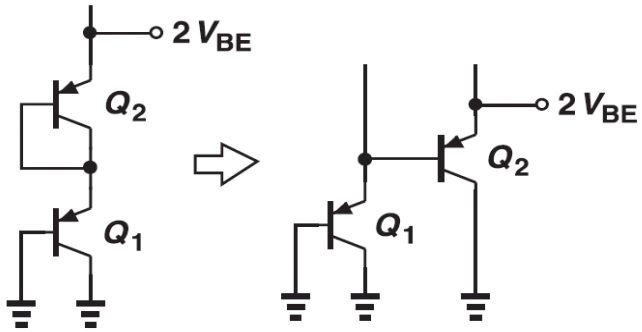
$$V_{BE1} + V_{BE2} - V_{OS} = V_{BE3} + V_{BE4} + R_3 I_2$$

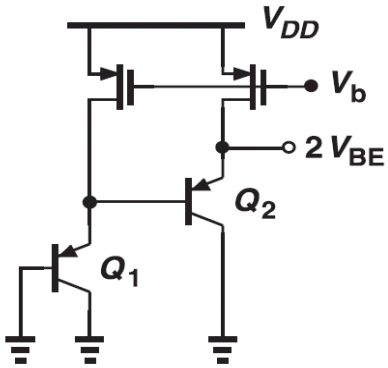
$$V_{out} = V_{BE3} + V_{BE4} + (R_3 + R_2) I_2$$

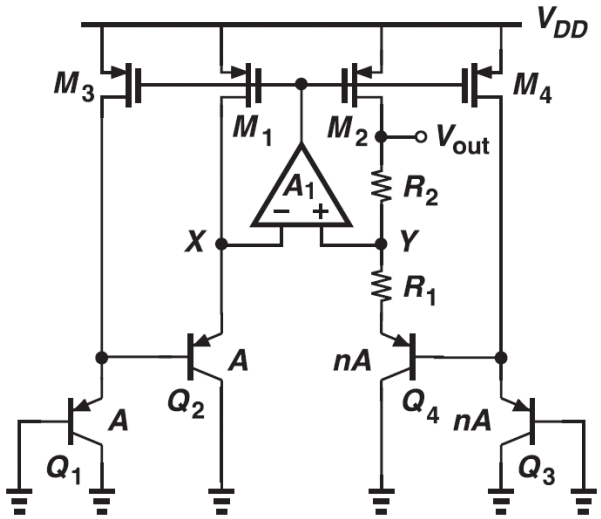
$$V_{out} = V_{BE3} + V_{BE4} + (R_3 + R_2)\frac{2V_T \ln(mn) - V_{OS}}{R_3} = 2V_{BE} + \left(1 + \frac{R_2}{R_3}\right)[2V_T \ln(mn) - V_{OS}] \approx 2 \times 1.25V = 2.5V$$

- Difficult to generate by the op amp at low supply voltage.
- Not feasible in a standard CMOS technology because the collectors of Q2 and Q4 are not grounded.

Topologies with Grounded Collectors







- Must ensure that the bias currents of both transistors have the same behavior with temperature.
  - Bias each transistor with current source.
- The OP amp experiences no resistive loading, but the mismatch and channel length modulation of the PMOS devices induce error at the output.
- The current gain of native *pnp* transistors are low.
  - Generate an error in the emitter current of Q1 and Q3.
  - A means of base current cancellation may be necessary.

Feedback Polarity

- The feedback signal produced by the OP amp returns to both of its input.
- The negative feedback factor is given by

$$\beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_3 + R_2}$$

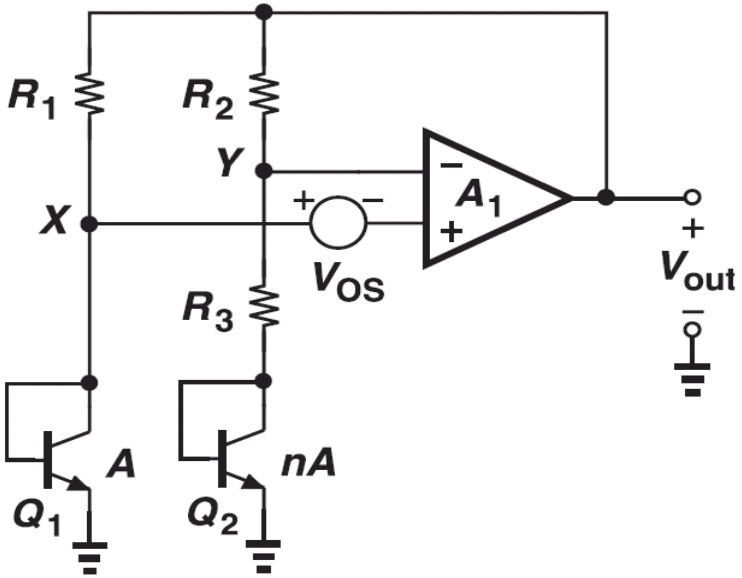
- The positive feedback factor is given by

$$\beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1}$$

- To ensure an overall negative feedback, we must have

$$2\beta_P < \beta_N$$

  - So that the circuits transient response remains well-behaved with large capacitive load



Bandgap Reference

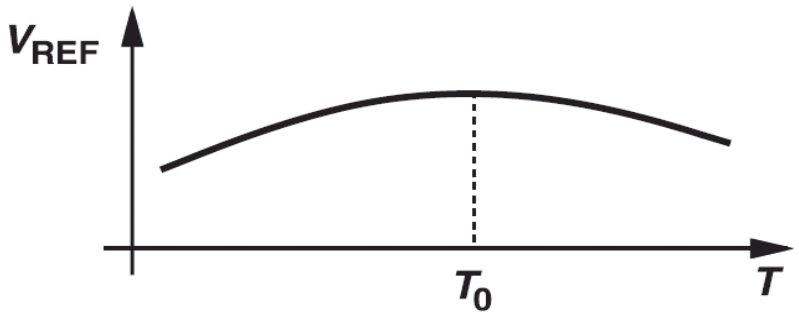
- Since
$$V_{REF} = V_{BE} + V_T \ln n, \quad \frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{V_T}{T} \ln n = 0$$
- We have
$$\frac{V_{BE} - (4+m)V_T - E_g/q}{T} = -\frac{V_T}{T} \ln n, \quad V_{REF} = \frac{E_g}{q} + (4+m)V_T$$
- The reference voltage exhibiting a nominally-zero TC is given by a few fundamental numbers
  - The bandgap voltage of silicon, E_g/q
  - The temperature exponent of mobility, m
  - The thermal voltage, V_T.

$$T \to 0 \Rightarrow V_{REF} \to E_g/q$$

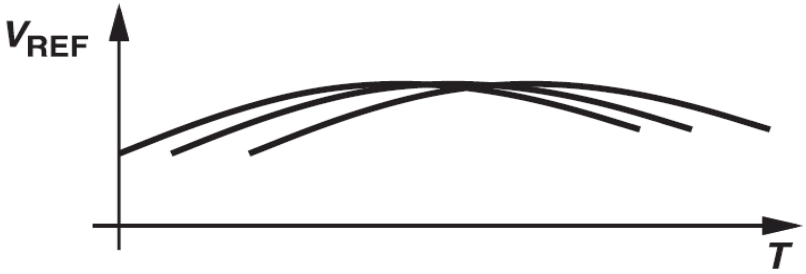
- Supply Dependence and Start-up
  - The output voltage is independent of the supply voltage so long as the open-loop gain of the op amp is sufficiently high.
  - Start-up techniques can be added to ensure the op amp turns on when the supply is applied.
  - The supply rejection of the circuit typically degrades at high frequencies.

Curvature Correction

- Bandgap voltages exhibit a finite curvature
  - Their TC is typically zero at one temperature and positive or negative at other temperature.
  - The curvature arises from temperature variation of base emitter voltages, collector currents, and offset voltages.



- Due to large offsets and process variations, samples of a bandgap reference display substantially different zero-TC temperatures.



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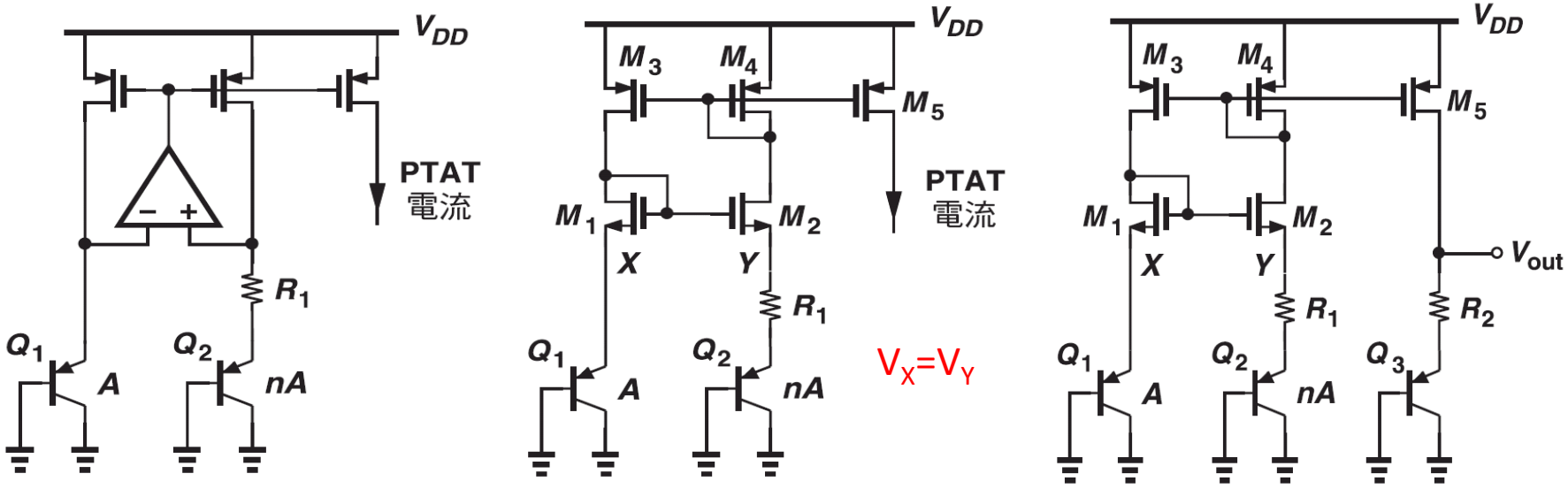
PTAT Current Generation



- Assume that M1-M2 and M3-M4 are identical pairs

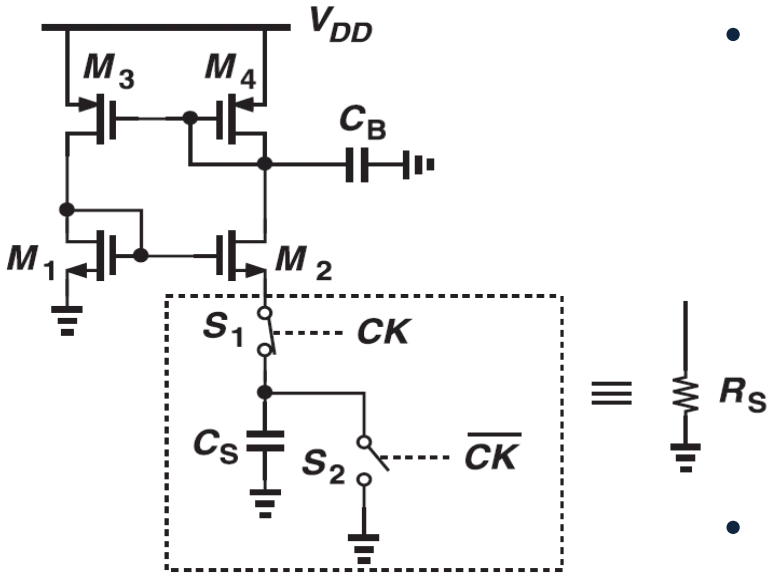
$$For \quad I_{D1} = I_{D2} \Rightarrow V_X = V_Y \Rightarrow I_{D1} = I_{D2} = (V_T \ln n)/R_1$$

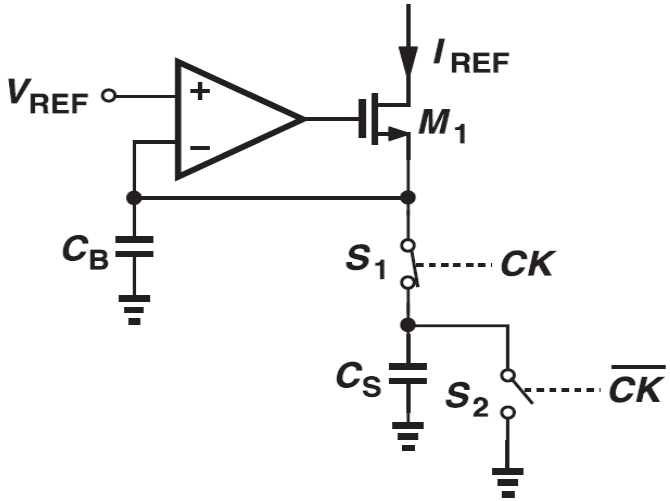
- Due to mismatch between the transistors and the temperature coefficient of R_1, the variation of I_{D5} deviates from the ideal equation.
- Can be readily modified to provide a bandgap reference voltage.

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n$$

- Mismatches of the PMOS devices introduce error in V_{out}.

Constant Gm Biasing





- The transconductance of MOSFETs determine
  - Noise
  - Small signal gain
  - Speed

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_{D1}} = \frac{2}{R_S}\left(1-\frac{1}{\sqrt{K}}\right)$$

- The value of R_s does vary with temperature and process
  - Replace R_S by switched capacitor equivalent

$$R_S = \frac{1}{C_S f_{CK}}$$

- The absolute value of capacitor is typically more tightly controlled and the TC of capacitors is much smaller than that of resistors.
  - V-to-I conversion with high accuracy

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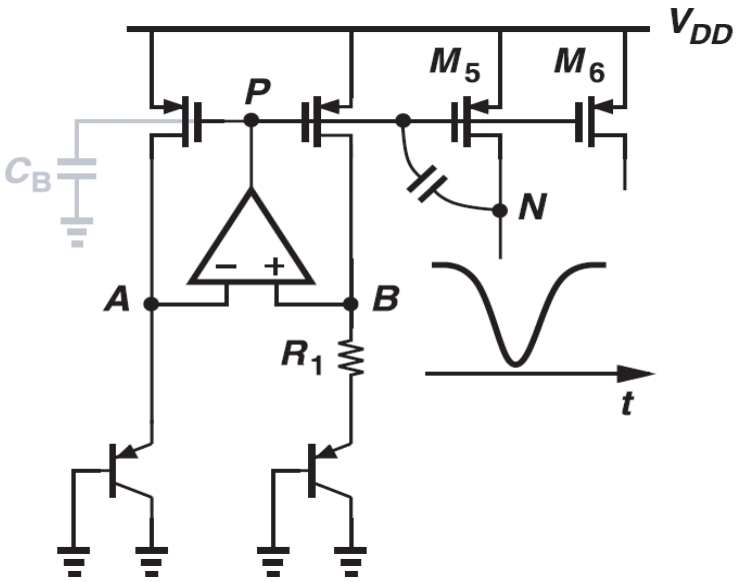
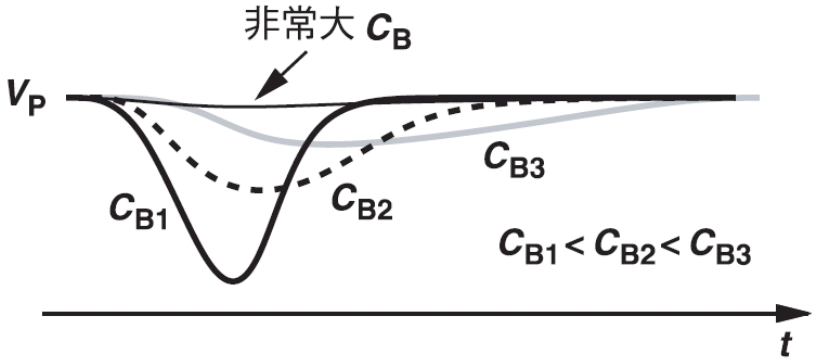
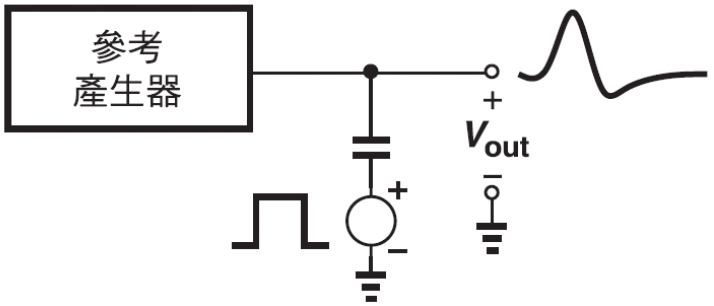
Speed and Noise Issues



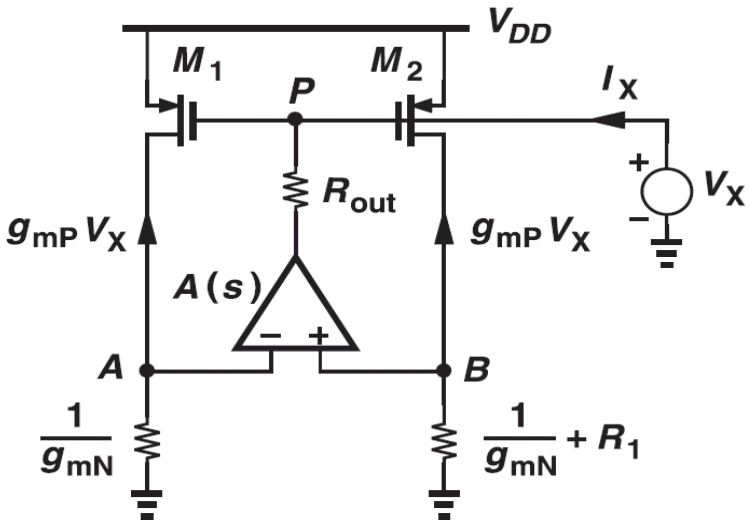
- Assuming the voltage at node N is heavily disturbed by the circuit fed by M_5
  - The OP amp can not maintain Vp, I_{bias} of M_5 & M_6 experience large transient changes.
  - Transient duration of P may be quite long.
  - May require a high-speed OP amp.
- Node *P* can be bypass to ground by C_B.
  - Requiring the op amp to be of one stage nature
  - Applying a disturbance at the output and observing the settling behavior.

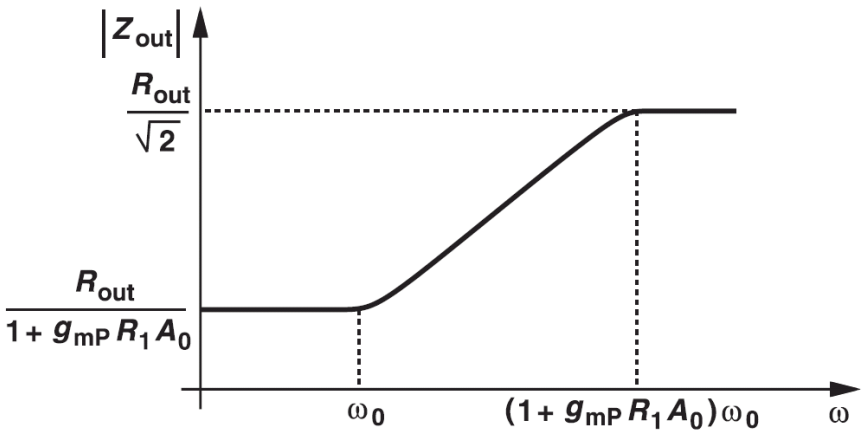




R_{out} of the Bandgap Reference

- Output Impedance of the Bandgap Reference





$$V_{AB} = -g_{mP}V_X\frac{1}{g_{mN}} + g_{mP}V_X\left(\frac{1}{g_{mN}}+R_1\right) = g_{mP}V_XR_1$$

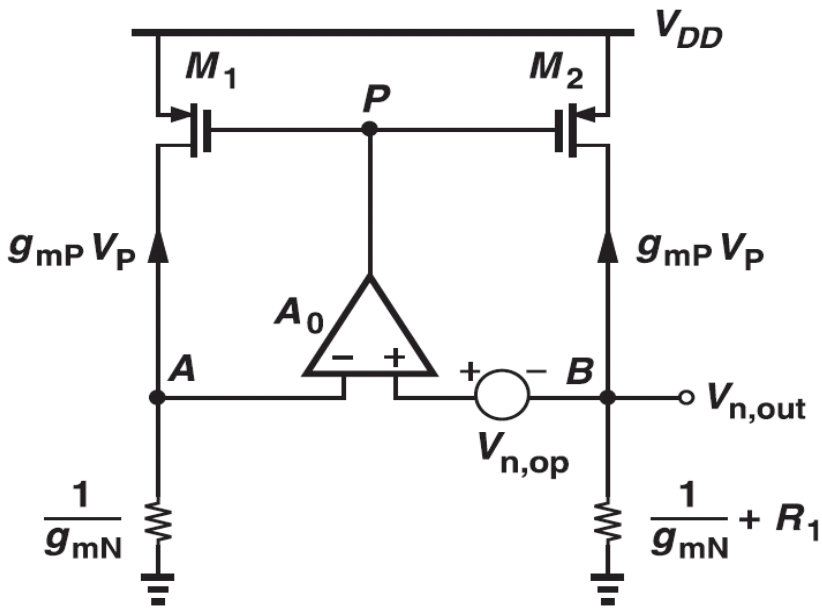
$$I_X = \frac{V_X + g_{mP}V_XR_1A(s)}{R_{out}}$$

$$\frac{V_X}{I_X} = \frac{R_{out}}{1+g_{mP}R_1A(s)} = \frac{R_{out}}{1+g_{mP}R_1\dfrac{A_0}{1+s/\omega_0}}$$

$$= \frac{R_{out}}{1+g_{mP}R_1A_0}\frac{1+\dfrac{s}{\omega_0}}{1+\dfrac{s}{(1+g_{mP}R_1A_0)\omega_0}}$$

$$|Z_{out}| = \frac{R_{out}}{1+g_{mP}R_1A_0}\left|\frac{1+j(1+g_{mP}R_1A_0)}{1+j}\right| = \frac{R_{out}}{\sqrt{2}}$$

Noise in Reference Generator



- Taking into account the input referred noise voltage of the op amp, the small signal drain currents of M1 and M2 are equal to

$$\frac{V_{n,out}}{R_1 + g_{mN}^{-1}}$$

- We have

$$V_p = -\frac{V_{n,out}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mP}}$$

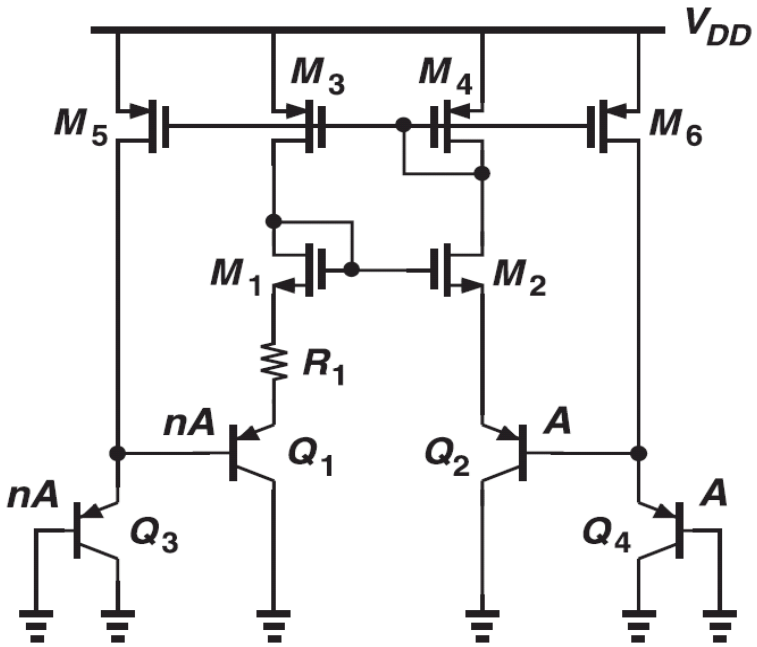
- The differential voltage at the input of the op amp as

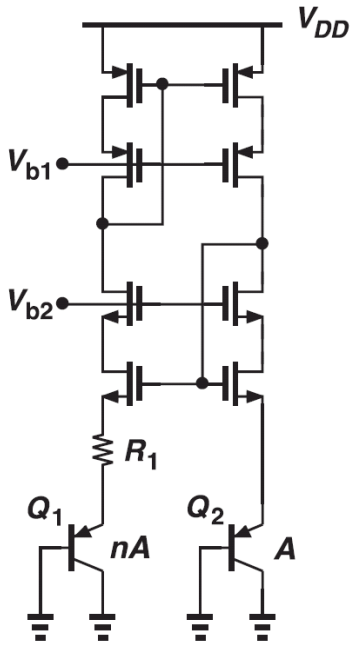
$$-\frac{V_{n,out}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mP}} \cdot \frac{1}{A_0}$$

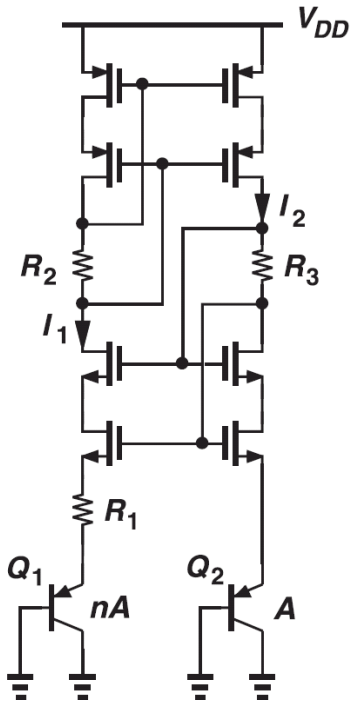
$$\frac{V_{n,out}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mN}} - \frac{V_{n,out}}{g_{mP} A_0 (R_1 + g_{mN}^{-1})} = V_{n,op} + V_{n,out}, \quad V_{n,out}\left[\frac{1}{R_1 + g_{mN}^{-1}}\left(\frac{1}{g_{mN}} - \frac{V_{n,out}}{g_{mP} A_0}\right) - 1\right] = V_{n,op}$$

$$\textit{Typically} \quad g_{mP} A_0 >> g_{mN} >> R_1^{-1} \qquad |V_{n,out}| \approx V_{n,op}$$

Case Study-I







- 2 series B-E voltages in each branch to reduce the effect of MOSFET mismatches.
- PMOS current mirror arrangement ensures equal collector currents for Q1-Q4.
- Use cascode current mirror to resolve channel length modulation.
- Use self-biased cascode to obviate the need for V_{b1} and V_{b2}.
  - R2 and R3 sustain proper voltages to allow all MOSFETS to remain in saturation

Generation of a Floating Ref. Voltage

- M_{11} sets the gate voltage of M9 at $V_{BE4} + V_{GS11}$

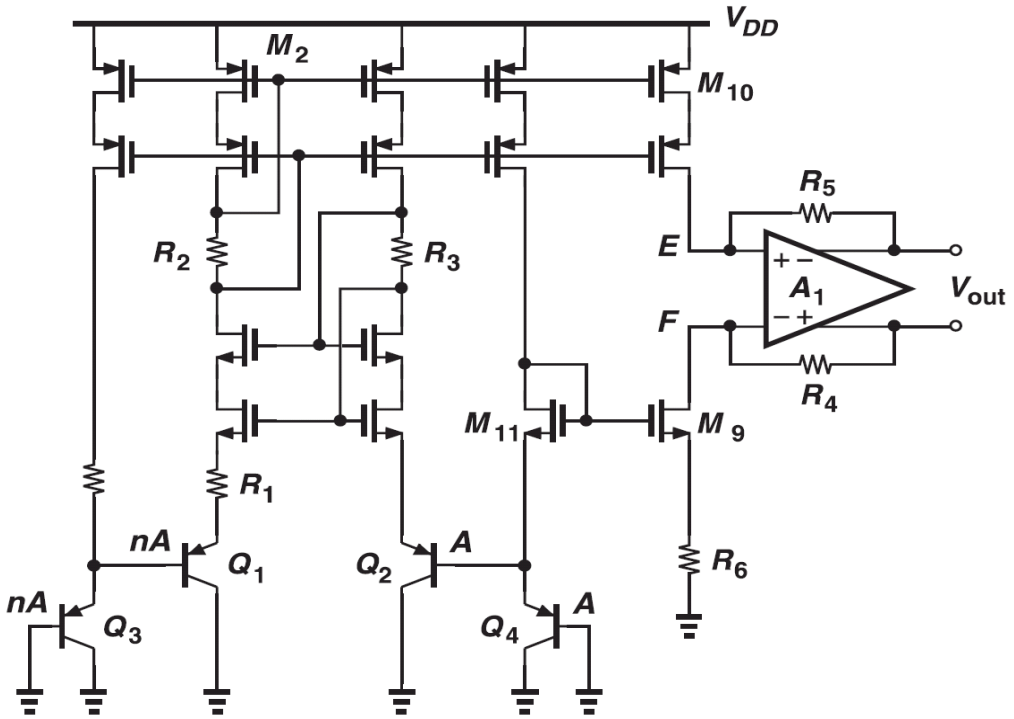
$$I_{D9} = \frac{V_{BE4}}{R_6} \Rightarrow V_{R4} = V_{BE4}\frac{R_4}{R_6}$$

- If M10 is identical to M2

$$|I_{D10}| = 2\frac{V_T \ln n}{R_1} \Rightarrow V_{R5} = 2(V_T \ln n)\frac{R_5}{R_1}$$

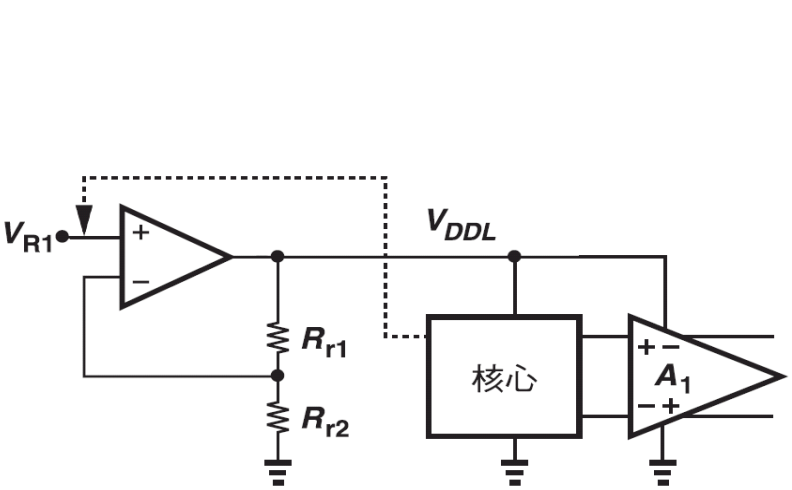
- The OP amp ensures that

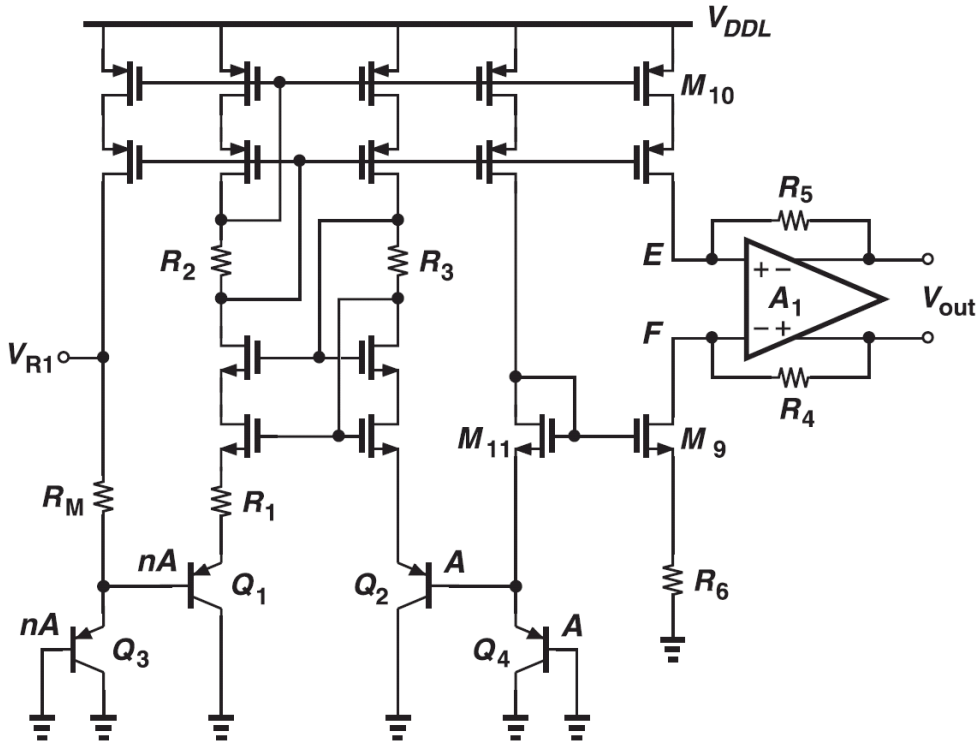
$$V_E \approx V_F \Rightarrow V_{out} = \frac{R_4}{R_6}V_{BE4} + 2\frac{R_5}{R_1}V_T \ln n$$



- This design regulates the supply voltage of the core and the OP amp to enhance the PSRR

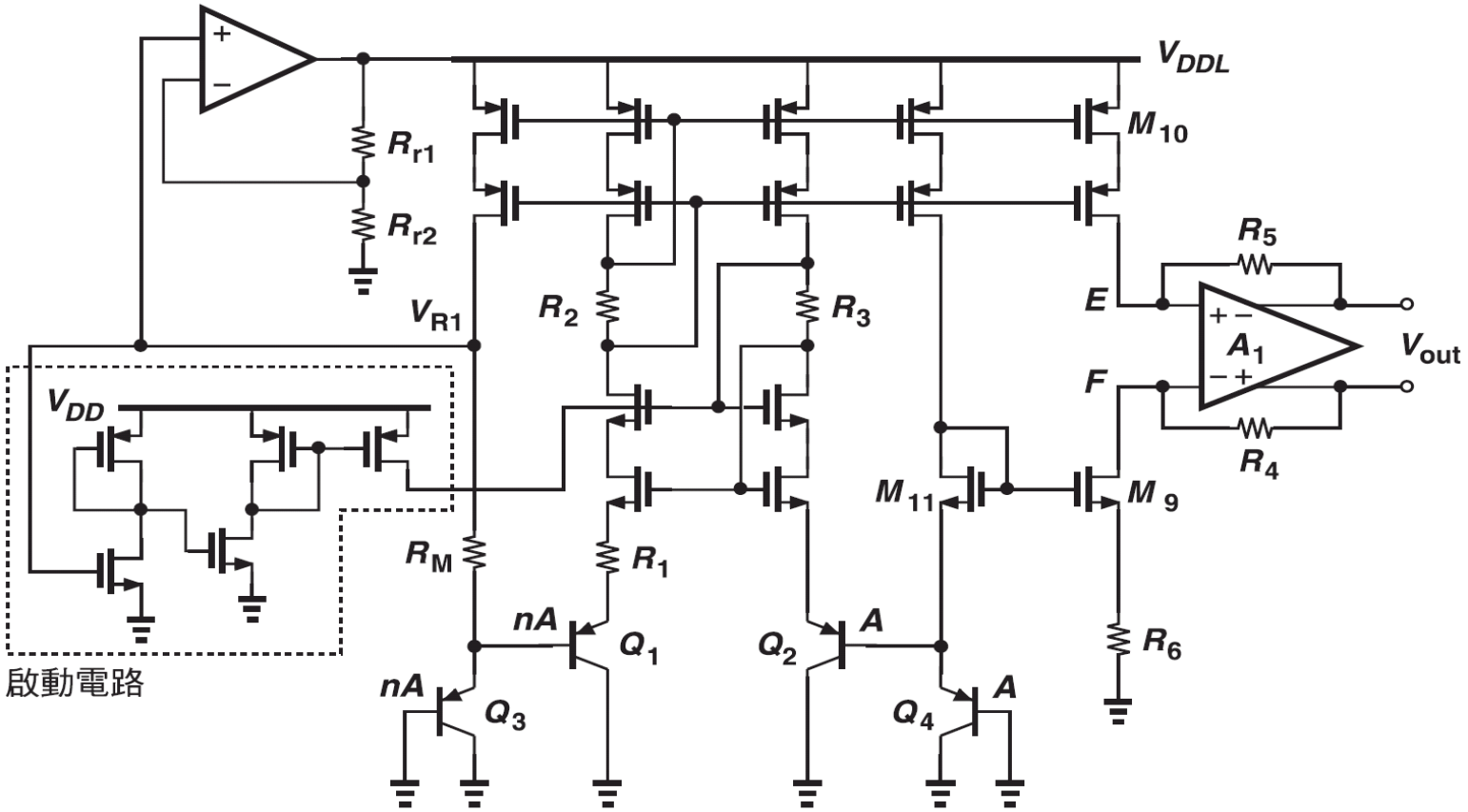
To Improve PSRR





- A local supply V_{DDL} is defined by a reference V_{R1} and the ratio of R_{r1} and R_{r2}.
- To minimize the dependence of V_{R1} upon the supply, this voltage is established inside the core.

Overall Circuit of the Bandgap Gen.



- A start-up circuit is also used.
- Operating from a 5V supply. V_{out} = 2V.
- Supply rejection is 94dB at low frequencies, dropping to 58 dB at 100 kHz.

Bonus Sharing

- 每位企業家都該看的10段YouTube影片
  - http://www.bnext.com.tw/article/view/cid/103/id/18714
- **Steve Jobs Stanford Commencement Speech 2005**
  - http://www.youtube.com/watch?v=D1R-jKKp3NA&feature=player_embedded&hd=1
  - http://stanley5.blogspot.com/2007/01/steve-jobs-stanford-commencement.html
- 求知若飢，虛心若愚（**Stay Hungry, Stay Foolish**）
- 謝謝 大家 這學期 的投入…. **It's a great experience for me..**
  - 記得去按＂**讚！**＂