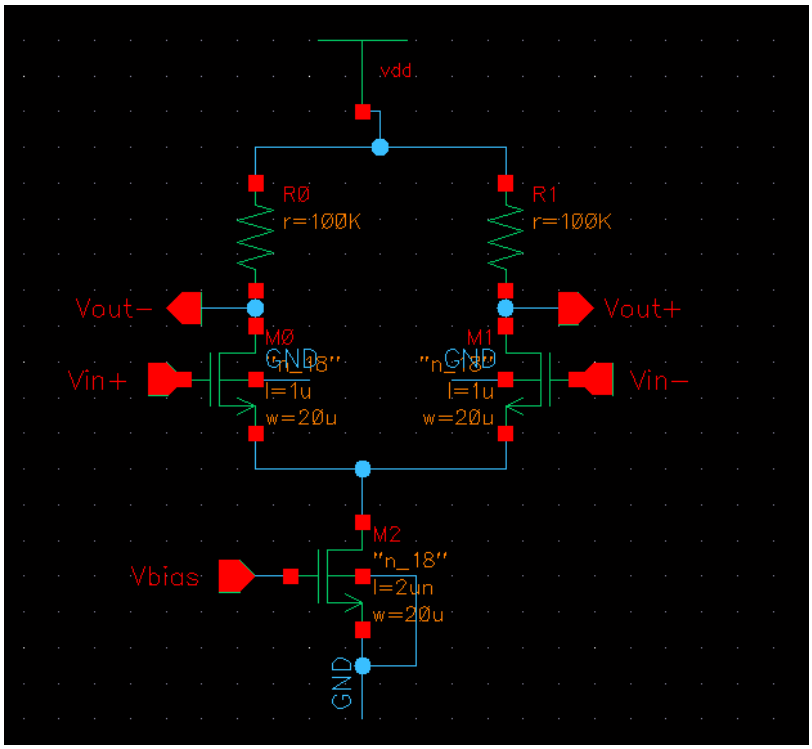
2017 Analog IC Design Homework 3

103061119 陳佳怡

1. (a)



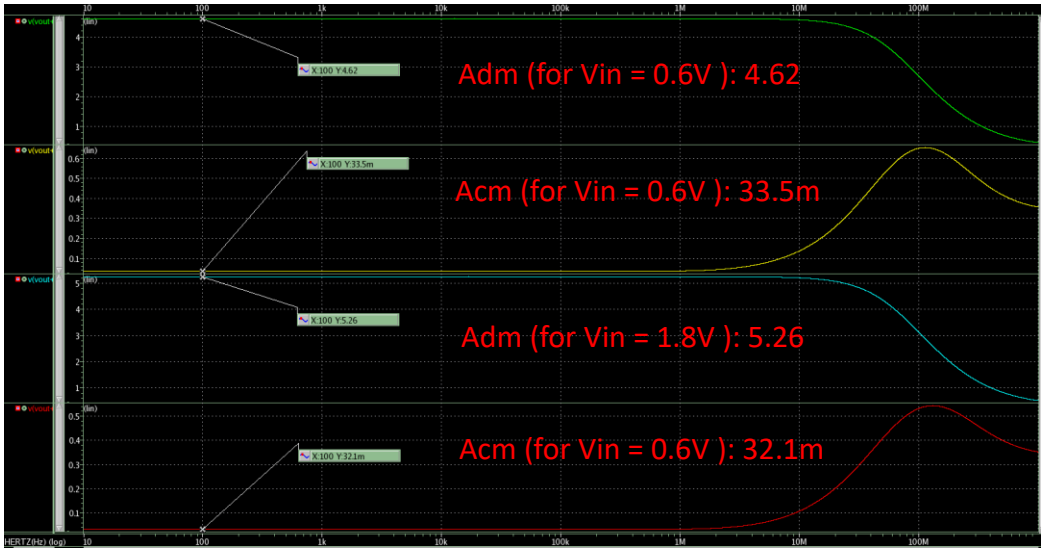
M0 W=20um ; L=1um ; m=1

M1 W=20um ; L=1um ; m=1

M2 W=20um ; L=2um ; m=1

Vb DC=0.362V

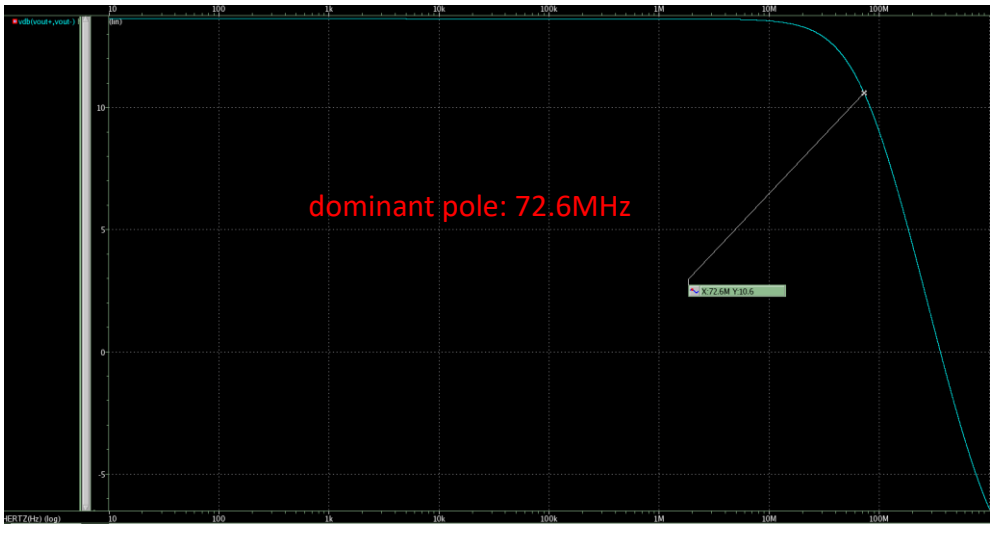
```
hw3_1_a
.protect
.lib 'cic018.l' TT
*.inc 'hw3_1_a.spi'
.temp 25
.unprotect
.option post
.option acout=0

RR1 vdd Vout+ 100K
RR0 vdd Vout- 100K
MM2 net28 Vbias GND GND n_18 W=20u L=2u m=1
MM1 Vout- Vin- net28 GND n_18 W=20u L=1u m=1
MM0 Vout+ Vin+ net28 GND n_18 W=20u L=1u m=1

Vbias Vbias gnd 0.362
Vin- Vin- gnd DC=1.8 AC=0.5 0     $Adm
Vin+ Vin+ gnd DC=1.8 AC=0.5 180   $Adm
*Vin- Vin- gnd DC=0.6 AC=1      $Acm
*Vin+ Vin+ gnd DC=0.6 AC=1      $Acm
Vdd Vdd gnd 1.8

.OP
.AC DEC 10000 10 1G
.probe AC V(Vout+,Vout-)  $Adm
.probe AC V(Vout+)      $Acm

.end
```

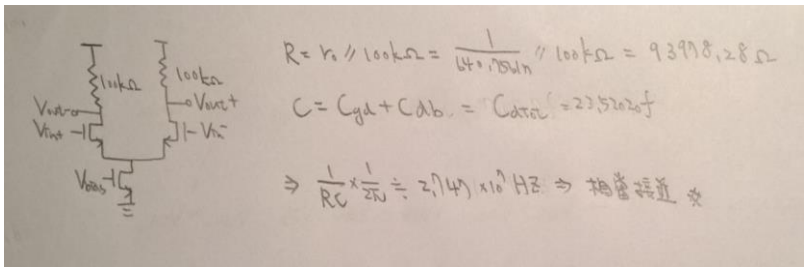


comment:

這次要調變三顆 mos 並測量 Adm 和 Acm，一開始我都讓三顆 mos 的 size 相同，先調 Vbias，發現當 W 變小時，gain 會變小，因為 Adm 和 Acm 皆與 gm 呈正相關，但是後來調很久會發現，如果讓三顆 mos 都維持一樣的 size，那在 Vin=0.6 和 1.8 分別在 Adm 和 Acm 的四種狀況下必有其中一種不合，例如說 Vin=0.6 的 Adm 如果剛好等於 4.5，則 Vin=1.8 時 Acm 必然會超過 0.05，所以我改變了 M2，可能是因為 M2 影響 Rss，所以 M2 不能和 M1 以及 M0 維持相同的大小。

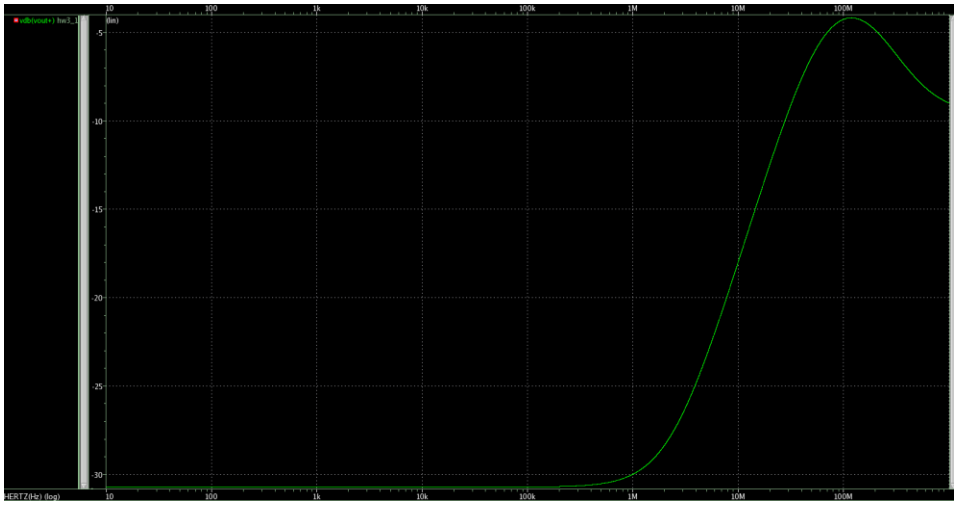
(b)





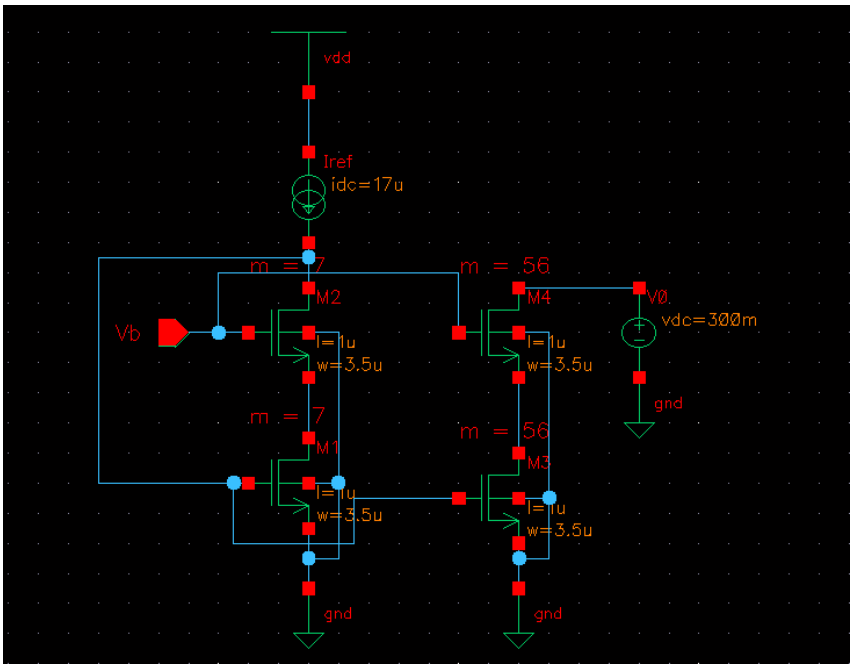
subckt			
element	0:mm2	0:mm1	0:mm0
model	0:n_18.1	0:n_18.1	0:n_18.1
region	Saturati	Cutoff	Cutoff
id	4.0630u	2.0315u	2.0315u
ibs	-6.267e-22	-720.3326a	-720.3326a
ibd	-720.3316a	-2.3684f	-2.3684f
vgs	362.0000m	414.3391m	414.3391m
vds	485.6609m	1.1112	1.1112
vbs	0.	-485.6609m	-485.6609m
vth	348.8654m	469.3900m	469.3900m
vdsat	65.5032m	50.2404m	50.2404m
vod	13.1346m	-55.0509m	-55.0509m
beta	3.0304m	6.2725m	6.2725m
gam eff	507.4459m	519.5784m	519.5784m
gm	85.0243u	51.0913u	51.0913u
gds	686.1149n	640.7561n	640.7561n
gmb	17.6967u	8.0947u	8.0947u
cdtot	27.6281f	23.5202f	23.5202f
cgtot	196.7657f	51.5826f	51.5826f
cstot	190.2710f	40.2953f	40.2953f
cbtot	110.2742f	61.6470f	61.6470f
cgs	151.0918f	19.6154f	19.6154f
cgd	7.2126f	7.6707f	7.6707f

(c)



因為在低頻率時，C 的值非常大，因此 Acm 受到影響變得非常小，但是當 DP 進入高頻區時，C 的值變得很小，只剩下 R 在影響 Acm，因此 Acm 在高頻區產生劇烈的變化。

2. (a)



M1 W=3.5um ; L=1um ; m=7

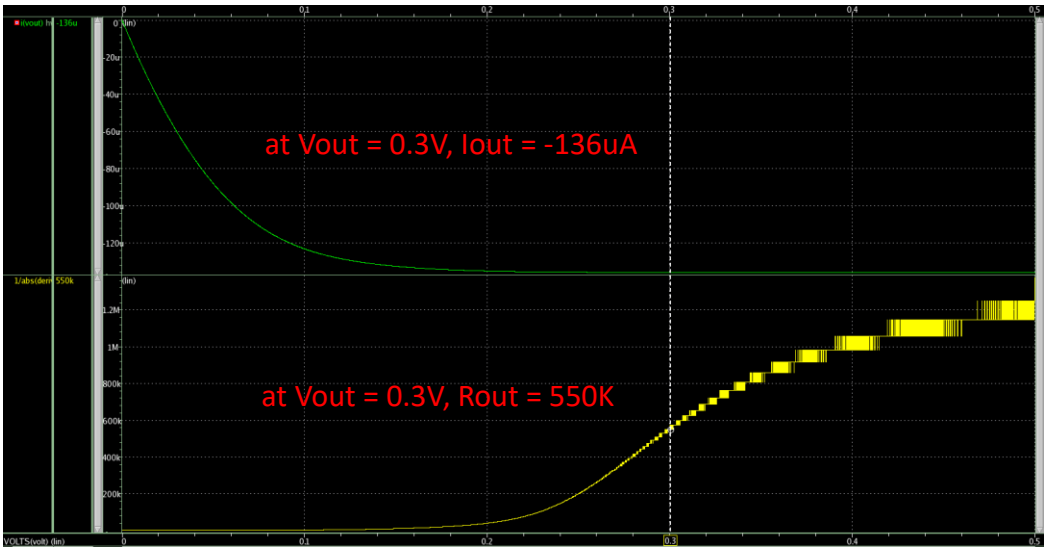
M2 W=3.5um ; L=1um ; m=7

M3 W=3.5um ; L=1um ; m=56

M4 W=3.5um ; L=1um ; m=56

Vb DC=0.6V

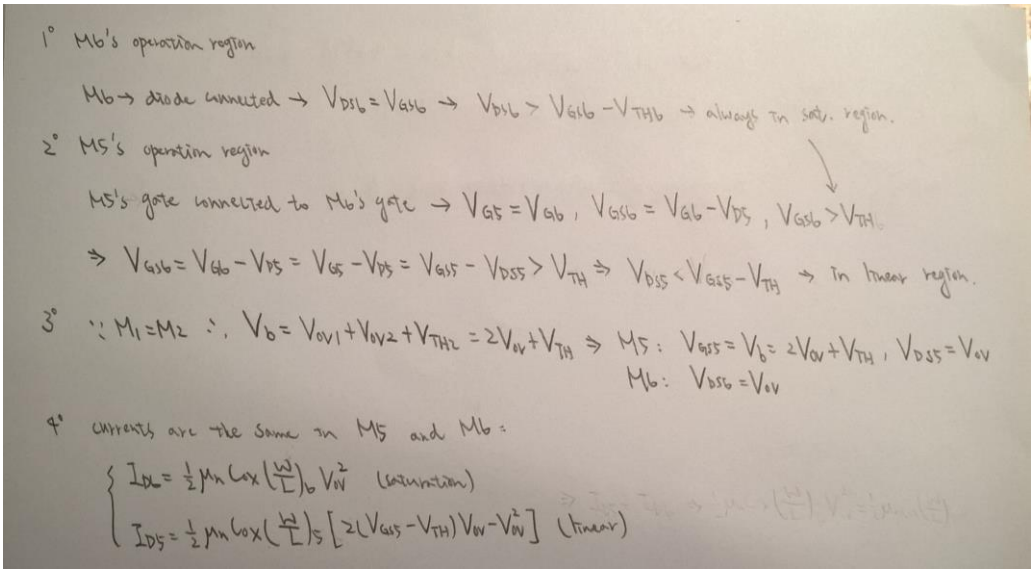
```
hw3_2_a
.protect
.lib 'cic018.l' TT
*.inc 'hw3_2_a.spi'
.temp 25
.unprotect
.option post
.param W1 = 3.5u L1 = 1u Vb = 0.5 m1 = 20

MM4 Vout Vb net9 gnd! n_18 W=W1 L=L1 m=56
MM3 net9 net19 gnd! gnd! n_18 W=W1 L=L1 m=56
MM2 net19 Vb net17 gnd! n_18 W=W1 L=L1 m=7
MM1 net17 net19 gnd! gnd! n_18 W=W1 L=L1 m=7

Vdd Vdd gnd 1.8
*Vb Vb gnd 0.6
Iref Vdd net19 17u
Vout Vout gnd 0.3

.OP
.dc Vout 0 0.5 0.0001

.end
```

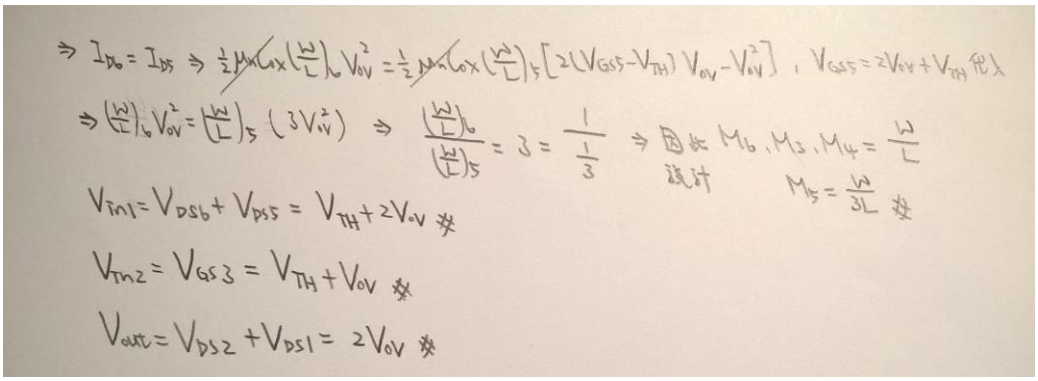


Comment:

因為這題限定 Vout 必須在 0.3V，又必須要達到 8 倍的 mirror current 和超過 500K 的 Rout，所以 W 必須非常大，但又因為製程上限的限制，所以必須利用並聯的方式增加 W，加上 Vbias 也是重要的因素，因為 Vbias 越大，Iout 越大，但是 Rout 卻越小，因此才必須藉由大幅調整 W 才能符合條件。一開始我已經把 W 調至上限了，R 卻只有幾十 K，又不能調整 Vbias，因為會使得 Iout 變小，所以只能調整 m 利用並聯來增加寬度，甚至有兩顆 mos 必須到 m=56 最後才能符合條件。

(b)





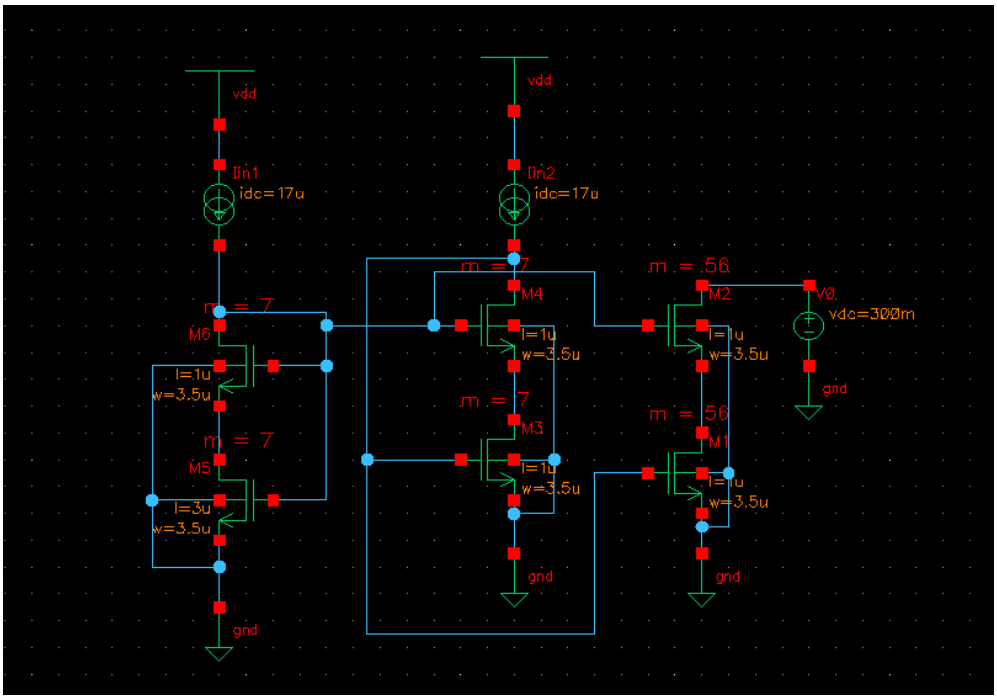
$$\Rightarrow I_{D6} = I_{D5} \Rightarrow \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 V_{ov}^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_5\left[2(V_{GS5}-V_{TH})V_{ov}-V_{ov}^2\right],\ V_{GS5}=2V_{ov}+V_{TH}\ 代入$$

$$\Rightarrow \left(\frac{W}{L}\right)_6 V_{ov}^2 = \left(\frac{W}{L}\right)_5 (3V_{ov}^2) \Rightarrow \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} = 3 = \frac{1}{\frac{1}{3}} \Rightarrow 因此 M_6, M_3, M_4 = \frac{W}{L}, \quad M_5 = \frac{W}{3L}$$ 設計 ※

$$V_{in1} = V_{DS6} + V_{DS5} = V_{TH} + 2V_{ov}$$ ※

$$V_{in2} = V_{GS3} = V_{TH} + V_{ov}$$ ※

$$V_{outc} = V_{DS2} + V_{DS1} = 2V_{ov}$$ ※




```
hw3_2_a
.protect
.lib 'cic018.l' TT
*.inc 'hw3_2_a.spi'
.temp 25
.unprotect
.option post
.param W1 = 3.5u L1 = 1u Vb = 0.5 m1 = 20

MM2 Vout Vb net13 gnd n_18 W=3.5u L=1u m=56
MM1 net13 net23 gnd gnd n_18 W=3.5u L=1u m=56
MM4 net23 Vb net21 gnd n_18 W=3.5u L=1u m=7
MM3 net21 net23 gnd gnd n_18 W=3.5u L=1u m=7
MM5 net1 Vb gnd gnd n_18 W=3.5u L=3u m=7
MM6 Vb Vb net1 gnd n_18 W=3.5u L=1u m=7

Vdd Vdd gnd 1.8
*Vb Vb gnd 0.6
Iin2 Vdd net23 DC=17u
Iin1 Vdd Vb DC=17u
Vout Vout gnd 0.3

.OP
.dc Vout 0 0.5 0.0001

.end
```

subckt						
element	0:mm2	0:mm1	0:mm4	0:mm3	0:mm5	0:mm6
model	0:n_18_1	0:n_18_1	0:n_18_1	0:n_18_1	0:n_18_1	0:n_18_1
region	Saturati	Saturati	Saturati	Saturati	Linear	Saturati
id	134.6335u	134.6335u	17.0000u	17.0000u	17.0000u	17.0000u
ibs	-1.0348f	-2.557e-20	-131.8644a	-3.229e-21	-3.229e-21	-133.0471a
ibd	-5.3696f	-1.0348f	-992.8154a	-131.8579a	-133.0407a	-1.1128f
vgs	439.5614m	443.7495m	438.4389m	443.7495m	497.3755m	437.9103m
vds	242.1859m	57.8141m	384.8130m	58.9366m	59.4652m	437.9103m
vbs	-57.8141m	0.	-58.9366m	0.	0.	-59.4652m
vth	403.7588m	392.9847m	402.8762m	392.9762m	341.7780m	402.5701m
vdsat	79.7495m	87.1147m	79.6373m	87.1194m	147.5276m	79.5286m
vod	35.8026m	50.7648m	35.5627m	50.7733m	155.5975m	35.3402m
beta	60.8883m	60.8306m	7.6106m	7.6038m	2.4644m	7.6104m
gam eff	509.0411m	507.4460m	509.0716m	507.4460m	507.4460m	509.0859m
gm	2.5488m	2.0337m	322.2187u	257.8701u	131.6295u	322.4067u
gds	38.2779u	1.2353m	3.9110u	149.9604u	211.0215u	3.7949u
gmb	510.5769u	426.5933u	64.3054u	54.0727u	27.1607u	64.2516u
cdtot	290.6263f	497.0162f	34.8819f	61.2423f	367.1239f	34.4642f
cgtot	1.1645p	1.3067p	145.1187f	163.0871f	572.7222f	144.9210f
cstot	1.2587p	1.3548p	157.2222f	169.3211f	542.1776f	157.0135f
cbtot	749.6284f	795.1959f	92.4882f	99.3479f	194.2590f	92.0843f
cgs	950.4674f	1.0460p	118.3214f	130.7970f	406.0880f	118.0717f
cgd	71.8040f	146.1610f	8.8575f	17.9213f	143.4360f	8.8454f

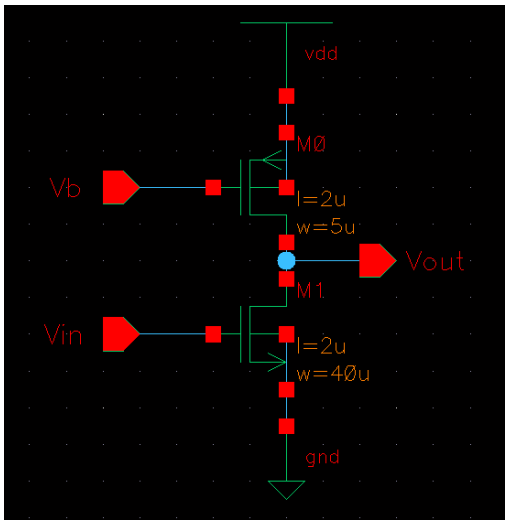
```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:net1    =  59.4652m 0:net13   =  57.8141m 0:net21   =  58.9366m
+0:net23   = 443.7495m 0:vb      = 497.3755m 0:vdd     =   1.8000
+0:vout    = 300.0000m
```

Comment:

Iout 的模擬算很準確，但是 Vb 卻差了有點多，會不準確的原因應該是當作 current mirror 的 M5 和 M6 的 size 比例時，並未考慮 channel length modulation effect 和 body effect 等等，而影響 mirror 出來的 bias 電壓不準確。使用 current mirror 給 bias voltage 的好處是比較穩定，因為是用固定電流來給電壓，會比直接使用 ideal voltage source 來的好。(在第三題有證明到)

3. (a)

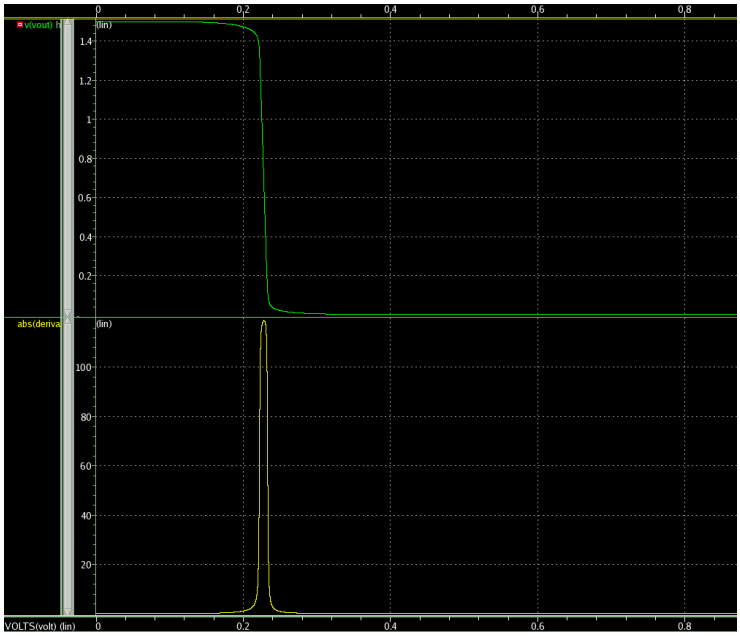
```
hw3_3_a
.protect
.lib 'cic018.l' TT
*.inc 'hw3_3_a.spi'
.temp 25
.unprotect
.option post

MM1 Vout Vin gnd gnd n_18 W=40u L=2u m=1
MM0 Vout Vb vdd vdd p_18 W=5u L=2u m=1

Vdd Vdd gnd 1.5
Vb Vb gnd 1
Vin Vin gnd 0.228

.OP
.dc Vin 0 1.5 0.0001

.alter
.prot
.lib "cic018.l" SF
.unprot
.alter
.prot
.lib "cic018.l" FS
.unprot

.end
```



M1 W=40um ; L=2um ; m=1

M0 W=5um ; L=2um ; m=1

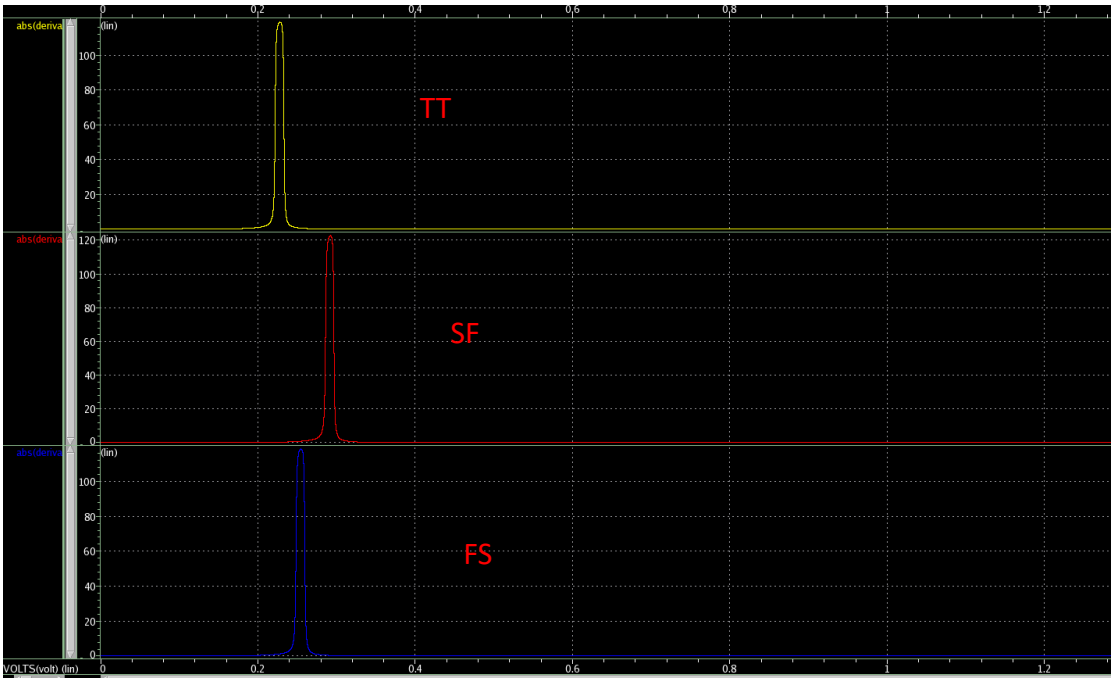
Vb DC=1V



Comment:

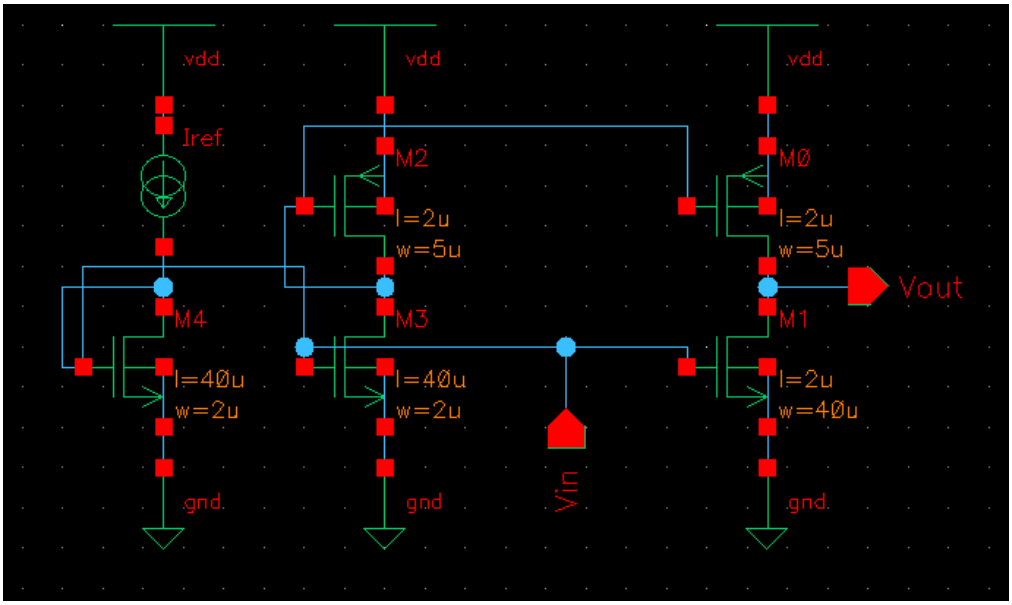
在做這題的時候發現，無論在 cutoff 還是 saturation 或是 linear region，都可以達到 gain>100，且圖形相當類似，推測 common source 的 gain 不太受到 operation region 的影響，但是若是考慮電容，則有可能會有影響。(在 cutoff 之下，寄生電容極大。)

(b)



只有先後順序的差別，圖形和 gain 大致相同。

(c)



M0 W=5um ; L=2um ; m=1

M1 W=40um ; L=2um ; m=1

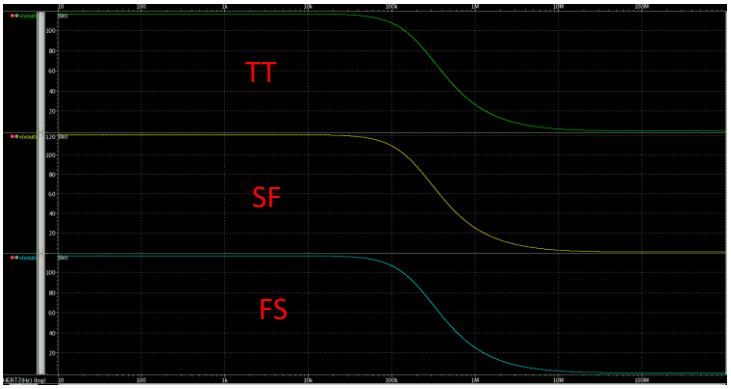
M2 W=5um ; L=2um ; m=1

M3 W=40um ; L=2um ; m=1

M4 W=40um ; L=2um ; m=1

Iref DC=290.7214Na (CS 的 drain current)

```
hw3_3_c
.protect
.lib 'cic018.l' TT
*.inc 'hw3_3_c.spi'
.temp 25
.unprotect
.option post
.option acout=0

MM1 Vout Vin2 gnd gnd n_18 W=40u L=2u m=1
MM0 Vout netVb vdd vdd p_18 W=5u L=2u m=1
MM2 netVb netVb vdd vdd p_18 W=5u L=2u m=1
MM4 Vin Vin gnd gnd n_18 W=40u L=2u m=1
MM3 netVb Vin gnd gnd n_18 W=40u L=2u m=1

Vdd Vdd gnd 1.5
Vin Vin Vin2 DC=0 AC=1
Iref Vdd Vin 290.7214n

.op
.ac dec 10000 10 1G
.probe ac V(Vout)

.alter
.prot
.lib "cic018.l" SF
.unprot
.alter
.prot
.lib "cic018.l" FS
.unprot

.end
```



Comment:

先用 Iref 提供 CS drain current，確保他符合 gain>100，並利用 1:1 的 mos 作 current mirror，最後作為 bias 輸入 CS。

(d)

會發現使用 mirror current 做 bias voltage 比較不會受到 corner 的影響，使用 mirror current 較容易使 operation region 維持在 saturation，因為 current source 提供的是穩定電流，再加上固定的電阻，可以提供穩定的電壓，比起直接提供電壓源來的更好。