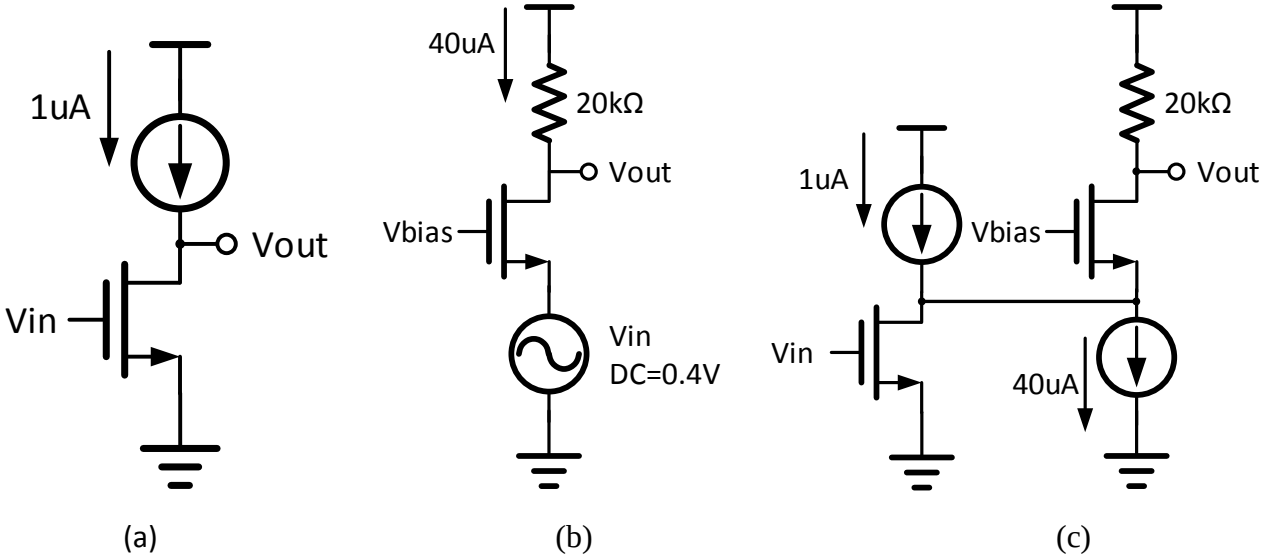
1. Use composer and hsipce to simulate the circuits in Fig. 1 (ideal current source) with Vdd=1.8V and do the calculation. (40%)
   (a) Design a common source stage with gain A1 >100 and **output DC voltage=0.4 (static current=1uA)** as shown at Fig. 1. (a). (5%)
   (b) Base on the simulation parameter of .lis file to calculate gain of common source and comment. (5%)
   (c) Design a common gate stage with gain A2>10 and **input DC voltage=0.4 (static current=40uA)** as shown at Fig. 1. (b). (5%)
   (d) Base on the simulation parameter of .lis file to calculate gain of common gate and comment. (5%)
   (e) Connect two stage and add additional 40uA current source as shown at Fig. 1. (c). Whether the DC bias stays the same? The overall gain equals to A1×A2 or not? If not, why not? (20%)



(a) (b) (c)

Fig. 1.

2. Design a common-source amplifier with cascaded loading as shown in Fig. 2. (30%)
   (a) With Vdd=1.8V and Ibias=9uA, design the W/L sizes of M1~M4, the dc bias to get voltage gain Av=Vout/Vin>45dB and Vout-swing>1V. (20%)
   (b) Keep W/L as the same and double all of m(finger) in (a), check the differences of the bias current, voltage gain and output swing and make a comment. (10%)

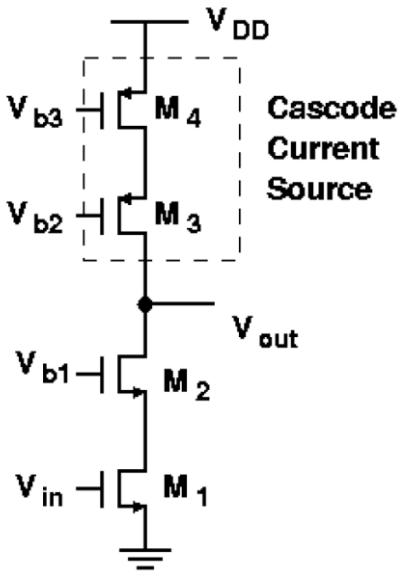


Fig. 2.

3. Design a source-follower amplifier with Vdd=1.8V as shown in Fig. 3. (20%)
   (a) Design the W/L sizes and Vb to get voltage gain Av=Vout/Vin>0.8 for Vin DC voltage from 0.5V to 1.8V. (5%)
   (b) Assume the deep-nwell is available. Design the W/L sizes and Vb to get voltage gain Av=Vout/Vin>0.96 for Vin DC voltage from 0.5V to 1.8V. (5%)
   (c) Comment on the differences between (a) and (b). (10%)

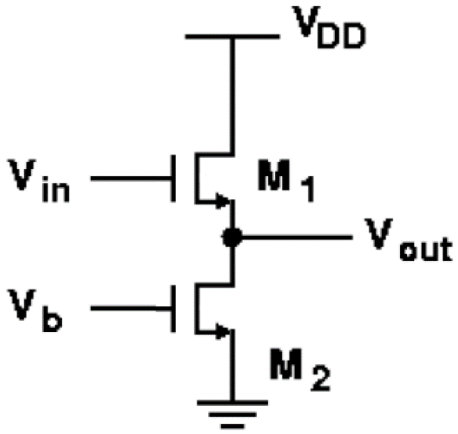


Fig. 3.

4. Assume the fabrication process is suffered from process variation, the length of input devices of Fig. 2. (M1) (Problem 2. (a)) and Fig. 3. (M1)(Problem 3. (a)) become 97% smaller. What happens to the gain of these amplifiers? Which one is more sensitive to the misalignment of MOS dimension? Why? (10%)

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***

by CCHsieh