2017 Analog IC Design Final (100%) *due date: 06/20/2017*

1. **Design a Fully-differential (differential-input, differential output) OP. You can select your structure to meet the specifications but have to include the common-mode feedback (CMFB) circuit and OP biasing circuits.**
   - **A.** The OP has to design in sub-circuit, and the sub-circuit nodes need to be ".subckt AICopamp iref vdd vin vip vocm von vop vss". The netlist has to be named as "My_op.spi".
   - **B.** The output has to drive a loading 25kΩ and 80pF.
   - **C.** The simulation should contain all the corners.
   - **D.** If the supply voltage is decreased, you will get additional bonus. (1% for 0.1V lower)
   - **E.** The Demo will use the test-bench offered by TAs, only the current of iref can be adjusted by your design consideration.
   - **F.** Specification (50%). (ps. Please fill the provided Table)

2. **Report Must Contain：(50%)**
   - **A. Schematic with device size, component value, node voltage and branch current. (10%)**
     Must contain core amplifier circuit, common mode feedback, biasing circuits, etc.
   - **B. Simulation results of each specification (AC/DC/transient/…) and contains all corners. (15%)**
     Please explain how to find the spec for your OP and make the comparison.
   - **C. Design procedure and consideration. (15%)**
     Briefly express your design consideration and optimization on selected circuit structure, device value, voltage, compensation, and common mode feedback issues.
   - **D. Discussion and conclusion. (10%)**
     Discuss your experience on this project, problem during design, and conclude what you get and suggest for this course.

✧ ***The following should be included in your report (a) schematic (b) HSPICE netlist & simulation file (c) waveform with cursor values (d) comments.***

✧ ***Please named your report as AICfinal_xxxxxx_xxxxxx (replaced by your student ID) and saved in PDF format.***

by CCHsieh

Specification

Design Items	Specifications	TT	SS	SF	FS	FF
Technology	CIC pseudo technology					
Supply voltage	<1.8V, low as possible					
power	<5mW (10%) Small as possible					
Loading	80pF / 25K Ω					
DC gain	>70dB (10%) large as possible					
GBW	>30MHz (10%) large as possible					
P.M.	$>60^{o}$ (10%)					
C.M.R.R.@10KHz	>85db (5%)					
P.S.R.R.+@10KHz	>85db (7.5%)					
P.S.R.R.-@10KHz	>85db (7.5%)					
Unity-gain configuration						
S.R.+(10% ~ 90%)	>3.5V/us (7.5%)					
S.R.- (10% ~ 90%)	>3.5V/us (7.5%)					
Settling+(1Vpp,0.01)	<3.5us (7.5%)					
Settling-(1Vpp,0.01)	<3.5us (7.5%)					
Figure of Merit (FoM)						
Small signal	$\frac{GBW(MHz)}{Power(mW)}$ (5%)					
Large signal	$\frac{SR(V/us)}{Power(mW)}$ (5%)					

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