

Composer Tutorial



Outline

- Full custom IC Design Flow
- Composer Tutorial
 - Making library and cells
 - Drawing schematics –an inverter example
 - Opening existing cells
 - Creating symbol

Full Custom IC Design Flow

Circuit Netlist/ Schematic

Composer, Text Editor

Pre-layout simulation

Hspice, Spectre, Eldo...

Layout

Virtuoso, Laker

DRC, LVS

Calibre

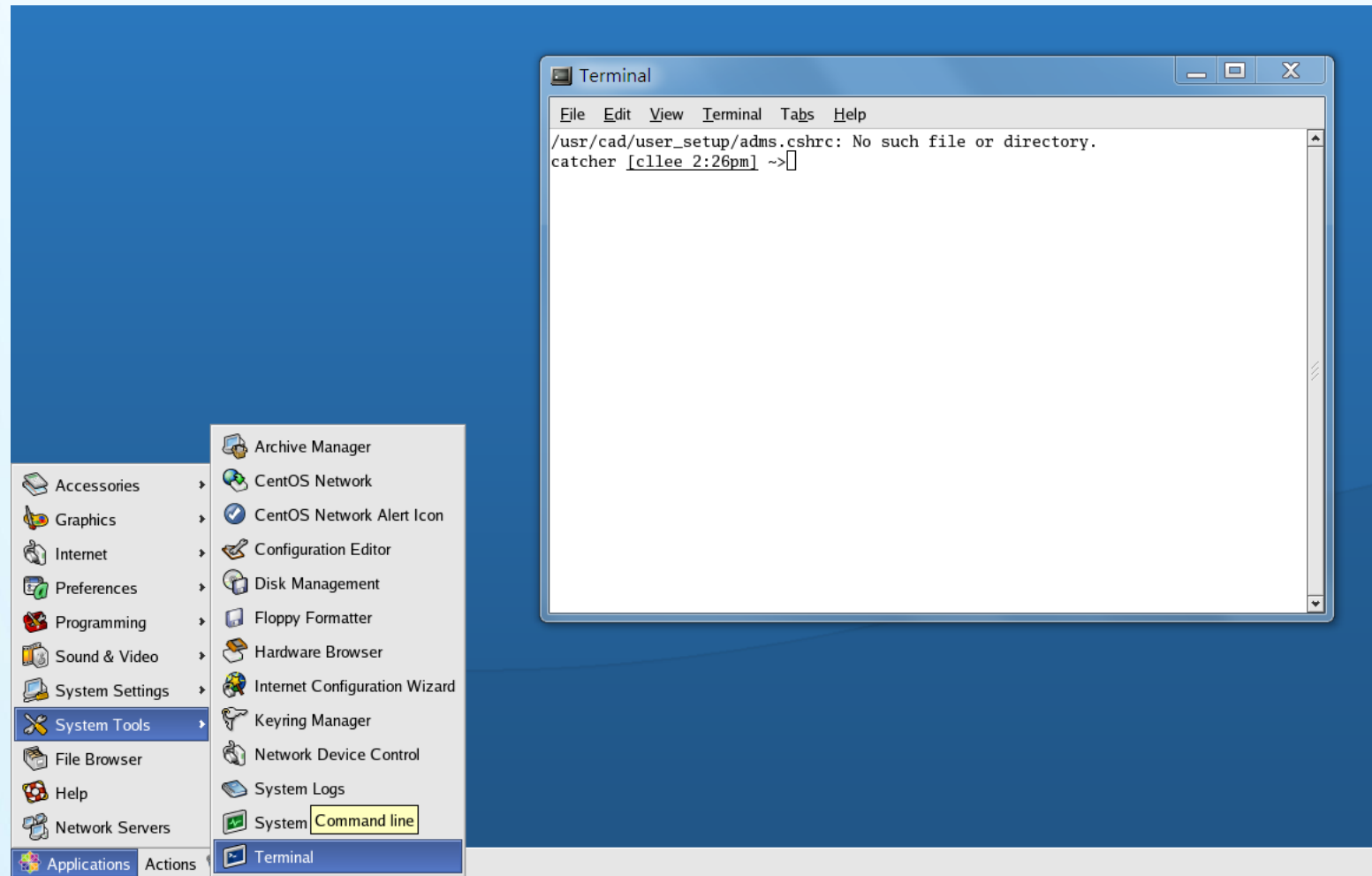
Parasitic Extraction

Calibre

Post-layout simulation

Hspice, Spectre, Eldo...

Open the Terminal Environment



Start Cadence Environment

Invoking ***icfb &*** in terminal

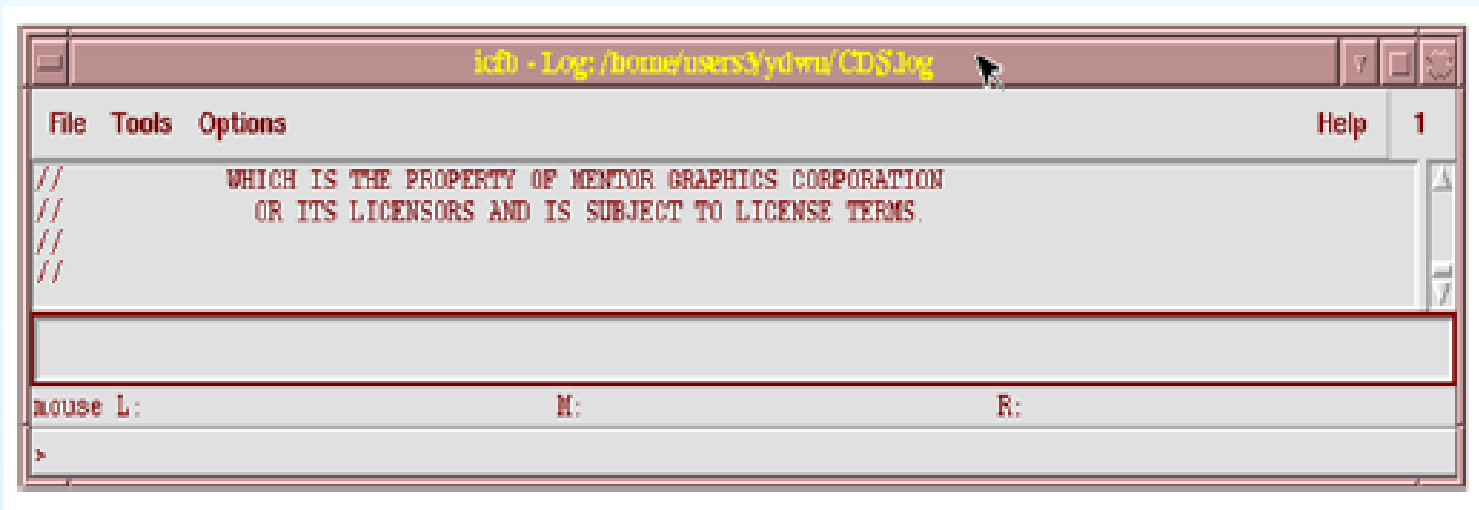
```
bigbird:~(m9761571)%  
bigbird:~(m9761571)%telnet ws2  
Trying 140.114.24.112...
```

```
[m9761571@ws2 ~]$ mkdir vlsi_composer  
[m9761571@ws2 ~]$ cd vlsi_composer/  
[m9761571@ws2 ~/vlsi_composer]$ icfb &
```



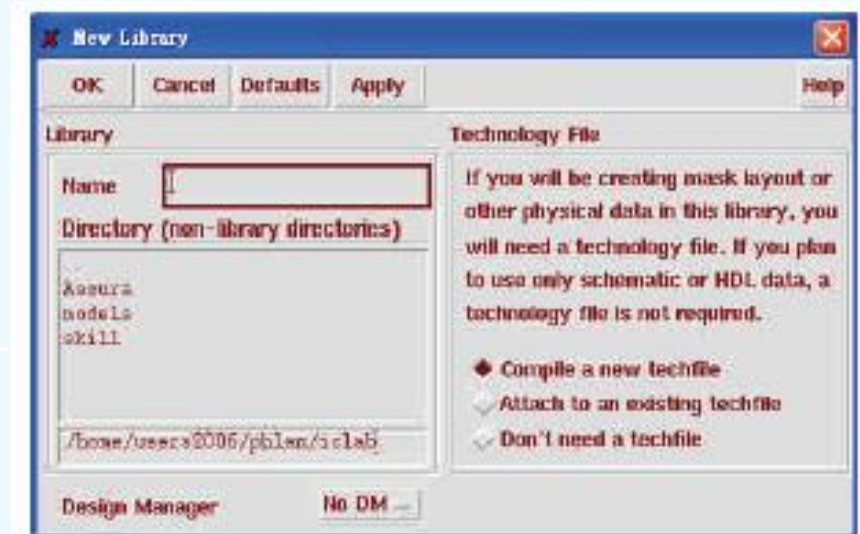
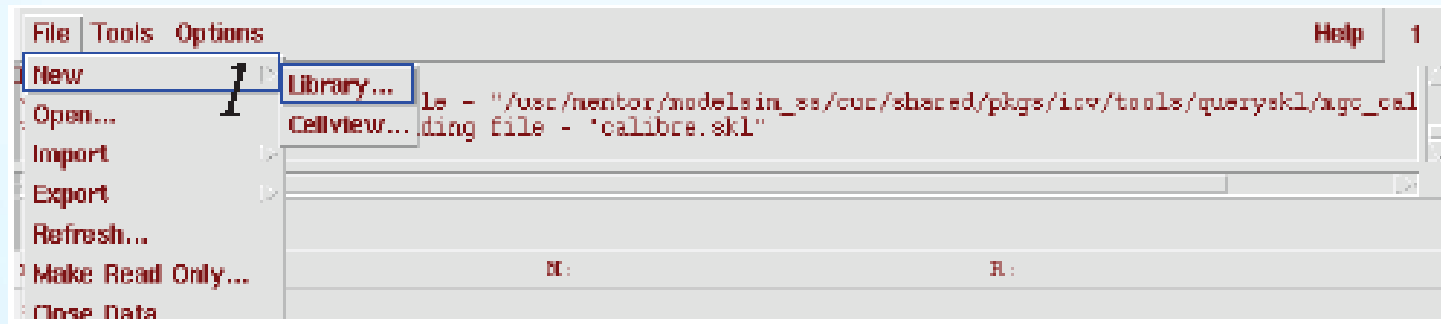
Main Window

After successfully checking license, the main window shows



Making library

From main window, **File** → **New** → **Library...**
A new window called **New Library** pops up



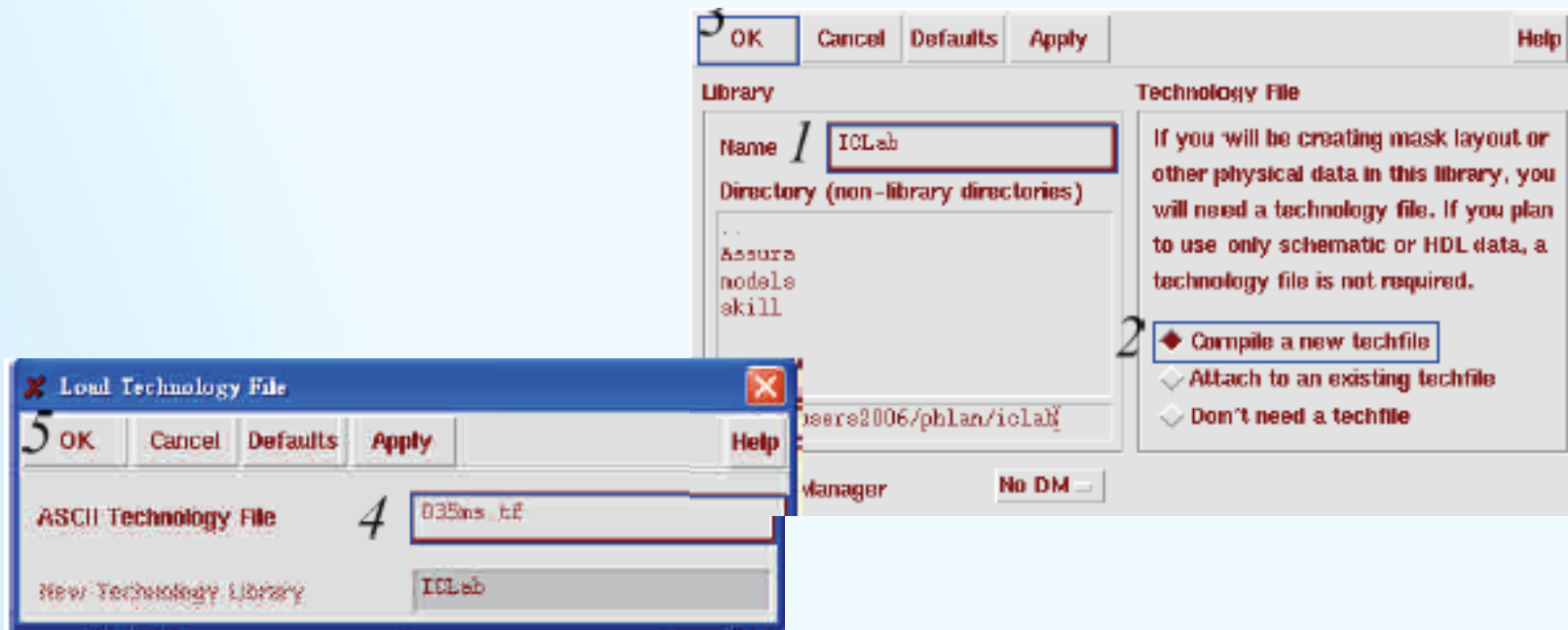
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Making Libraries

Enter the library name in the **Name** field

If you have techfile (018ms.tf), you can choose the option of **Compile a new techfile** option, and press **OK**.

or , you choose the option “**Don't need a techfile**” .



Making Cells

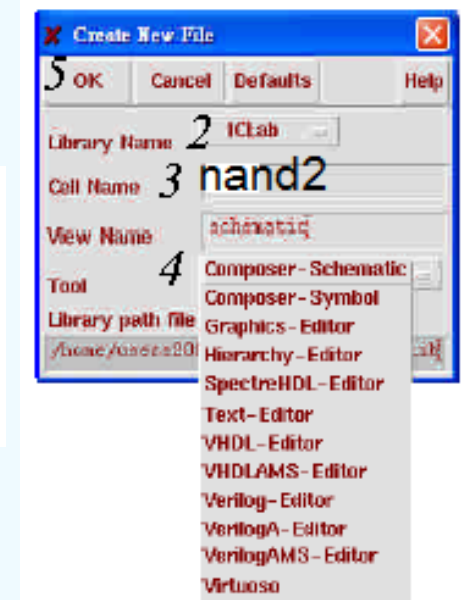
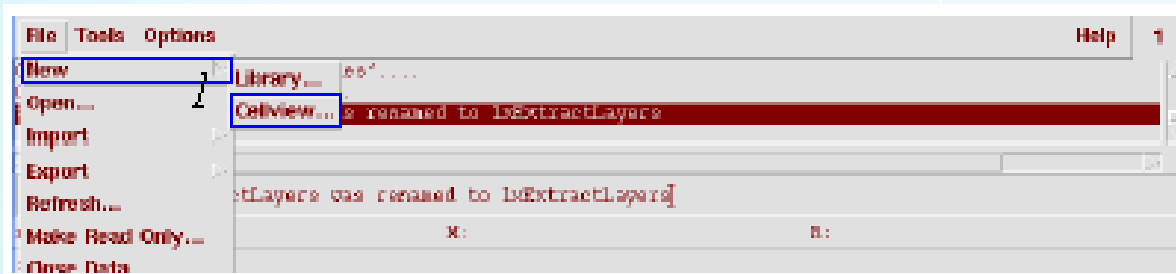
From main window, **File** → **New** → **Cellview...**

Choose the Library at which the cell is created

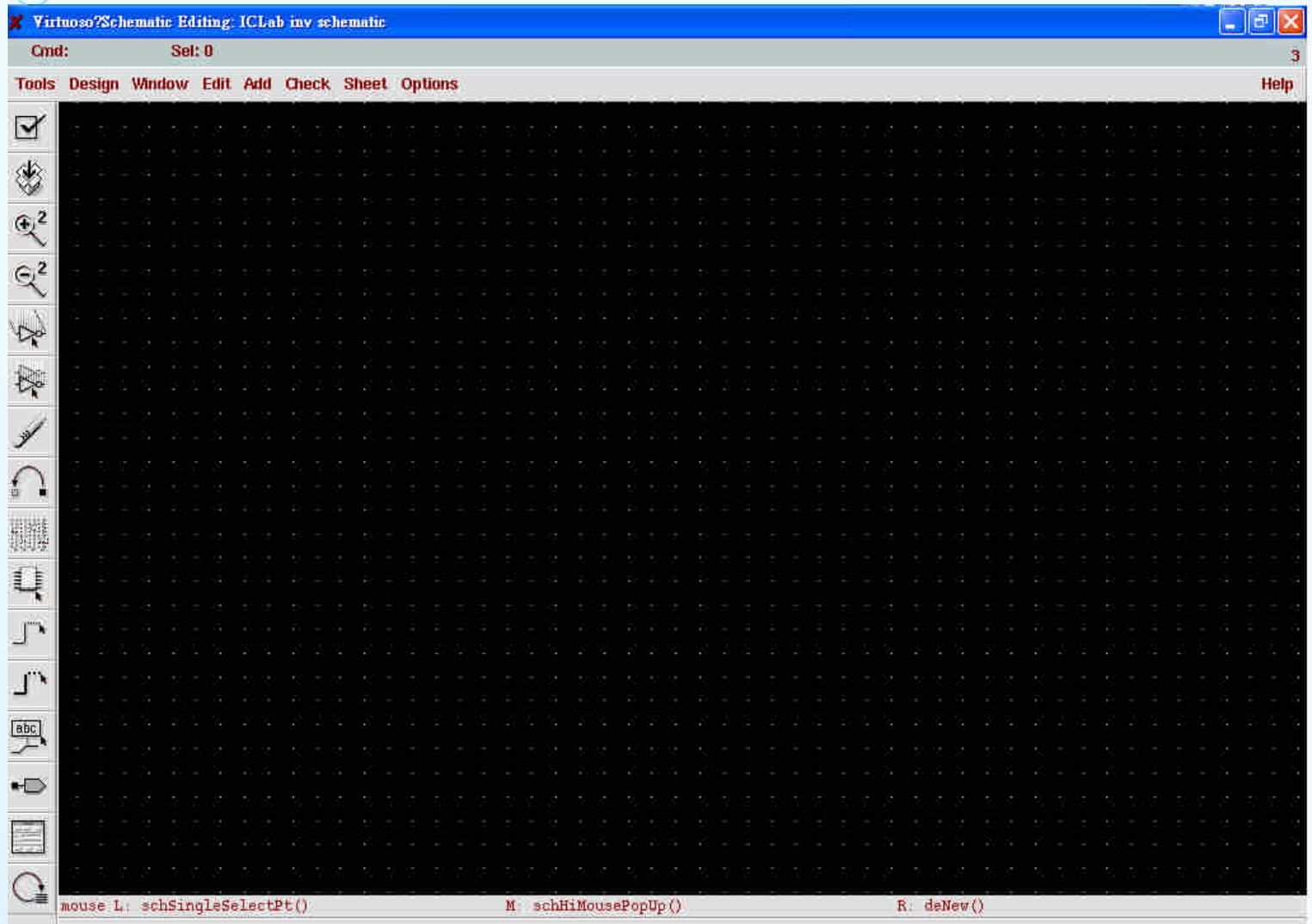
Enter the desired name in the **Cell Name** field (nand2)

Choose **Composer-Schematic** in the Tool field

Press **OK**



Schematic Editing Window



Inserting Symbols

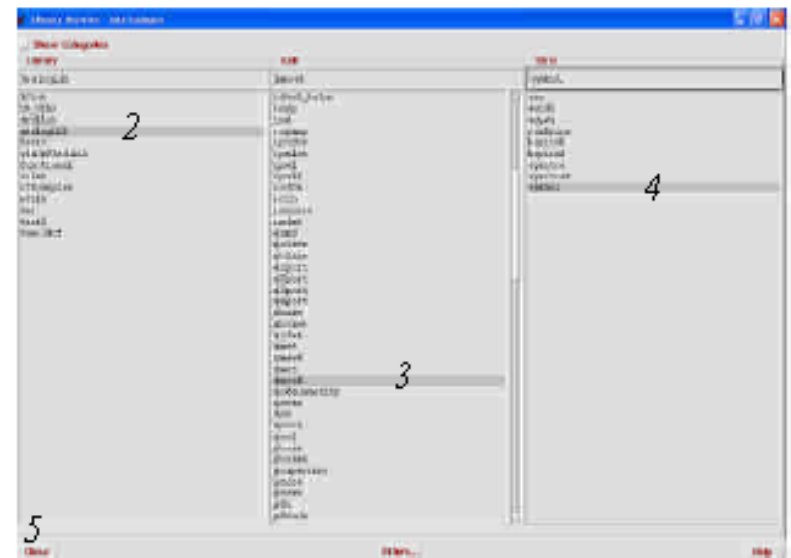
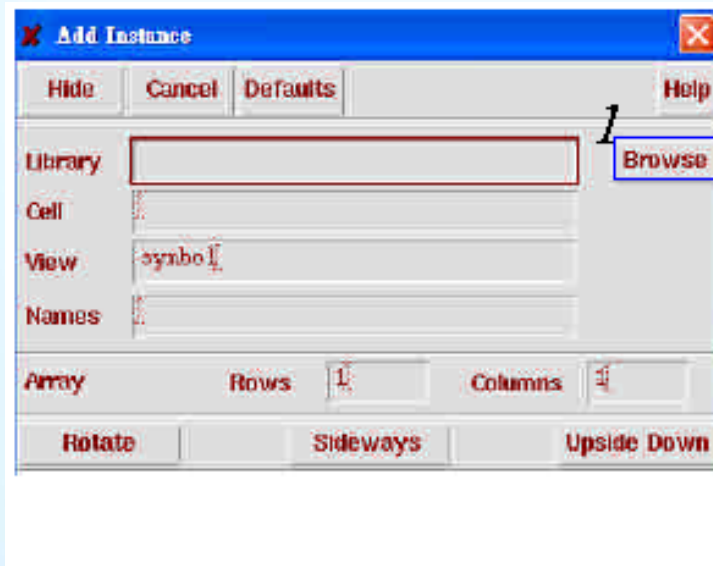
Press key “i” or the instance button from  the toolbar

Press “**Browse**” from the popped window

Pick the desired cell from library manager

Choose **symbol** view for schematic editing, and press **close**

analogLib → nmos4 → symbol



Editing Properties of Symbol

After closing the library manager, the corresponding library and cell name appears in the popped window

Fill some properties for the symbol

Name: Mn

Model Name: nch

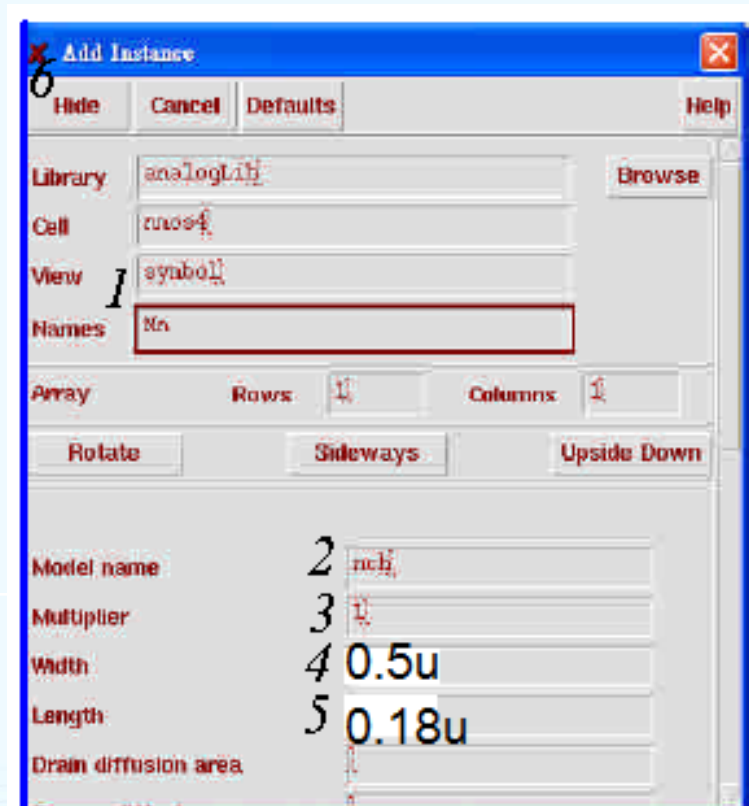
Multiplier: 1

Width: 0.5u

Length: 0.18u

Press **Hide** Button

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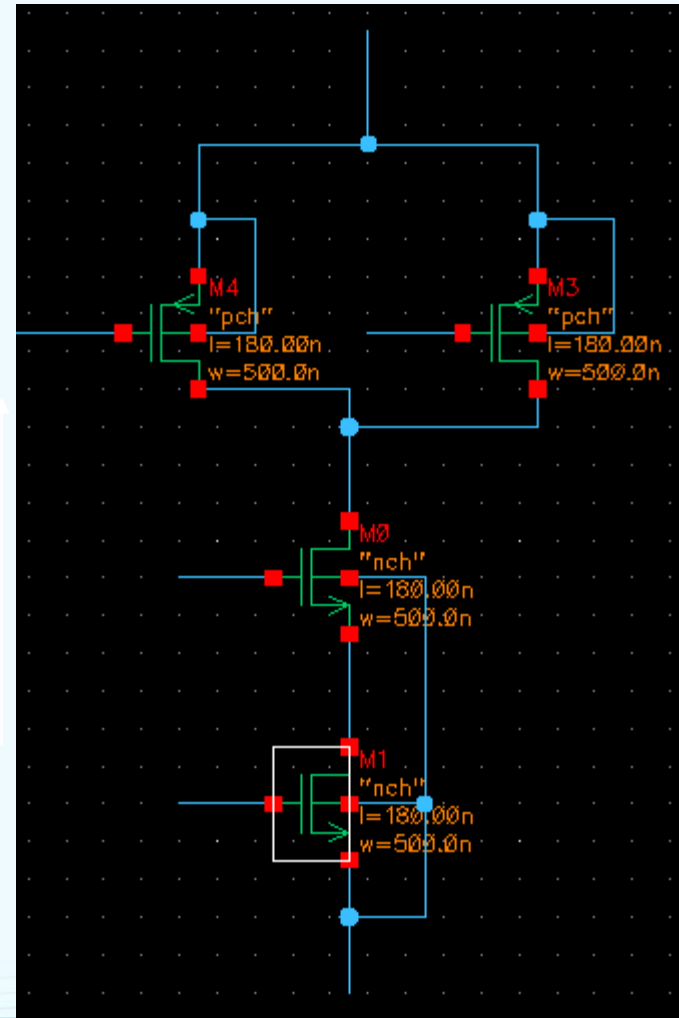


Adding and Connecting

Insert nmos4, pmos4, symbols from the analogLib library

nmos4: 0.5u/0/18u/1
pmos4: 0.5u/0.18u/1
vdc: DC voltage=3.3V
gnd

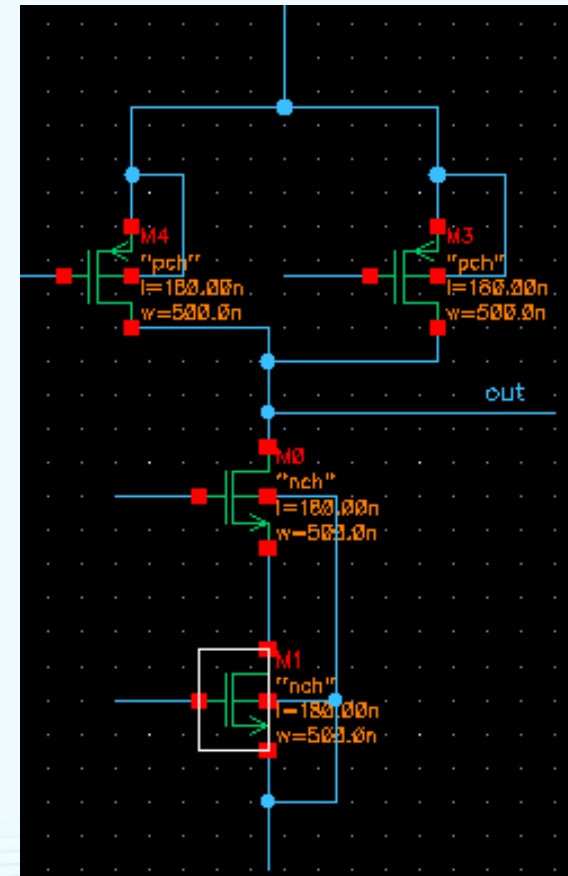
Press key "w" to place wire




Adding Net Names

Press key **"I"**(Label) and keyin the corresponding node name in the popped window

Press **Hide** and drag the "net name" to some wire/node

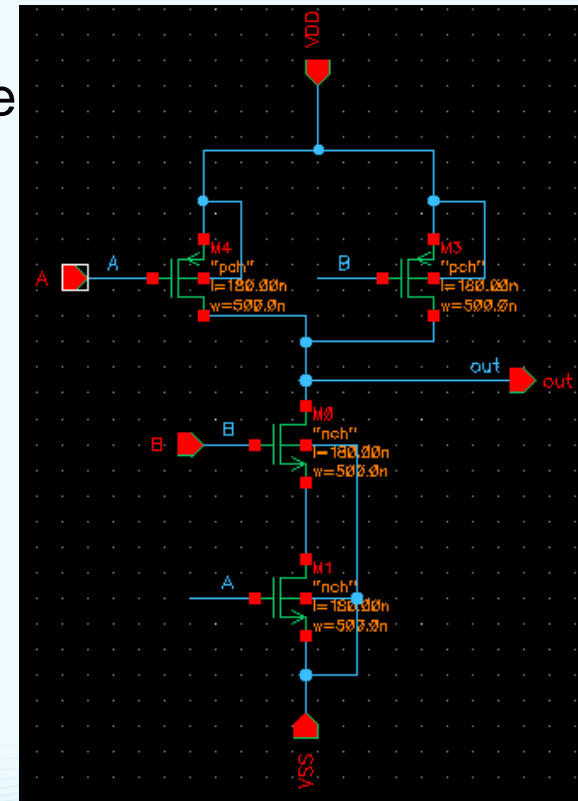
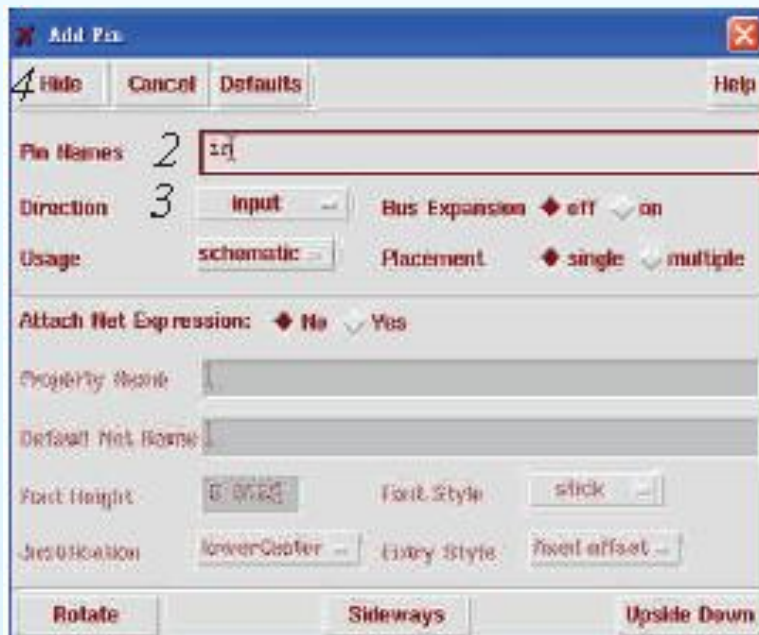


Indicating I/O Ports


Press key “**p**” or the pin button  from the toolbar
Specify the **Pin Name** and choose the **Direction**
(input/output/bidirection)

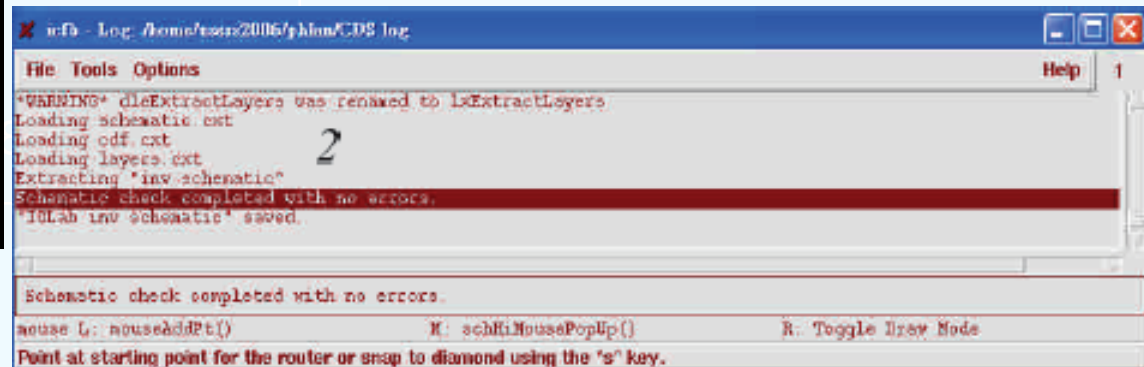
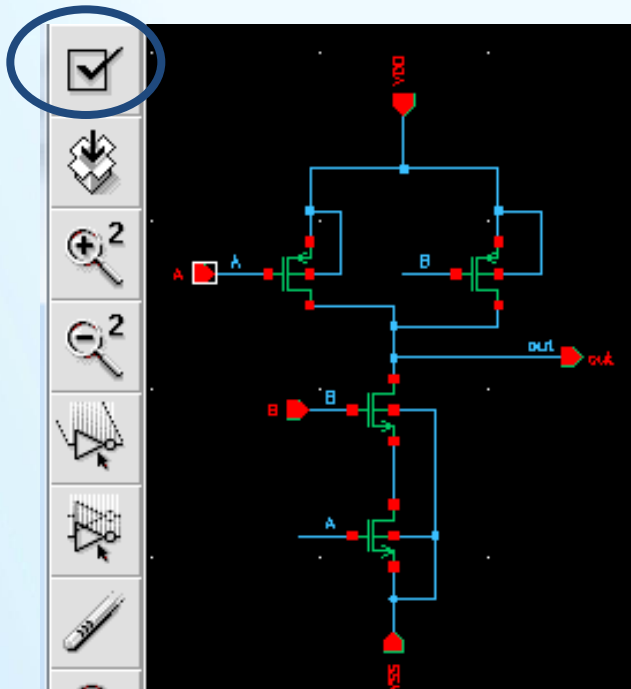
If pin connect to some net, the pin name should be identical to net name to avoid confusion.

Press **Hide** and drag the pin to the right place



Saving the Schematic

Press key “X” or check and save button  from the toolbar
To save the schematic and make sure schematic is error free
The main window reports the status of schematic



Open Existing Cell

From main window, choose **File** → **Open**

In the popped window, choose the **Library** and **Cell Name** you want
Choose the desired **View Name**, and Press **OK**

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5

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File Tools Options Help 1

New Layers was removed to InExtraLayers
st

Open...
Import
Export
Refresh...
Make Read Only...
Close Data...
Defragment Data
Exit...

OK Cancel Defaults Help

Library Name hw1

Cell Name nand2

View Name schematic

Mode edit read

Library path file /home/m97/m9761614/cds.lib

Cell Names
PRBS
hw1_1
hw1_1_FR4
hw1_2
hw1_2_PRBS
hw1_3
hw1_3_P
nand2

Creating Symbol

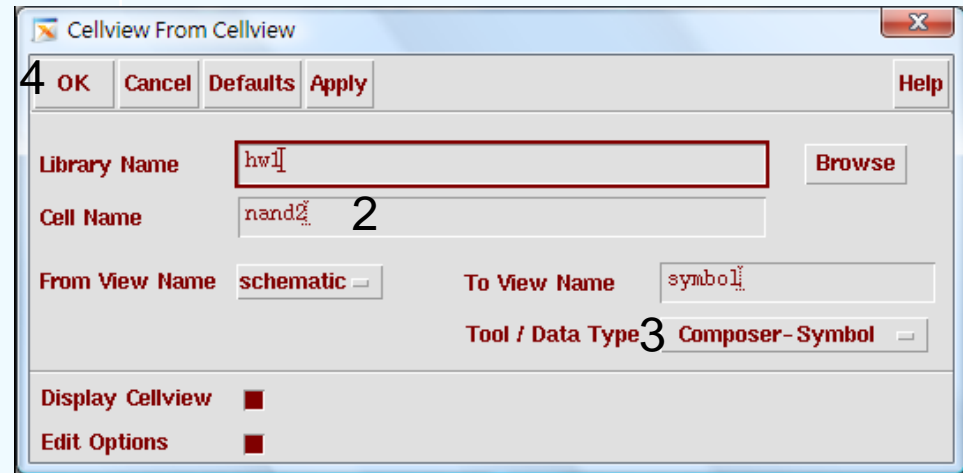
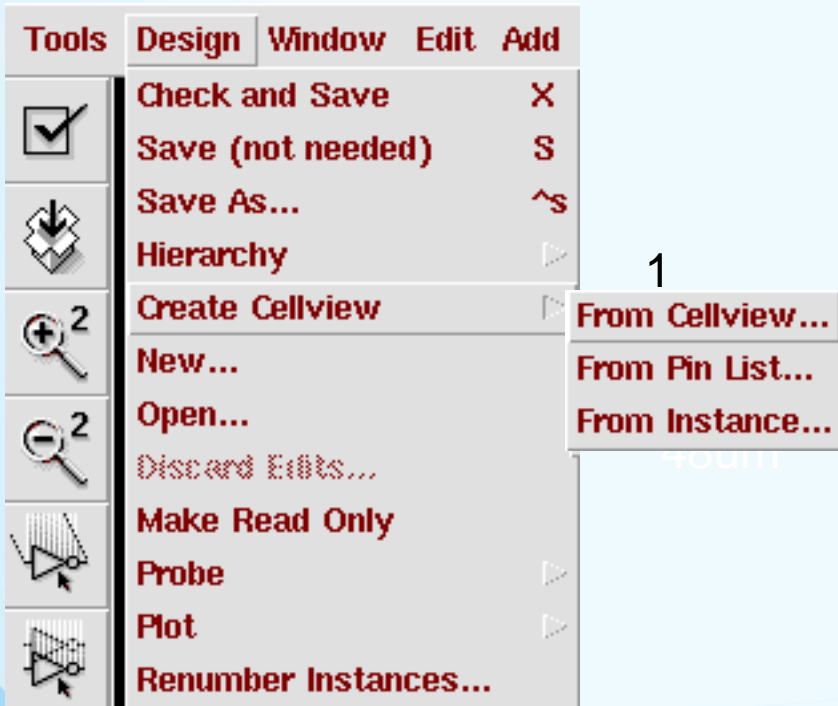
Open **nand2** schematic first

From schematic editing window, **Design** → **Create Cellview**

→ **From Cellview...**

Make sure that **Library** and **Cell Name** are correct.

Choose **Composer-Symbol** and Press **OK**



Defining I/O Ports

Another window pops up

The **I/O Pins** listed in the window accord with **Pins** that was inserted in Schematic Editing Window

You can decide the position of **Pins** on your own

Press OK if the I/O pins list is correct

2

Symbol Generation Options

OK Cancel Apply Help

Library Name: hw1 Cell Name: nand2 View Name: symbol

Pin Specifications	Attributes
Left Pins: A B	List
Right Pins: out 1	List
Top Pins: VDD	List
Bottom Pins: vss	List

Exclude Inherited Connection Pins:

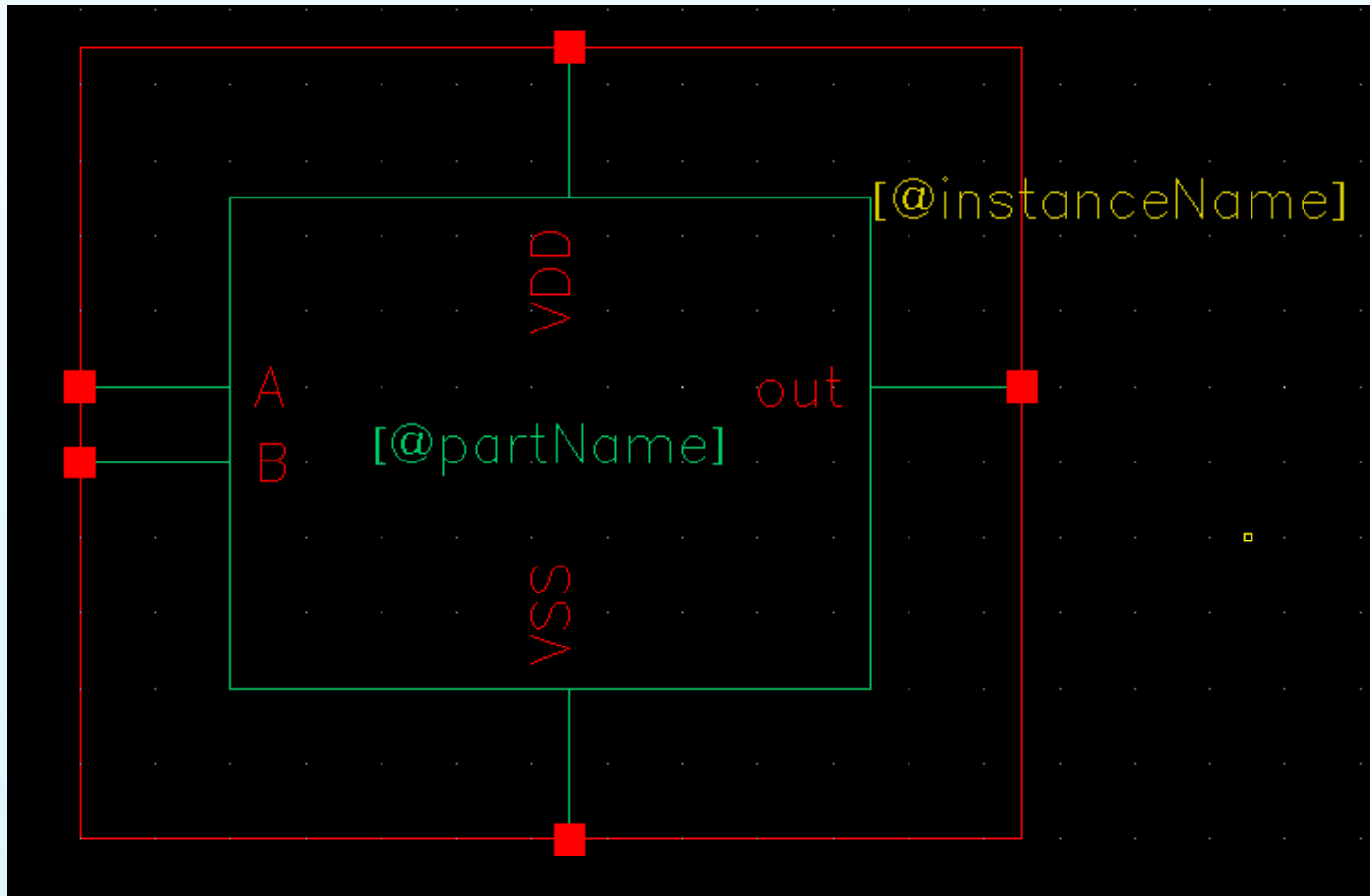
None All Only these: []

Load/Save Edit Attributes Edit Labels Edit Properties

Symbol Editing Window

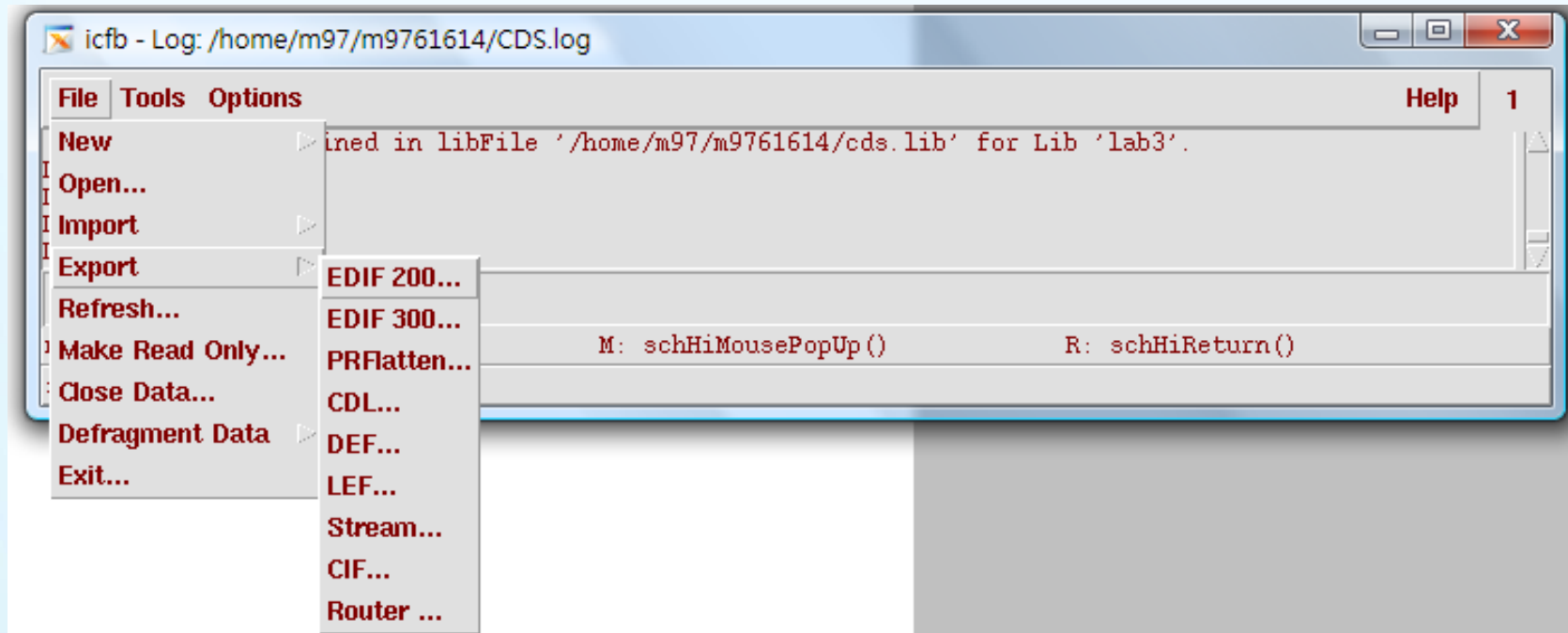
Then, **Symbol Editing Window** pops up

Input (output) ports lie at left (right) as previous page's setup



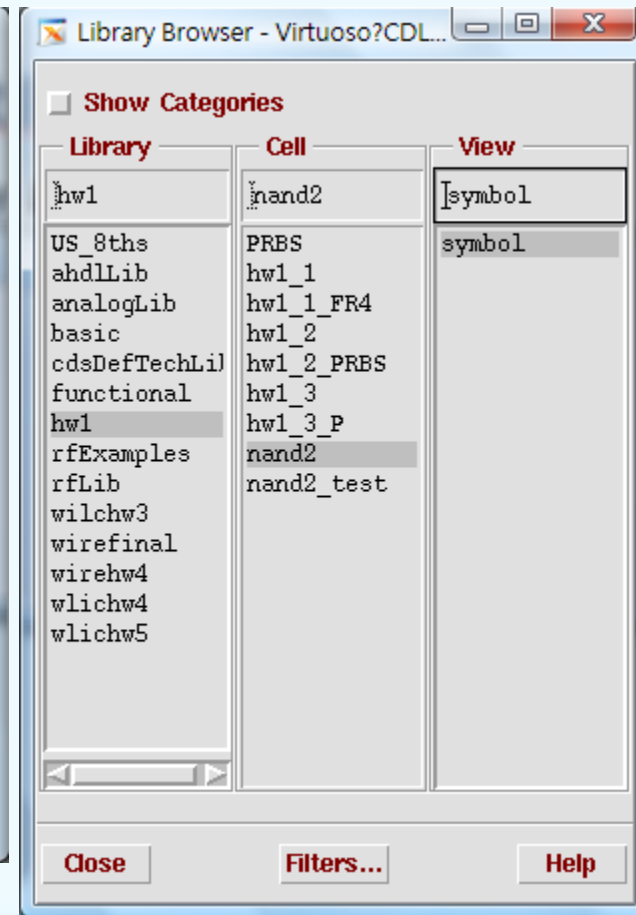
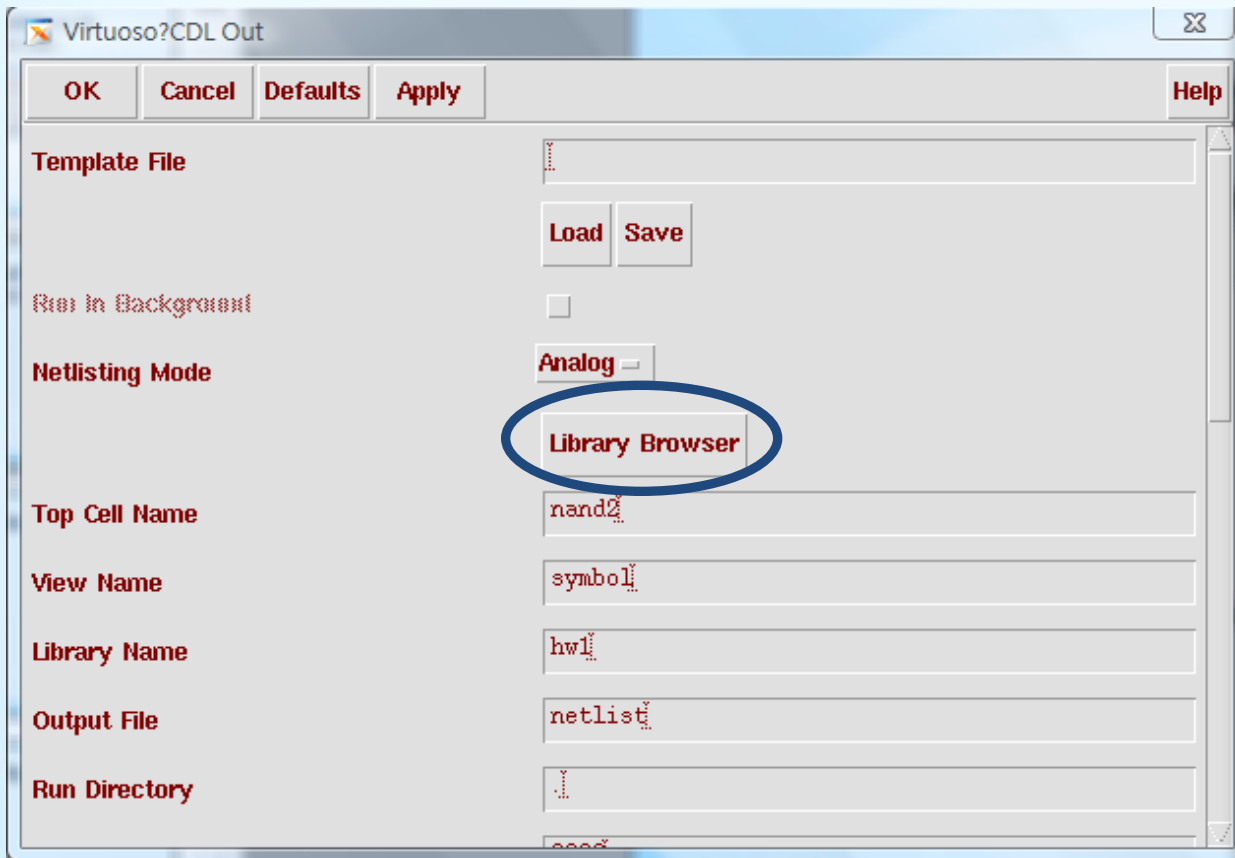
Export Netlists (1/3)

File → *Export* → *CDL...*



Export Netlists (2/3)

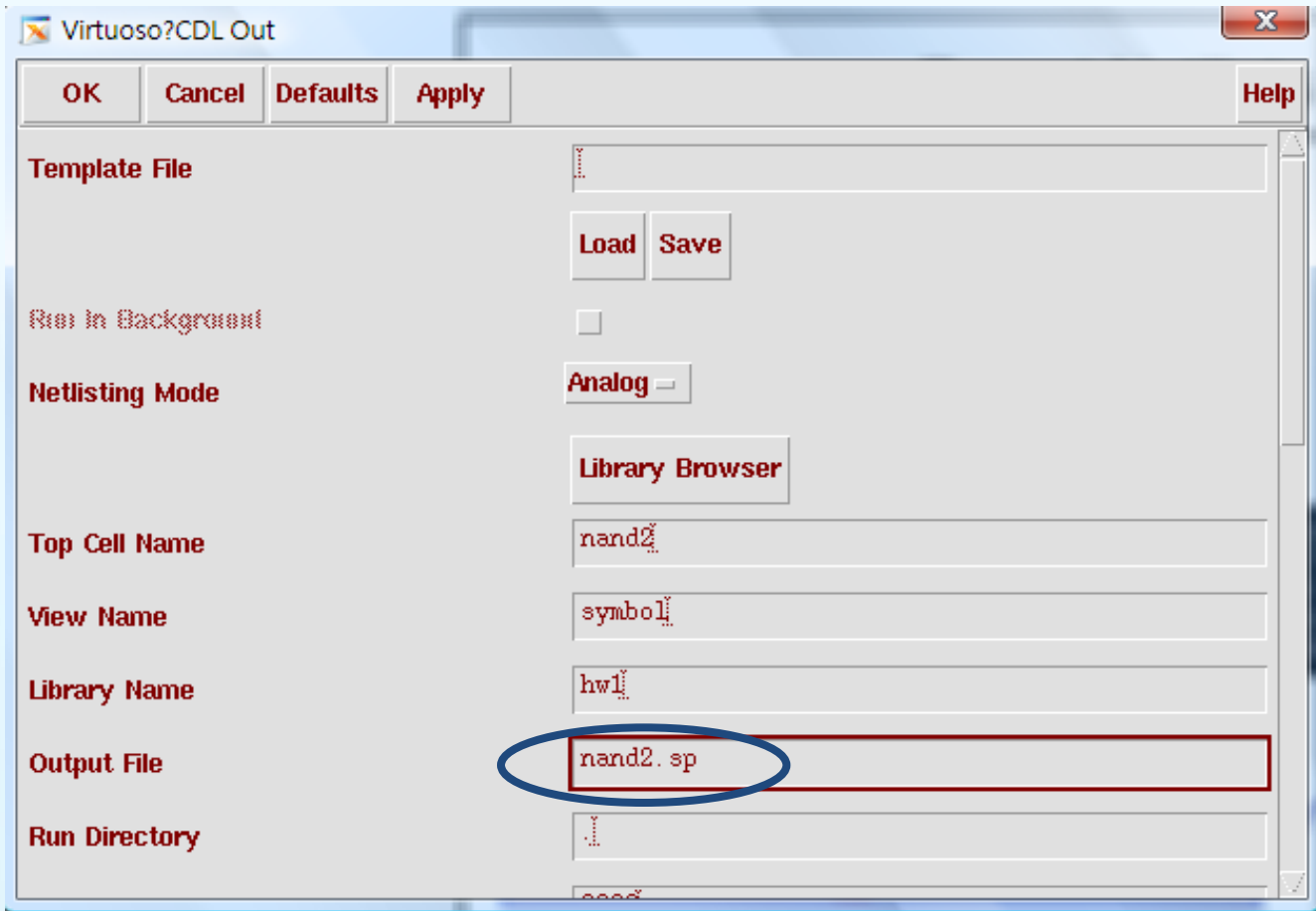
Choose ***“Library Brower”***



Export Netlists (3/3)

Specify output netlist name (.sp)

View the generated netlist



Hotkeys

Instance	i	Copy	c
Narrow Wire	w	Move	M
Wide Wire	W	Delete	del
Pin	p	Rotate	r
Undo	u	Property	q
Redo	U	Zoom	z
Stretch	m	Check & Save	X
Descend Edit/Read	E/e	Ascend one level	Ctrl+e

Thank you!