

#### **Frequency Response of Amplifiers**

**Analog IC Analysis and Design** 

#### 1. Miller Effect / Poles

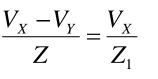
- 2. Common-Source (CS) Stage
- 3. Source Follower (SF)
- 4. Common-Gate (CG) Stage
- 5. Cascode Stage
- 6. Differential Pair (DP)

# Why Frequency Response

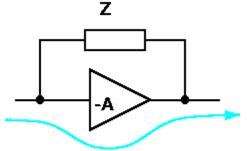
- In most analog circuits, the speed trades with many other parameters such as gain, power dissipation, and noise.
- Transient signal varied with time need to consider the capacitive and inductive effect inherent in circuit.

# Miller Effect

• For the current flowing through Z from X to Y is

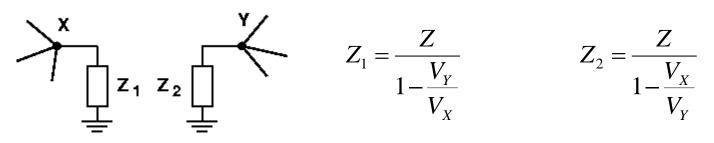




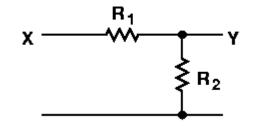


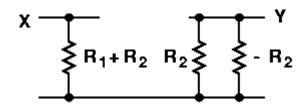
• That is

Main Signal Path

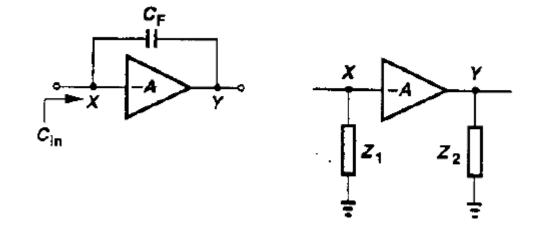


• If the impedance Z forms the only signal path between X and Y, then the conversion is often invalid.





#### Miller Effect of Feedback Capacitor

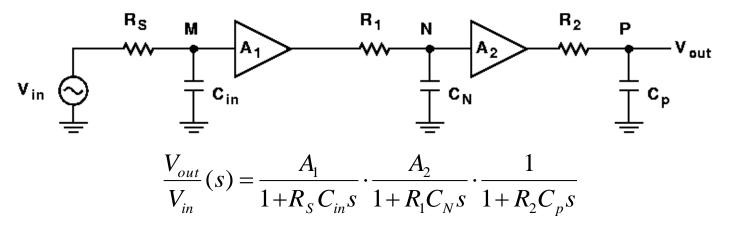


$$Z_{1} = \frac{Z}{1 - A_{v}} = \frac{Z}{1 + A} = \frac{1}{sC_{F}(1 + A)}, \quad C_{1} = C_{F}(1 + A)$$
$$Z_{2} = \frac{Z}{1 - (1/A_{v})} = \frac{Z}{1 + (1/A)} = \frac{1}{sC_{F}(1 + A^{-1})}, \quad C_{2} = C_{F}(1 + A^{-1})$$

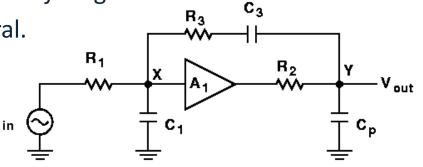
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# Association of Poles with Nodes

Assume A<sub>1</sub> and A<sub>2</sub> are ideal amplifiers, R<sub>1</sub> and R<sub>2</sub> model the output resistance of each stage, C<sub>in</sub> and C<sub>N</sub> represent the input capacitance of each stage, and C<sub>p</sub> denotes the load capacitance.



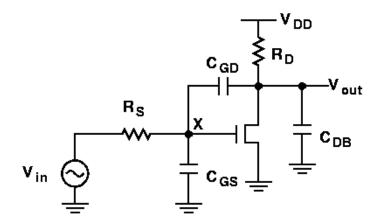
- Each pole with one node of the circuit, i.e.,  $\omega_j = \tau_j^{-1}$ , where  $\tau_j$  is the product of the capacitance and resistance seen at node *j* to ground.
- The above statement is not valid in general.
  - The location of the pole is difficult to calculate.



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- 2. Common-Source (CS) Stage
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#### **Common Source Stage**

• Provides voltage gain and high input impedance.



$$\omega_{in} = \frac{1}{R_S [C_{GS} + (1 + g_m R_D) C_{GD}]}$$
$$\omega_{out} = \frac{1}{R_D (C_{DB} + C_{GD})}$$

• To obtain the exact transfer function  $\frac{V_X - V_{in}}{R_S} + V_X C_{GS} s + (V_X - V_{out}) C_{GD} s = 0,$   $\frac{V_{In}}{\xi} = C_{GS} C_{GD} + C_{GS} C_{DB} + C_{GD} C_{DB} = 0,$   $\frac{V_{out}}{V_{in}} (s) = \frac{(C_{GD} s - g_m) R_D}{R_S R_D \xi s^2 + [R_S (1 + g_m R_D) C_{GD} + R_S C_{GS} + R_D (C_{GD} + C_{DB})] s + 1}$ 

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#### **Dominant Pole Approximation**

• Two independent capacitors (initial conditions) in the circuit yield a second order differential equation for the time response.

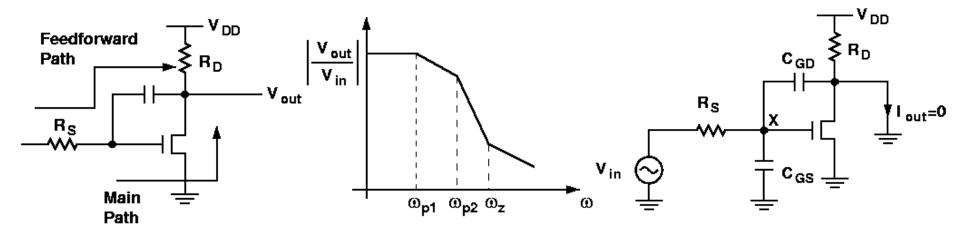
$$\begin{aligned} \frac{V_{out}}{V_{in}}(s) &= \frac{(C_{GD}s - g_m)R_D}{R_s R_D \xi s^2 + [R_s(1 + g_m R_D)C_{GD} + R_s C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \\ &= -g_m R_D \frac{(1 - C_{GD}s / g_m)}{R_s R_D \xi s^2 + [R_s(1 + g_m R_D)C_{GD} + R_s C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \\ &= -g_m R_D \frac{(1 - s / z_1)}{\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} = -g_m R_D \frac{(1 - s / z_1)}{\frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1} \end{aligned}$$

$$\bullet \quad |\mathbf{f} \mid \omega_{p1}| << \mid \omega_{p2} \mid \end{aligned}$$

$$z_{1} = \frac{g_{m}}{C_{GD}}, \quad \omega_{p1} = \frac{1}{R_{S}(1 + g_{m}R_{D})C_{GD} + R_{S}C_{GS} + R_{D}(C_{GD} + C_{DB})}$$
  
$$\omega_{p2} = \frac{1}{\omega_{p1}} \cdot \frac{1}{R_{S}R_{D}(C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})} \cong \frac{R_{S}C_{GS}}{R_{S}R_{D}(C_{GS}C_{GD} + C_{GS}C_{DB})} = \frac{1}{R_{D}(C_{GD} + C_{DB})}$$
  
If  $C_{GS} >> (1 + g_{m}R_{D})C_{GD} + R_{D}(C_{GD} + C_{DB})/R_{S}$ 

# **Right-Half Plane Zero**

- C<sub>GD</sub> provides a feed forward path that conducts the input signal to the output at very high frequencies.
- A zero in the right half plane causes stability issue in feedback Amp.



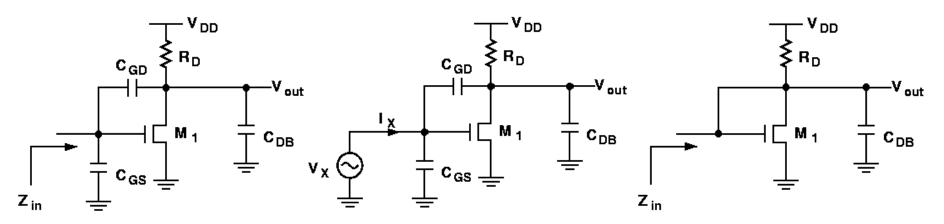
- The zero,  $s_z$ , can be computed by noting that the  $V_{out}(s)/V_{in}(s)$  must drop to zero for  $s = s_z$ .
- $V_{x}C_{GD}s_{z} = g_{m}V_{x}$

 $s_z = \frac{\delta_m}{2}$ 

The currents through C<sub>GD</sub> and M<sub>1</sub> are equal and opposite.

## Input Impedance of a CS Stage

• As a first-order approximation  $Z_{in} = \{ [C_{GS} + (1 + g_m R_D)] C_{GD} \}^{-1}$ 



• At high frequencies, take the effect of the output node into account

Ignore 
$$C_{GS}$$
,  $(I_X - g_m V_X) \frac{R_D}{1 + R_D C_{DB} s} + \frac{I_X}{C_{GD} s} = V_X \implies \frac{V_X}{I_X} = \frac{1 + R_D (C_{GD} + C_{DB}) s}{C_{GD} s (1 + g_m R_D + R_D C_{DB} s)}$ 

• At low frequencies

$$Z_{in} \approx \frac{1}{sC_{GS}} \parallel \frac{1}{sC_{GD}(1+g_mR_D)}$$

• At high frequencies

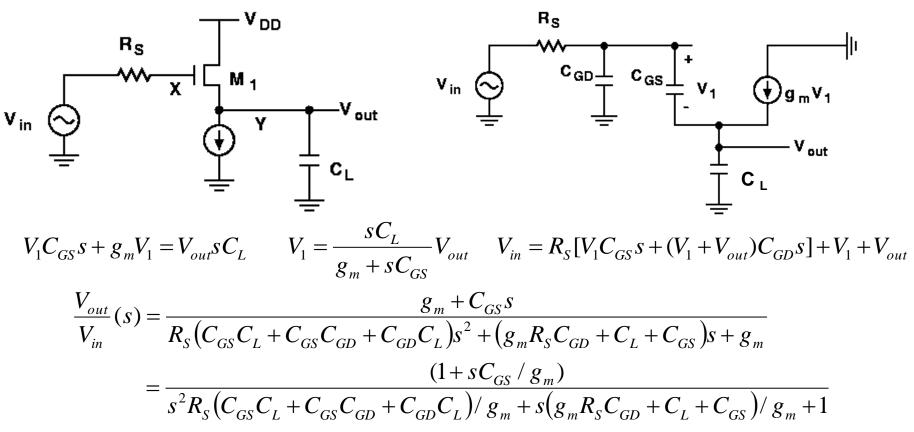
$$Z(C_{GD}) = 0, \quad Z_{in} \approx \frac{1}{sC_{GS}} \|\frac{1}{g_m}\| R_D$$

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#### Source Follower

• Source followers are occasionally used as level shifters or buffers.



> The signal conducted by  $C_{GS}$  at high frequencies adds with the same polarity to the signal produced by the intrinsic transistor. (*left half plane* zero)

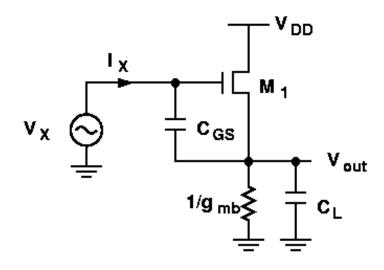
#### Input Impedance of Source Follower

$$\frac{V_{out}}{V_{in}}(s) = \frac{(1 + sC_{GS} / g_m)}{s^2 R_s \left( C_{GS} C_L + C_{GS} C_{GD} + C_{GD} C_L \right) / g_m + s \left( g_m R_s C_{GD} + C_L + C_{GS} \right) / g_m + 1}$$

If the two poles are far apart

$$\omega_{p1} \approx \frac{g_m}{g_m R_S C_{GD} + C_L + C_{GS}} = \frac{1}{R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}} \quad If \ R_S = 0, \text{ then } \omega_{p1} = \frac{g_m}{C_L + C_{GS}}$$

Input impedance (ignore C<sub>GD</sub>)



$$V_{X} = \frac{I_{X}}{C_{GS}s} + \left(I_{X} + \frac{g_{m}I_{X}}{C_{GS}s}\right) \left(\frac{1}{g_{mb}} \| \frac{1}{sC_{L}}\right)$$
$$Z_{in} = \frac{1}{C_{GS}s} + \left(1 + \frac{g_{m}}{C_{GS}s}\right) \frac{1}{g_{mb} + C_{L}s}$$
At low frequencies,  $g_{mb} \gg \|C_{L}s\|$ 
$$Z_{in} = \frac{1}{C_{GS}s} \left(1 + \frac{g_{m}}{g_{mb}}\right) + \frac{1}{g_{mb}}$$
$$C_{in} = C_{GS} \frac{g_{mb}}{g_{mb} + g_{m}}$$

# Input Impedance of Source Follower

- At relatively low frequencies, the equivalent input  $C_{in} = \frac{C_{GS}g_{mb}}{g_m + g_{mb}}$ 
  - By Miller effect

$$A_{v} = \frac{g_{m}}{g_{m} + g_{mb}} \qquad C_{eq} = C_{GS} \left[ 1 - \frac{g_{m}}{g_{m} + g_{mb}} \right] = \frac{C_{GS} g_{mb}}{g_{m} + g_{mb}}$$

- The overall input capacitance is equal to  $C_{GD}$  plus a fraction of  $C_{GS}$ .
- At high frequencies,

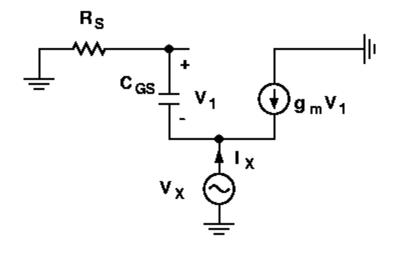
$$Z_{in} = \frac{1}{C_{GS} s} + \left(1 + \frac{g_m}{C_{GS} s}\right) \frac{1}{g_{mb} + C_L s}$$

$$g_{mb} <<|sC_L| \text{ and } Z_{in} \approx \frac{1}{sC_{GS}} + \frac{1}{sC_L} + \frac{g_m}{s^2 C_{GS} C_L} = \frac{1}{j\omega C_{GS}} + \frac{1}{j\omega C_L} - \frac{g_m}{\omega^2 C_{GS} C_L}$$

- The input impedance consists of the series combination of capacitors  $C_{GS}$  and  $C_{L}$  and a negative resistance.
- The negative resistance property can be utilized in oscillators.

# **Output Impedance of Source Follower**

• Neglecting  $g_{mb}$  ,  $C_{SB}$  &  $C_{GD}$ 



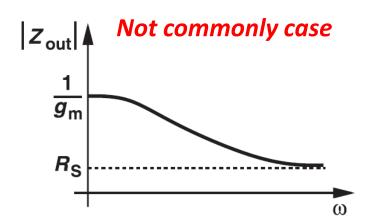
$$V_1 C_{GS} s + g_m V_1 = -I_X, \quad V_1 C_{GS} s R_S + V_1 = -V_X$$

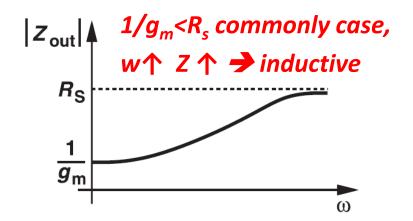
$$Z_{out} = \frac{V_X}{I_X} = \frac{sR_SC_{GS} + 1}{g_m + sC_{GS}}$$

 $\succ$  At low frequencies,  $Z_{out} \approx 1/g_m$ 

➤ At high frequencies,  $Z_{out} \approx R_S$  with  $Z(C_{GS}) = 0$ 

➢ If  $1/g_m < R_s$ , the output impedance contains an inductive component.

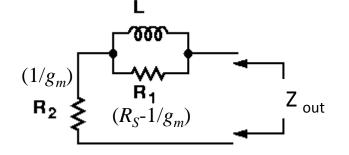




**Analog IC Analysis and Design** 

### **Output Impedance of SF**

• Equivalent network of output impedance

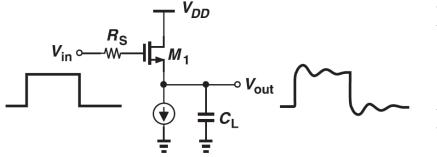


At low frequencies,  $Z_{out} = 1/g_m$  when  $\omega = 0$ 

At high frequencies, 
$$Z_{out} = R_s$$
 when  $\omega = \infty$ 

> Therefore, 
$$R_2 = 1/g_m$$
  $R_1 = R_S - 1/g_m$ 

$$Z_{out} - \frac{1}{g_m} = \frac{sC_{GS}(R_s - 1/g_m)}{g_m + sC_{GS}}, \quad \frac{1}{Z_{out}} - \frac{1}{g_m} = \frac{1}{R_s - 1/g_m} + \frac{1}{\frac{sC_{GS}}{g_m}(R_s - 1/g_m)}, \quad L = \frac{C_{GS}}{g_m}(R_s - 1/g_m)$$

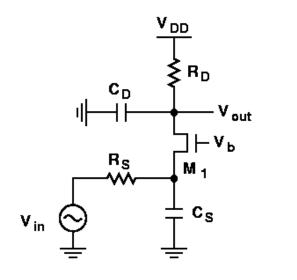


- If a source follower is driven by a large resistance, then it exhibits substantial inductive behavior.
- This effect manifests itself as ringing in the step response. If it drive a large C<sub>L</sub>.

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#### **Common-Gate Stage**

Neglect channel length modulation effect



$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S} \frac{1}{\left(1 + \frac{C_S}{g_m + g_{mb} + R_S^{-1}}s\right)\left(1 + R_D C_D s\right)}$$

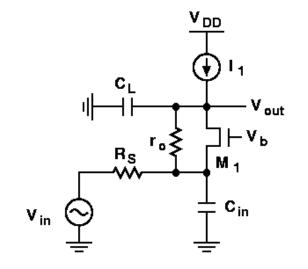
- □⊢𝔥
   ▷ It exhibits no Miller multiplication of capacitances,
   𝑘₁
   potentially achieving wide band.
   □ 𝔅 𝔅
   ▷ Low Input impedance may load the preceding stage.

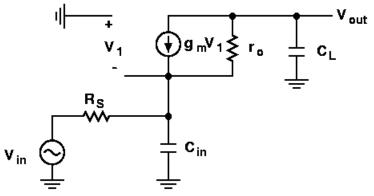
  - The DC level of the input signal must be quite low.

*if* 
$$\lambda \neq 0$$
,  $Z_{in} \approx \frac{Z_L}{(g_m + g_{mb})r_0} + \frac{1}{g_m + g_{mb}}$ ,  $Z_L = R_D || [1/sC_D]$ 

• Since  $Z_{in}$  now depends on  $Z_i$ , it is difficult to associate a pole with the input node.

#### Input Impedance of Common Gate





$$(-V_{out}C_{L}s + V_{1}C_{in}s)R_{s} + V_{in} = -V_{1}$$

$$V_{1} = -\frac{-V_{out}C_{L}sR_{s} + V_{in}}{1 + C_{in}R_{s}s}, \quad r_{0}(-V_{out}C_{L}s - g_{m}V_{1}) - V_{1} = V_{out}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{1 + g_{m}r_{0}}{r_{0}C_{L}C_{in}R_{s}s^{2} + [r_{0}C_{L} + C_{in}R_{s} + (1 + g_{m}r_{0})C_{L}R_{s}]s + 1}$$

$$\frac{V_{out}}{V_{in}} = 1 + g_{m}r_{0}(@ \text{ Low Freq} : s = jw = 0)$$

$$\blacktriangleright \text{ The body effect can be included by simply replacing } g_{m} \text{ with } g_{m} + g_{mb}.$$

$$Z_{in} \approx \frac{Z_{L}}{(g_{m} + g_{mb})r_{0}} + \frac{1}{g_{m} + g_{mb}}$$

$$Z_{L} = \frac{1}{sC_{L}}, \quad Z_{in} = \frac{1}{g_{m} + g_{mb}} + \frac{1}{sC_{L}} \cdot \frac{1}{(g_{m} + g_{mb})r_{0}}$$
As  $C_{L}$  or  $s$  increases,  $Z_{in} = \frac{1}{g_{m} + g_{mb}}$ , independent of  $C_{L}$ 

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#### Cascode Stage

- Common source + common gate gain stage.
- Increase the voltage gain of amplifiers and the output impedance of current source.

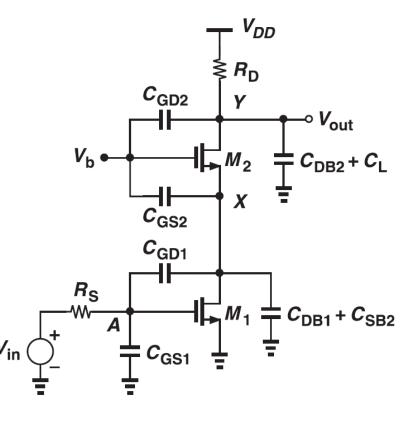
$$Z_{out} = (1 + g_{m2} r_{O2}) Z_X + r_{O2}$$

- Providing shielding suppressing the Miller effect.
- The low frequency gain from M<sub>1</sub> gate to drain

$$A_{v} = -\frac{g_{m1}}{g_{m2} + g_{mb2}} \approx -1$$

• The input pole is at

$$\omega_{p,A} = \frac{1}{R_{S} \left[ C_{GS1} + \left( 1 + \frac{g_{m1}}{g_{m2} + g_{mb2}} \right) C_{GD1} \right]}$$



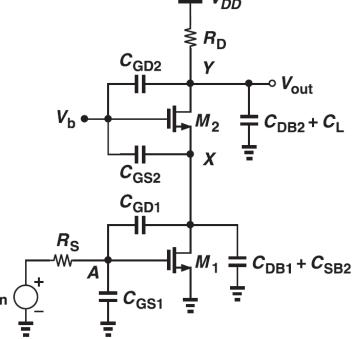
#### Cascode Stage

 The total capacitance at node X is (typically chosen farther from the origin than the other two)

$$C_{X} = 2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}$$
$$\omega_{p,X} = \frac{1}{R_{X}C_{X}} = \frac{g_{m2} + g_{mb2}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}$$

• The output pole at node Y is

$$\omega_{p,Y} = \frac{1}{R_D \left( C_{DB2} + C_L + C_{GD2} \right)}$$

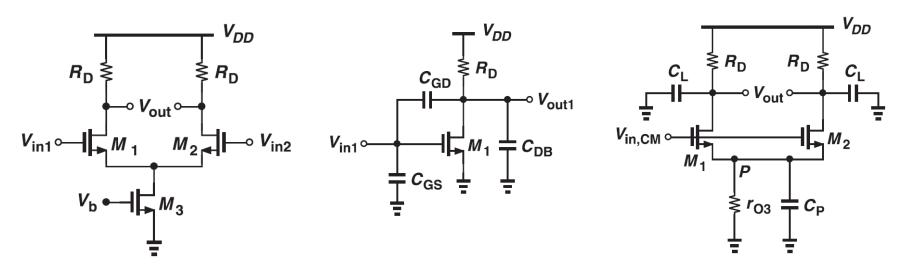


Output impedance of a cascode current source (neglect C<sub>γ</sub>, C<sub>GD1</sub>)

$$Z_{out} = (1 + g_{m2}r_{O2})Z_X + r_{O2}, Z_X = r_{O1} || (C_X s)^{-1}$$
  
pole =  $(r_{O1}C_X)^{-1}$ 

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#### **Differential Pair**

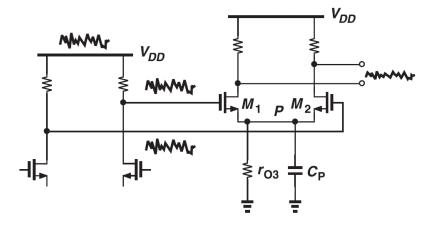


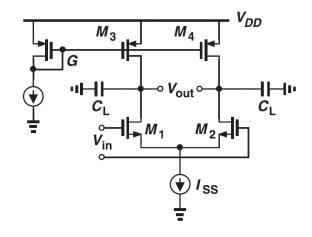
- For differential signals, the response is identical to that of a CS stage.
- For CM gain, the total capacitance at node P determines the HF gain.

$$A_{\nu,CM} = -\Delta g_m \left[ R_D \parallel \left( \frac{1}{C_L s} \right) \right] / \left\{ \left( g_{m1} + g_{m2} \right) \left[ r_{O3} \parallel \left( \frac{1}{C_P s} \right) \right] + 1 \right\}$$

- If the output pole >> the pole at the tail node of current source, the CM rejection of the circuit degrades considerably at high frequencies (HF).
- If the V<sub>DD</sub> contains HF noise and the circuit exhibits mismatches, the resulting CM disturbance at node P leads to a differential noise component at the output.

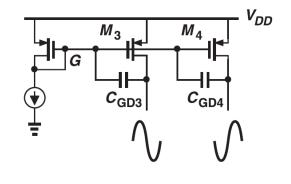
# Effect of High-Frequency Supply Noise

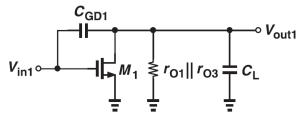




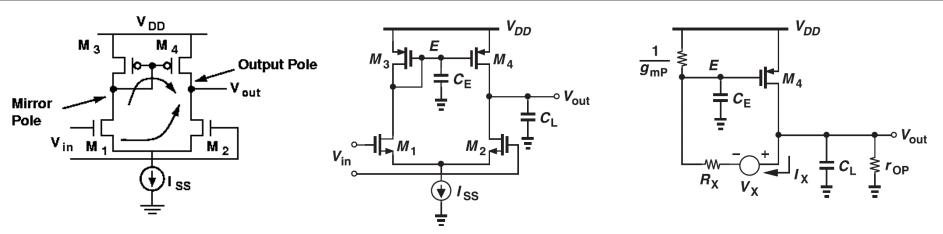
- Trade-off between voltage headroom and CMRR.
- To minimize voltage headroom,  $M_{tail} \uparrow, C_p \uparrow$ , high frequency CMRR  $\downarrow$ .
- For differential output signals, C<sub>GD3</sub> and C<sub>GD4</sub> conduct equal and opposite currents to G, making this node an AC ground.
- The dominant pole is at

$$\omega_p = \frac{1}{\left[r_{O1} \parallel r_{O3}\right]C_L}$$





#### **DP with Active Current Mirror**



- This topology contains two signal paths with different transfer functions.
- Pole at node *E* (*Mirror pole*)

$$\omega_{pE} = \frac{g_{m3}}{C_E}, \quad C_E \approx C_{GS3} + C_{GS4} + C_{DB3} + C_{DB1} + 2C_{GD1} + g_{m4} (r_{O4} || r_{O2}) C_{GD4}$$

$$V_X = g_{mN} r_{ON} V_{in}, \quad R_X = 2r_{ON}, \quad V_E = (V_{out} - V_X) \frac{(C_E s + g_{mP})^{-1}}{(C_E s + g_{mP})^{-1} + R_X}, \quad -g_{m4} V_E - I_X = V_{out} (sC_L + r_{OP}^{-1})$$

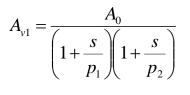
$$\frac{V_{out}}{V_{in}} = \frac{g_{mN} r_{ON} r_{OP} (2g_{mP} + sC_E)}{2r_{OP} r_{ON} C_E C_L s^2 + [(2r_{ON} + r_{OP})C_E + r_{OP} (1 + 2g_{mP} r_{ON})C_L]s + 2g_{mP} (r_{ON} + r_{OP})}$$

$$\omega_{P1} \approx \frac{2g_{mP}(r_{ON} + r_{OP})}{(2r_{ON} + r_{OP})C_E + r_{OP}(1 + 2g_{mP}r_{ON})C_L} \approx \frac{1}{(r_{ON} \parallel r_{OP})C_L} \quad \text{if} \quad 2g_{mP}r_{ON} >> 1 \qquad \omega_{P2} \approx \frac{g_{mP}}{C_E}$$

Analog IC Analysis and Design

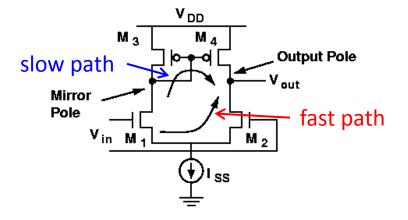
# **DP with Active Current Mirror**

- To find zero
  - Consider that the circuit consists of a "slow path" ( $M_1$ ,  $M_3$ , and  $M_4$ ) in parallel with a "fast path" ( $M_1$ , and  $M_2$ )
  - Slow path



- Fast path

$$A_{\nu 2} = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)}$$



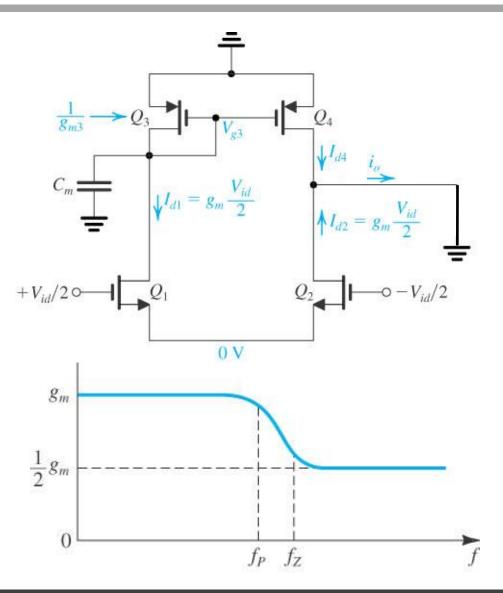
We have

$$\frac{V_{out}}{V_{in}} = A_{v1} + A_{v2} = \frac{A_0}{1 + \frac{s}{p_1}} \left( 1 + \frac{1}{1 + \frac{s}{p_2}} \right) = \frac{A_0 \left( 2 + \frac{s}{p_2} \right)}{\left( 1 + \frac{s}{p_1} \right) \left( 1 + \frac{s}{p_2} \right)} \implies z = 2p_2$$

 Fully differential pair has no mirror pole, which is better than differential-tosingle ended amp.

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# G<sub>m</sub> Frequency Response



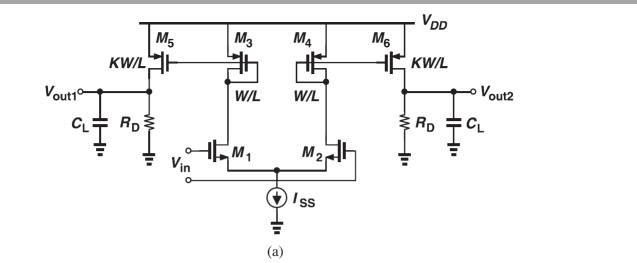
At low frequency:  $C_m$  is OPEN  $i_{d4} = i_{d1} = g_m \frac{V_{id}}{2}, i_{d2} = g_m \frac{V_{id}}{2}$   $i_o = i_{d4} + i_{d2} = g_m V_{id}$   $G_m = i_o / V_{id} = g_m$ At high frequency:  $C_m$  is SHORT

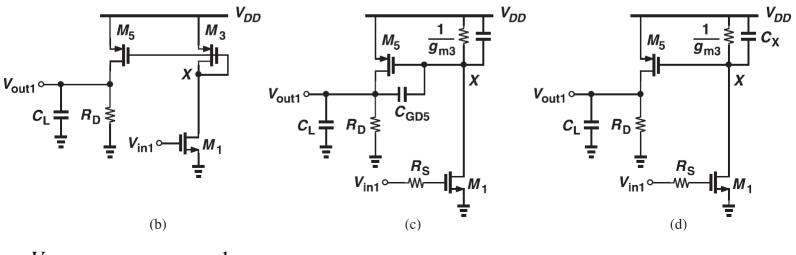
$$V_{g3} = 0, i_{d4} = 0, i_o = i_2 = g_m \frac{V_{id}}{2}$$
$$G_m = i_o / V_{id} = g_m / 2$$

 $G_{m} \text{ transfer function}$   $G_{m} \equiv \frac{i_{o}}{V_{id}} = g_{m} (\frac{1 + sC_{m} / 2g_{m3}}{1 + sC_{m} / g_{m3}})$   $f_{P} = \frac{g_{m3}}{2\pi C_{m}}, f_{Z} = \frac{2g_{m3}}{2\pi C_{m}}$ 

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# **Fully Differential Amplifier**





 $\frac{V_{out1}}{V_X}(s) = -g_{m5}R_D \frac{1}{1 + sR_DC_L} \qquad C_X \approx C_{GS3} + C_{GS5} + C_{DB3} + C_{GD5}(1 + g_{m5}R_D) + C_{DB1}$ 

#### **Analog IC Analysis and Design**