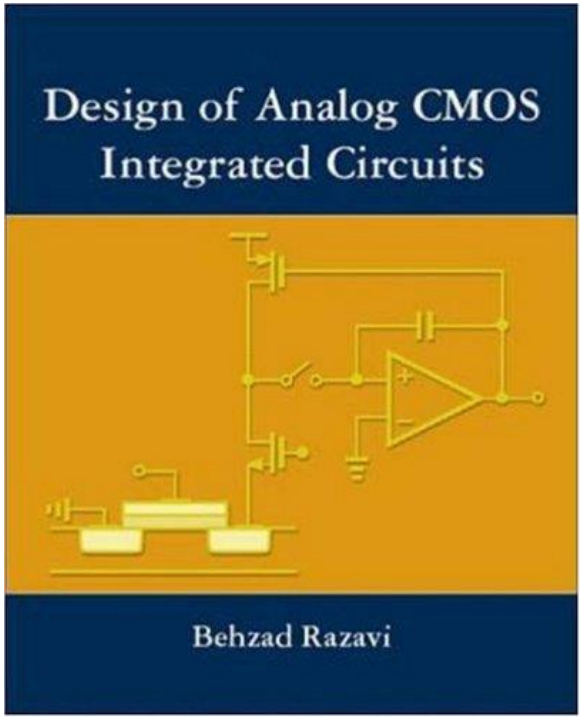
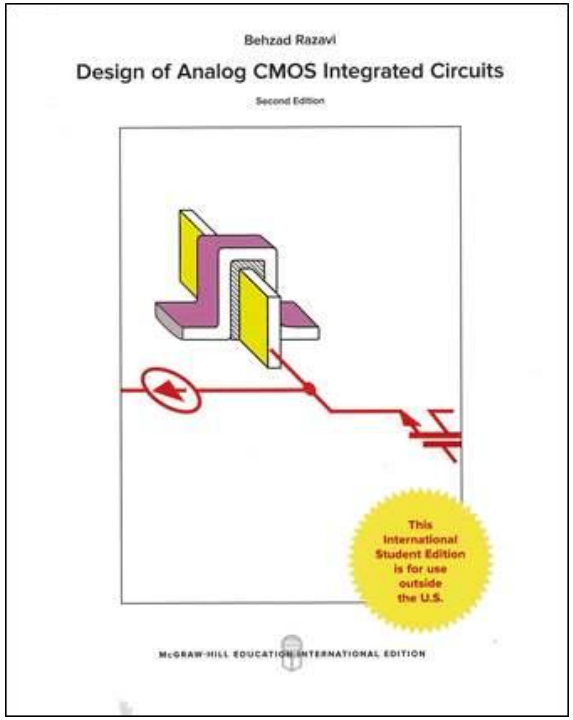
Analog Integrated Circuits Analysis and Design I

EE3235



1/e 2001



2/e 2016

Lecturer & TA

- EE3235 Analog Integrated Circuits Analysis and Design I
- Class room: 台達館 216, T7T8R7
- Instructor: 謝志成 老師
  - Office hours: Thu. 1:30~2:20pm or by reservation. @ 台達館 837
  - Email : cchsieh@ee.nthu.edu.tw
  - Website: http://www.ee.nthu.edu.tw/cchsieh
- Teaching Assistant :
  - 謝頌恩 shakesong@hotmail.com
  - 張福文 farnkgogo@gmail.com
  - 林宜玄 s101061225@m101.nthu.edu.tw

Course Description

- Course description:
  - This is a fundamental course for analysis and design analog integrated circuits. It covers quantitative analyses, design considerations and system applications from circuit and physical viewpoints.
- Topics:
  - Modern VLSI technologies, device operations and models.
  - Elementary gain stages.
  - Current sources.
  - Frequency responses.
  - Feedback, stability and compensation.
  - Operational amplifiers.
  - Bandgap references.

Syllabus

– Week 1	Introduction, CMOS and BJT technologies
– Week 2	BJT / MOS Device and modeling
– Week 3-5	Single-stage amplifier, Multi-stage amplifier
– Week 6-7	Differential configuration
– Week 8	Current mirrors
– Week 9	Frequency response
2017.04.11	Midterm (Tue, 3:30 pm)
– Week 10	Noise
– Week 11-12	Feedback
– Week 13	Introduction of op-amp
– Week 14	Two-stage op-amp, Differential op-amp
– Week 15	Design technique for op-amp
– Week 16	Stability and compensation
– Week 17-18	Voltage and current source
2017.06.13	Final Exam (Tue, 3:30 pm)

Grading

- Homework 25%
  - The homework will be assigned at every Thur. class, and it should be finished and hand-in at the following Thur.'s class. Schedule delay is not allowed except it's with instructor's approval.
  - CAD tools are required for homework.
  - CAD tool introduction will be arranged in proper time.
- Midterm 25% @ week 9 : 2.5hrs (2017/4/11)
- Final Exam 30% @ week 18 : 3hrs (2017/6/13)
- Final Project 20% @ 2017/6/20 : 10mins/team (2 students/team)
- In-Class performance

Design and Analysis

- A circuit analysis and design is not "black magic“ !
- Circuit **analysis**
  - The technique to decompose a large circuit into manageable pieces.
  - The analysis is based on the simplest, but sufficiently accurate models.
  - Each circuit has one solution.
- Circuit **design**
  - The art to synthesize circuits that is based on many experience of extensive analysis.
  - One set of specifications has many solutions.
  - Design skills are best acquired through "learning by doing“.
- So, we have **5 practical homeworks and one design project** !!

Goal & Vision

- Touch, Explore, and Study Analog circuit ….
- Then Think, Act and Like to be an analog designer. Or… NOT to be an analog designer.
- Know how and where to dig Knowledge & Skill inside when necessary.
- Homework & Project are the vehicles to train your logistic thinking, design skill and team work altitude.
- You can study hard by yourself… however…

! Interact with me & TA & classmates

as more as you can is the best way to learn !

CHAPTER 1

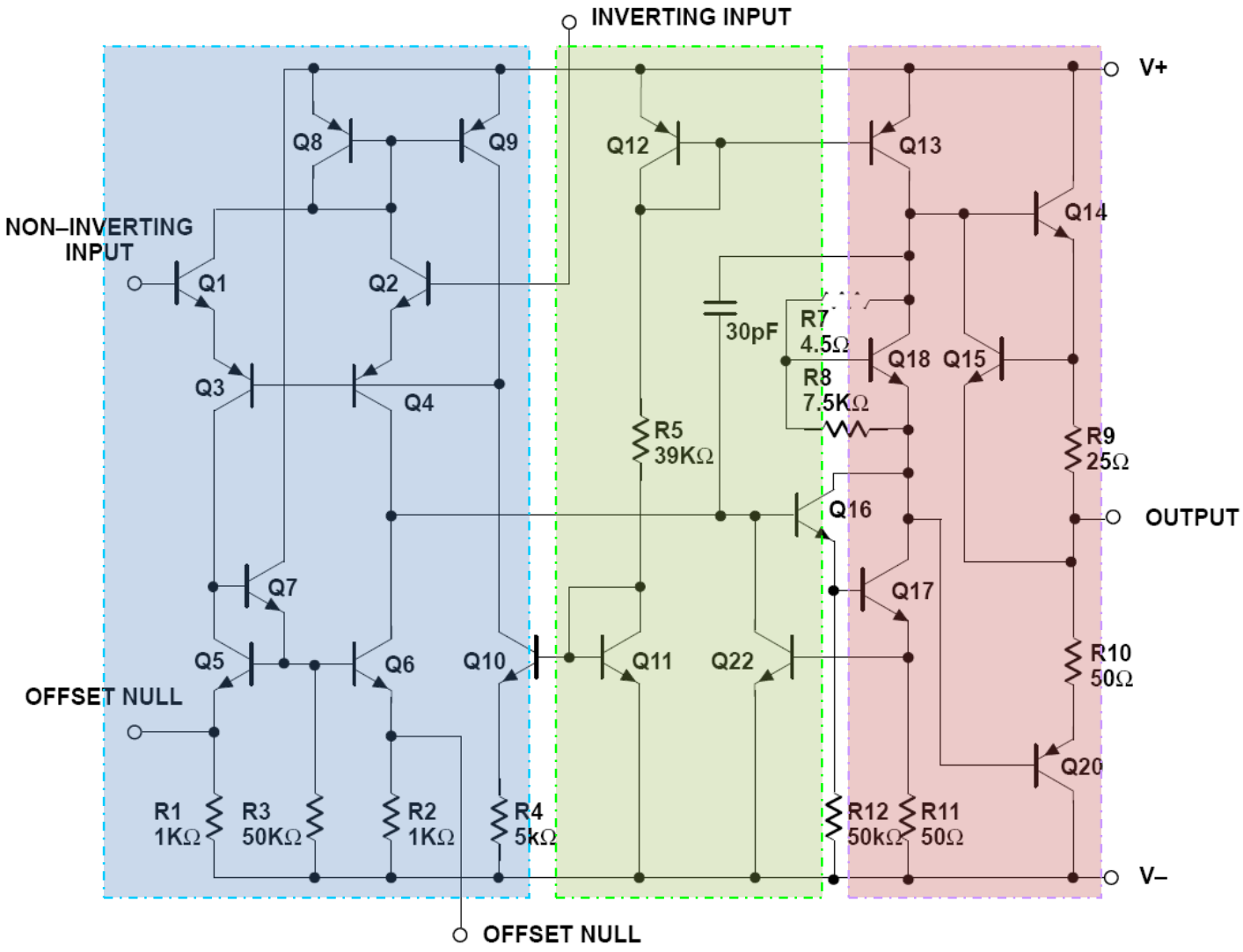
Introduction, CMOS Technologies

Outline

1. **Introduction**
2. MOS Technologies

This is Analog Circuit ??

Op-741

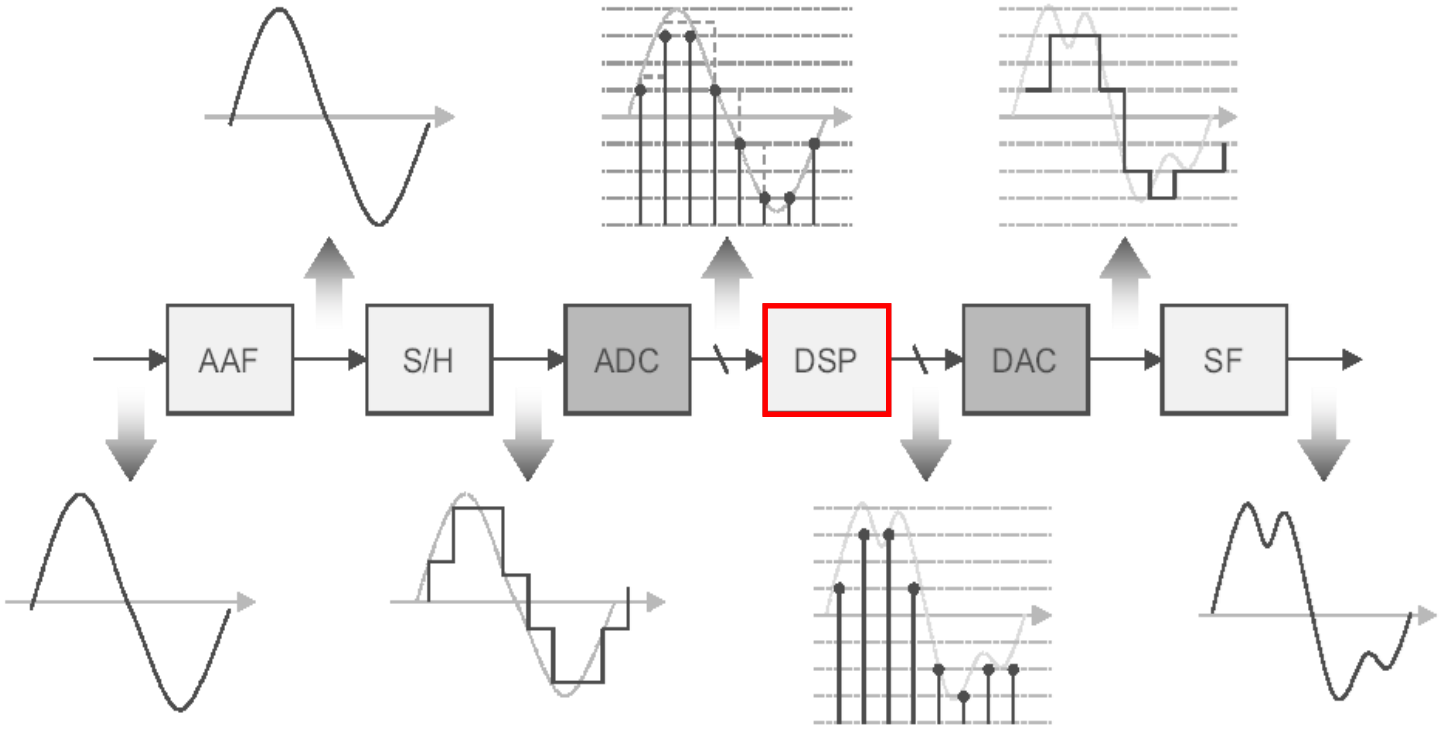


What the $@# is this?

Find the components you need

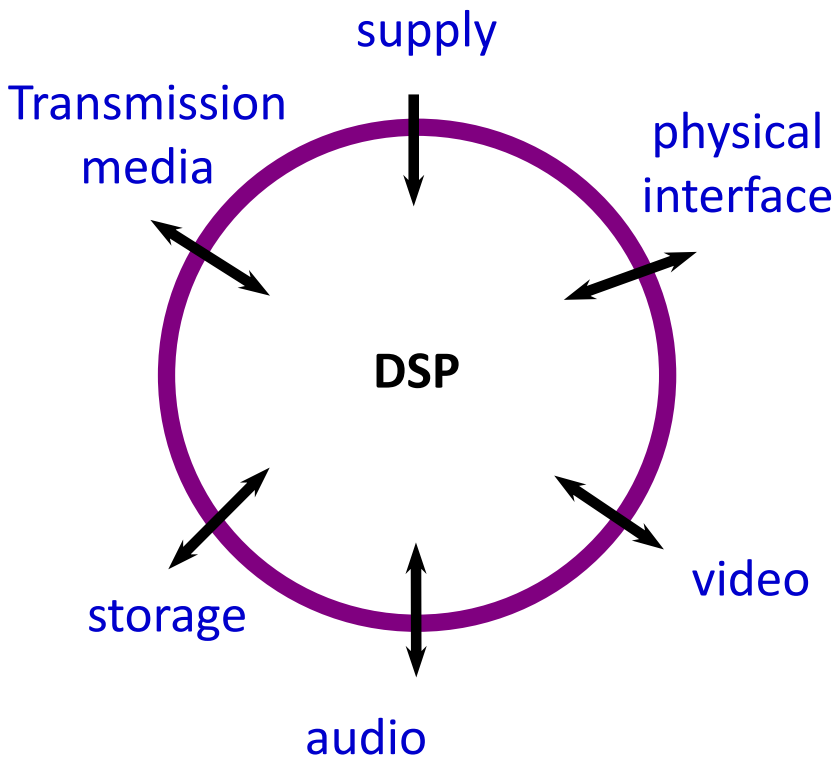
You can make it!

What is Analog ?



- Always continuous in amplitude
- Either continuous in time (s-domain)
  or discrete in time (z-domain)

Where is Analog ?



- Amplification
- Filtration
- Supply
- Conversion (A/D, D/A)
- Translation (freq, time, volt …)

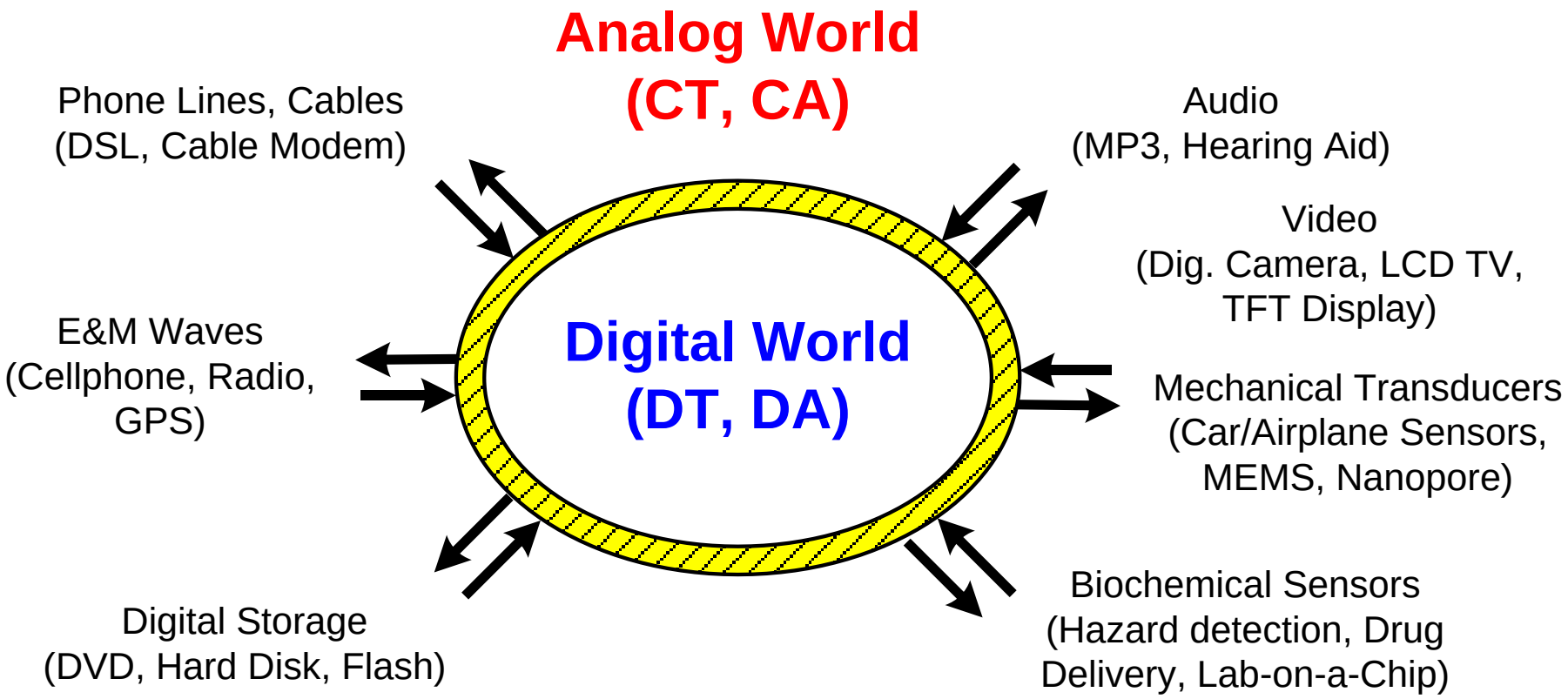
Advantages of Digital VLSI

- Noise immunity, robustness
- Unlimited precision or accuracy (depends on # of bits)
- Flexibility, programmability, and scalability
- Electronic design automation (EDA) tools widely available and successful
- Benefiting from **Moore's law** – "The number of transistors on a chip doubles every 18 months," *IEDM*, 1975
  - Cost/function drops 29% every year
  - That's 30X in 10 years

Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Why Need Analog?

Paul Gray's eggshell diagram



Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Challenges for Analog

- Sensitive to noise – SNR (signal-to-noise ratio)
- Subject to device nonlinearities – THD (total harmonic distortion)
- Sensitive to device mismatch and process variations
- Difficult to design, simulate, layout, test, and debug
- Inevitable, often limits the overall system performance
- Scaling scenario outlook
  - High-speed, low-resolution applications keep benefiting
  - High SNR design difficult to scale with low supply voltages

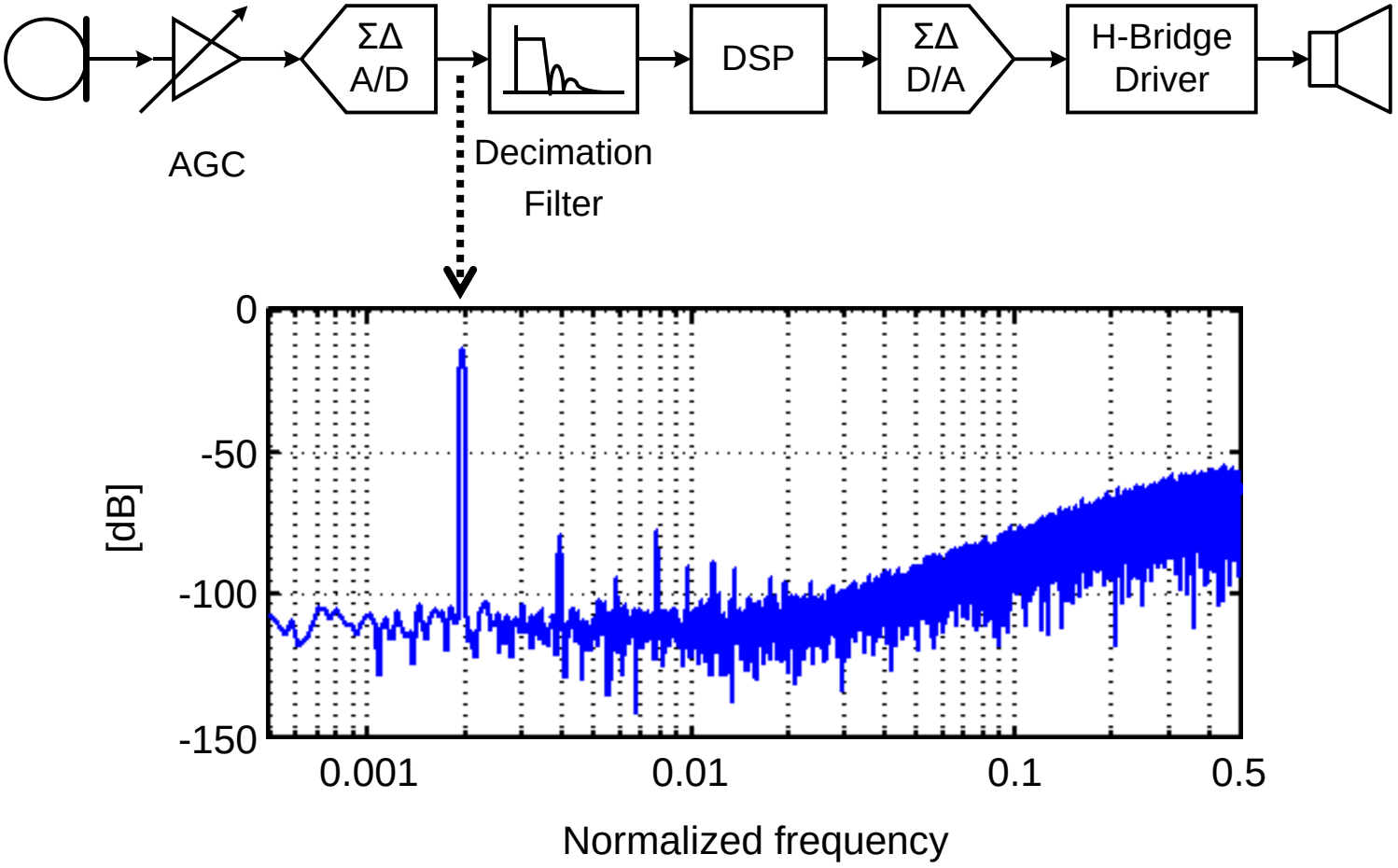
Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Analog Skills

- Operation point
  - ✓ bias voltage, current ….
- Large signal analysis
  - ✓ settling, slew rate, distortion ….
- Small signal model
  - ✓ gain, bandwidth, stability ….
- Practical issue in VLSI
  - ✓ variation, noise, temperature ….
- Cost estimation
  - ✓ technology, power, size, yield, package ….

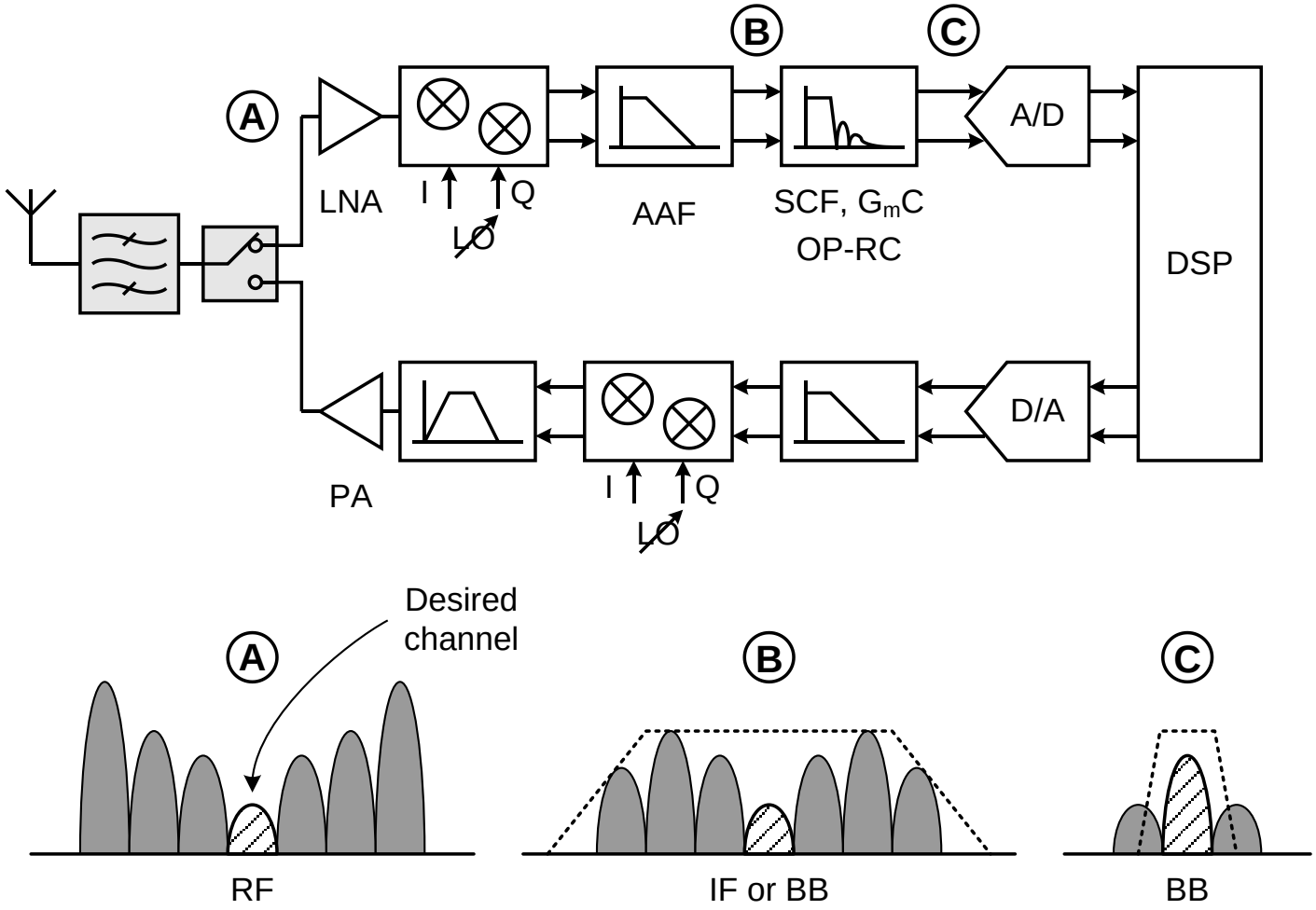
Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Example 1 – Mixed-Signal Hearing Aid



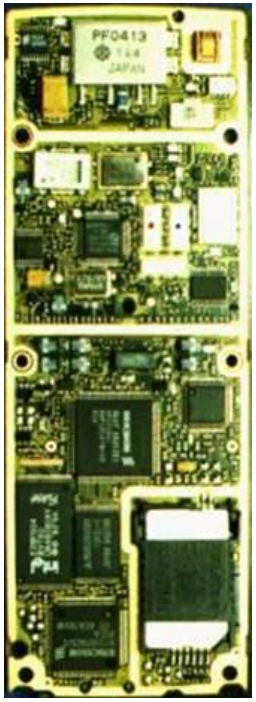
Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Example 2 – RF Transceiver



Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

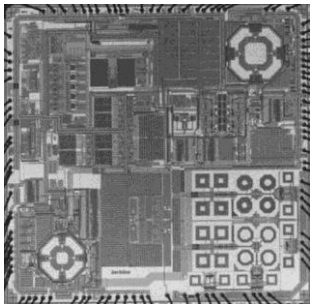
SoC – RF Transceiver



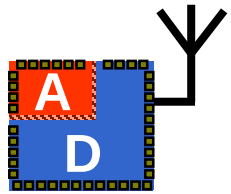
Ericsson CH388
(Hybrid, 1995)

- **Small form factor, high integration, low power, low cost**
- **Economy is the ultimate driving force**

Ericsson Bluetooth
(CMOS, 2001)



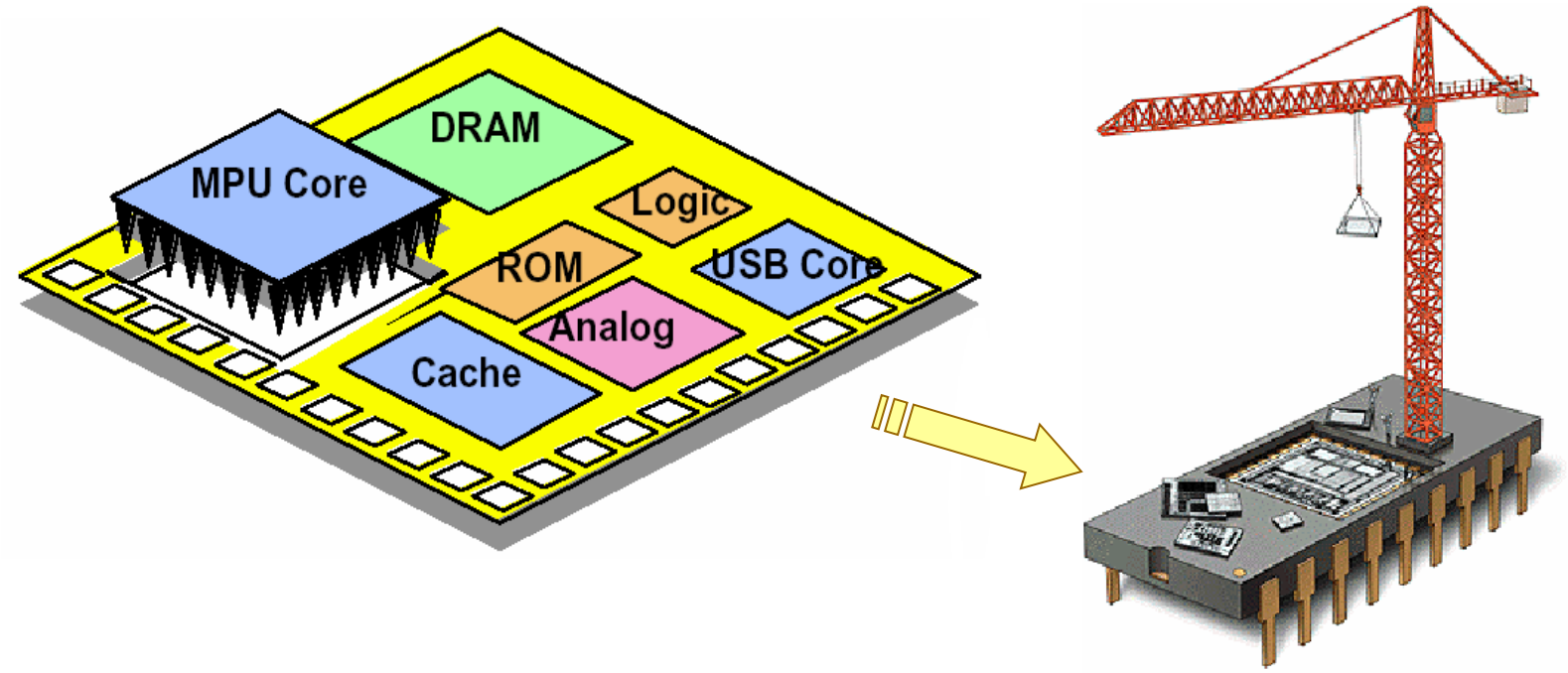
Berkäna GSM/GPRS
(CMOS, 2005)



Nano-CMOS?
Nanotube?

Past → **Present** → **Future**

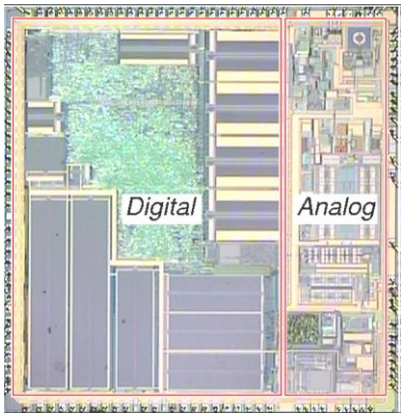
System-on-a-Chip

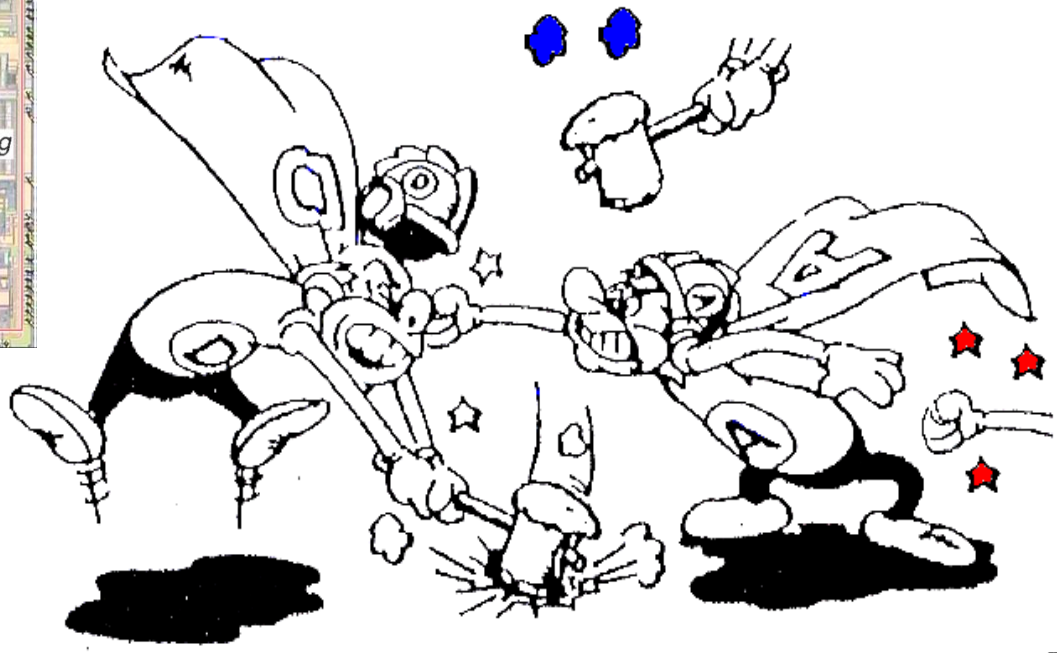


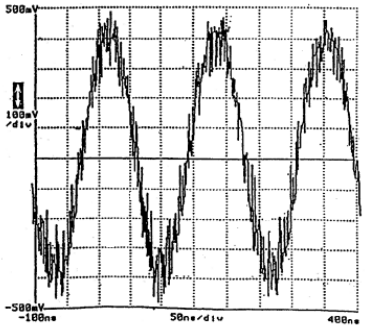
System integration is the way for the future IC development.

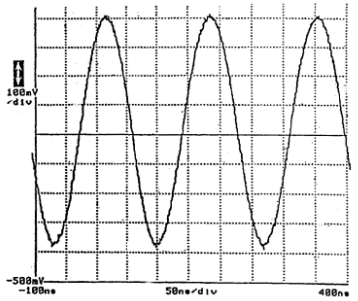
You need multi-domain knowledge to survive in the SOC era.

Analog in VLSI









- from ISSCC '92

For Future Nanometer Technology

⇨ Integration !

- Digital has to be treated as Analog.
- Analog needs the help from Digital.
- Parasitic effects become dominant.

Courses

Microelectronics

Communication / Control / Logic / …

VLSI Design

Analog ICs

Digital ICs

Digital Signal Processing

Semiconductor Devices

RF/MW Integrated Circuits

Communication Systems

Design Automation

Special Topics on VLSIs

Advanced Analog ICs

Mixed Signal ICs

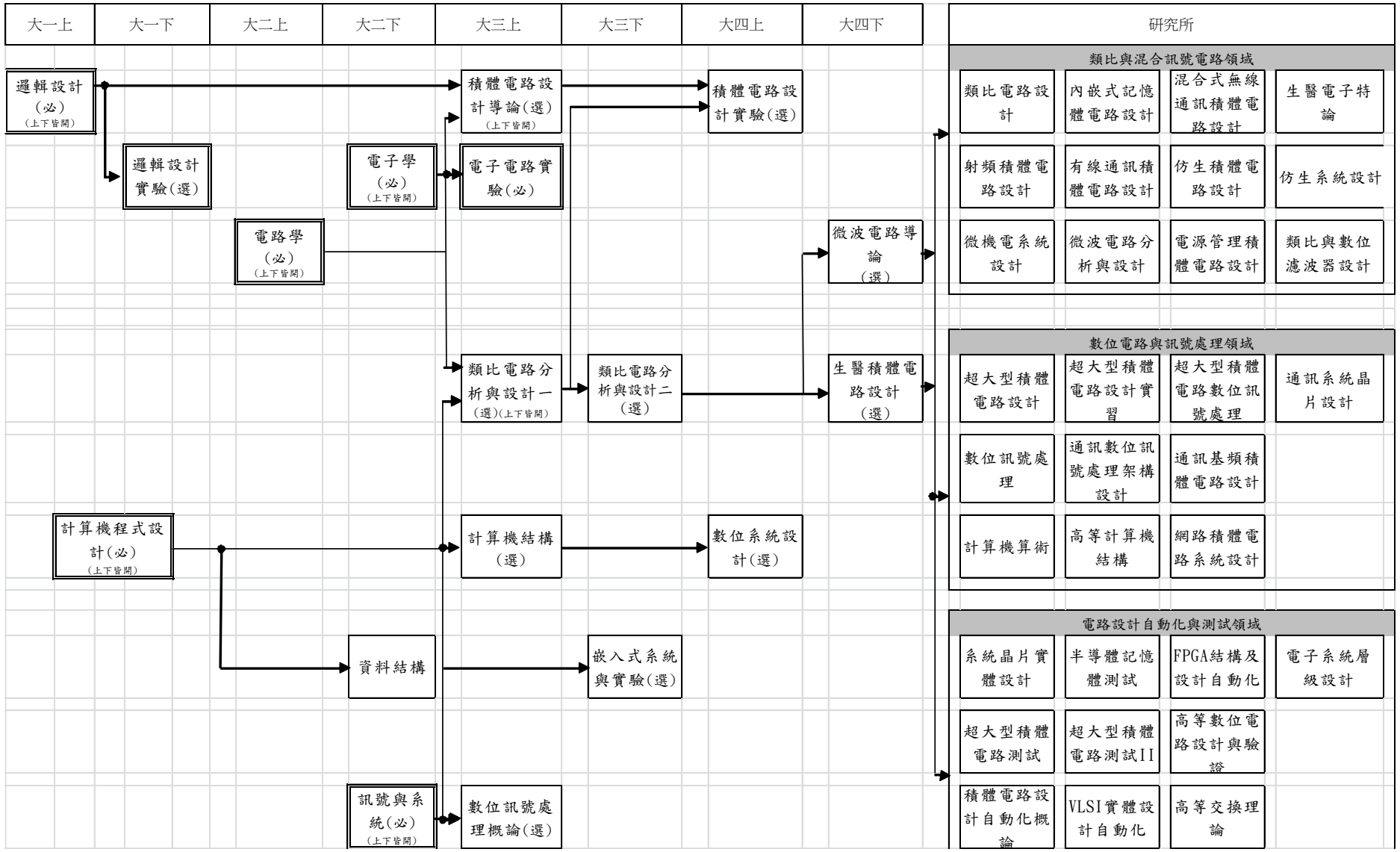
Communication VLSIs

VLSI Testing

IC Design Related Course Plan

建議時程	類別	課名課號				
大一	入門課程	邏輯設計 EE2280				
		邏設實驗 EE2230	計算機程式語言 EE2310			
大二	核心課程	電子學 EE2250	電路學 EE2210	資料結構 EE2410		
		電子學 EE2250	數位電路分析與設計 EE3230	訊號與系統 EE3610	電子電路實驗 EE2270	
大三		類比電路分析與設計II EE4280	積體電路設計導論 EE4290	計算機結構 EE3450	嵌入式系統與實驗 EE2405	數位系統設計
		類比電路分析與設計I EE3235	積體電路設計實習 EE4249	實作專題 EE3900	數位訊號處理概論	
大四/研究所	核心課程	超大型積體電路設計 EE5250*	超大型積體電路測試 EE6250	積體電路設計自動化 EE5265	*若無修過EE4290 則需修 EE5250	
	進階課程	影像感測器IC設計 EE5215	類比電路設計 EE5230	有線通訊IC設計 EE5285	內嵌式記憶體電路 EE5220	
		電源管理IC設計 EE5275	通訊基頻IC設計 EE5250	仿神經IC設計I,II EE6260,6261	系統晶片實體設計 EE5253	

電子電路設計學程


大一上
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大四上
大四下
研究所
邏輯設計（必）（上下皆開）
邏輯設計實驗(選)
電路學（必）（上下皆開）
電子學（必）（上下皆開）
積體電路設計導論(選)（上下皆開）
電子電路實驗(必)
積體電路設計實驗(選)
類比電路分析與設計一（選）(上下皆開)
類比電路分析與設計二（選）
微波電路導論（選）
生醫積體電路設計（選）
計算機程式設計(必)（上下皆開）
計算機結構（選）
數位系統設計(選)
資料結構
嵌入式系統與實驗(選)
訊號與系統(必)（上下皆開）
數位訊號處理概論(選)
類比與混合訊號電路領域
類比電路設計
內嵌式記憶體電路設計
混合式無線通訊積體電路設計
生醫電子特論
射頻積體電路設計
有線通訊積體電路設計
仿生積體電路設計
仿生系統設計
微機電系統設計
微波電路分析與設計
電源管理積體電路設計
類比與數位濾波器設計
數位電路與訊號處理領域
超大型積體電路設計
超大型積體電路設計實習
超大型積體電路數位訊號處理
通訊系統晶片設計
數位訊號處理
通訊數位訊號處理架構設計
通訊基頻積體電路設計
計算機算術
高等計算機結構
網路積體電路系統設計
電路設計自動化與測試領域
系統晶片實體設計
半導體記憶體測試
FPGA結構及設計自動化
電子系統層級設計
超大型積體電路測試
超大型積體電路測試II
高等數位電路設計與驗證
積體電路設計自動化概論
VLSI實體設計自動化
高等交換理論

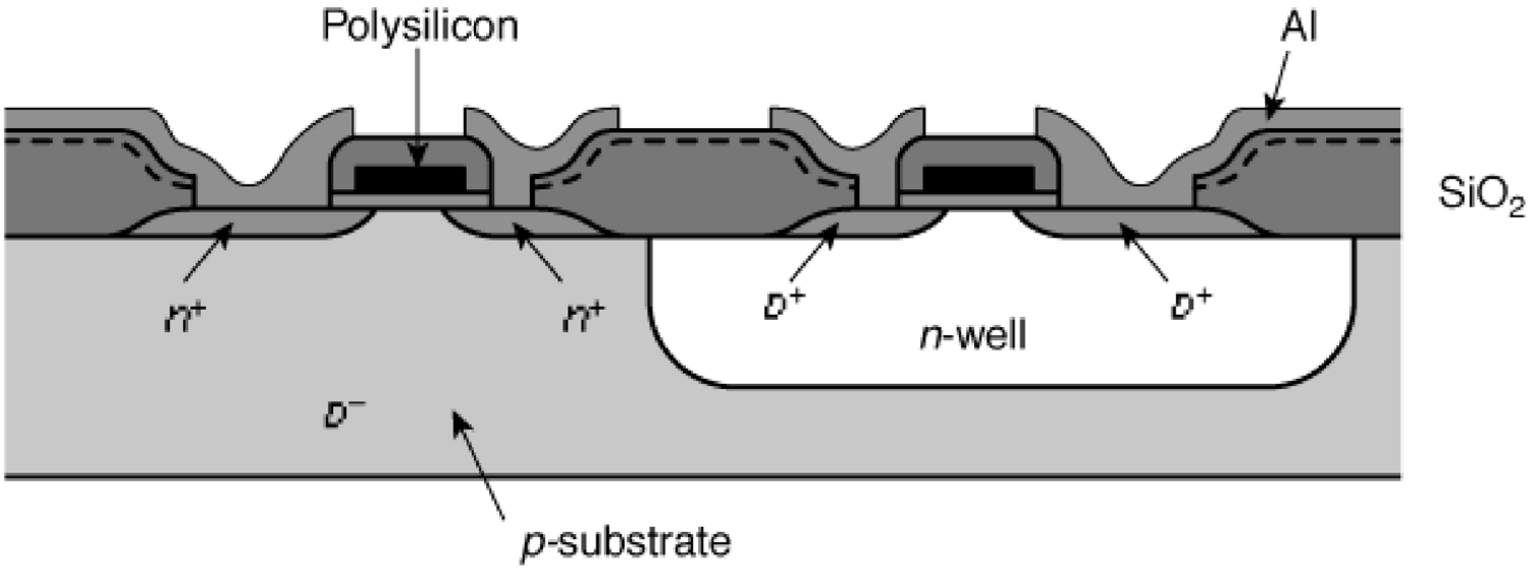
Outline

1. Introduction
2. **MOS Technologies**

Content

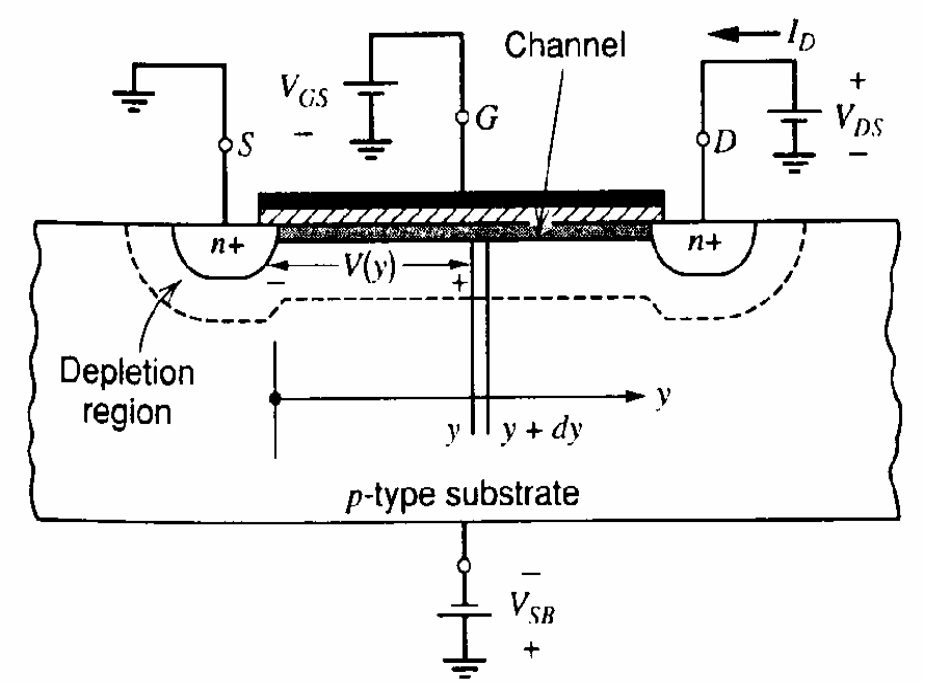
- CMOS Device Background
- CMOS Process Key Step
- CMOS Process Flow
- CMOS Passive Devices

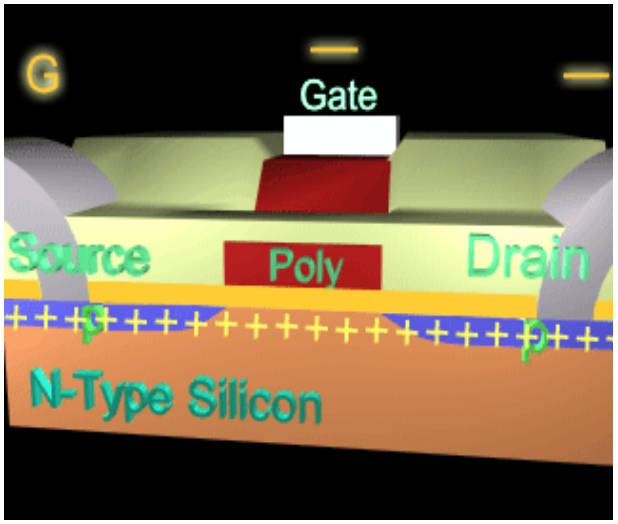
Generic CMOS

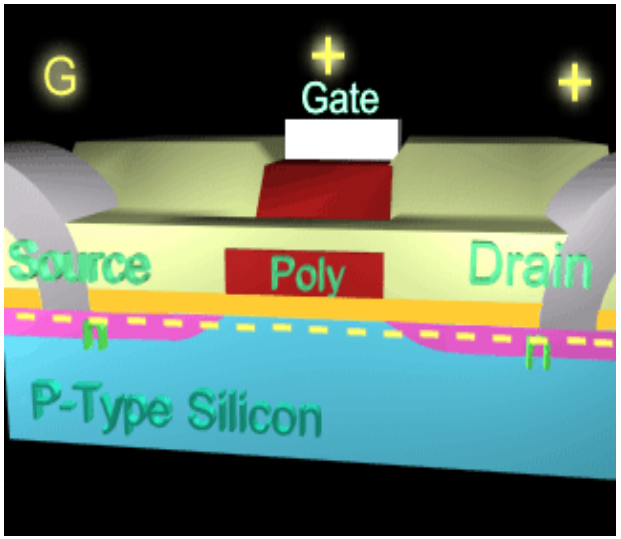


- This course concentrates on CMOS technology, as it is the mainstream of modern VLSI.

What is Semi-Conductor Device ?





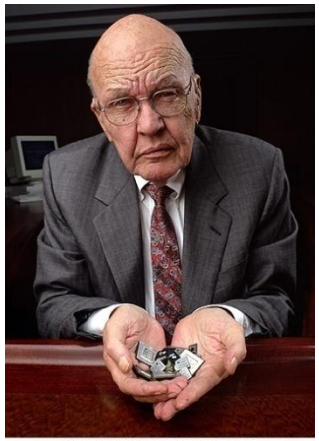


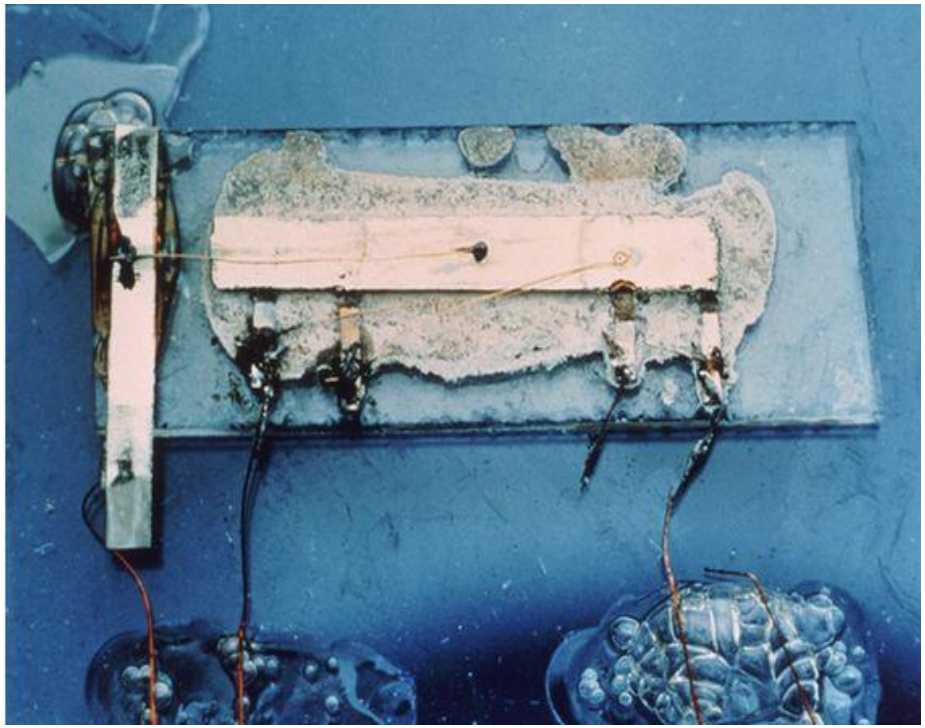
First IC

1952, Royal Radar Establishment of the British Ministry of Defense, Geoffrey W.A. Dummer, No successful implementation !!

1958,

Jack Kilby,
(2000 Nobile prize)
Texas Instruments


Courtesy Texas Instruments



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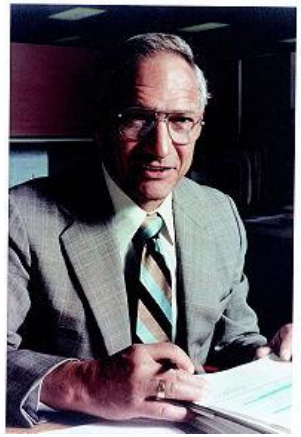
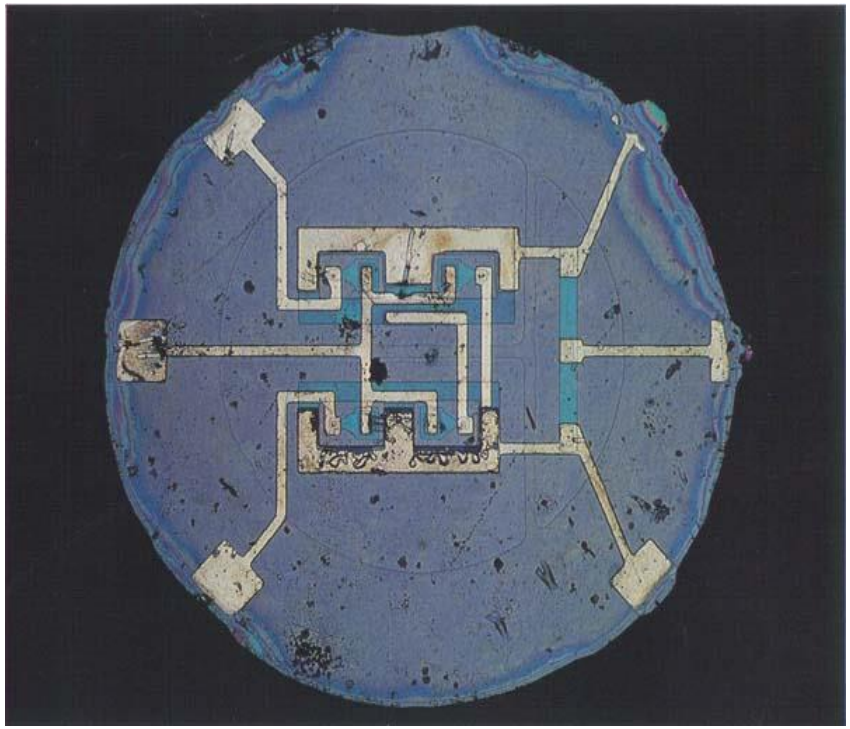


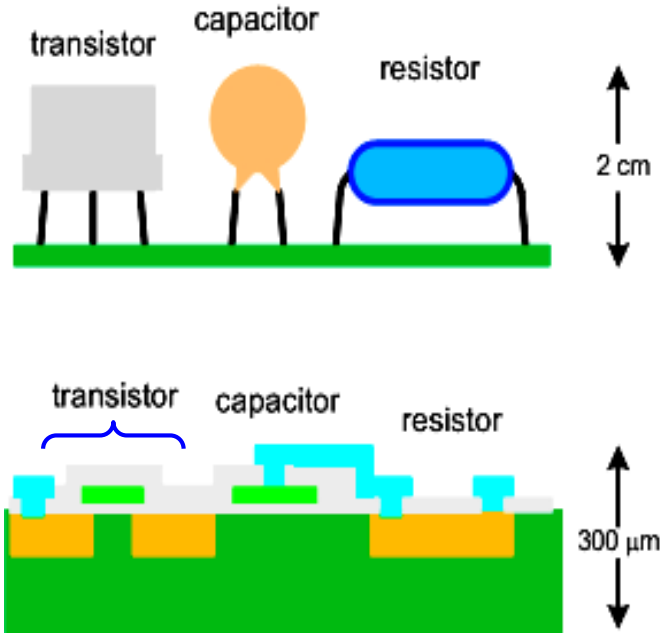
Robert Noyce,
Fairchild Semiconductor

http://en.wikipedia.org/wiki/Integrated_circuit

First Planar IC

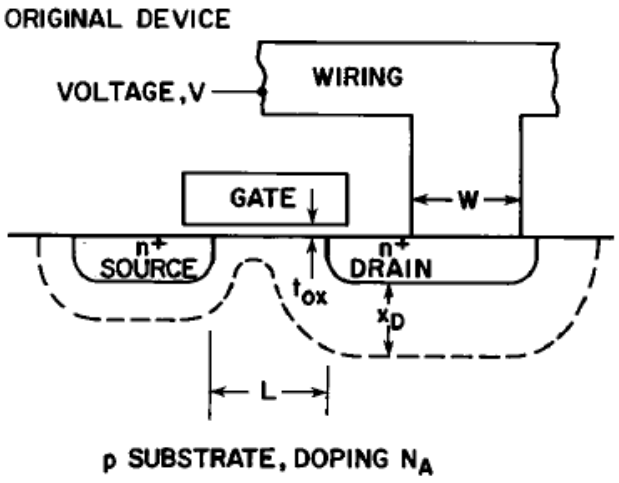
- Planar Technology Invented
  - Made by Robert Noyce of Fairchild in 1959





History of VLSI development is reviewed at http://smithsonianchips.si.edu/augarten/index.htm

Scaling !

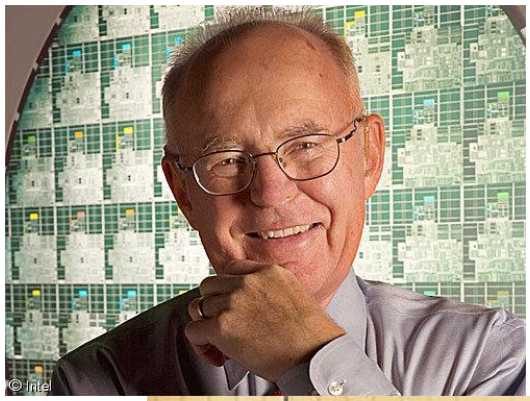


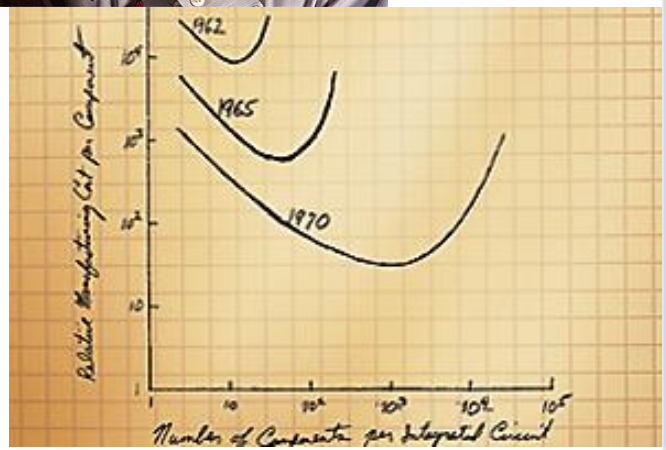
Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

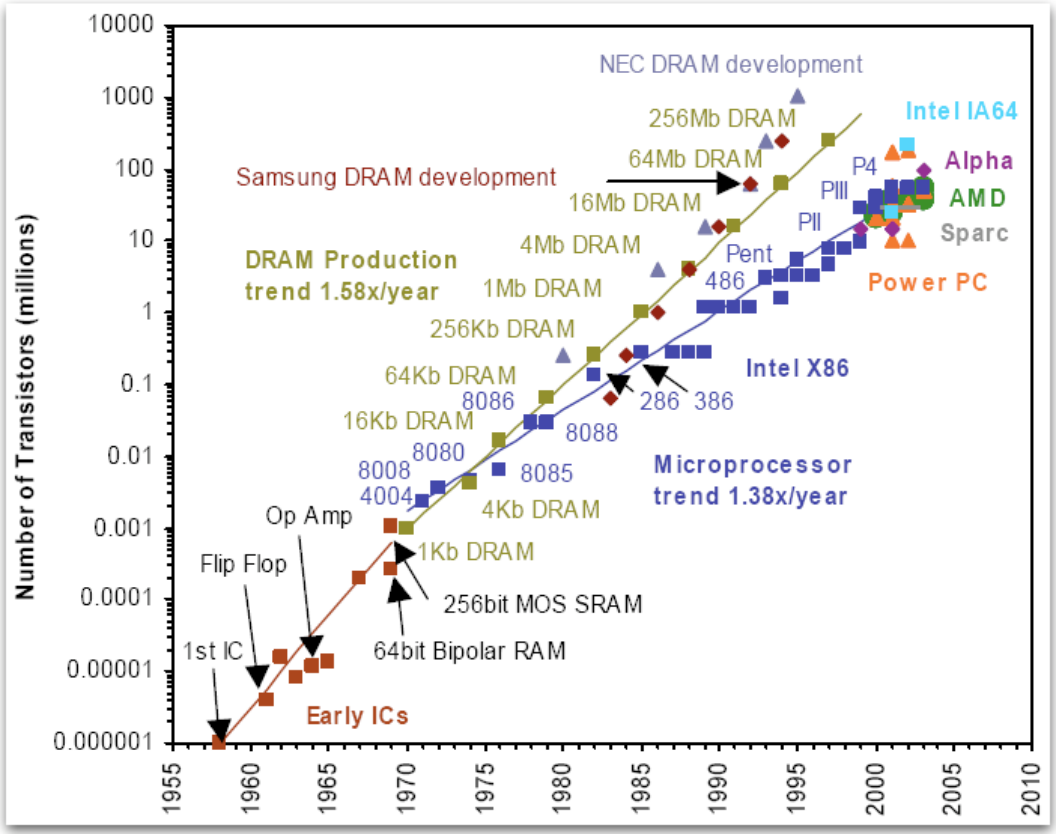
R. H. Dennard, et. al., IEDM. Dec. 1972.

Moore's Law

- Intel's co-founder Gordon Moore notices in 1964
  - # of transistors per chip doubled every 12 months
  - Slow down in the 1980s to every 18 months

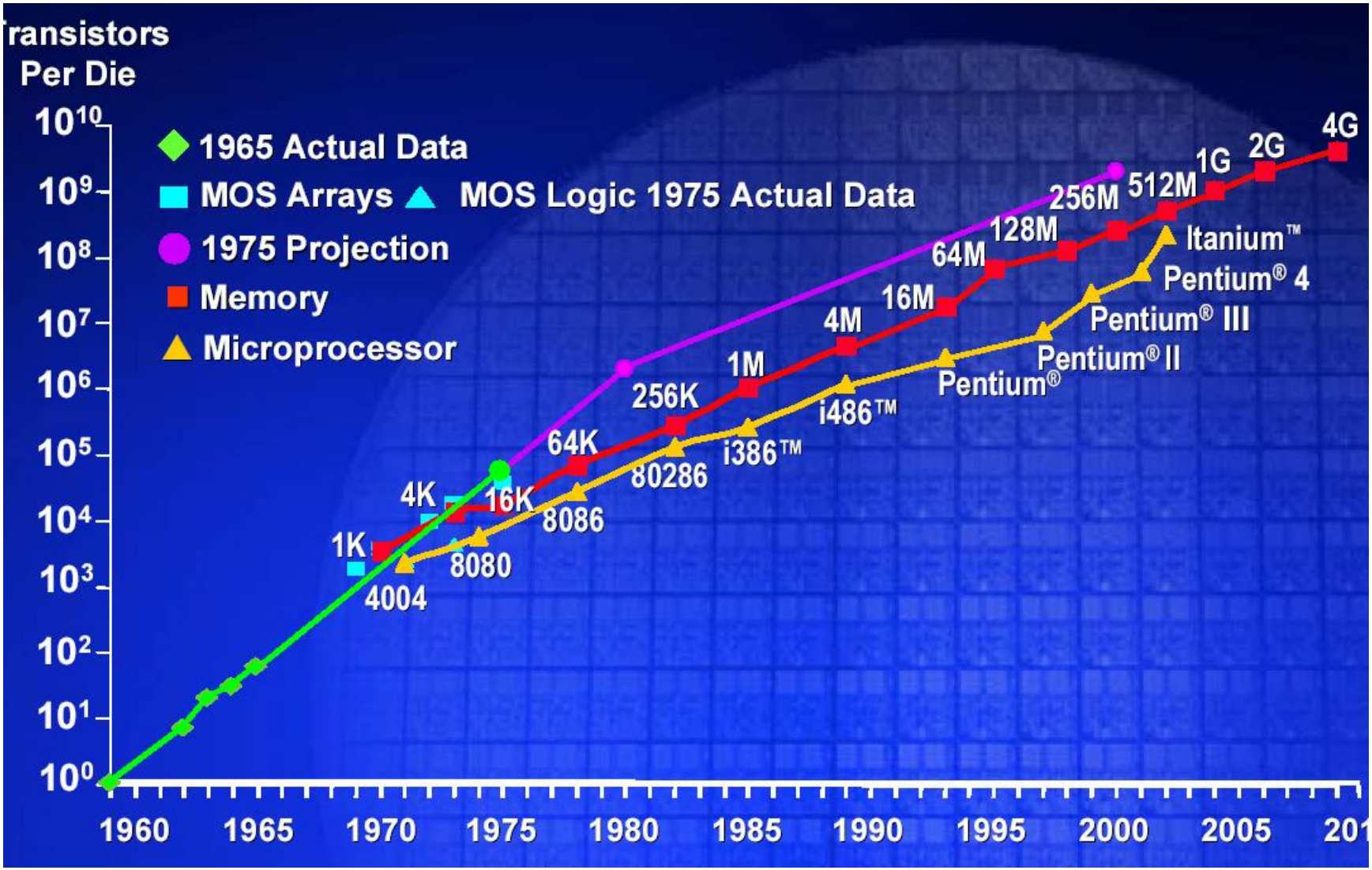




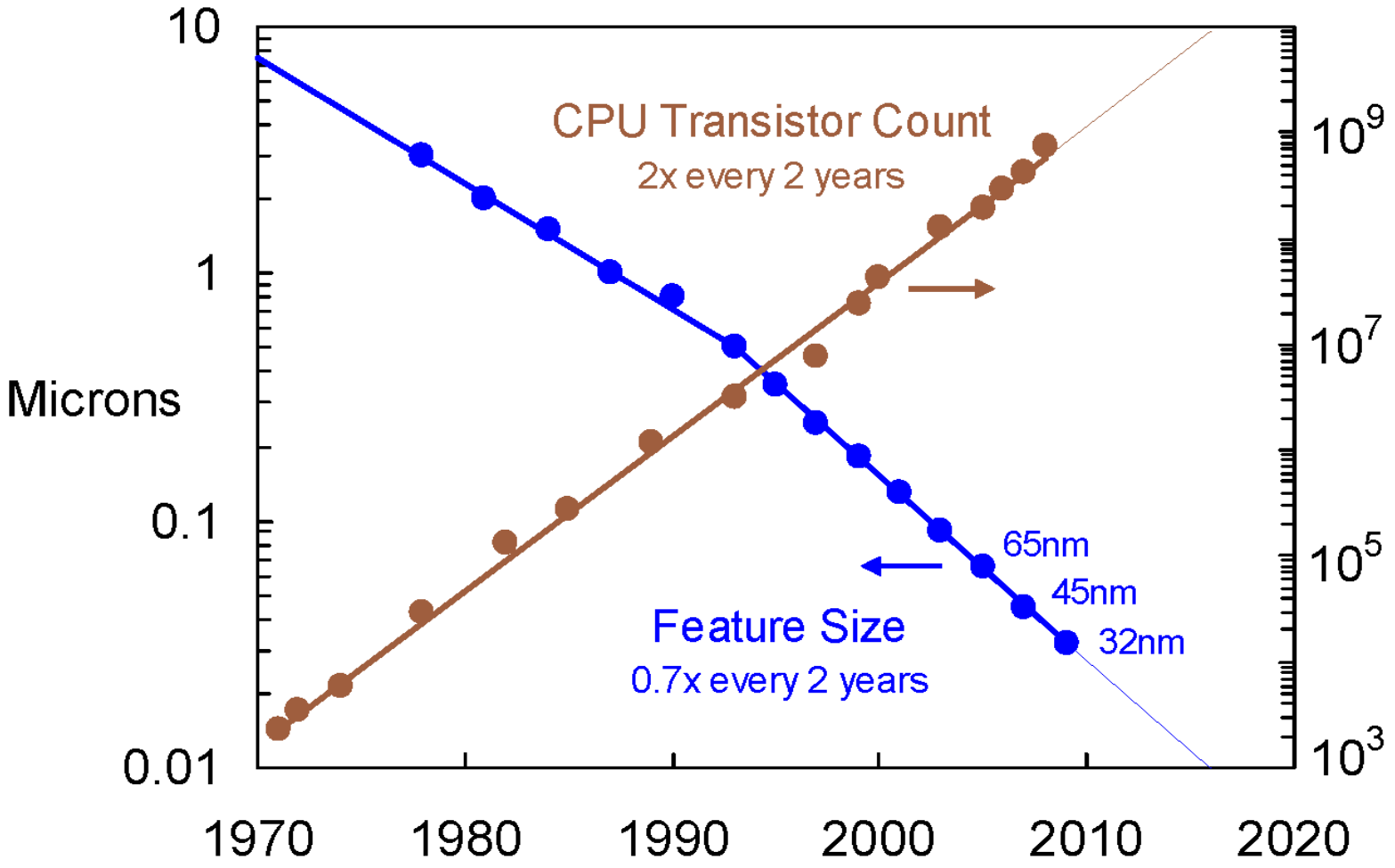


http://video.intel.com/?fr_story=c11efd497dce83c4ca94278fb30c7dfeb01aef16&rf=bm

Moore's Prospect



CPU Transistor # vs. Feature Size

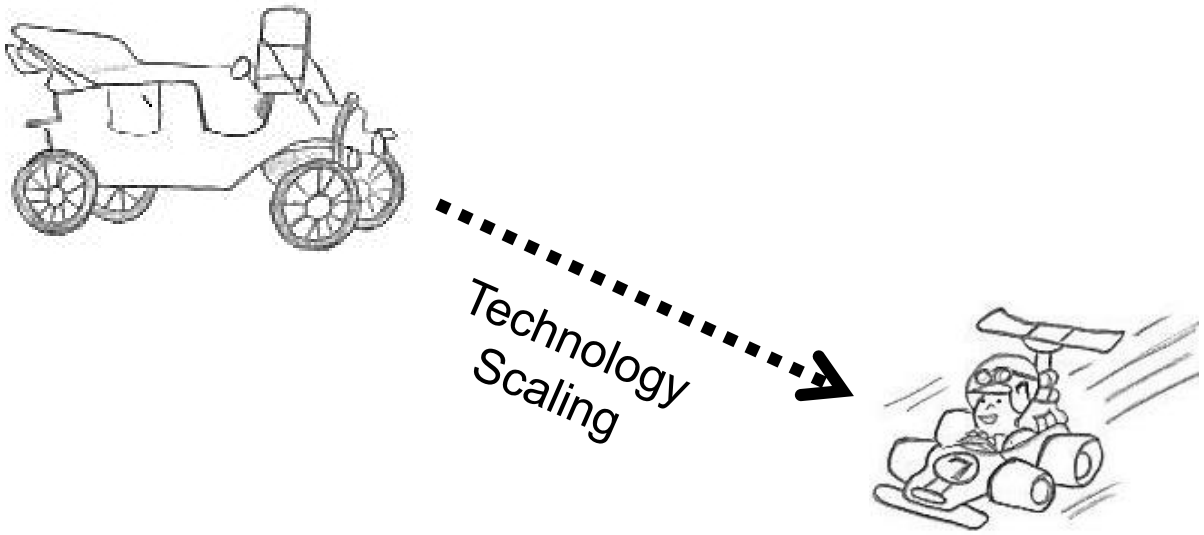


Mark Bohr, "The New Era of Scaling in an SoC World", Plenary session, ISSCC 2009

Moore's Law

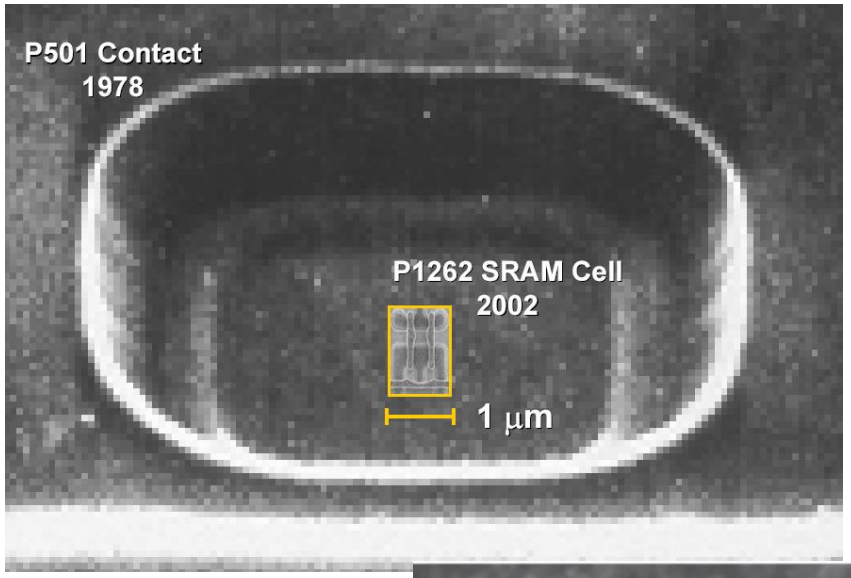
"If GM had kept up with technology like the computer industry has, we would all be driving $25 cars that got 1,000 miles to the gallon…"

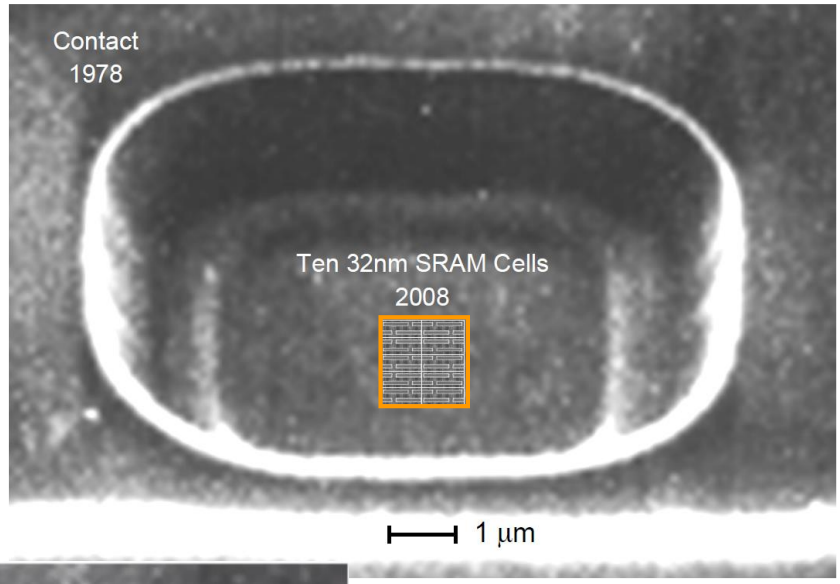
– Bill Gates, *COMDEX* keynote

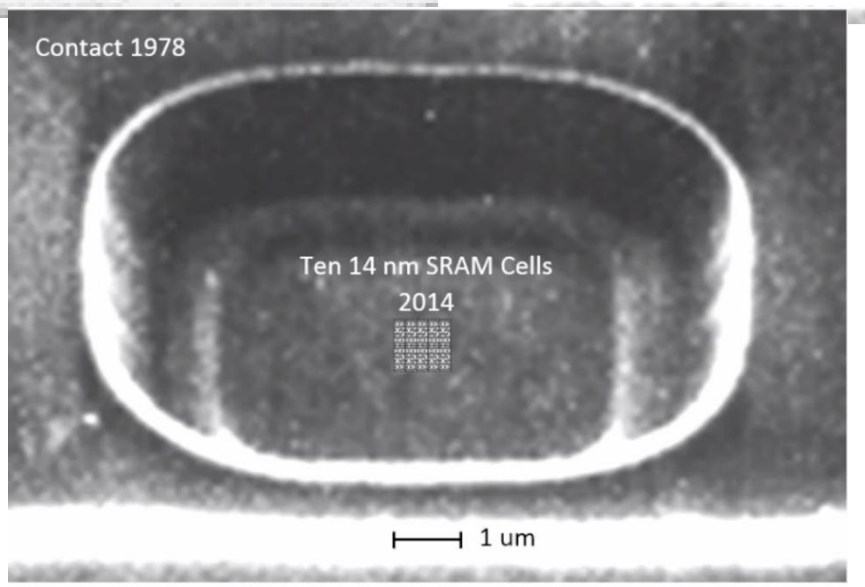


Ref: Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

Physical Dimension

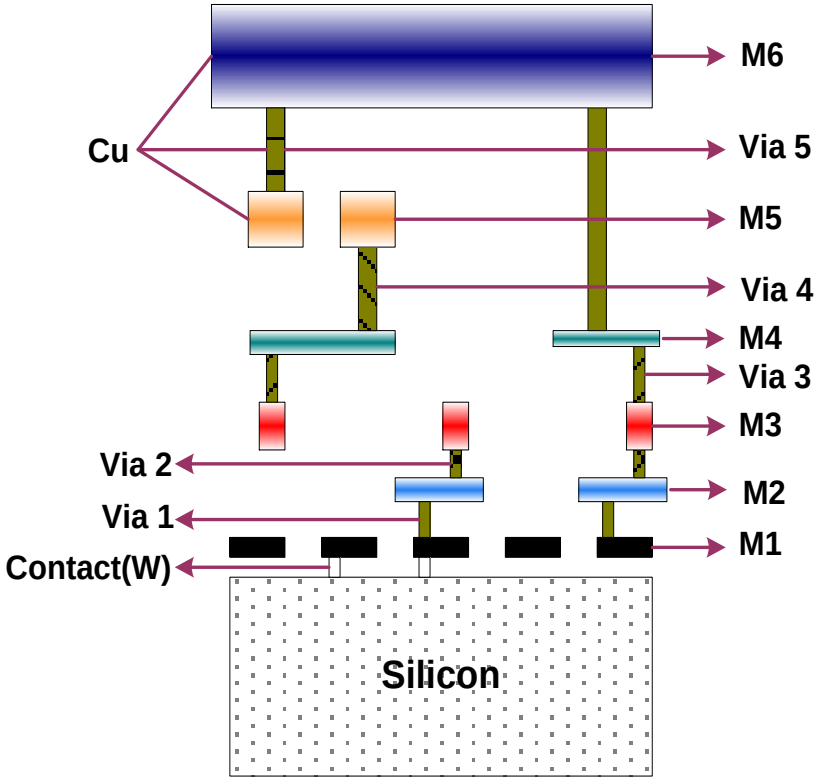


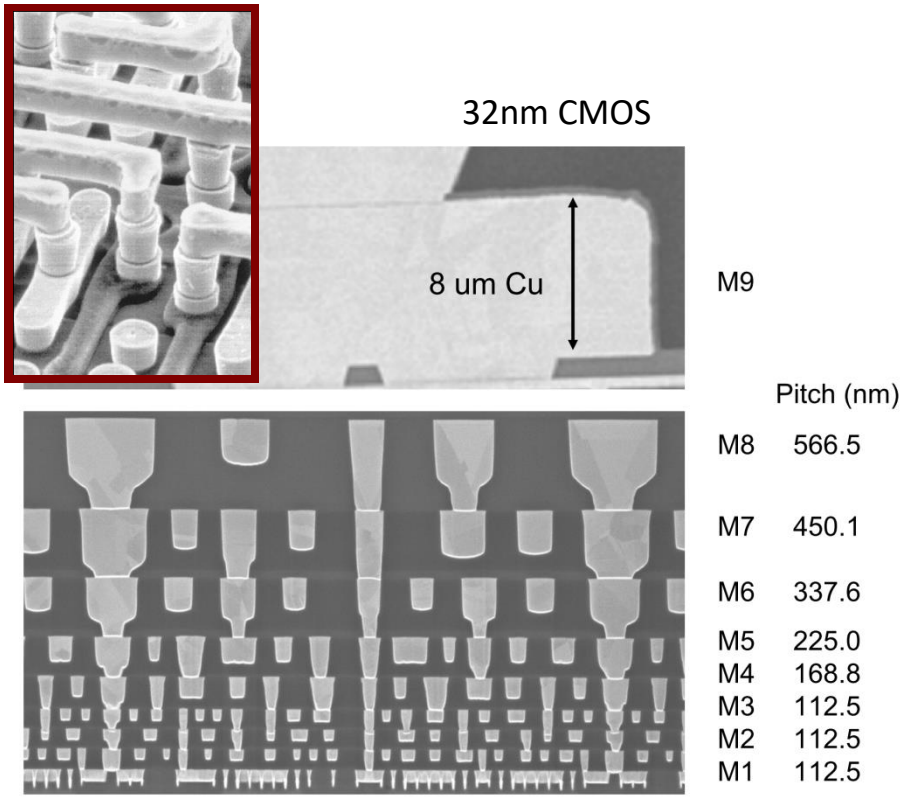




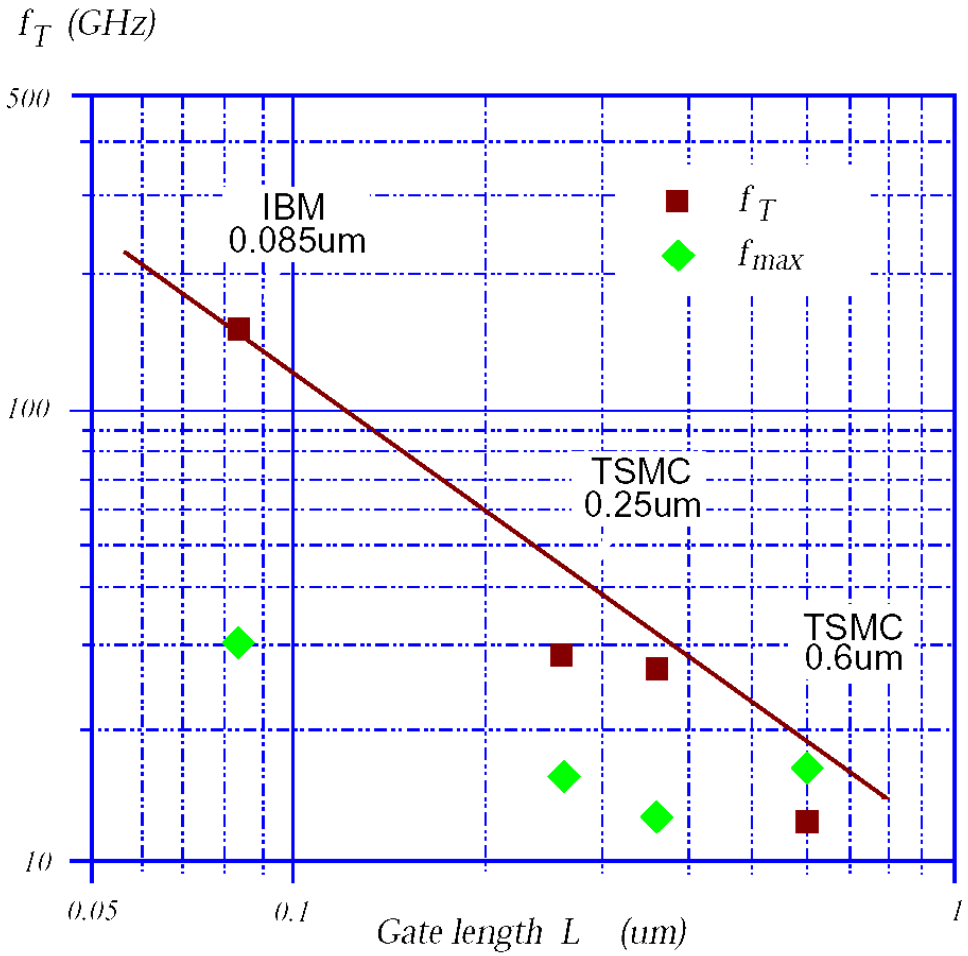
What We can do in IC ?

- Profile of IC
  - 9 metal layers – over the past 30 years





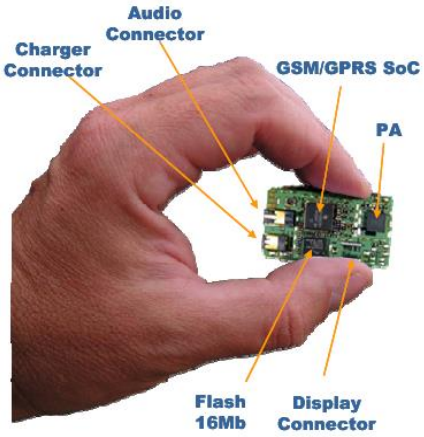
CMOS Device Speed



Integration !

GSM Phone (Siemens) from 1991

GSM 2-nd Generation
1994 Monoband



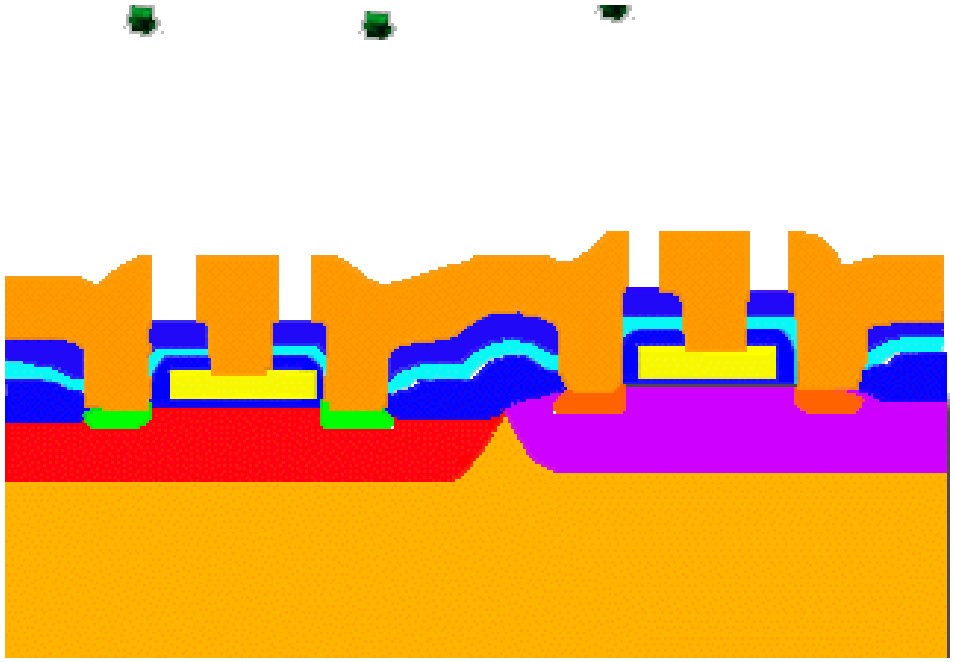
GSM/GPRS
TI 2006.

Outline

- CMOS Device Background
- CMOS Process Key Step
- CMOS Process Flow
- CMOS Passive Devices

Cleaning

- Prior to any high temperature or deposition step
  - To remove particle, organic films, metals and any pre-existing “native” oxide films



Clean Room

- US FED STD 209E Cleanroom Standards

US FED STD 209E Cleanroom Standards

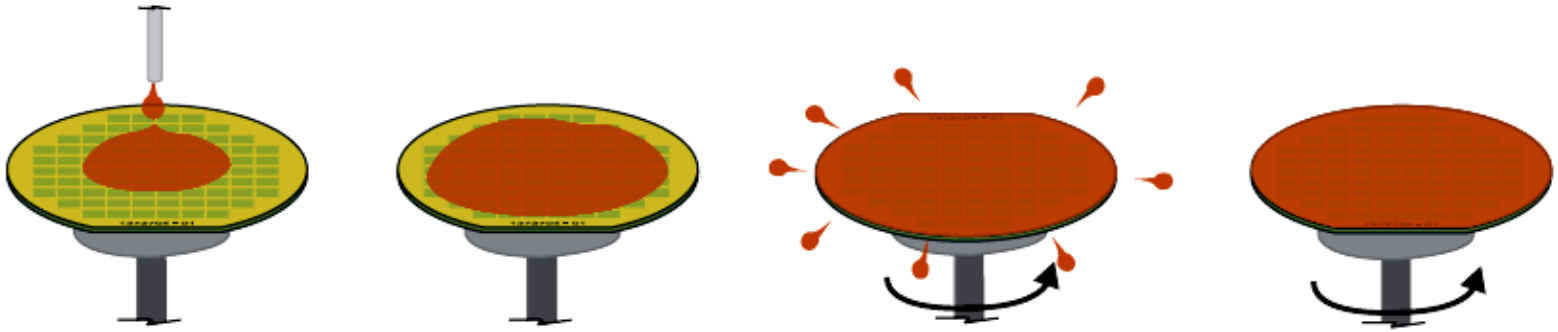
Class	maximum particles/ft³					ISO equivalent
	≥0.1 µm	≥0.2 µm	≥0.3 µm	≥0.5 µm	≥5 µm	
1	35	7	3	1		ISO 3
10	350	75	30	10		ISO 4
100		750	300	100		ISO 5
1,000				1,000	7	ISO 6
10,000				10,000	70	ISO 7
100,000				100,000	700	ISO 8

Photolithography

- Lithography
  - Transfer the circuit layout to the wafer
  - The heart of fabrication technologies
    - Defines the patterns through **mask**
      - Chromium on a transparent glass
      - With etching processing
        - » Deposited
        - » Ion implantation – change the property of silicon
    - Create patterns in **photoresist**
      - A liquid photosensitive chemical that resists etching processes
  - Owing to the necessary precision
    - A slow and expensive task

Photoresist

- Photoresist Coating Process
  - A small amount of photoresist
    - Is dispensed onto the center of the wafer
    - Is spun to produce the uniform thin film



Dispense a controlled amount of photoresist

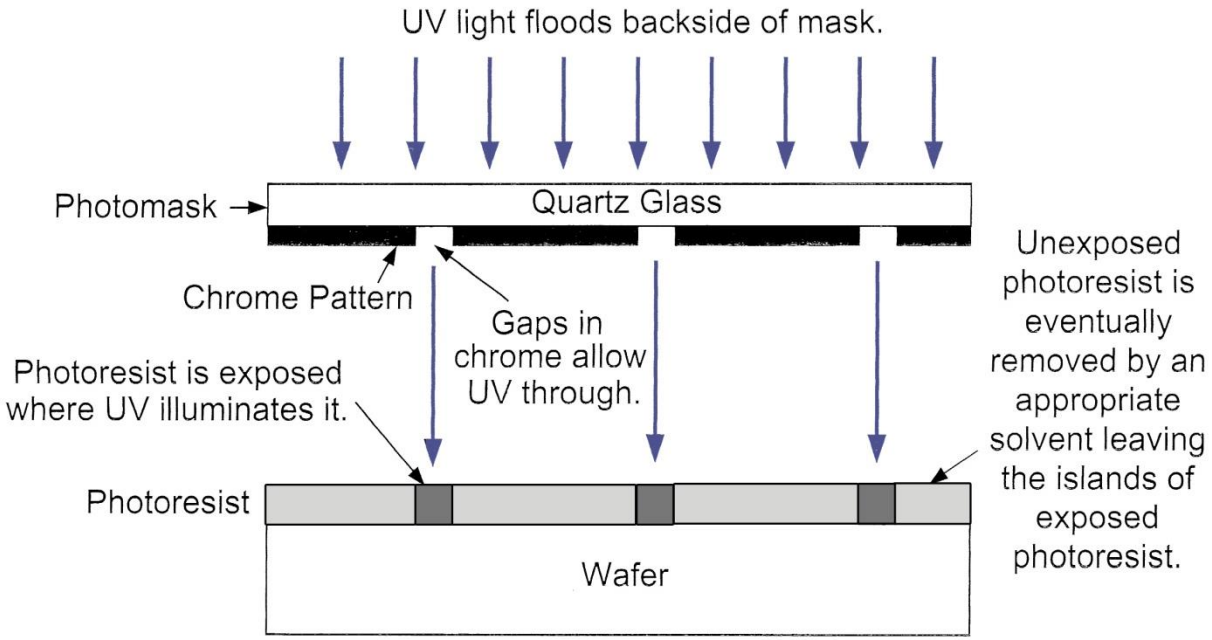
Allow the photoresist to spread across the wafer

Rapidly ramp - up the coater spin speed throwing off excess photoresist

Spin at high speed to form a thin dry film of photoresist

Photoresist

- Positively Photoresist
  - Developer dissolves the areas exposed to light quickly
- Negative Photoresist
  - Developer dissolves the areas not exposed to light quickly



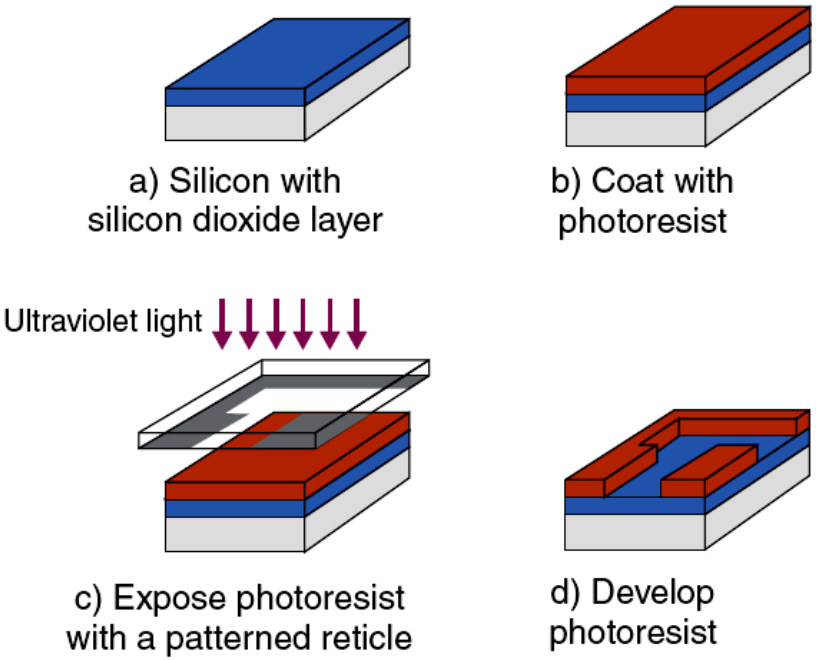
Exposure

- Light Sources
  - Ultraviolet (UV) light
  - Deep ultraviolet (DUV) light
  - Ion beam
  - Minimum linewidth and exposure wavelength

Year	Linewidth (nm)	Wavelength (nm)
1986	1,200	436
1988	800	436/365
1991	500	365
1994	350	365/248
1997	250	248
1999	180	248
2001	130	248
2003	90	248/193
2005 (fcst)	65	193
2007 (fcst)	45	193

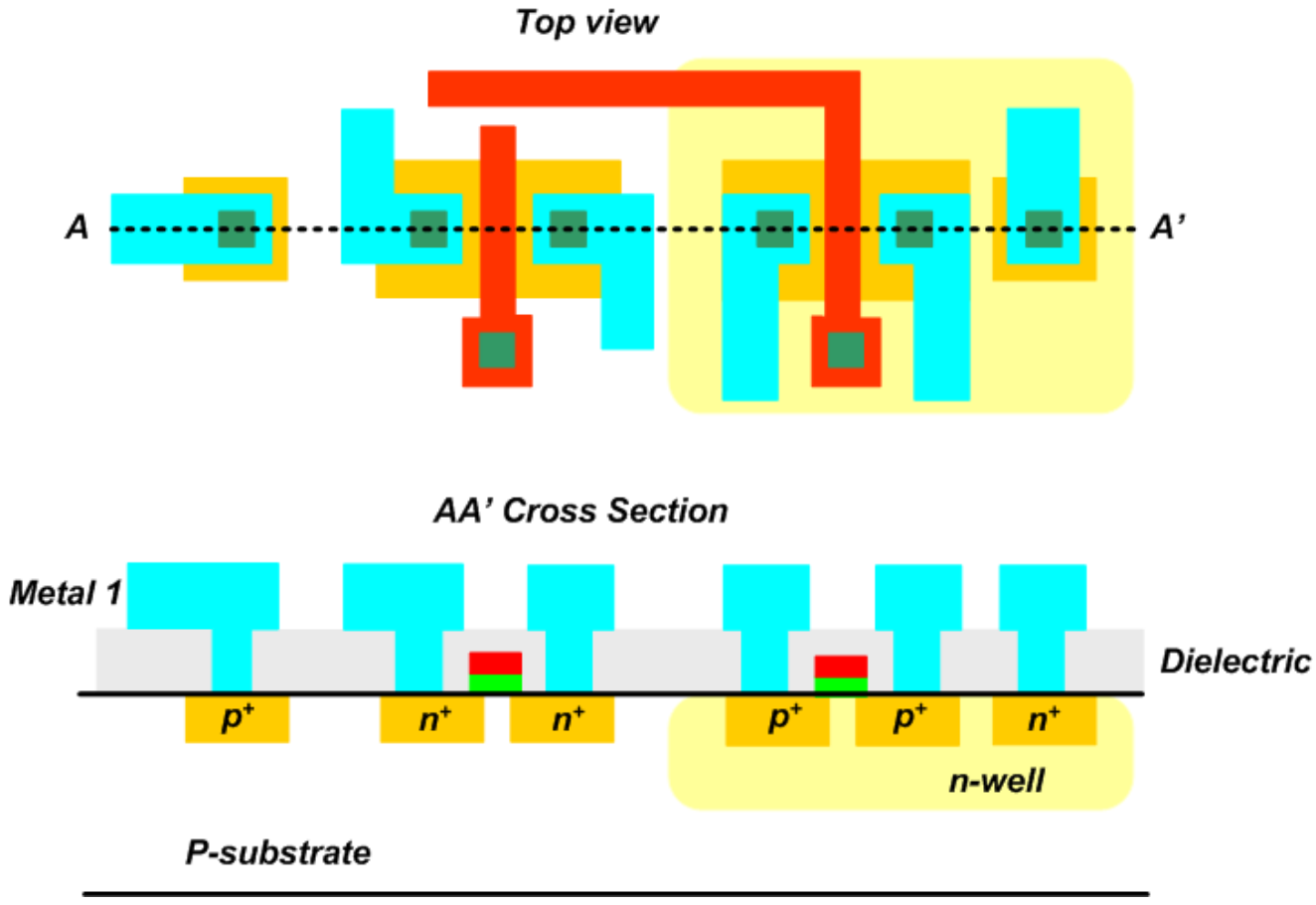
Develop

- Wash away the photoresist
  - Whenever light exposed a pattern into the photoresist
- Leave the photoresist
  - Whenever the light was blacked



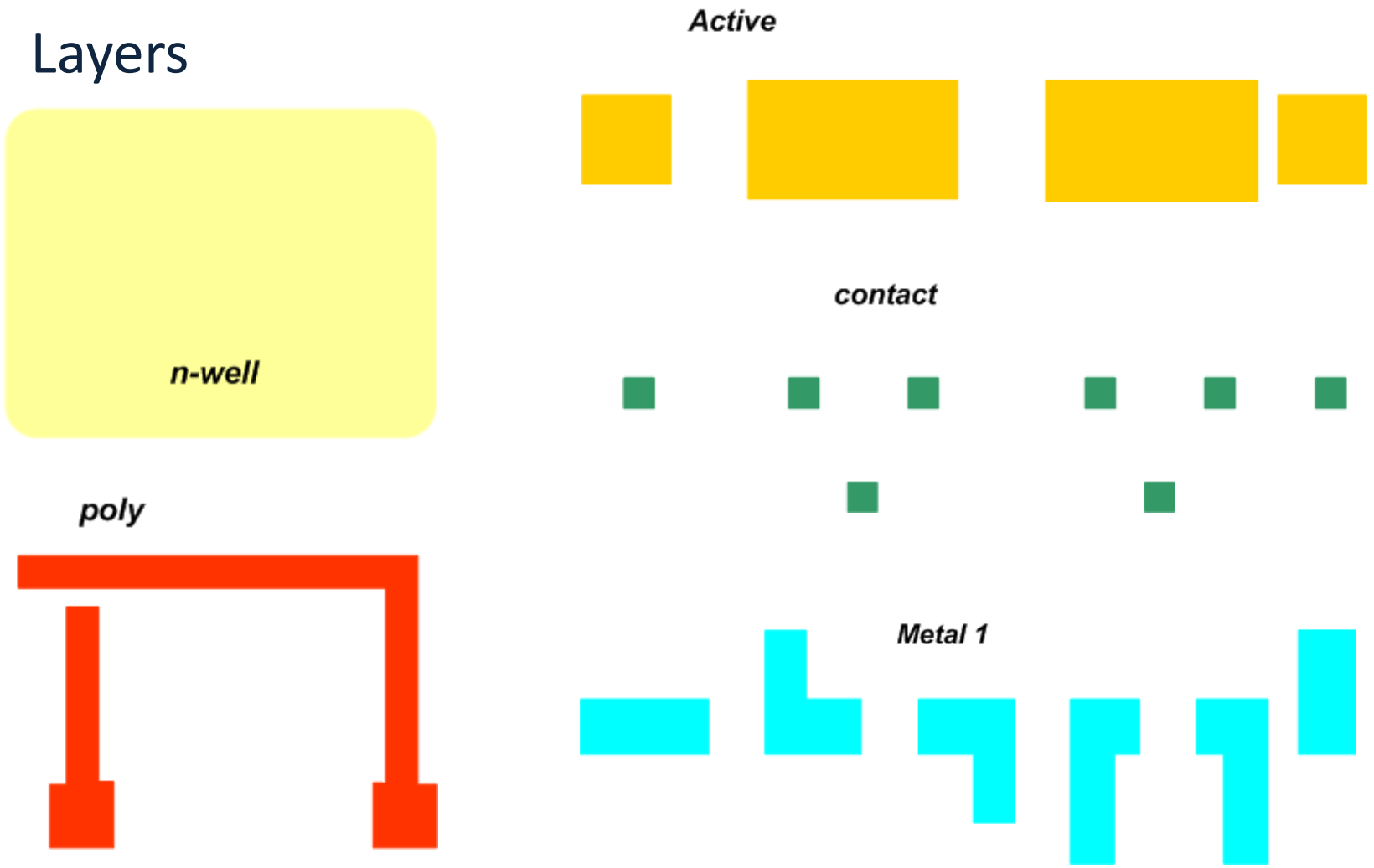
Layout

- Top View & Profile of MOS Devices



Mask Layer

- Layers

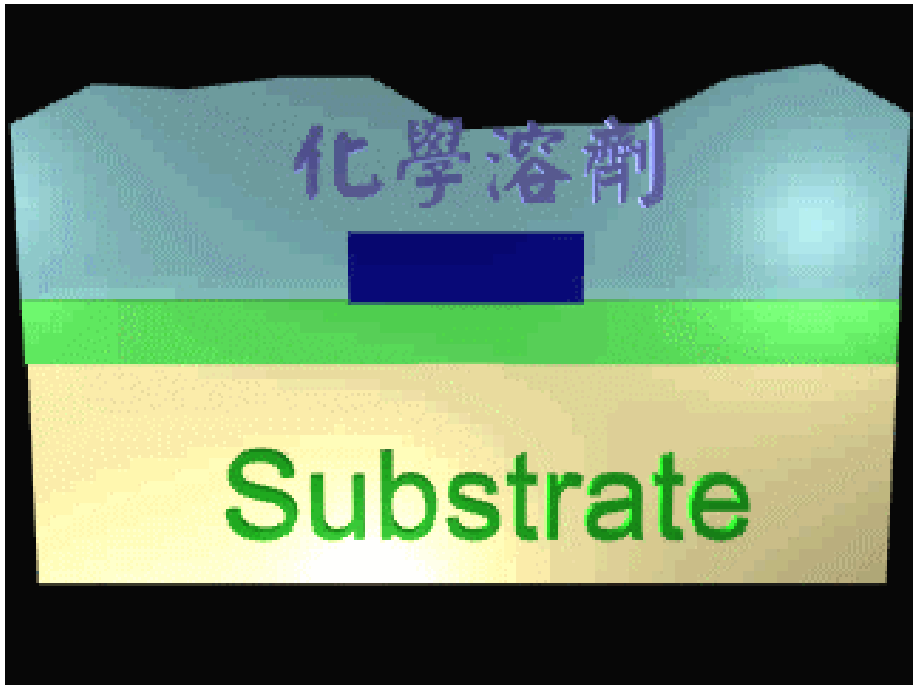


Etching

- Isotropic
  - Etches in all directions at the same rate
- Anisotropic
  - Achieve the faster etching in one direction than in other directions

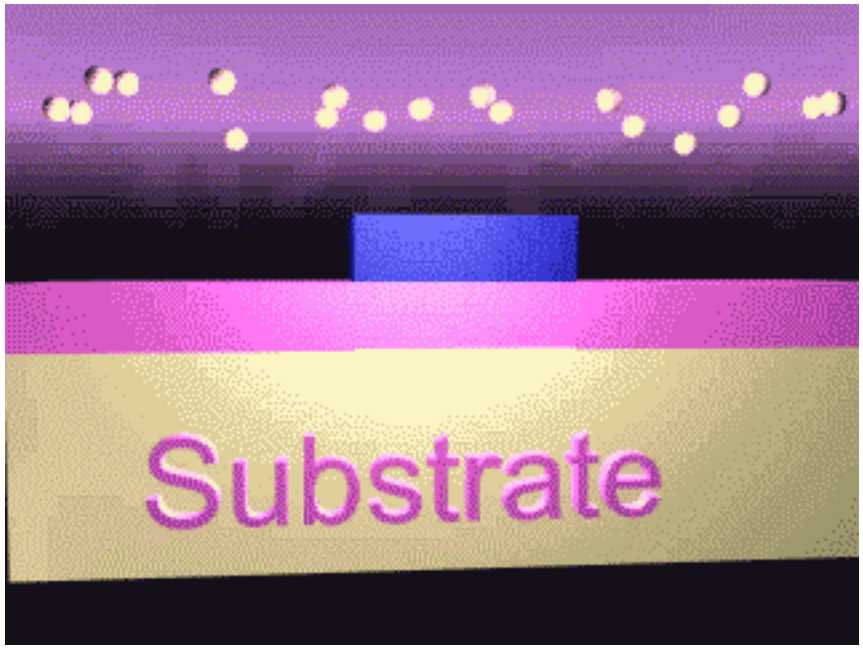
Wet Etching

- Place the wafer in a chemical liquid
  - Isotropic
    - Low precision



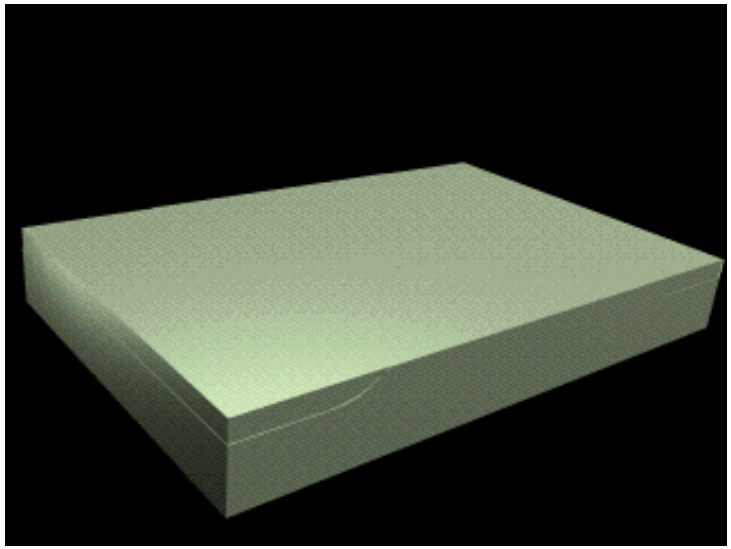
Dry Etching

- Plasma Etching
  - bombarding the wafer with a plasma gas
  - Anisotropic
    - High precision



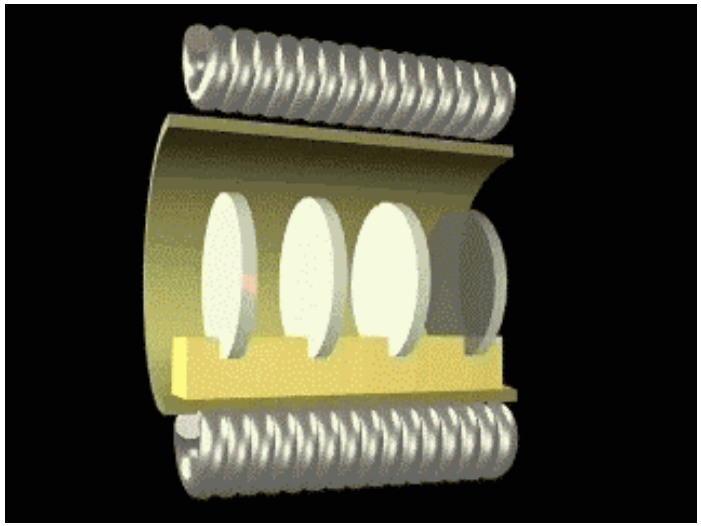
Oxidation

- Object
  - Gate dielectric
  - Protective coating in many steps of fabrication



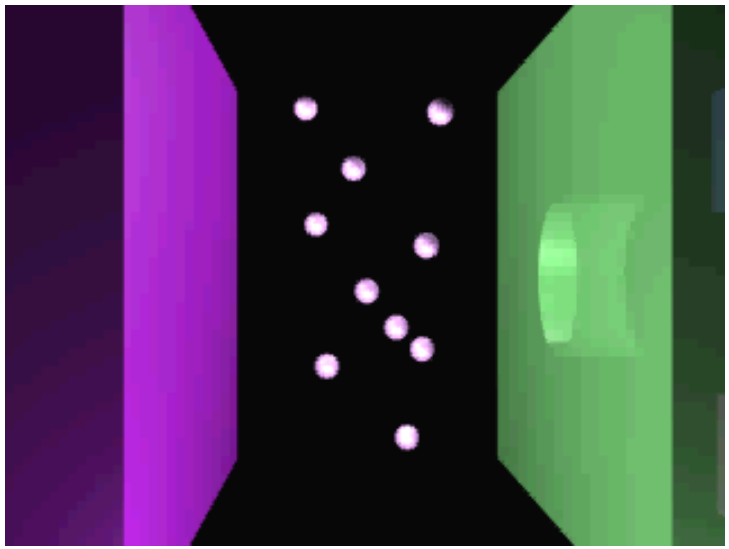
Oxidation

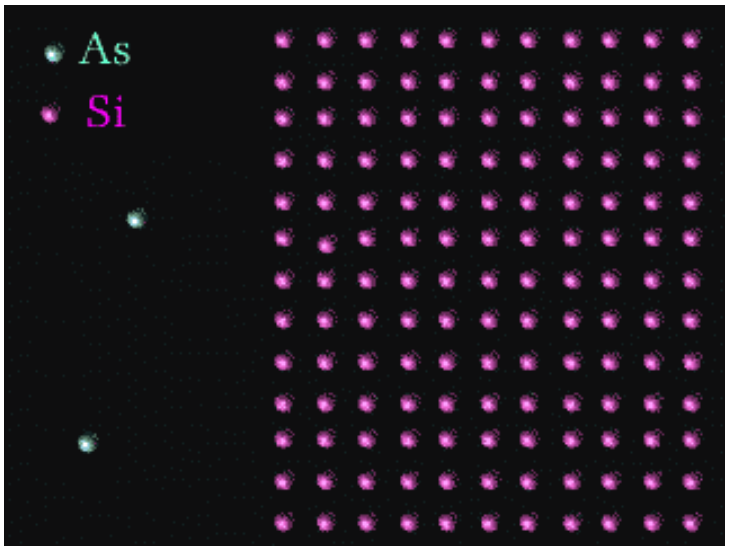
- Silicon Dioxide (SiO2)
  - Place the silicon in an oxygen gas at 1000°C



Ion Implementation

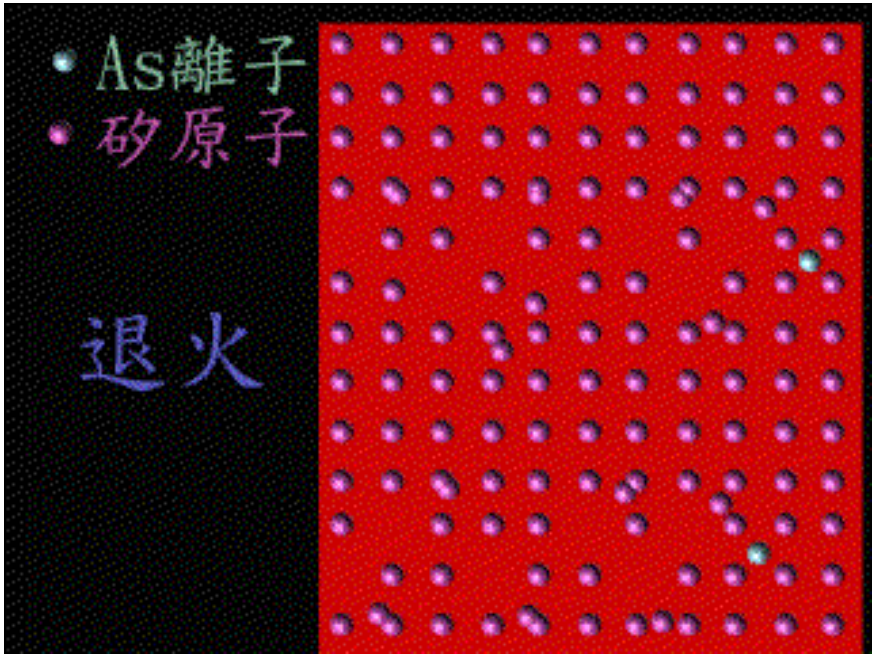
- Introduce Impurities (Dopants)
  - To change the electrical properties of the silicon
  - The most common method for introducing impurities into silicon wafers
    - Impurities with an electric charge are accelerated to high energy and shot into the exposed area of the wafer surface





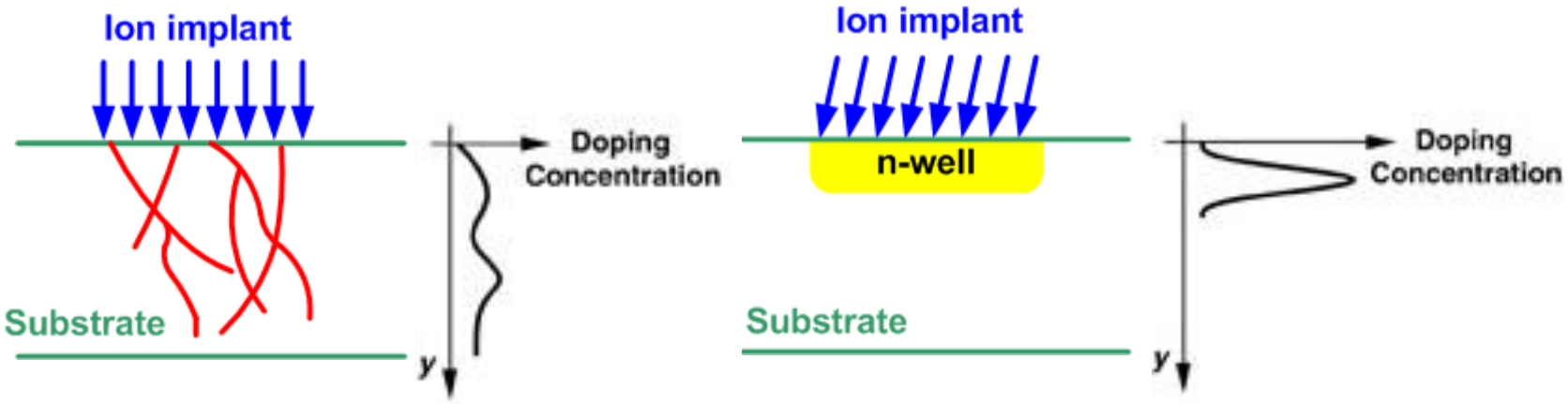
Ion Implementation

- Annealing
  - Following the ion implementation
    - A high temperature furnace process is used to anneal out the damage



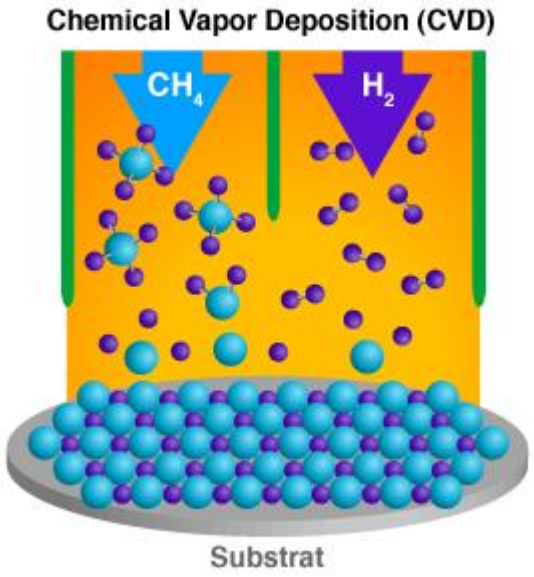
Ion Implementation

- Channeling
  - The implant beam is aligned with the crystal axis
    - The ions penetrate the wafer to a greater depth
  - The implant beam is tilted by 7-9°



Chemical Vapor Deposition

- A process of depositing films by reacting chemical vapors to produce a film on a substrate
  - May be activated by
    - Heat
    - RF energy (plasma enhanced, PECVD)
    - Light (photon induced, PHCVD)
  - CVD process is used to deposit
    - Poly and single crystal silicon
    - Dielectric films
    - Metal films



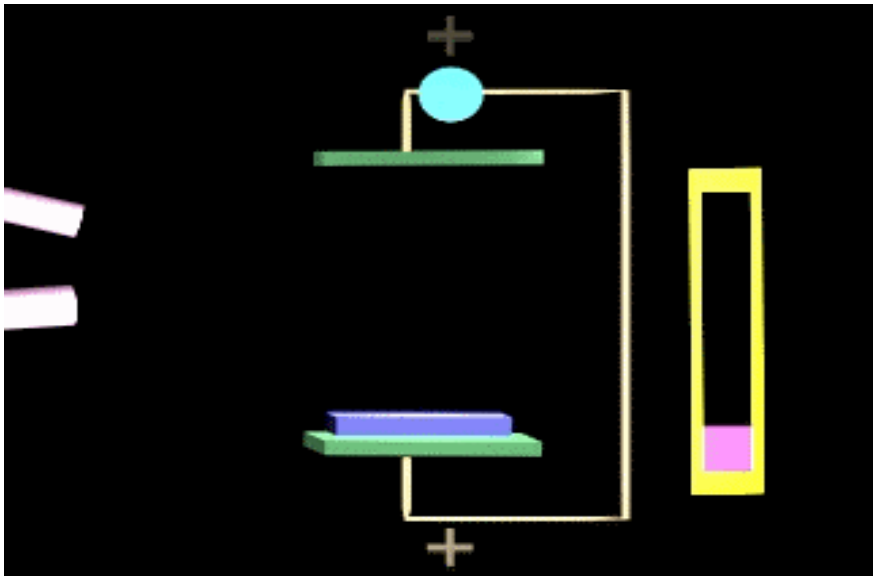
Chemical Vapor Deposition

- Atmospheric Pressure CVD (APCVD)

- Low Pressure CVD (LPCVD)
  - The most commonly process
  - More uniformity

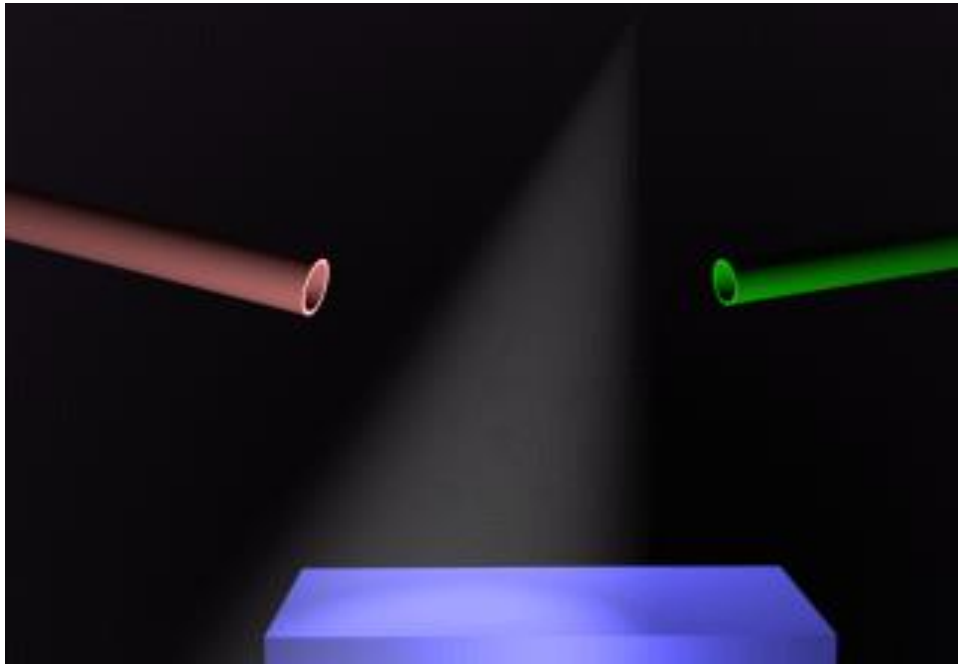
Chemical Vapor Deposition

- Plasma Enhanced CVD (PECVD)
  - Induced by high frequency energy



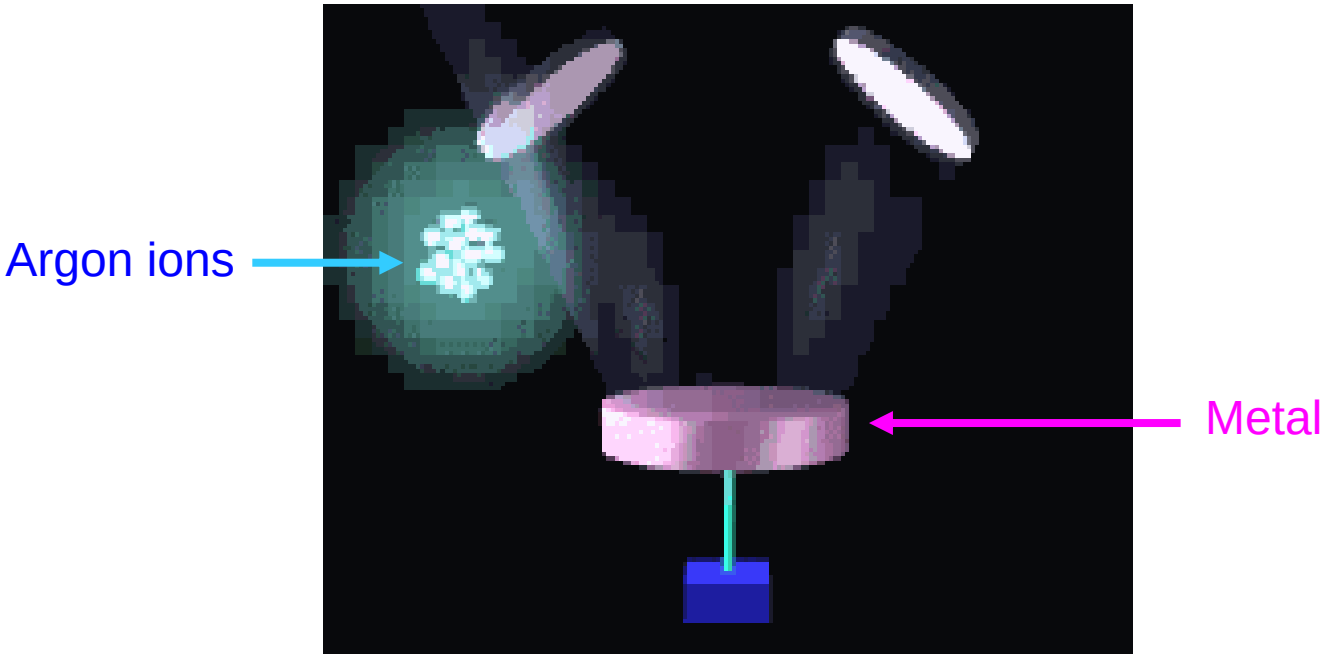
Chemical Vapor Deposition

- Photon Induced CVD (PHCVD)
  - Induced by light



Sputter Deposition

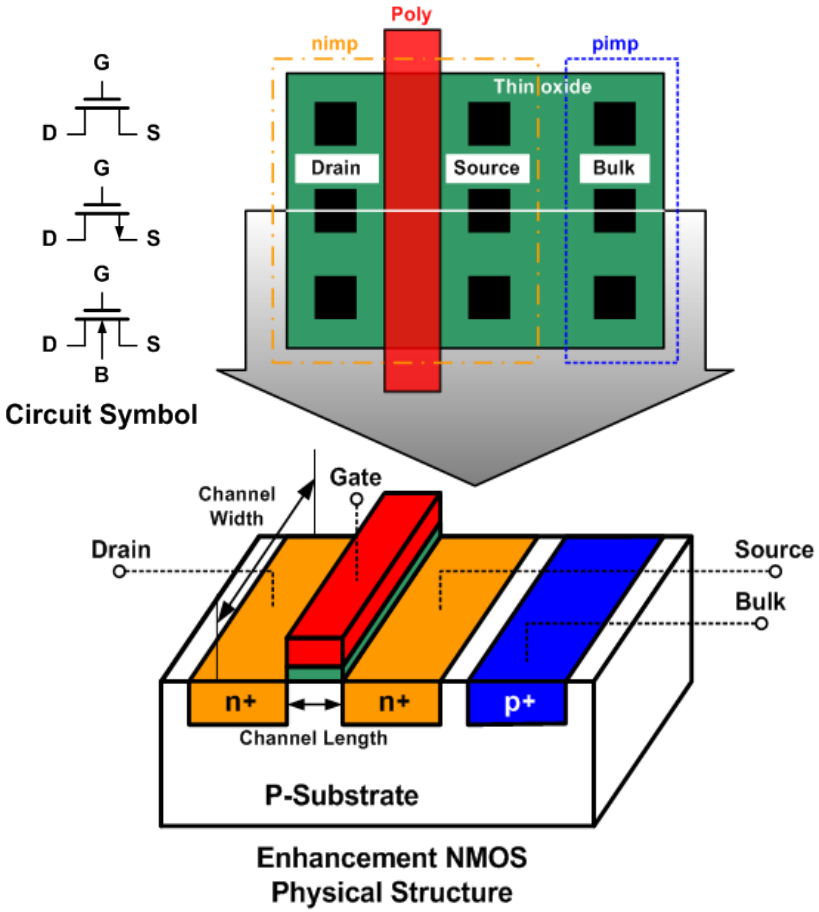
- Sputter Process
  - Metal films are used in IC fabrication
    - Argon gas is excited by a high energy field

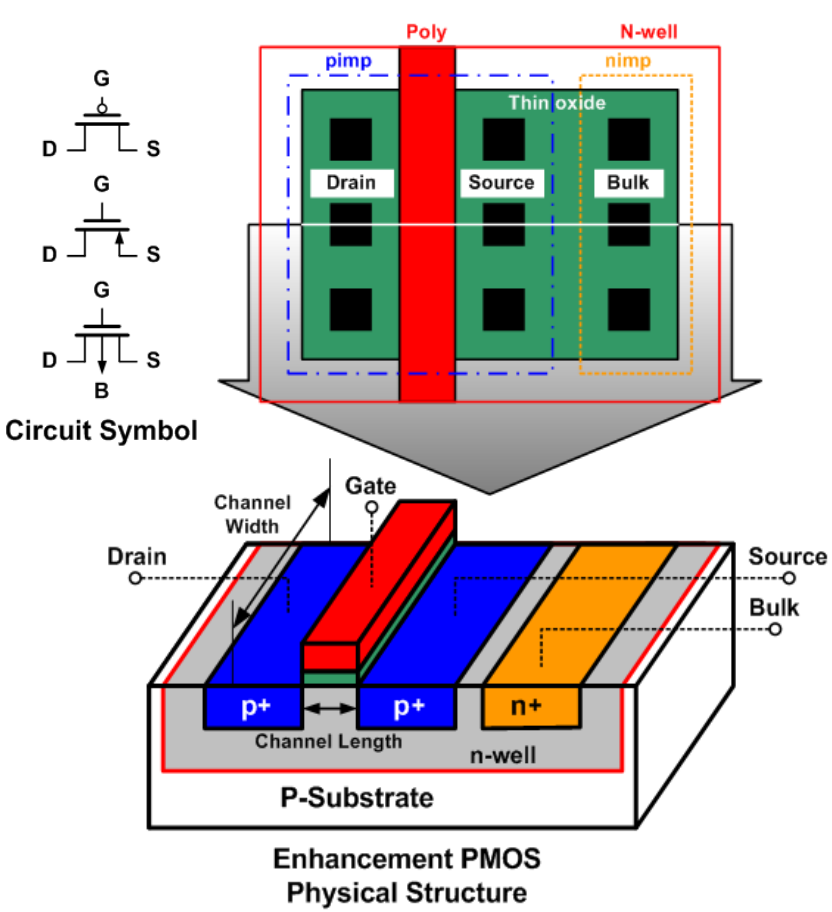


Outline

- CMOS Device Background
- CMOS Process Key Step
- CMOS Process Flow
- CMOS Passive Devices

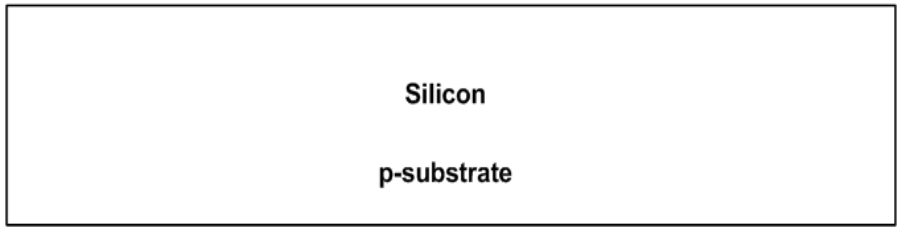
CMOS Active Device Layout





An Inverter Example - 0

Cross-section

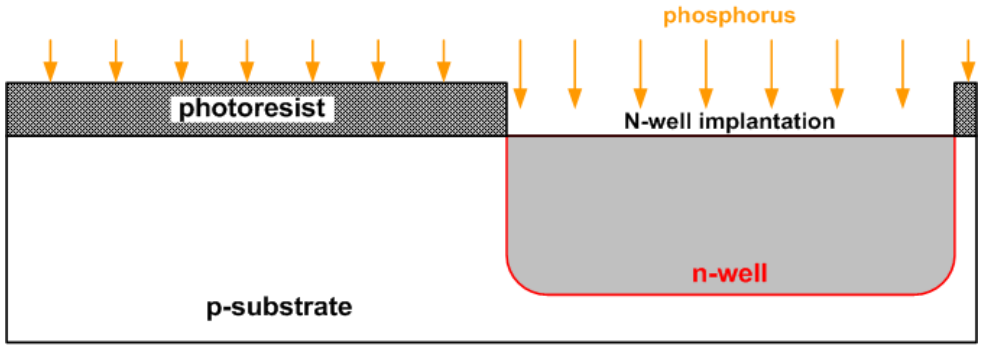


Top View

An Inverter Example - 1

Step1 : N-Well (NW)

Cross-section

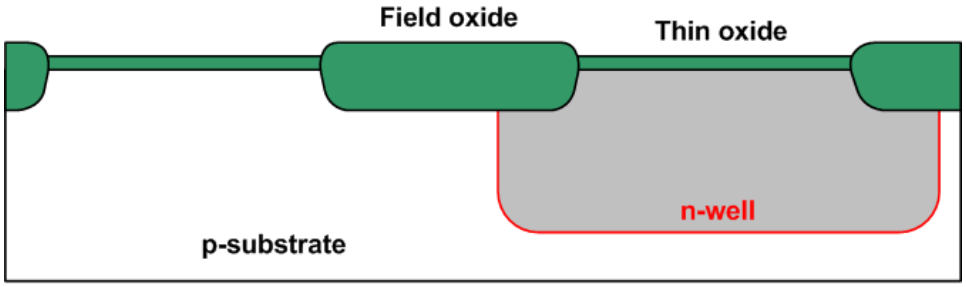


Top View

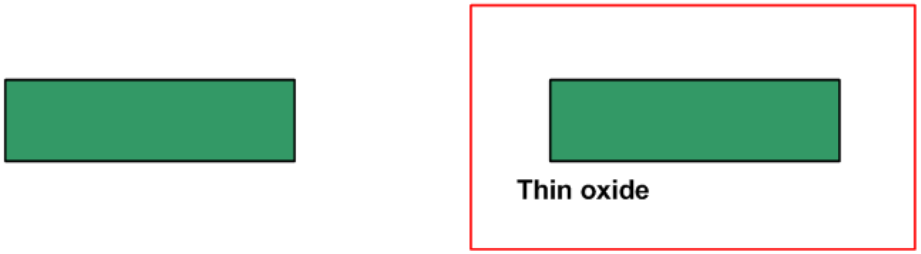
An Inverter Example - 2

Step2 : Thin Oxide (OD)

Cross-section



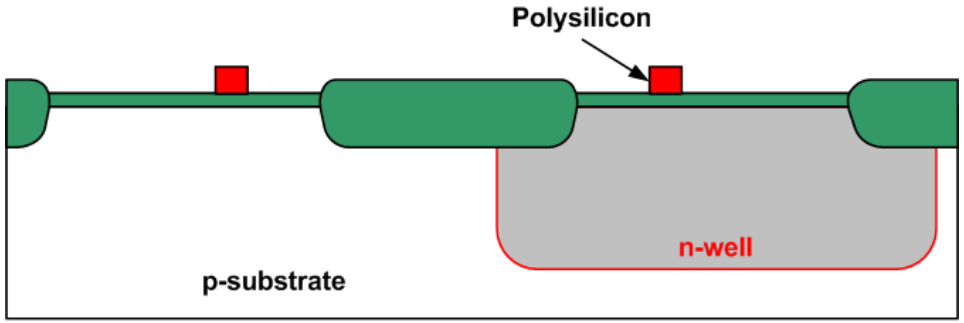
Top View



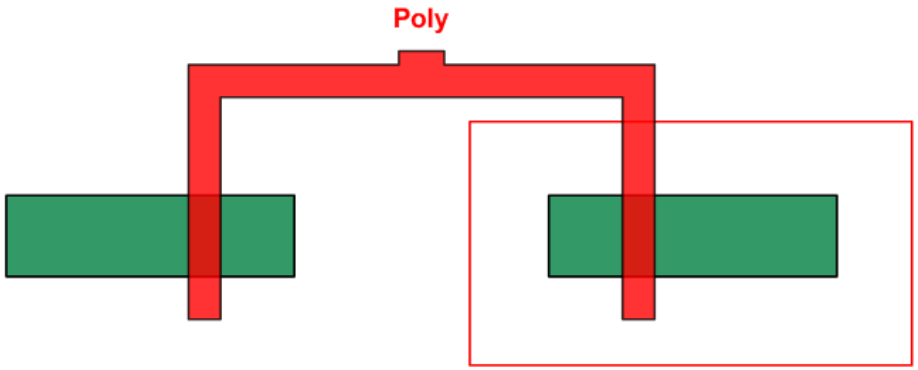
An Inverter Example - 3

Step3 : Poly (PO)

Cross-section



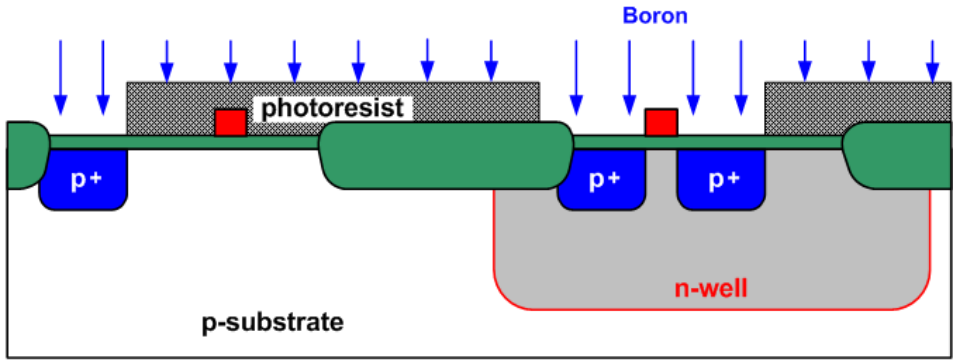
Top View



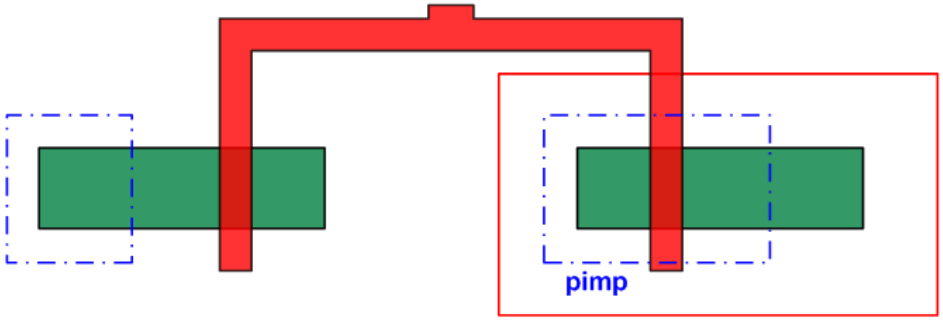
An Inverter Example - 4

Step4 : P+S/D implant (PP)

Cross-section



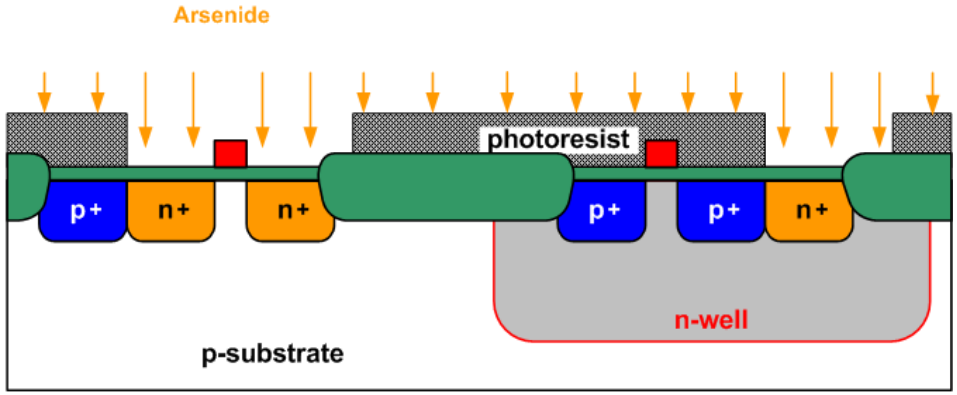
Top View



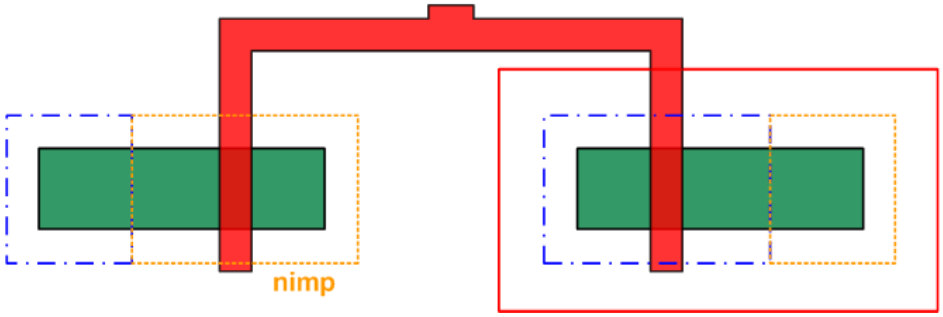
An Inverter Example - 5

Step5 : N+S/D implant (NP)

Cross-section



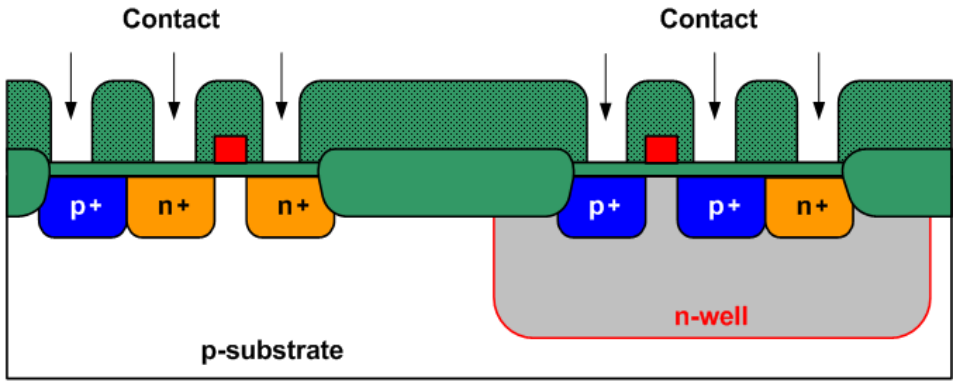
Top View



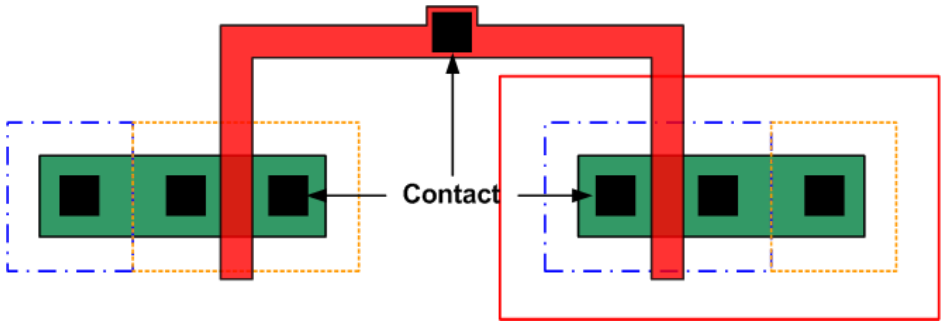
An Inverter Example - 6

Step6 : Contact (CO)

Cross-section



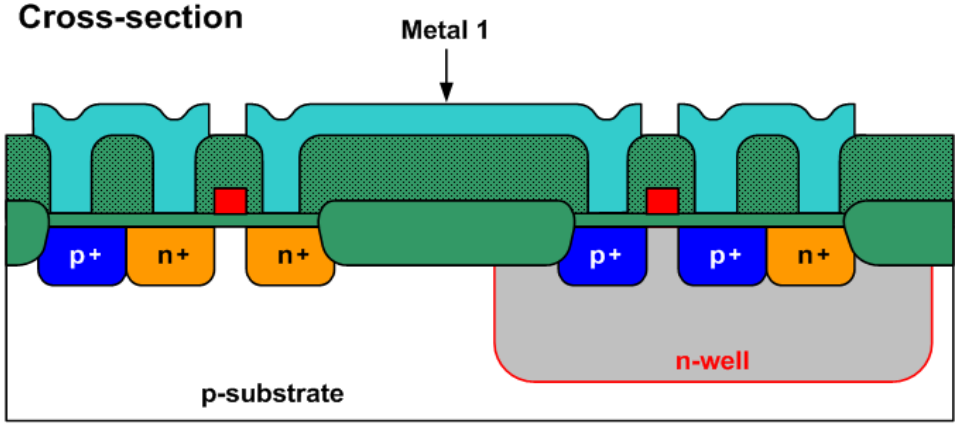
Top View



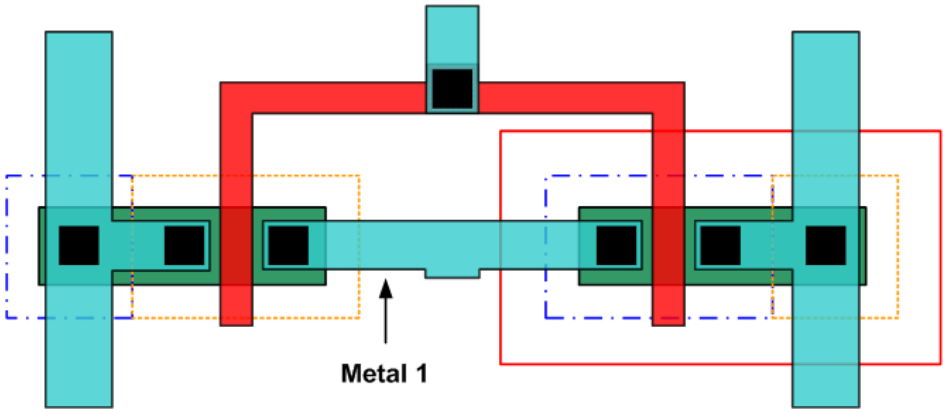
An Inverter Example - 7

Step7 : Metal-1 (M1)

Cross-section

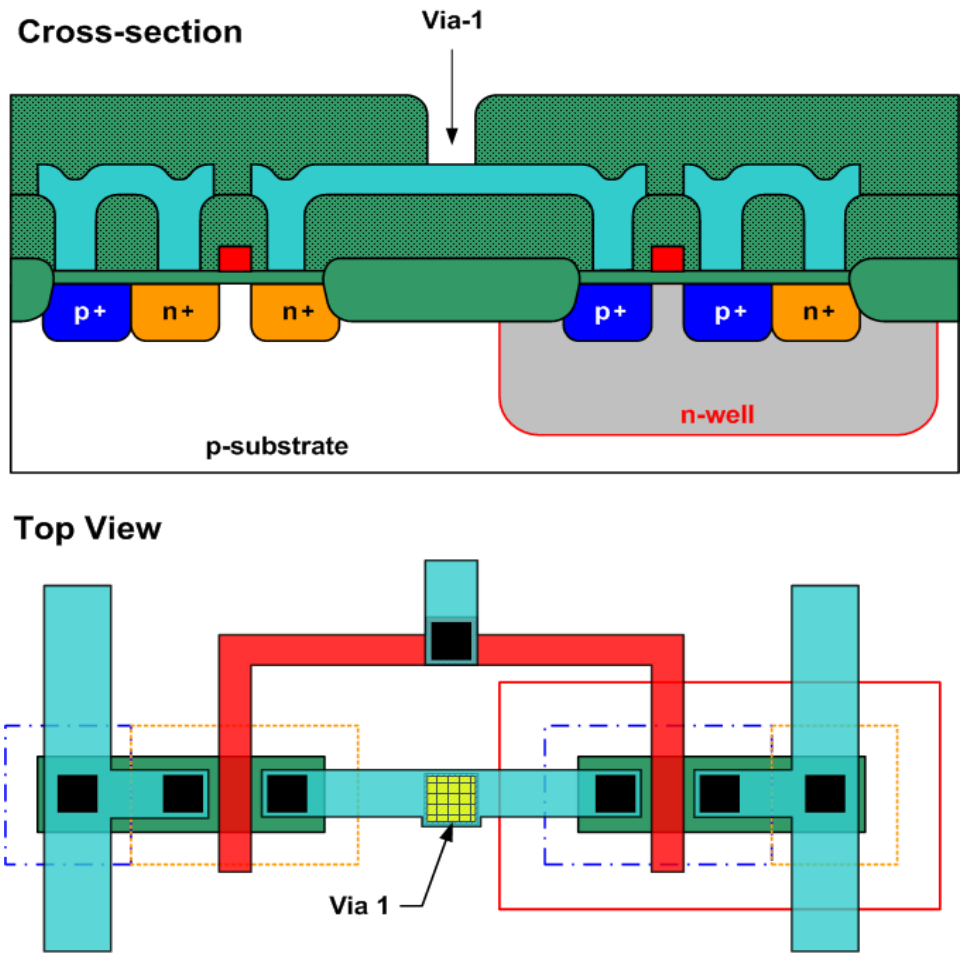


Top View

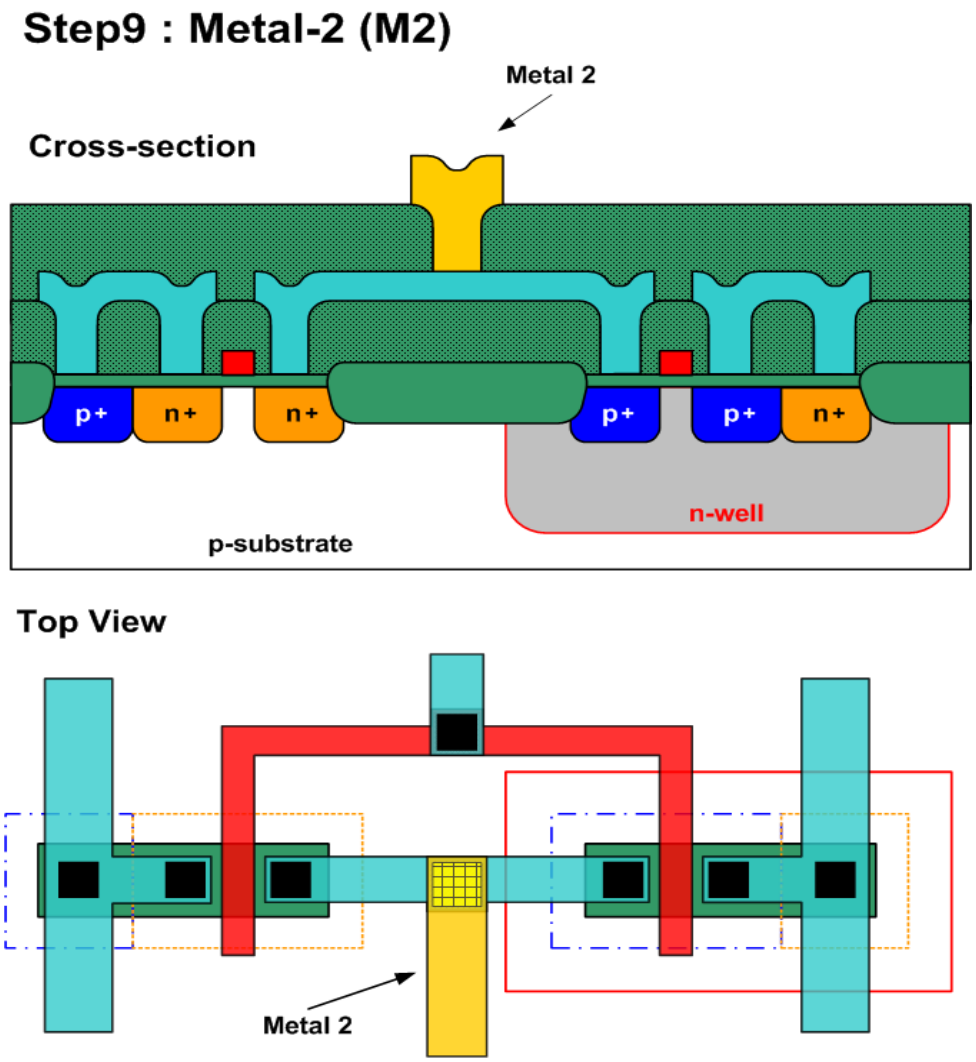


An Inverter Example - 8

Step8 : Via1 Hole



An Inverter Example - 9



Outline

- CMOS Device Background
- CMOS Process Key Step
- CMOS Process Flow
- CMOS Passive Devices

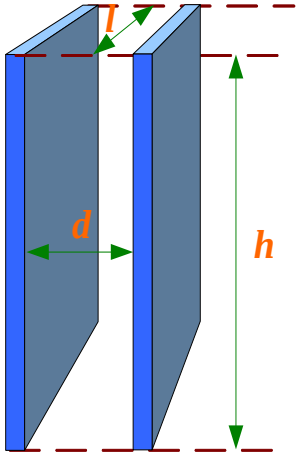
CMOS Active Device Parameter

- an example from *Boser, UC Berkeley*

	NMOS	PMOS	Variation	Matching
✓ V_{TH} (L =0.5μm)	600mV	-700mV	±100mV	±5mV (L =1μm)
γ	0.5$\sqrt{\text{V}}$	0.4$\sqrt{\text{V}}$		
Φ_s	0.6V	0.6V		
✓ μC_{ox} (V_d^{sat} = 200mV)	190μA/V^2	90μA/V^2	±5%	±0.1%
✓ μC_{ox} (V_d^{sat} = 1V)	90μA/V^2	55μA/V^2	±5%	±0.1%
n	1.5	1.6		
$g_m r_o$ (L = 0.35μm)	30	12	±30%	depends on ΔV_{DS}
$g_m r_o$ (L = 0.5μm)	50	25	±30%	
C_{ox}	5.3fF/μm^2	5.3fF/μm^2	±4%	< ±0.05%
C_{ol}	0.24fF/μm	0.48fF/μm		
C_j	0.85fF/μm^2	1.1fF/μm^2		
C_{jsw}	0.49fF/μm	0.48fF/μm		
M_j	0.39	0.48		
Φ_B	0.51V	0.93V		
K_f	0.5×10^{-25}V	0.25×10^{-25}V		

Capacitor

- Charge storage device
  - Memory Devices, esp. DRAM
  - Two boards of semiconductor material as a capacitor
- Capacitances
  - are proportional to the area
  - are inverse proportional to the distance



symbol

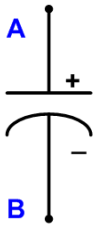
$$C = k\varepsilon_0 \frac{hl}{d}$$

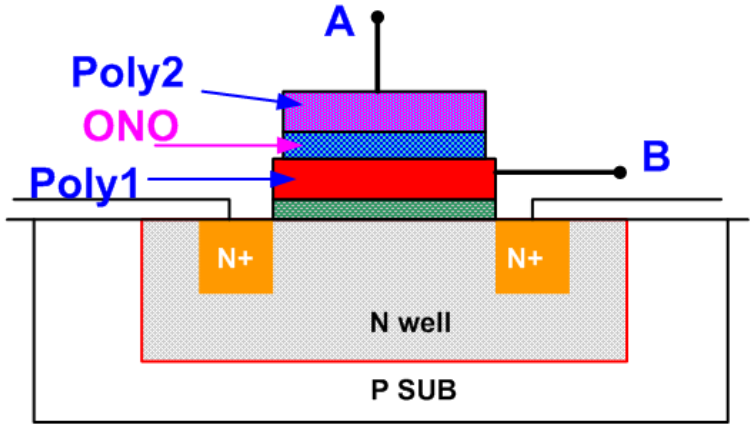
k = dielectric constant

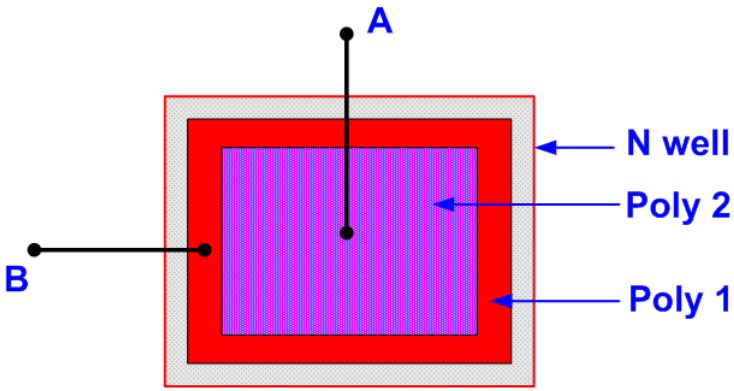
ε_0 = permittivity

CMOS Poly-Poly Capacitor

- Usually for >0.35um or memory technology



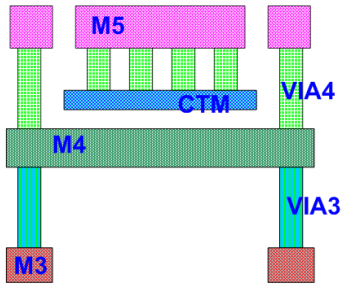


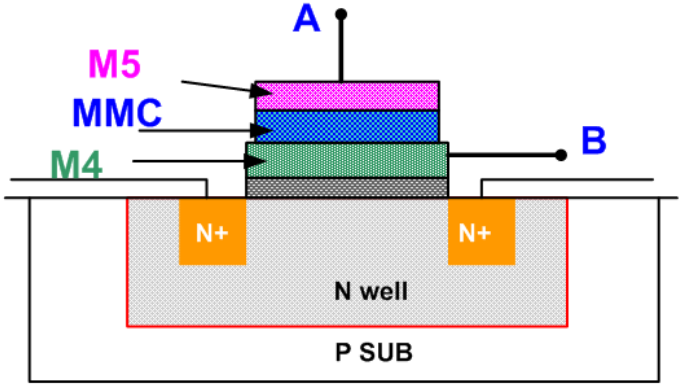


CMOS Metal-Metal Capacitor

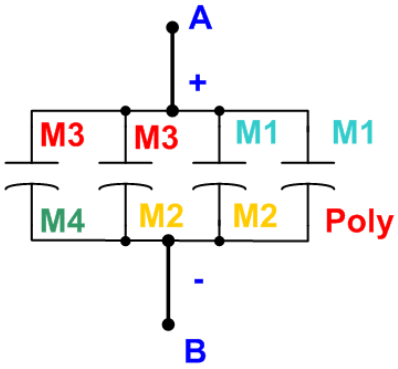
- Usually for <0.25um mixed signal/RF technology

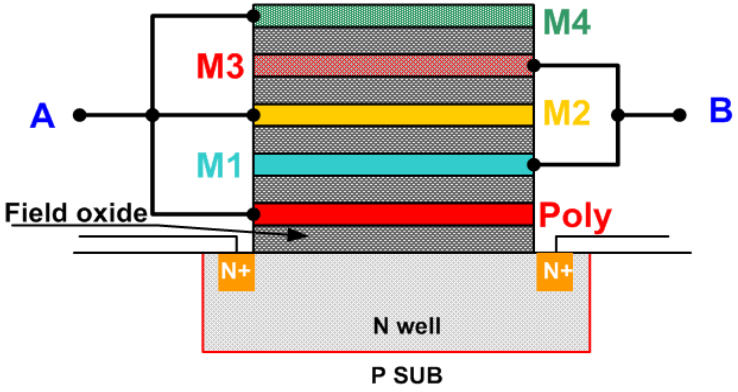
M-I-M





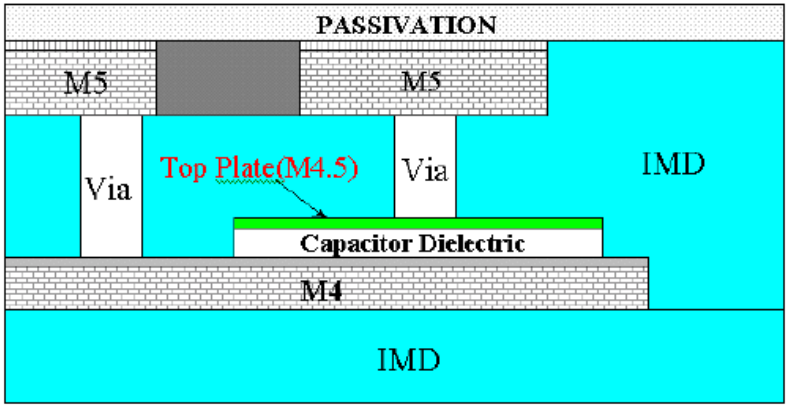
M-O-M

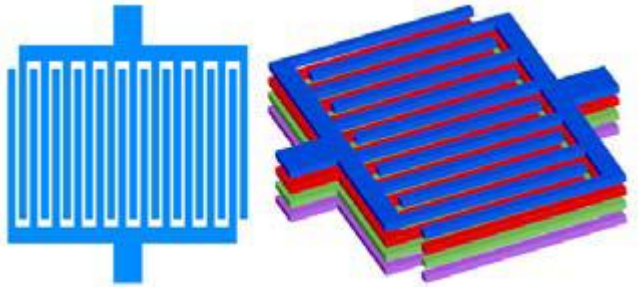


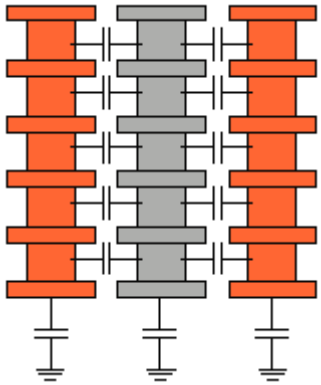


MIM vs. MOM

- Metal-Insulator-Metal
  - — Need extra layer
  - — More routing capability
- Metal-Oxide-Metal
  - — Free with modern process
  - — More layers : higher density

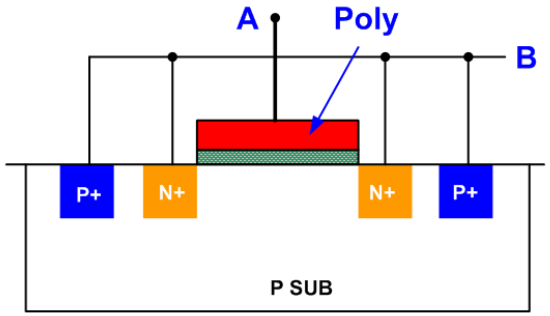


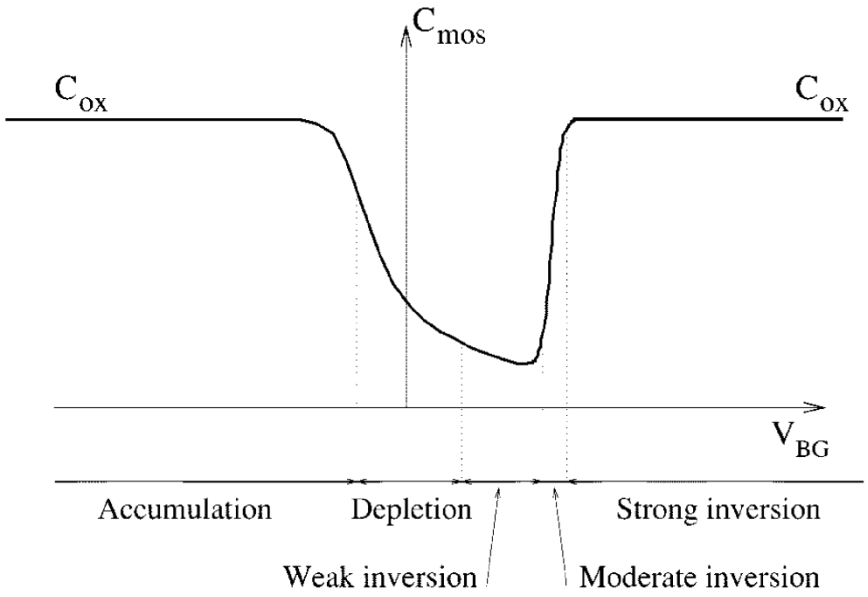




CMOS Active Capacitor

- from *P. Andreani, IEEE JSSC. 2000*





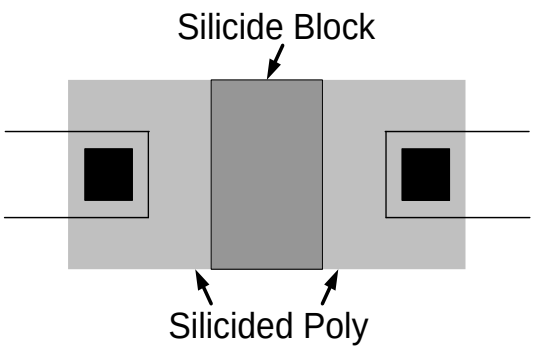
CMOS Passive Capacitor

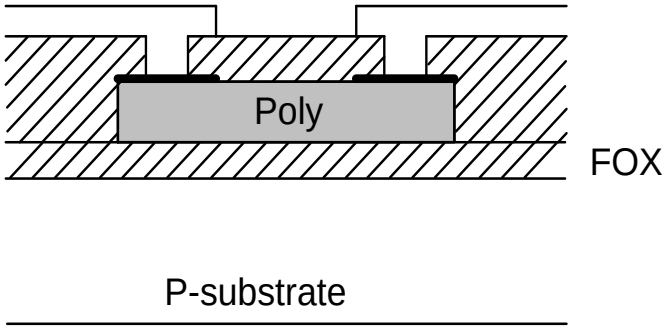
- an example from *Boser, UC Berkeley*

	Capacitor type	Capacitance	V_C	T_C
✓	Gate, C_{ox} $(V_{GS} > V_{TH}, V_{DS} = 0V)$	$5300\text{aF}/\mu\text{m}^2$		
✓	Poly-poly capacitor	$1000\text{aF}/\mu\text{m}^2$	10ppm/V	$25\text{ppm}/^o\text{C}$
✓	Metal-metal	$50\text{aF}/\mu\text{m}^2$	20ppm/V	$30\text{ppm}/^o\text{C}$
	Metal1-substrate	$30\text{aF}/\mu\text{m}^2$		
	Metal-poly	$50\text{aF}/\mu\text{m}^2$		
	Poly-substrate	$120\text{aF}/\mu\text{m}^2$		
✓	M-I-M	$1000\text{aF}/\mu\text{m}^2$		

Resistor

- Polysilicon resistor
  - is doped on an IC chip
  - Linear
    - Resistance is determined by length, area, and the resistivity of the material type

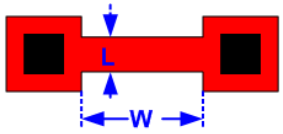


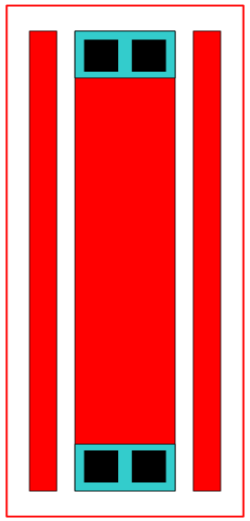


symbol

CMOS Resistor Layout

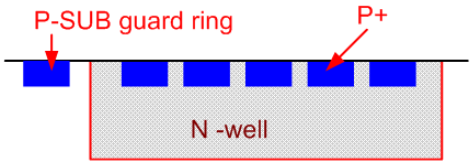
Poly

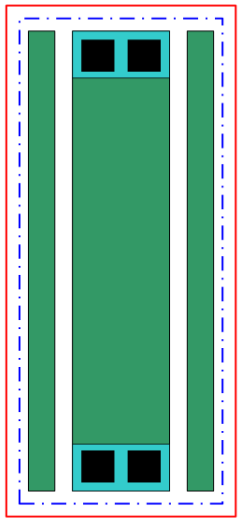




Well

Diffusion





CMOS Passive Resistor

- an example from *Boser, UC Berkeley*

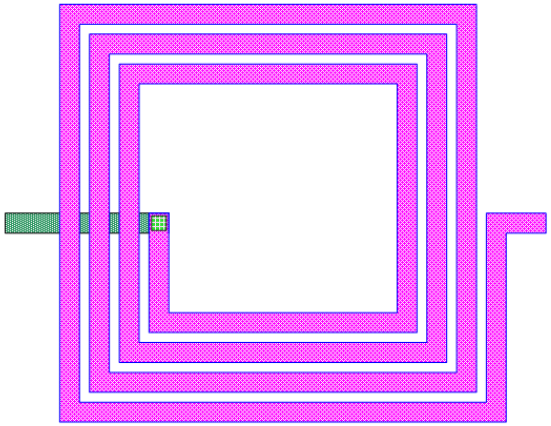
	Resistor type	R/□	T_C	V_C	B_C
✓	N+ polysilicon (not silicided)	100Ω/□	-800ppm/°C	50ppm/V	50ppm/V
✓	P+ polysilicon (not silicided)	180Ω/□	200ppm/°C	50ppm/V	50ppm/V
	N+ diffusion (not silicided)	50Ω/□	1500ppm/°C	500ppm/V	-500ppm/V
	P+ diffusion (not silicided)	100Ω/□	1600ppm/°C	500ppm/V	-500ppm/V
	N-well	1000Ω/□	-1500ppm/°C	0.02/V	0.03/V

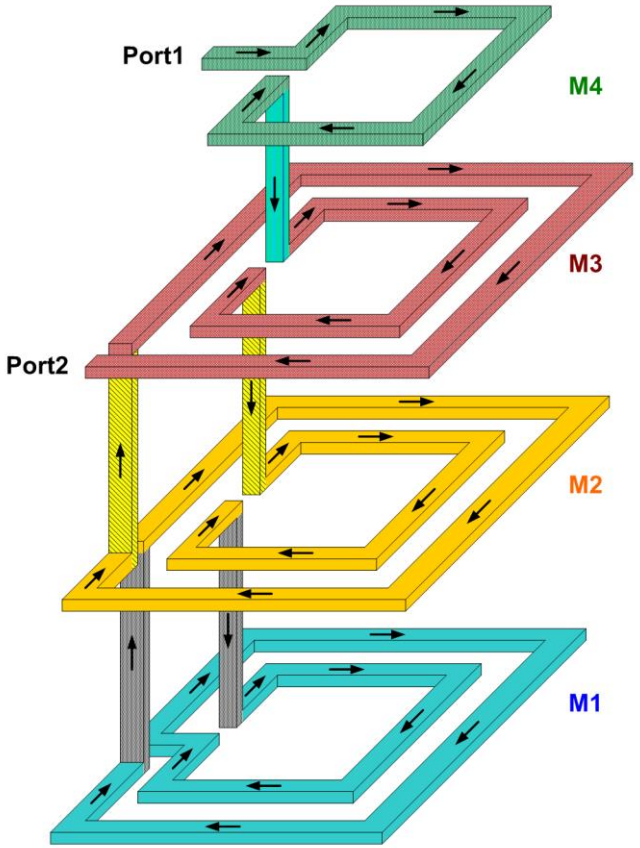
The resistance of a uniform slab of conducting material

$$R = \frac{\rho l}{A} = \frac{\rho l}{t w} = RS \frac{l}{w}$$

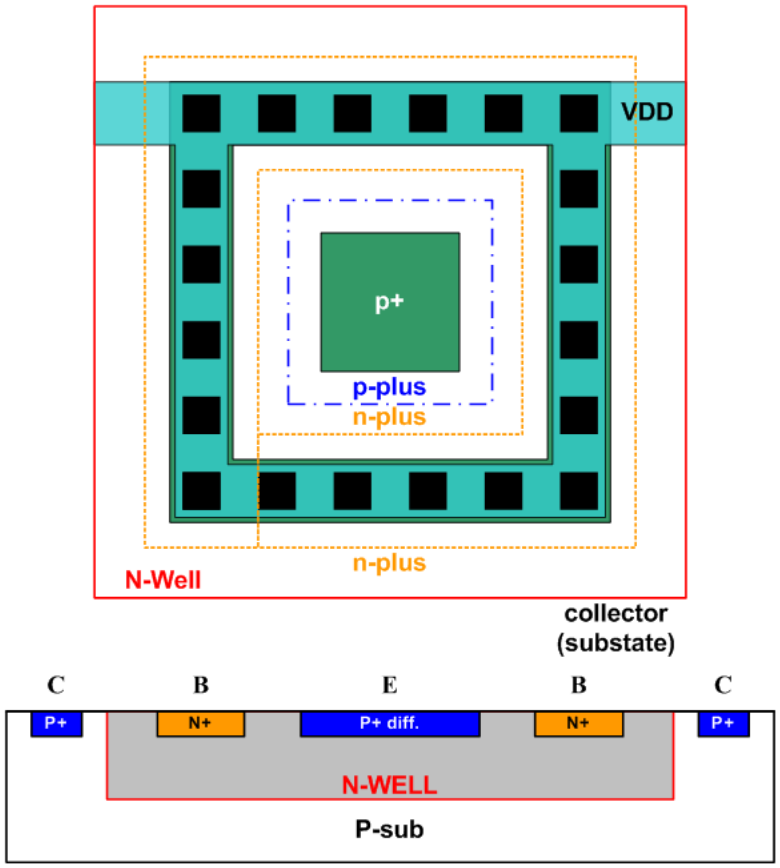
ρ : resistivity
t : thickness
l : conductor length
w : conductor width
RS : sheet resistance

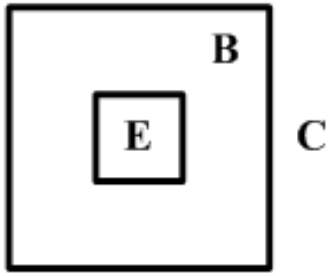
CMOS Passive Inductor





CMOS Parasitic BJT





Lateral bipolar pnp:

emitter P+,
base N-well,
collector P-subtrate

Reference

1. Hong-Yi Huang, *Mixed Signal IC Layout course slides*, FuJen Catholic University, 2004.

2. B. Boser, "*Submicron CMOS Technology for Analog Designers*", EECS dept, UC Berkeley, 2003.

3. Advanced Analog IC Design, Fall 2009, by Prof. Y. Chiu

4. NDL CMOS process introduction. http://www.ndl.org.tw/old/icfab/chinese1/index.htm.