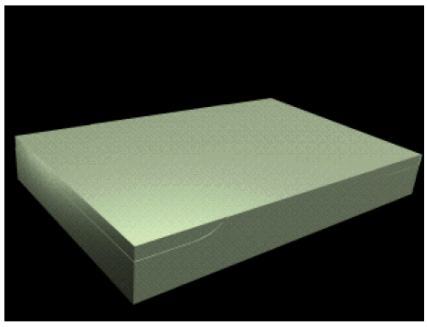
2016 Analog IC: Midterm Examination (110%)

1. Explain the following process key steps and list down one corresponding example layer manufactured by the procedure. **(10%)**

(a) Oxidation. (2%)

Oxidation

- Object
  - Gate dielectric
  - Protective coating in many steps of fabrication

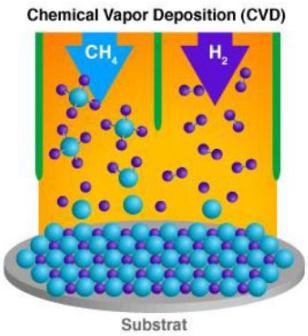


SiO_2

(b) Chemical vapor deposition. (2%)

Chemical Vapor Deposition

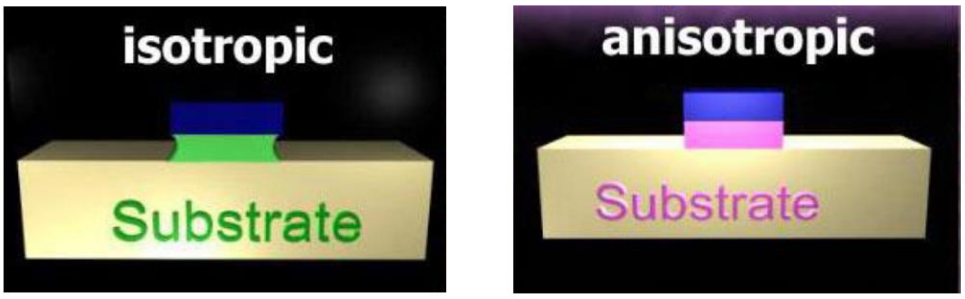
- A process of depositing films by reacting chemical vapors to produce a film on a substrate
  - May be activated by
    - Heat
    - RF energy (plasma enhanced, PECVD)
    - Light (photon induced, PHCVD)
  - CVD process is used to deposit
    - Poly and single crystal silicon
    - Dielectric films
    - Metal films



(c) Etching. (2%)

Etching

- Isotropic
  - Etches in all directions at the same rate
- Anisotropic
  - Achieve the faster etching in one direction than in other directions

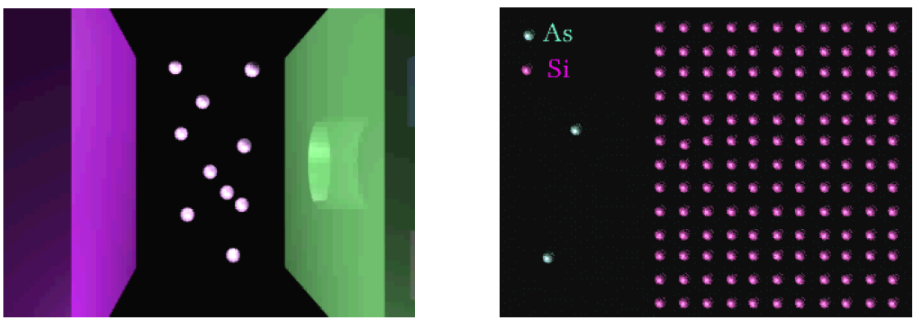


Metal, poly.

(d) Ion implementation. (2%)

Ion Implementation

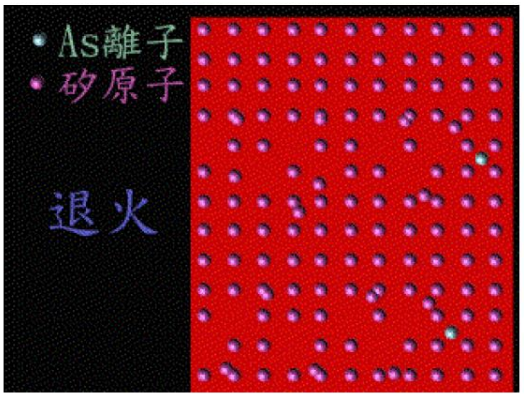
- Introduce Impurities (Dopants)
  - To change the electrical properties of the silicon
  - The most common method for introducing impurities into silicon wafers
    - Impurities with an electric charge are accelerated to high energy and shot into the exposed area of the wafer surface



p^+, n^+

(e) Annealing. (2%)

- Annealing
  - Following the ion implementation
    - A high temperature furnace process is used to anneal out the damage



p^+, n^+

2. Answer definitions of the following terms and explain the physical mechanisms. (10%)

(a) Threshold voltage. (2%)

Minimum gate-to-source voltage differential that is needed to create a conducting path between the source and drain

(b) Channel pinch off. (2%)

At $V_{DS}=V_{GS}-V_{TH}$, the bias point where current stop increase and no inversion layer at the drain end.

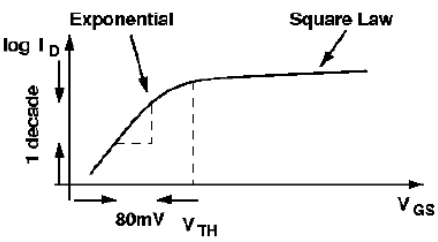
(c) Subthreshold conduction. (2%)

Subthreshold Conduction

- ***Weak Inversion*** : $V_{GS} \approx V_{TH}$, a weak inversion layer exists, small I_D .
- ***Subthreshold Conduction*** : $V_{GS} < V_{TH}$, I_D is finite, it exhibits an *exponential dependence* on V_{GS}. For V_{DS} *greater than roughly 200 mV,*

$$I_D \approx I_0 \exp \frac{V_{GS}}{\zeta V_T}$$

  - With typical values of ζ, at room temperature V_{GS} must decrease ~80 mV for I_D to decrease by one decade.
  - If $V_{TH} = 0.3\ V$, the drain current decreases by only a factor of $10^{3.75}$ when V_{GS} *is reduced to zero.*
  - In rough calculations, we often view V_{TH} as the gate source voltage yielding $I_D / W = 1\mu A / \mu m$
  - The transconductance of MOSFET in subthreshold region is $g_m = \frac{I_D}{\zeta V_T}$
  - Which is inferior to that of bipolar transistors.



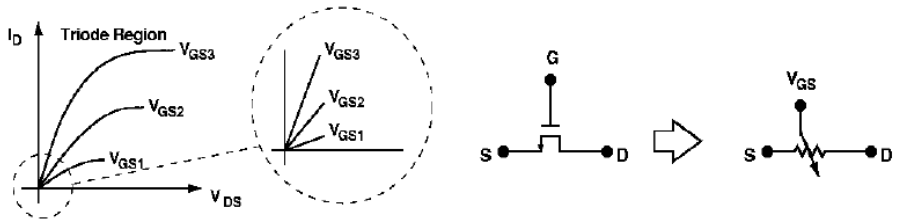
(d) Deep triode region. (2%)

Deep Triode Region

- If $V_{DS} << 2(V_{GS} - V_{TH})$

$$I_{D,\max} \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS} \quad \Rightarrow \quad R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

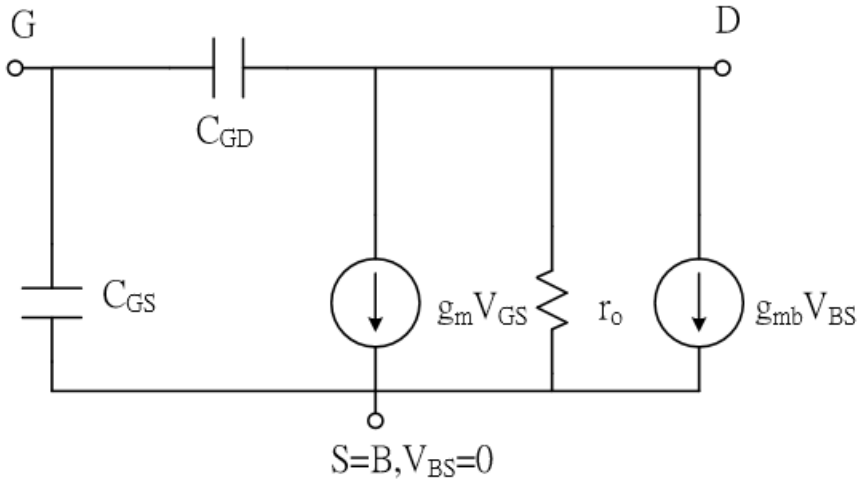
- I/V Characteristic
- MOSFET as a controlled linear resistor



(e) Punch through. (2%)

- *Punch through* : In short channel devices, an excessively large drain source voltage widens the depletion region around the drain so much that it touches around the source, creating a very large drain current.

3. (至少要畫出這樣)



4.

(a) $\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$

(b) $\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$

(c) $\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})$

(d) $\sqrt{2\mu C_{ox}\frac{W}{L}I_D}$

(e) $\frac{2I_D}{V_{ov}}$

5. Answer definitions of the following terms and explain the physical mechanisms. (10%)

(a) Body effect. (2%)

More holes are attracted to the substrate connection, and the depletion region becomes wider (Q_{dep} increases) when $V_{bs}<0$, resulting in the increasing of V_{TH}.

(b) Mobility degradation. (2%)

High vertical electrical field E_{ver} between the gate and the channel confines the charge carriers to a narrow region below the oxide-silicon interface, leading to more

scattering and hence lower mobility.

(c) Velocity saturation. (2%)

In semiconductors, when a strong enough electric field is applied, the carrier velocity in the semiconductor reaches a maximum value.

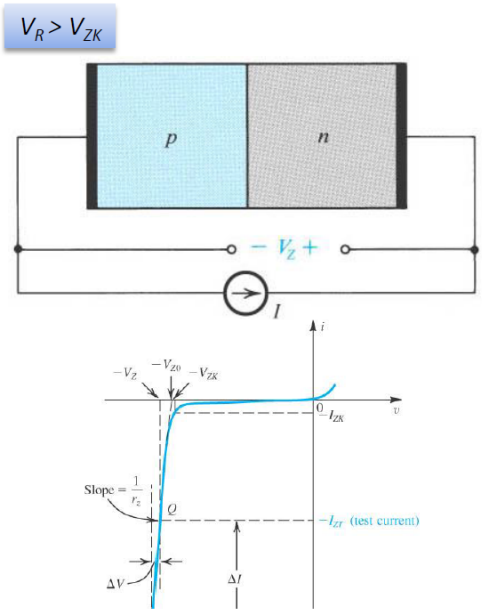
(d) Hot carrier effect. (2%)

While the average velocity of carrier saturates at high fields, the instantaneous velocity and hence the kinetic energy of the carries continue to increase, especially as they accelerate towards the drain. In the vicinity of the drain region, hot carrier may “hit” the silicon atoms at high speeds, thereby creating impact ionization.

(e) Breakdown. (2%)

Voltage breakdown (MOS): At high gate-source voltages, the gate oxide breaks down irreversibly, damaging the transistor.

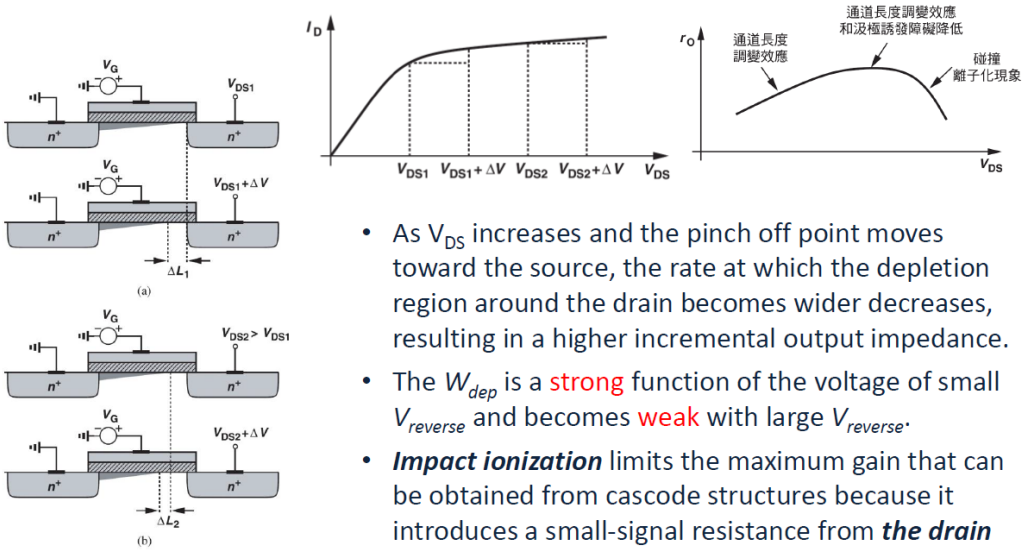
P-N Junction - Breakdown



- Zener breakdown
  - Reverse bias V_R↑, E of depletion region ↑, Covalent bond break
  - Hole-electron pair generation in depletion region, electrons swept to n-type (holes swept to p-type)
- Avalanche breakdown
  - Reverse bias V_R↑, minority swept by electric filed E , kinetic energy break covalent bond
  - Ionizing collision , Hole-electron pair generation in depletion region
- Punch through
  - Two neighboring junction depletion regions meet.

6. Sketch the transfer curve of ro with increasing V_{DS}. List down and explain the 3 effects related to the modification of output impedance. (5%)

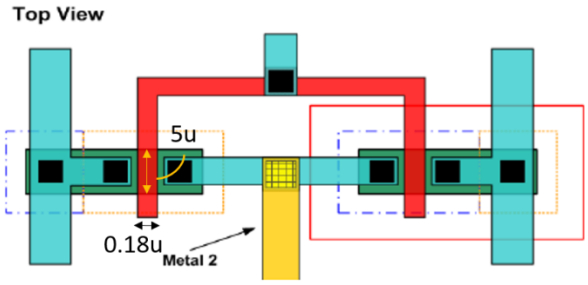
r_o Variation with V_{DS}



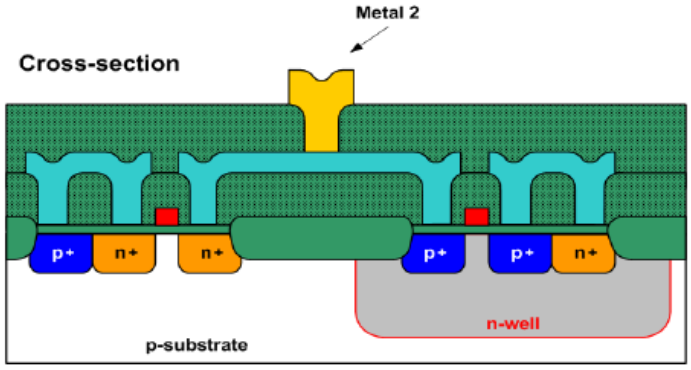
- As V_{DS} increases and the pinch off point moves toward the source, the rate at which the depletion region around the drain becomes wider decreases, resulting in a higher incremental output impedance.
- The W_{dep} is a strong function of the voltage of small $V_{reverse}$ and becomes weak with large $V_{reverse}$.
- ***Impact ionization*** limits the maximum gain that can be obtained from cascode structures because it introduces a small-signal resistance from ***the drain to the substrate*** rather than ***to the source***.

7. To implement an inverter with all MOS devices in a dimension of 5um/0.18um. (5%)

(a) Sketch the layout and mark the dimensions. (2.5%)



(b) Sketch the cross section of MOS devices. (2.5%)



8. Assume $g_{mb} = 0.2g_m$, sketch the small-signal equivalent circuit and derive the equation of voltage gain V_{out}/V_{in} of the amplifier in Fig. 8 in terms of $(W/L)_{<n>}$ and $ro_{<n>}$ with n=1~2. (5%)

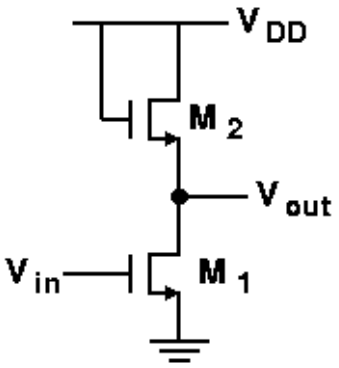
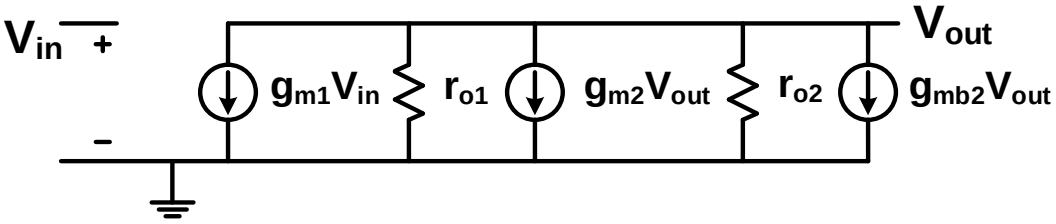
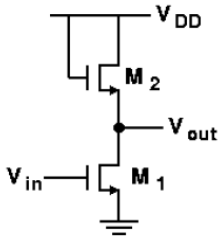


Fig . 8



$V_{out}/V_{in}=-g_{m1}(r_{o1} // r_{o2} // 1/g_{m2} // 1/g_{mb2})$



$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}} = -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta} \qquad \eta = \frac{g_{mb2}}{g_{m2}}$$

$$A_v = -\frac{\sqrt{2\mu_n C_{ox}(W/L)_1 I_{D1}}}{\sqrt{2\mu_n C_{ox}(W/L)_2 I_{D2}}}\frac{1}{1+\eta} = -\frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}}\frac{1}{1+\eta}$$

9.

(a) Find the output impedance Rou. (2.5%)

$$\text{Rout} = \frac{1}{gm_1} || \frac{1}{gmb_1} || r_{o1} || r_{o2} \cong 416.67 \text{ ohm}$$

(b) Find the voltage gain Vout/Vin. (2.5%)

$$\text{Av} = gm_1(Rout || RL) \cong 0.825\ (V/V)$$

(c) By swapping Vin to M2 and Vb to M1, find the voltage gain without RL. (2.5%)

$$\text{Av} = gm_2(\frac{1}{gm_1} || \frac{1}{gmb_1} || r_{o1} || r_{o2}) \cong 0.833\ (V/V)$$

(d) With RL, find th voltage gain. (2.5%)

$$\text{Av} = gm_2(Rout || RL) \cong 0.825\ (V/V)$$

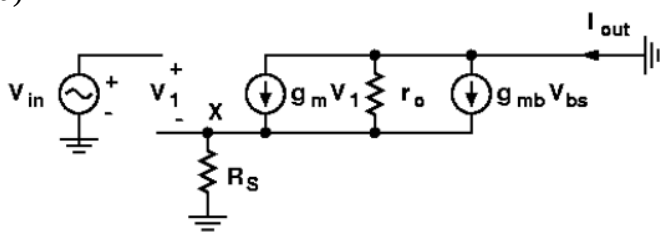
10.

(a) $\text{VDD} - 4V_{ov} = 2.5V$

(b) $\frac{V_{out}}{V_{in}} = -\frac{g_m^2 r_o^2}{2} = -20000(V/V)$

11.

(a)



$$G_m = \frac{g_m}{1+(g_m+g_{mb})R_s} = 4.16\mu$$

(b)

$$\frac{V_{out}}{V_{in}} = -G_m(R_D // g_m r_o R_s) \cong -G_m R_D = -0.83(V/V)$$

12.

(a) $I_{out} = \frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{gs}-V_{th})^2(1+\lambda V_{DS2})}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{gs}-V_{th})^2(1+\lambda V_{DS1})} \times I_{REF} = 2 \times \frac{(1+0.1\times1)}{(1+0.1\times0.8)} \times 10\mu A = 20.37\mu A$

(b) $r_o \approx \frac{1}{\lambda I_{out}} = 490909.090\Omega$

13. ~

(a) Find the differential gain $A_{v.DM.}$ (2.5%)

$$|A_{v,DM}| = Gm(R_D||r_o) = 100\ (V/V)$$

(b) Find the common-mode gain $A_{v.CM}$ without consideration of ro and gmb. (2.5%)

$$|A_{v,CM}| = \frac{\frac{R_D}{2}}{1/2gm + Rss} \cong 0.498\ (V/V)$$

(c) Find the maximum input differential range. (2.5%)

$$\Delta V_{in} = \sqrt{\frac{2Iss}{\mu C_{ox} W/L}} = \sqrt{2}V_{ov} = 0.353\ (V)$$

(d) Find the highest and lowest input common mode level. (2.5%)

$$V_{GS1} + (V_{GS} - V_{TH}) \le V_{in,CM} \le \min[V_{DD},\ V_{DD} - R_D\, I_{SS}/2 + V_{TH}\ ]$$

$$1V \le V_{in,CM} \le 1.7$$

14.

(a) $g_{m3} = g_{m4} = \frac{2 \times I_{ref}}{V_{ov}} = 0.64m(A/V)$

$g_{m3} = g_{m4} = 4g_{m1} = 8m(A/V)$

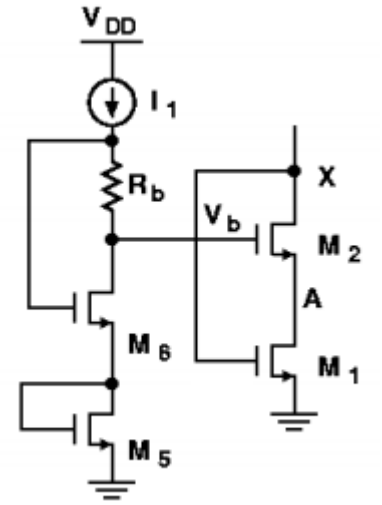
(b) $R_{out} = g_{m4} r_{o4} r_{o3} = 6.4M\ ohm$

$R_{out} = g_{m4} r_{o4} r_{o3} = 80M\ ohm$

(c) $V_b = 2V_{ov} + V_{th} = 1V$

$V_{out} = 2V_{ov} = 0.5V$

(d)



15. TFTTF