Reversed Nested Miller Compensation With Voltage Buffer and Nulling Resistor

Kin-Pui Ho, Cheong-Fat Chan, Chiu-Sing Choy, and Kong-Pang Pun

***Abstract*—This paper presents a new reversed nested Miller compensation technique for multistage operational amplifier (opamp) design. The new compensation technique inverts the sign of the right half complex plane zero and shifts the frequency of the complex conjugate poles to a higher frequency. Simulation results indicate that the gain-bandwidth product and settling time are improved by factors of two and three, respectively, without degrading stability and power consumption. To verify the proposed technique, a three-stage opamp is fabricated with 0.6-μm CMOS technology. The measured results of the test circuit agree with the results that are obtained from theoretical analysis and circuit simulation.**

I. Introduction

THE USE OF the reversed nested Miller circuit is a common technique that is used for multistage operational amplifier (opamp) design. However, the reversed nested Miller compensation technique is still imperfect due to the undesired properties of its higher order zero and poles [1], which limit the maximum achievable bandwidth of the amplifiers. Their effects are even more dominant in low-power circuits [2], [3]. We will address these problems by introducing an improved compensation network.

II. Reversed Nested Miller Compensation With Voltage Buffer and Nulling Resistor

A block diagram of the new compensation circuit is shown in Fig. 1. The new compensation circuit proposed in [4] with an extra nulling resistor. The design in [4] inserted a voltage buffer between the output of the second-stage amplifier and the feedback capacitor Cc_1. The voltage buffer implements an impedance transformation, such that its high input impedance eliminates the loading effect of the second gain stage. Moreover, the low output impedance of the voltage buffer replaces the high impedance output of the second gain stage to drive the feedback capacitor Cc_1. Effectively, the design in [4] reduces the time constant of the second gain stage, and thus the size of Cc_1 can be reduced to a lower value without degrading the phase margin.

In reversed nested Miller compensation, the capacitive feedback loops stabilize the amplifier by introducing negative feedback. However, the capacitive feedback paths represent an internal loading inside the amplifier. The feedforward effect from these compensation capacitors creates a right-half-plane (RHP) zero because the feedforward current through them is out of phase with the current that is flowing into the loading capacitor [5]. In line with this observation, we inserted a nulling resistor R at the output node of the capacitive feedback paths, as shown in Fig. 1. The nulling resistor blocks the feedforward paths. Thus, it can prevent the output impedance of the first stage from being pulled down by the compensation capacitors at high frequency. Consequently, the nulling resistor improves the phase margin by reducing the first-stage gain drop at high frequency.

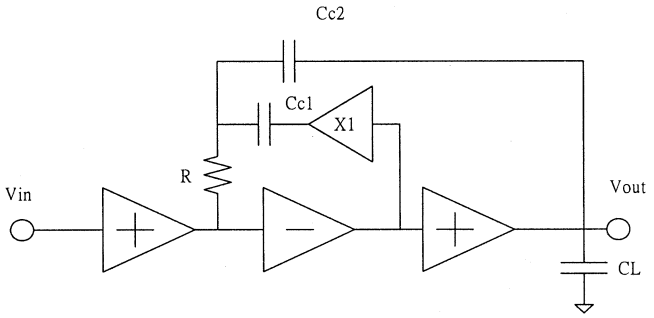

Fig. 1. Block diagram of the improved reversed nested Miller compensation technique.

A schematic diagram and small-signal model of the proposed compensation technique are shown in Figs. 2 and 3, respectively. In Fig. 3, the parasitic capacitances at the output of the first and second stages are neglected because their effects are insignificant when compared with the two feedback capacitors. This model takes into account the finite output resistance of the voltage buffer. Solving $V_{\rm out}/V_{\rm in}$, the transfer function of the proposed circuit is given by (1), shown at the bottom of the next page, where

$$A_{\rm DC} = -gm_1gm_2gm_3r_1r_2r_3$$
$$\text{Dominant Pole} = -\frac{1}{Cc_2gm_2gm_3r_1r_2r_3}.$$

Similar to reversed nested Miller compensation, the gain-bandwidth product is equal to $gm1/Cc2$. From (1), we can see that the second-order term of the quadratic equation which determines the complex conjugate poles is suppressed by a factor equal to $r_{\rm out}/r_2$, where $r_{\rm out}$ is the output impedance of the voltage buffer and r_2 is the total output impedance of stage two, as illustrated in Fig. 2. This observation demonstrates the significance effect of the impedance transformation by the voltage buffer. In the frequency domain, the expression indicates that the real part of the complex conjugate poles is multiplied by a factor that is roughly equal to $r_2/r_{\rm out}$. Thus, the complex conjugate poles are shifted to a higher frequency if $r_{\rm out}$ is sufficiently small.

The design in [4] used a voltage buffer to shift the RHP zero to a higher frequency. The resulting location of the RHP zero is given by $\omega = gm_3gm_2r_2/Cc_2$, and its effect can be further suppressed by increasing gm_3. However, this leads to an increase in power consumption. In our design, the RHP zero is

Manuscript received April 18, 2003; revised June 26, 2003.

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Digital Object Identifier 10.1109/JSSC.2003.817598

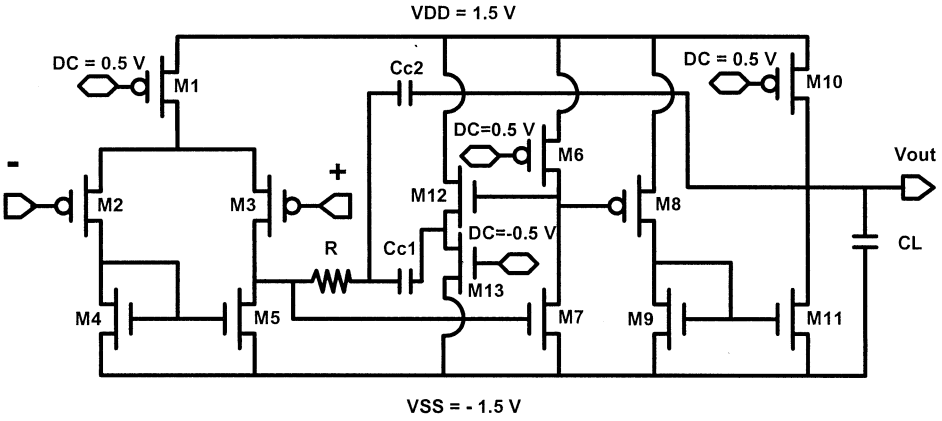

Fig. 2. Schematic diagram of the proposed amplifier.

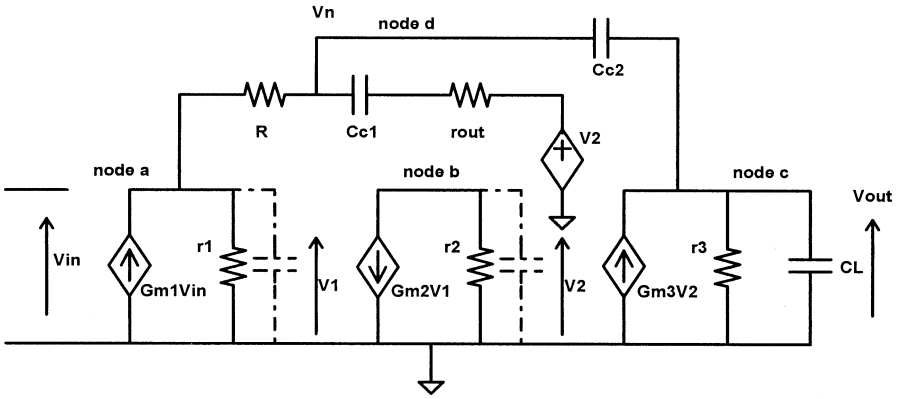

Fig. 3. Small-signal model of the amplifier using the improved compensation network.

completely eliminated by introducing a nulling resistor. Moreover, adjustment of the nulling resistance R can modify the characteristics of (1). By setting the second-order term in the numerator to positive, the roots of the numerator are always located on the left-half-plane (LHP). Hence, we can invert the sign of the RHP zero of a conventional reversed nested Miller compensation circuit and move the zero to the LHP. The inversion takes place without the use of extra power. The condition for the sign inversion to take place is approximately given by

$$R \geq \frac{r_{\text{out}}}{gm_2 r_2 (1 + gm_3 r_{\text{out}})}. \tag{2}$$

We compared simulations of the design in [4] and the proposed design. The results are presented in Table I. The new design has approximately 33% improvement in settling time. The proposed RHP zero cancellation technique appear to be very similar to that which is commonly used in the two-stage opamp design [6], [7], but there are subtle differences. First, the suggested solution inverts the sign of the RHP zero and moves it to the LHP. In the traditional technique, a nulling resistor generates a pole over the RHP zero to exactly channel it. Unfortunately, process tolerance or temperature variation often makes the resistance different from the theoretical value. Consequently, the pole cannot fall exactly over the RHP zero, and closely spaced pole-zero doublets are usually left. The new technique does not require perfect matching of the nulling resistor, as indicated

TABLE I
COMPARISON BETWEEN COMPENSATION TECHNIQUE WITH AND WITHOUT NULLING RESISTOR

	Buffer without nulling resistor	Buffer with nulling resistor
Gain-bandwidth product (MHz)	19.6	19.6
Phase Margin (degrees)	48.21	59.7
Settling time (Within 1% of step size) (ns)	95.5	64.22
DC Power Consumption (mW)	1.44	
DC gain (dB)	96.9	
Loading Capacitance (pF)	15	

$$A_{\text{IRNMC}}(s) = \frac{A_{\text{DC}} \left(1 + \left(R(Cc_1 + Cc_2) + Cc_1 r_{\text{out}} - \frac{Cc_2}{gm_2 gm_3 r_2}\right) s + Cc_1 Cc_2 R \left(\frac{1}{gm_3} + r_{\text{out}} - \frac{r_{\text{out}}}{gm_2 gm_3 R r_2}\right) s^2\right)}{(Cc_2 gm_2 gm_3 r_1 r_2 r_3 s + 1)\left(\frac{r_{\text{out}}}{r_2}\frac{Cc_1 C_L}{gm_2 gm_3} s^2 + \left(\frac{Cc_1 C_L}{Cc_2 gm_3} + \frac{Cc_1(1 + gm_3 r_{\text{out}})}{gm_3}\right) s + 1\right)} \tag{1}$$

TABLE II
NULLING RESISTOR SENSITIVITY COMPARISON

	Original resistance value (320 ohm)	Resistance increased by 30% (416 ohm)	Resistance decreased by 30% (224 ohm)
Gain-bandwidth product (MHz)	19.6	19.6	19.6
Phase Margin (degrees)	59.7	63.11	56.69
Settling time (Within 1% of step size) (ns)	64.22	61.32	66.73

by (2). To further prove that the new technique does not require a perfect match of the nulling resistor, we simulated a three-stage opamp in which the nulling resistor's value varied by $\pm 30\%$. The results are displayed in Table II. The settling time changes less than $\pm 5\%$.

Second, in traditional compensation networks, the nulling resistor value is usually equal to the reciprocal of the output stage transconductance $1/gm$ [1], [2], where gm is proportional to the dc biasing current. Thus, a large nulling resistor is needed for low-power operation. The large resistor uses more chip area and generates large parasitic capacitance that cannot be simply neglected. However, the nulling resistor of the new proposed technique is suppressed by a factor that is equal to the gain of the second stage, as indicated by (2). Therefore, we can implement the smaller nulling resistor with polysilicon, which provides a more accurate resistor with less parasitic capacitances.

Third, we computed the values of Cc_2, Cc_1, and a damping factor for the conventional reversed nested Miller and improved reversed nested Miller techniques. The calculation assumes a unity-feedback configuration with a third-order Butterworth frequency response. The two compensation techniques have the same gain-bandwidth product of gm_1/Cc_2. However, the feedback capacitor Cc_2 is suppressed by a factor of $1/4gm_1(r_{\text{out}} + 1/gm_3)$ in the new circuit. In other words, the gain-bandwidth product is improved by a factor of $4gm_1(r_{\text{out}} + 1/gm_3)$. In addition, the damping factor of the complex conjugate poles is enhanced by a factor that is roughly equal to $\sqrt{r_2/r_{\text{out}}}$, which will reduce the settling time of the amplifier.

III. EXPERIMENTAL RESULTS

We designed two three-stage opamps with the conventional reversed nested Miller and improved reversed nested Miller compensation techniques that are shown in Fig. 2, using 0.6-μm CMOS technology to verify the design. The cores of the three-stage opamps are identical except for the different frequency compensation circuits. Both opamps have the same capacitive load, phase margin, and power consumption of 15 pF, 60°, and 1.4 mW, respectively. The simulation results indicate that the improved reversed nested Miller circuit has a gain-bandwidth product of 20 MHz, while the conventional reversed nested Miller circuit has a gain-bandwidth product of only 11 MHz. Moreover, the improved reversed nested Miller circuit decreases the settling time from 195 to 65 ns. The simulation results and the values of the feedback capacitances and resistance are summarized in Table III. The improved reversed nested Miller circuit with an extra voltage buffer consumes approximately the same power (1.44 mW) as the conventional

TABLE III
SIMULATED RESULTS COMPARISON BETWEEN CONVENTIONAL AND IMPROVED REVERSED NESTED MILLER COMPENSATION CIRCUITS

	Reversed Nested Miller Compensation (Schematic simulation)	Improved Reversed Nested Miller Compensation (Post-layout simulation)
Loading Capacitance (pF)	15	
Phase Margin (degrees)	61.2	59.7
DC Power Consumption (mW)	1.46	1.44
Gain-bandwidth product (MHz)	10.97	19.60
Settling time (Within 1% of step size) (ns)	194.9	64.22
Cc_2 (pF)	5.8	3.0
Cc_1 (pF)	1.3	0.7
R (Ω)	-	300
DC gain (dB)	96.9	96.9

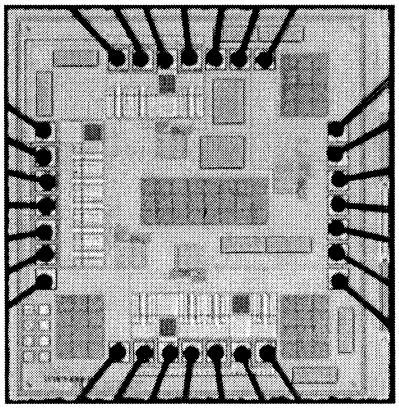

Fig. 4. Microphotograph of the test chip.

TABLE IV
MEASURED PERFORMANCE OF THE OPERATIONAL AMPLIFIER USING THE IMPROVED REVERSED NESTED MILLER COMPENSATION TECHNIQUE

Power supply (V)	±1.5
Biasing voltage (V)	±0.5
Input offset voltage (mV)	7.4
Input common mode voltage range	-1.4V to +1.27V
Loading capacitance (pF)	15
Gain-bandwidth product (MHz)	19.46
Phase margin (degree)	55.50
DC Gain (dB)	83.12
+ Slew rate (V/μs)(Unity gain configuration)	11.1
- Slew rate (V/μs)(Unity gain configuration)	16.5
Overshoot (%)	12.8
Settling time (ns) (Within 1% of the step size)(unity gain +1)	75.3
DC power consumption (mW)	1.4

design, because the voltage buffer reduces the driving power of the second gain stage. Consequently, the addition of an extra voltage buffer does not significantly increase the power consumption.

We used the suggested compensation technique to fabricate a three-stage opamp with a 0.6-μm CMOS technology. A microphotograph of the test chip is shown in Fig. 4. The measurement results are summarized in Table IV. The measured gain-bandwidth product is equal to 19.46 MHz, which is consistent with the post-layout simulation result. However, there is a 13-dB difference between the simulated and measured dc gain. We believe the difference is caused by the measurement

method. We extracted the dc gain by forcing the opamp into oscillation using positive feedback [8]. The dc gain was extracted from the measured oscillation frequency and the values of the passive feedback components. We used this indirect measurement method because our limited equipment prevented us from doing a direct dc gain measurement.

IV. Conclusion

We have presented the design, operating principles, and measurement results of a three-stage opamp using improved reversed nested Miller compensation. The compensation technique includes the sign inversion of a right half complex plane zero and the frequency multiplication of a pair of complex conjugate poles. The new compensation technique substantially improves the bandwidth, settling time, and slew rate of a conventional reversed nested Miller compensated opamp. The measured results that are listed in Table III match the simulation results that are listed in Table IV. For example, the measured GBP is 19.46 MHz and the simulated GBP is 19.6 MHz. Thus, we conclude that the new compensation technique can improve the GBP and settling time by factors of two and three, respectively.

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