approximately 409 kHz. Since this being-tuned center frequency is still less than 450 kHz, the tuning voltage would increase until the desirable center frequency is found. This tuning process is similar to the scenario that has been illustrated in Fig. 4. The final tuning voltage is approximately 1.7 V, which is about 300 mV less than the nominal value of the tuning voltage V_c at the beginning of the tuning process.

In a similar fashion, the tuning process for the center frequency that starts out at 225 kHz is shown in Table III. Here, the first three MSBs of the SAR are compensated to be logic 1's, and after that, the SAR keeps increasing until 450 kHz is found. The final tuning voltage is about 2.6 V, signifying that the tuning voltage has been increased from the nominal value of 2.0 V to correspond appropriately to the increasing of the center frequency from the initial start of 225 kHz. Utilizing the logic gates from the standard-cell library of a 0.25 μm CMOS process and a 12.6-MHz external clock, the maximum duration of one iteration is allotted to be 100 μs. Thus, the total tuning time is about 800 μs in the worst case. The simulation result of this tuning process is illustrated in Fig. 13.

IV. Conclusion

In this paper, a tuning scheme based on the step response of a high-Q BPF and the SA algorithm is proposed. To reduce the complexity of the system, the constant-Q tuning characteristic of a BPF is introduced. To improve the tuning time, a compensation technique is also presented. The main disadvantage of this compensation technique is that it requires a high degree of matching among the transconductors, which may not be appropriate for a large number of compensating MSBs, and/or in the case where a highly sensitive filter architecture is implemented, such as biquad filters. Nevertheless, the proposed tuning technique without the SA compensation still yields a high tuning resolution (0.4%) with only B iterations for a B-bit SAR in the worst case.

Acknowledgment

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Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers

Rosario Mita, Gaetano Palumbo, and Salvatore Pennisi

***Abstract*—The reversed nested Miller compensation technique applied to a three-stage operational amplifier is discussed in this paper and new and simple design equations, accurately predicting the loop-gain phase margin, are developed. Techniques for parasitic positive-zero cancellation are also investigated and compared. For this purpose, we found that using nulling resistors is unpractical. Instead, exploiting only one follower (either a voltage or a current one) in the compensation branch results to be more appropriate. Indeed, not only does it avoid any additional constraint on stage transconductance, but it also overcomes the inherent limitations incurred by voltage and current followers when used to compensate two-stage amplifiers. Post-layout simulations on a CMOS opamp using the parameters of a 0.35-μm process are found to be in good agreement with the expected results.**

***Index Terms*—Analog circuits, CMOS, frequency compensation, Nested Miller, OTA.**

I. Introduction

Modern integrated circuit (IC) applications increasingly demand low-voltage, high-gain, and wide-swing capabilities. In several situations, the gain of a two-stage amplifier is not sufficient and the use of more stages is necessary [1]–[4]. As the traditional approach of cascoding gain stages is not suitable for low-voltage environments, cascading is the only viable option. However, this approach needs more complex frequency compensation because of the increased number of high impedance nodes (and, in turn, low frequency poles) [5]–[11].

When the amplifier is made up of three gain stages and the inner stage is the only inverting one, reversed nested Miller compensation (RNMC) becomes the most suitable [5].

In the discussion to follow, a three-stage amplifier will be considered with emphasis being placed on a CMOS implementation. Compared to bipolar solutions, CMOS counterparts require parasitic-zero removal because of the lower transistor transconductance. In this context, we will describe simple compensation strategies including three different techniques for the zero cancellation.

II. Reversed Nested Miller Compensation

In this section, the RNMC technique is reviewed by using a design-oriented approach that, unlike the one already proposed in [5], uses the phase margin of the loop gain as the main design parameter. To this end, let us consider the small-signal equivalent circuit of a three-stage amplifier depicted in Fig. 1. Parameters g_{mi} and r_{oi} are the ith stage transconductance and output resistance, respectively. Capacitor C_L is the equivalent load capacitor while capacitors C_{oi} represent the equivalent capacitances at the output of each stage, which will be neglected due to their lower values compared with C_{C1}, C_{C2} and C_L. Throughout this paper it will be assumed that parameters g_{mi}, r_{oi}, and C_L have been determined from a different set of constraints and hence will be treated as constants.

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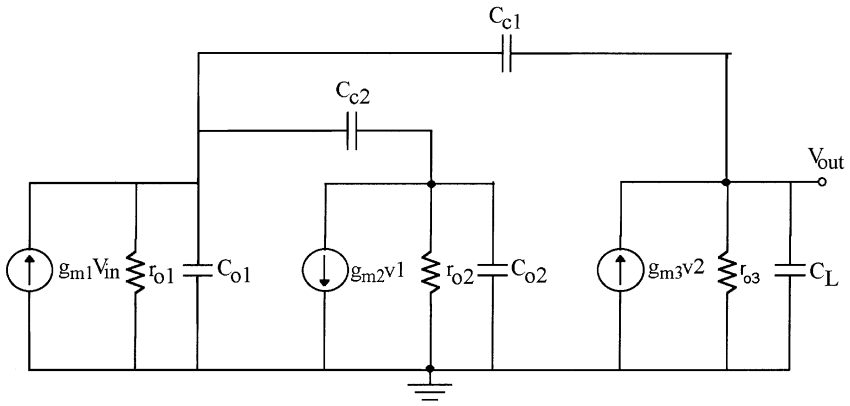

Fig. 1. Small-signal model of a three-stage amplifier with reversed nested Miller compensation.

Under these assumptions and neglecting second-order terms, the open-loop gain of the circuit in Fig. 1 is expressed by

$$A(s) = A_o \frac{1 - \left(\frac{C_{C2}}{g_{m2}} + \frac{C_{C1}}{g_{m2}g_{m3}r_{o2}}\right)s - \frac{C_{C1}C_{C2}}{g_{m2}g_{m3}}s^2}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1+\left(\frac{C_{C2}C_L}{g_{m3}C_{C1}} - \frac{C_{C2}}{g_{m2}} + \frac{C_{C2}}{g_{m3}}\right)s + \frac{C_{C2}C_L}{g_{m2}g_{m3}}s^2\right]} \tag{1}$$

where A_o is the dc open-loop gain equal to $A_1A_2A_3 = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$ and ω_{P1} is the angular frequency of the dominant pole which is due to the compensation capacitor C_{C1} amplified by the Miller effect. Therefore, the dominant pole is

$$\omega_{P1} \approx \frac{1}{r_{o1}A_2A_3C_{C1}} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{C1}} \tag{2}$$

and the gain-bandwidth product, ω_{GBW}, becomes g_{m1}/C_{C1}.

Equation (1) also includes two other (higher) poles and two zeros. The two nondominant poles can be complex and conjugate, thus making compensation difficult. Besides, since the coefficients of the s and s^2 terms in the numerator are both negative, a right-half-plane (RHP) zero is created that is located at a lower frequency than the other left-half-plane (LHP) zero.

For power amplifiers in which g_{m3} is very large (due to the large dimension and quiescent current of the output transistors), the zeros are positioned at a much higher frequency than ω_{GBW} and their contribution to both the loop-gain magnitude and phase margin can be neglected. However, this cannot generally be assumed in a low-power context where, as a result, it becomes mandatory to remove the RHP-zero. Unfortunately, no strategy for RHP-zero cancellation has been reported in the literature.

Ideally, both zeros can be eliminated by using two voltage or current followers in series with compensation capacitors. In these cases (1) becomes respectively

$$A(s) = A_o \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{C_{C2}C_L}{g_{m3}C_{C1}}s\right)} \tag{3a}$$

$$A(s) = A_o \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1+\frac{C_{C2}(C_{C1}+C_L)}{g_{m3}C_{C1}}s\right]}. \tag{3b}$$

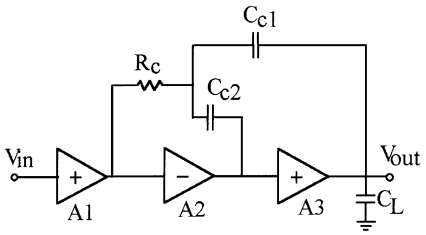

Fig. 2. Technique for the RHP-zero elimination with one nulling resistor.

Assuming to have canceled the two zeros, a specified phase margin m_φ [with $\tan m_\varphi = (\omega_{P2})/(\omega_{GBW})$] requires in the two cases that

$$\tan m_\varphi = \frac{g_{m3}}{g_{m1}}\frac{C_{C1}^2}{C_{C2}C_L} \tag{4a}$$

$$\tan m_\varphi = \frac{g_{m3}}{g_{m1}}\frac{C_{C1}^2}{C_{C2}(C_{C1}+C_L)}. \tag{4b}$$

Since C_{C1} is set by the required unity-gain bandwidth, and assuming g_{m1}, g_{m3} and C_L to be already set, (4a) and (4b) give the needed value of C_{C2}. These equations describe ideal compensation schemes. More realistic conditions, which take into account the effects of the zero-canceling technique adopted, will be analyzed in the following. For the sake of completeness, we shall first deal with the nulling resistor technique which for two-stage OTA's is the simplest and most widely used one [12].

III. RHP Zero Cancellation With Resistors

In this section the use of nulling resistors for RHP-zero cancellation is investigated and an approach utilizing only one resistor is proposed. Indeed, the loop gain of the usual compensation network employing two nulling resistors exhibits real and negative zeros only with complex matching between R_{C1} and R_{C2}.

A more effective solution which uses only one resistor is that given in Fig. 2. It leads to the following expression of $N(s)$

$$N(s) = 1 + \left[R_C(C_{C1}+C_{C2}) - \frac{C_{C2}}{g_{m2}}\right]s - \frac{C_{C1}C_{C2}}{g_{m3}}\left(\frac{1}{g_{m2}} - R_C\right)s^2 = 1 + \frac{C_{C1}}{g_{m2}}s \tag{5}$$

where the last identity is obtained setting $R_C = 1/g_{m2}$, and yields only one negative zero.[1] Of course, the denominator of the open-loop gain is still the same as in (1). In this case, it is convenient to have $g_{m2} = g_{m3}$. As we will show, this choice allows a pole–zero cancellation to be achieved. Indeed, assuming also

$$C_{C2}C_L > 4C_{C1}^2 \tag{6}$$

meaning that the determinant of the second-order factor in the denominator of (1) is positive, it follows that all poles are real and (1) becomes

$$A(s) = A_o \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{C_{C2}C_L}{g_{m3}C_{C1}}s\right)} \tag{7}$$

which for a given phase margin gives

$$C_{C2} = \frac{C_{C1}^2 g_{m3}}{\tan m_\varphi C_L g_{m1}}. \tag{8}$$

Now, using (8) in (6), we get $g_{m2,\,3}/g_{m1} > 4\tan m_\varphi$. Since a phase margin of about 60° is generally required, it follows that the transconductance of both the second and third stage of the amplifier must be at least seven times greater than the transconductance of the first stage. This implicitly limits the application of this technique to eliminating the RHP-zero since gain stage transconductances are usually set by other kinds of specifications.

IV. RHP-Zero Cancellation With Voltage Follower

Two voltage followers can be used to break the forward path through C_{C1} and C_{C2}. However the follower used in the external loop has its input connected to the output of the amplifier. As for the two-stage OTA, this unacceptably reduces the output swing especially in low voltage applications [14], [15].

By adopting a compensation approach which makes use of only one voltage follower in the inner loop, as shown in Fig. 3, the output swing is completely preserved. Besides, we will exploit the finite output resistance of the voltage follower, as done for a two-stage OTA in [15]. Denoting this output resistance as r_v, the loop-gain transfer function modifies to (9) shown at the bottom of the page, where the dominant pole ω_{P1} is again given by (2).

Equation (9) includes one dominant LHP-zero and a RHP-zero that is now shifted to a very high frequency (since it is multiplied by the stage gain $g_{m2}r_{o2}$). Moreover, it has two nondominant poles which are real under the condition (in practice usually met) $g_{m2}r_{o2}C_{C2} > 2C_L$.

To obtain some form of simplification in (9), we exploit the output resistance of the voltage follower. Among the possible alternatives, we choose this resistance proportional to the transconductance of the last stage

$$r_v = \frac{\gamma}{g_{m3}} \tag{10}$$

with $\gamma \geq 1$ is conveniently assumed. Note that since a voltage follower is usually implemented with a common-drain transistor, and (10) requires its transconductance to be a scaled replica of g_{m3}. Using (12) in

[1]At this purpose, techniques to perform the matching of MOS resistors and transconductances have been developed in [13].

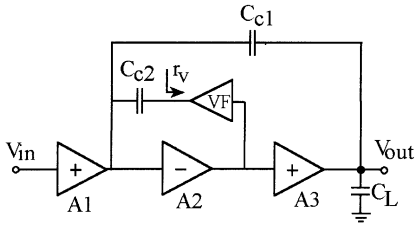

Fig. 3. Technique for the RHP-zero elimination with one voltage follower.

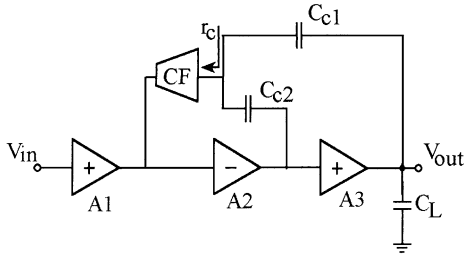

Fig. 4. Technique for the RHP-zero elimination with one current follower.

TABLE I
TRANSISTOR DIMENSIONS OF THE THREE-STAGES AMPLIFIER

Transistors	Dimensions
M1, M2	100/0.35
M3, M4, M5	60/0.35
M6	12/0.35
M7, M8, MB1, MB2	20/1
M9	480/0.35
MB3	10/1

(9) we obtain the following expressions for the nondominant poles and the two zeros:

$$\omega_{P2} = \frac{g_{m3}}{C_{C2}\left(\frac{C_L}{C_{C1}} + 1 + \gamma\right)} \tag{11a}$$

$$\omega_{P3} = \frac{\frac{C_L}{C_{C1}} + 1 + \gamma}{C_L} \frac{g_{m3}g_{m2}r_{o2}}{\gamma} \tag{11b}$$

$$\omega_{Z1} = \frac{g_{m3}}{\gamma C_{C2}} = \frac{1}{\alpha}\omega_{P2} \tag{11c}$$

$$\omega_{Z2} = -\frac{g_{m3}g_{m2}r_{o2}}{C_{C1}} \tag{11d}$$

where parameter α in (11c) is expressed by

$$\alpha = \frac{\gamma C_{C1}}{C_L + (1+\gamma)C_{C1}} \tag{12}$$

$$A(s) \approx \frac{A_o}{\left(1 + \frac{s}{\omega_{P1}}\right)} \frac{(1 + r_v C_{C2} s)\left(1 - \frac{C_{C1}}{g_{m2}g_{m3}r_{o2}}s\right)}{\left[1 + \frac{C_{C2}(C_L + C_{C1} + g_{m3}r_v C_{C1})}{g_{m3}C_{C1}}s\right]\left[1 + \frac{C_{C1}C_L r_v}{g_{m2}r_{o2}(C_L + C_{C1} + g_{m3}r_v C_{C1})}s\right]} \tag{9}$$

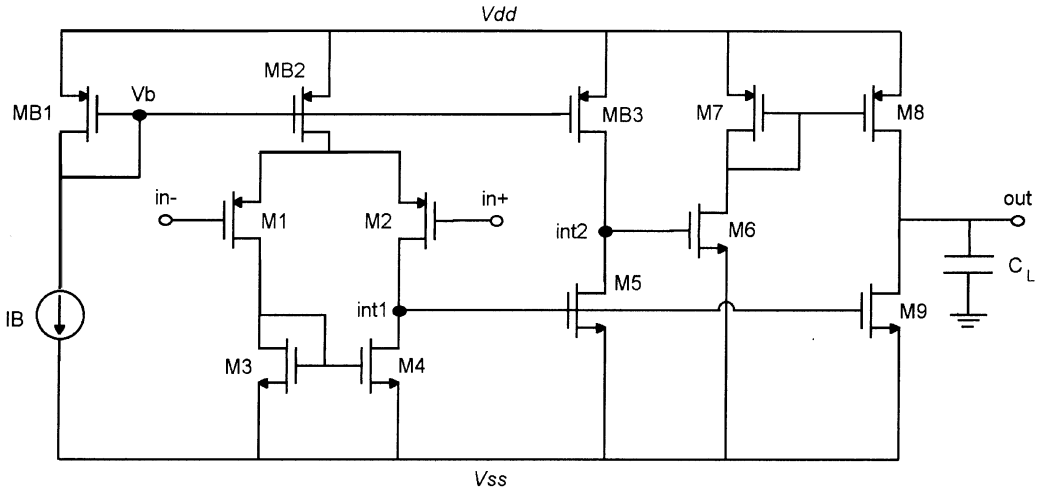

Fig. 5. Simplified schematic of the core amplifier used for the simulations.

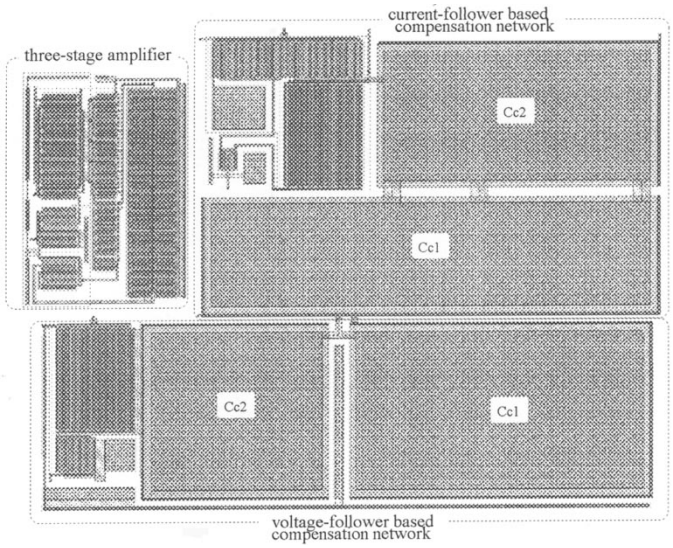

Fig. 6. Layout of the core amplifier and the two compensation networks.

which is positive and always lower than 0.5, i.e., the first zero is at least twice higher the second pole.

Moreover, It is apparent that ω_{P3} and ω_{Z2} are at a very high frequency (with $\omega_{P3} > \omega_{Z2}$) and their contribution to the phase margin can be neglected. Thus the phase margin is given by

$$m_\varphi = \tan^{-1}\frac{\omega_{P2}}{\omega_{GBW}} + \tan^{-1}\frac{\omega_{GBW}}{\omega_{Z1}} \approx \tan^{-1}\frac{\omega_{P2}}{\omega_{GBW}} \tag{13}$$

where the approximation holds if the zero can be neglected. Besides, using (11c) in (13), we obtain

$$C_{C2} = \frac{g_{m3}}{g_{m1}}\frac{2\alpha}{(1-\alpha)\tan m_\varphi + \sqrt{[(1-\alpha)\tan m_\varphi]^2 - 4\alpha}}C_{C1} \approx \frac{g_{m3}}{g_{m1}}\frac{C_{C1}}{\left(\frac{C_L}{C_{C1}} + 1 + \gamma\right)\tan m_\varphi}. \tag{14}$$

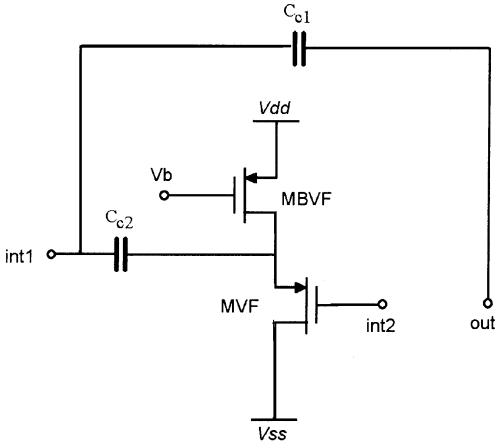

Fig. 7. Voltage-follower based compensation network.

V. RHP-Zero Cancellation With Current Follower

Two current followers nominally cancel the two zeros in (1). In two-stage OTAs, RHP-zero cancellation through the current follower is critical for its exacting requirements in terms of low current follower input resistance [17], [18]. This means high power and/or area consumption. For this reason it is rarely adopted. In contrast, the current follower can be profitably employed in the class of amplifiers under study, leading to a simple and viable design with more relaxed requirements. In partic-

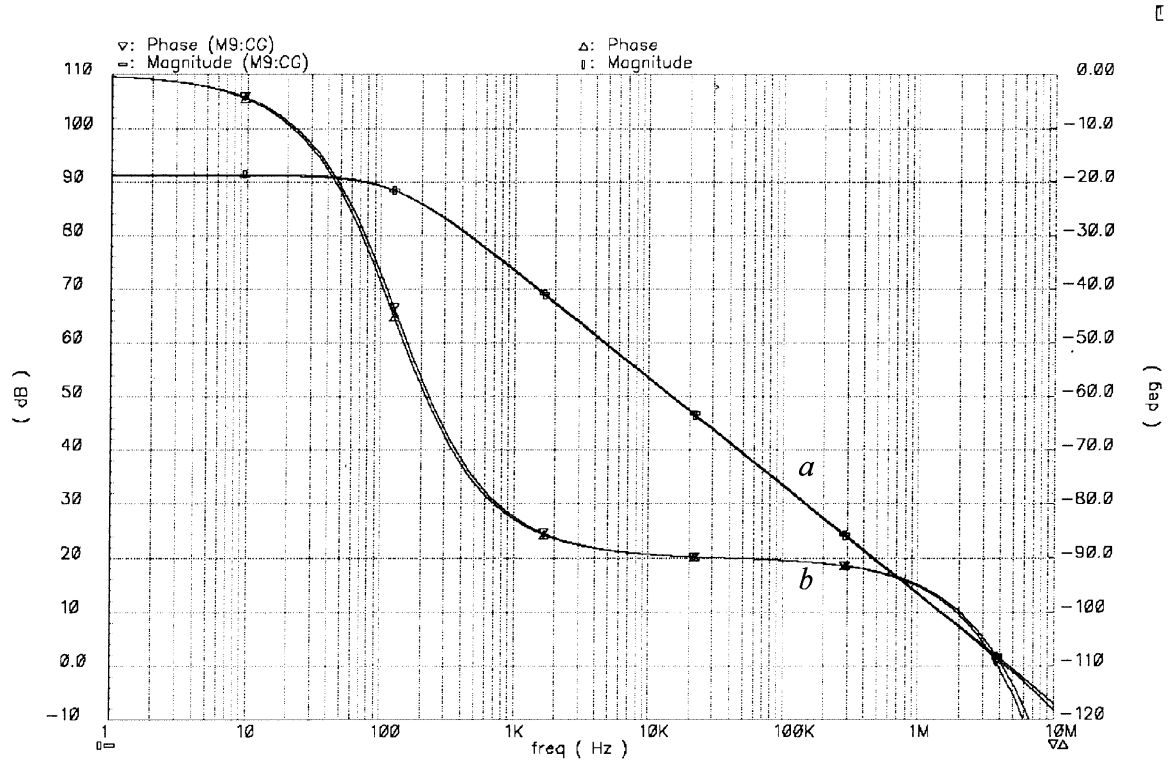

Fig. 8. Compensation using one voltage follower. Loop gain frequency response: magnitude (curves $\boldsymbol{a}$) and phase (curves $\boldsymbol{b}$).

ular, only *one* current follower is needed to break the forward path, as shown in Fig. 4. Since the overall feedback current is still the same, the loop-gain transfer function is again given by (3b), and (4b) still holds if an ideal current follower is considered.

If we take into account the finite input resistance of the current follower, r_c, the loop gain will include another pole and two zeros, as shown in the following:

$$A(s) = -\frac{A_0}{\left(1+\frac{s}{\omega_{P1}}\right)} \frac{1+(C_{C1}+C_{C2})\,r_c s+\frac{C_{C1}C_{C2}r_c}{g_{m3}}s^2}{\left[1+\frac{C_{C2}(C_{C1}+C_L)}{g_{m3}C_{C1}}s\right]\left[1+\frac{C_L C_{C1} r_c}{(C_L+C_{C1})g_{m2}r_{o1}}s\right]} \tag{15}$$

where the two zeros have a negative real part. Besides they are real if

$$r_c \leq 4\frac{C_{C1}C_{C2}}{g_{m3}\left(C_{C1}+C_{C2}\right)^2}. \tag{16}$$

Inequality (16) gives a higher limit for the current follower input resistance. If it is satisfied, the expressions of the two zeros become

$$\omega_{Z1} \approx \frac{1}{(C_{C1}+C_{C2})\,r_c} \tag{17a}$$

$$\omega_{Z2} \approx \frac{g_{m3}\left(C_{C1}+C_{C2}\right)}{C_{C1}C_{C2}}. \tag{17b}$$

Even choosing the highest value of r_c defined by equality in (16), it can be shown that ω_{Z2} is four times greater than ω_{Z1}. Moreover, we have that $\omega_{P2} \ll \omega_{P3}$ if $C_{C1}/C_{C2} \ll (g_m 2r_{o1})/4$, this condition is easily met in practice. Thus the second zero and the third pole in (17) are allocated well above the second pole, and do not appreciably modify the phase margin.

Finally, if $C_{C1} > C_{C2}$ we have that $\omega_{P2} < \omega_{Z1}$. This means that the first zero does not modify ω_{GBW}, and slightly improves the phase margin whose expression can be again approximated by (4b) that implicitly gives the value of C_{C2}.

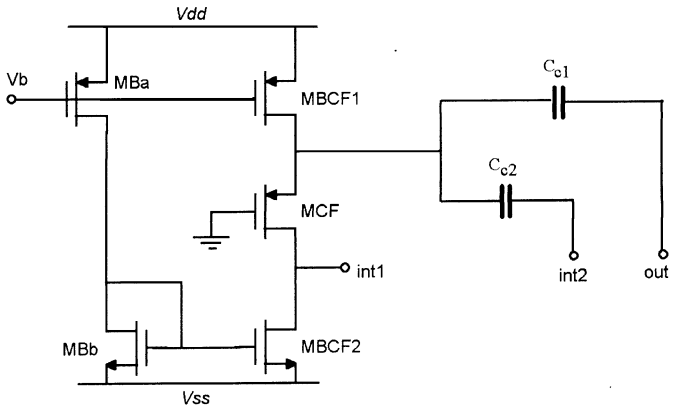

Fig. 9. Current-follower based compensation network.

VI. Simulations and Comparison

To confirm the proposed analysis and compensation techniques, post-layout Spectre simulations were carried out using the process parameters of a 0.35-μm triple-metal and double-poly CMOS process supplied by AMS. The simplified schematic of the three-stage amplifier used in the simulations is shown in Fig. 5. The input differential stage is made up of transistors M1–M4 and MB2. Transistors M6–M9 realize the output non inverting stage, while the intermediate inverting stage is a simple common source stage (M5 and MB3). It is worth noting that M9 is connected to the output of the differential stage thus implementing a push-pull output stage with improved slew-rate performance. Its contribution becomes relevant during positive transients where capacitor C_L has to be charged. Note that M9 bypasses the output stage (M6–M8) and could (advantageously) provide an increase in the phase margin through multipath feedforward compensation. To prevent this effect and to strictly evaluate only the effects of the proposed techniques, the transconductance of M9 is chosen sufficiently

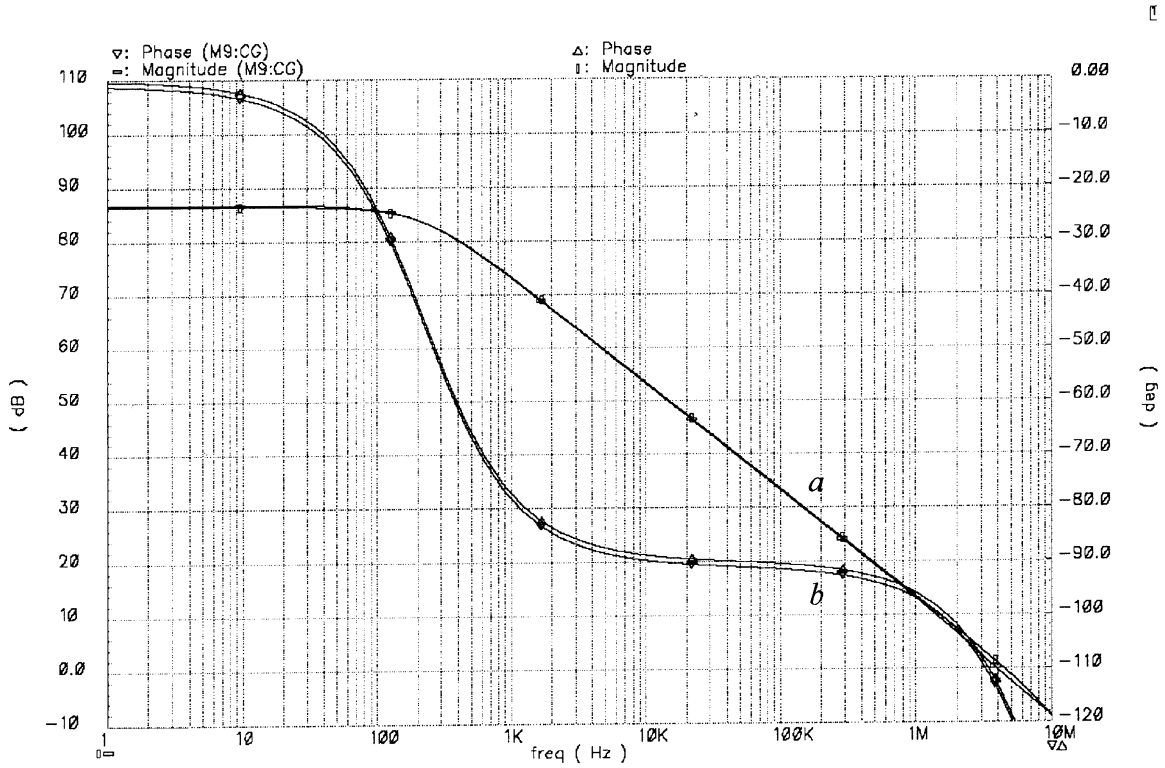

Fig. 10. Compensation using one current follower. Loop gain frequency response: magnitude (curves $\boldsymbol{a}$) and phase (curves $\boldsymbol{b}$).

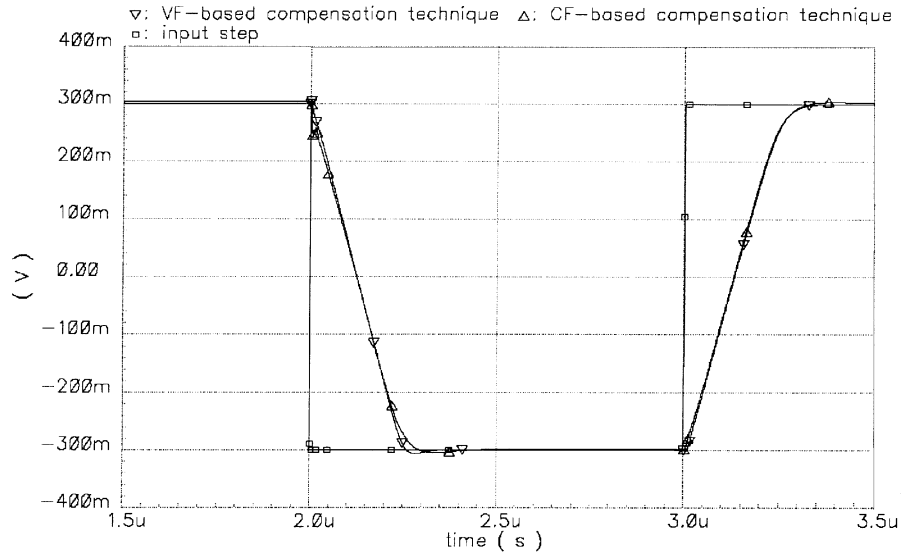

Fig. 11. Response to a 300-mV$_{pp}$ input step of the amplifier in unity gain.

low in order to avoid modifying the frequency response (both in magnitude and phase). To further analyze this issue, a second version of the circuit with the gate of M9 connected to a fixed voltage (i.e., with M9 acting as a bias current source) was considered. The circuits use a supply voltage of 1.5 V and a bias current (IB) of 10 μA giving an overall power dissipation of 82.5 μW. A capacitive load equal to 10 pF was also adopted. Table I summarizes the transistors aspect ratios. The layout of the main amplifier (as well as the compensation networks) is depicted in Fig. 6.

In the discussion to follow, the target gain-bandwidth product was chosen as equal to 5 MHz which requires $C_{C1} = 3.7$ pF. In addition, a phase margin of 60° was assumed.

First we considered the technique based on the voltage follower whose schematic is illustrated in Fig. 7, in which bias current generator MBVF is sized in order to supply a current of 25 μA ($W/L = 50/1$). The aspect ratio of transistor MVF is 450/0.35 in order to provide $r_v = 1/g_{m3} \approx 1.8$ kΩ [parameter γ was chosen equal to 1 in (10) for simplicity]. From (16) we obtain $C_{C2} = 2.2$ pF. Fig. 8 depicts the post-layout simulations of the amplifier loop gain, which is characterized by a dc-gain of 91 dB, a gain-bandwidth product of 4.5 MHz and a phase margin of 67°. The value of the phase margin is larger than that designed. This is due to the zero in (11c), neglected for simplicity and whose frequency is eight times the gain-bandwidth product. Superimposed in the same figure are the magnitude and

phase of the amplifier with M9 as a bias current generator (CG). It is apparent that the curves are almost undistinguishable.

To verify the latter compensation technique, a current follower was designed as shown in Fig. 9 using a bias current of 50 μA. The aspect ratio of the common gate transistor MCF was set 450/0.35 in order to give an input resistance of 600 Ω, as required by (16) which yields $r_c < 1.7$ K Ω. Using equation (4b), we get $C_{C2} = 2.8$ pF. The loop gain magnitude and phase of the amplifier are illustrated in Fig. 10. It shows a dc-gain of 86 dB (lower than the previous case, due to the effect of the current follower output resistance), a gain-bandwidth product of 4.4 MHz and a phase margin of 64°. The error in the phase margin is due to the zero in (17a) that we neglected. This zero is about ten times the gain-bandwidth product. Moreover, Fig. 10 shows no substantial modification in the frequency response by configuring M9 as a bias current generator (CG).

The step response of the amplifiers in unity gain was then evaluated. Fig. 11 shows the responses to a 600-mV_{pp} input step. The 1% settling time is 320 ns for the case with voltage follower, while it is about 470 ns for the other case.

The above data enable a comparison between the two proposed compensation techniques to be performed. Under the same gain-bandwidth product, the first approach requires a lower value of compensation capacitor C_{C2} and a lower transconductance (i.e., lower area and/or current dissipation) of the voltage follower, while providing a better phase margin. Area and current consumption can also further reduced by using a value of parameter γ higher than 1. In addition, the use of the current follower reduces the op-amp DC gain, and introduces a current unbalance into the input differential stage that causes offset and reduces the PSRR. To limit this drawback a careful matching of the two current generators (MBCF1 and MBCF2 in Fig. 9) biasing the follower must be ensured at the cost of additional circuit complexity. Finally, simulations varying the temperature from 0 ° to 80 °C show a substantial insensitivity of the solution exploiting the voltage follower. On the other hand, the amplifier using the current follower exhibits a phase margin variation of $\pm 10°$, while the gain-bandwidth product is almost constant.

VII. Conclusions

A three-stage amplifier with only the inner stage inverting can be compensated using the reversed nested Miller technique, which was first investigated by using a simple design-oriented approach. Then the need to eliminating the parasitic positive zero in the loop gain transfer function emerged. For this purpose, the nulling resistor technique was recognized as impractical and two methods were proposed employing one voltage or current follower. Both approaches allow the stage transconductances to be independently set and are amenable for low-voltage circuits as they do not reduce the output swing. However, it was shown that the approach employing the voltage follower is more attractive especially for its reduced power/area requirements.

The accuracy of the proposed techniques and related design equations were verified through post-layout simulations using a 0.35-μm CMOS process. All the simulation data were found to be in good agreement with expected results.

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