Design Techniques for Cascoded CMOS Op Amps with Improved PSRR and Common-Mode Input Range

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Abstract—**Internally compensated CMOS op amps have been widely used in sampled-analog signal processing applications over the past several years; however, the popular two-stage op amp suffers from poor ac power supply rejection to one of the power rails. This paper presents two circuits that overcome the PSRR problems of the earlier amplifier: one for virtual ground applications such as switched-capacitor integrators, and the other for buffer applications requiring wide common-mode input range. Small signal analysis is developed for the open loop and PSRR responses of the two amplifiers. In addition, design guidelines are suggested and test results are presented.**

I. INTRODUCTION

As the maturity of analog MOS amplifier technology progresses, the basic issues of designing workable amplifiers have been solved and many components employing first generation amplifiers have been marketed, principally in filter codecs and touch-tone decoders. After these initial successes, considerable effort is now underway in enhancing amplifier performance in terms of noise, power-supply rejection, gain–bandwidth product, and output drive. The popular two stage op amp shown in Fig. 1, for example, suffers from poor positive power supply rejection since the output drive transistor at moderate frequencies becomes "diode connected," with its drain ac shorted to its gate by the compensating capacitor, which couples the supply signal to the output.

This paper focuses on power supply rejection problems and examines a recently developed cascoding technique [1], [2], which greatly improves high-frequency rejection, as shown in Fig. 2. The addition of transistors M_3 and M_4 in the input stage permits the connection of the compensating capacitor to the source of a common-gate device (cascode transistor), which decouples the gate of the driver transistor from the compensation capacitor. This technique offers a much improved high-frequency power-supply rejection ratio (PSRR), but complicates the compensation of the amplifier. One disadvantage of this circuit, however, is a reduction in common-mode input range due to the voltage drop across the cascodes. This tends to restrict the use of such circuits to applications which use a virtual ground. Unity-gain buffers, however, require wide common-mode input range and therefore a folded cascode technique is presented in Fig. 3, which has wide common-mode range and retains the benefits of the compensation approach.

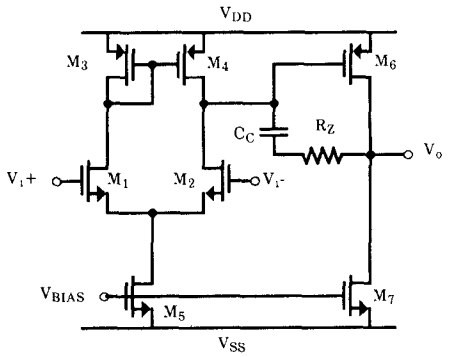

Fig. 1. A conventional internally compensated CMOS op amp.

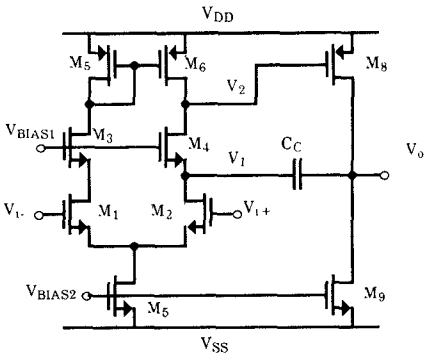

Fig. 2. An internally compensated cascoded CMOS op amp with high ac PSRR.

As a consequence of the inclusion of the cascode transistors, the design of an op amp becomes considerably more difficult; a second-order small-signal model is no longer sufficient to describe its performance. A detailed small-signal model for the cascoded op amp is presented in this paper which is equally applicable to either amplifier. Through the use of this model, design of these op amps is greatly simplified. In addition, a small-signal PSRR model is presented that demonstrates the improvement in PSRR of the new op amps over the earlier one in Fig. 1. A test

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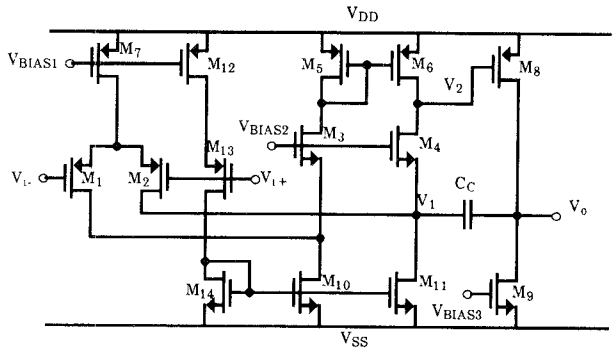

Fig. 3. An internally compensated folded cascode CMOS op amp with high ac PSRR and wide common-mode input range.

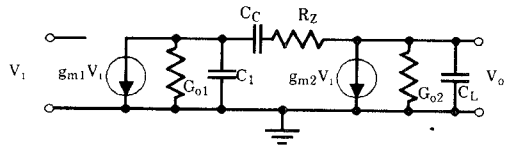

Fig. 4. An ac small-signal model for the op amp of Fig. 1.

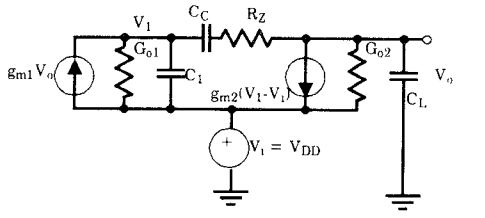

Fig. 5. An ac small-signal PSRR model for the op amp of Fig. 1.

circuit including these amplifiers has been fabricated, and experimental results are included which demonstrate their improved performance.

II. Internally Compensated Noncascoded Op Amps

The voice-band op amp of Fig. 1 has been widely used for several years but is primarily deficient in its ac PSRR to the positive rail. A version of this amplifier using p-channel input transistors would similarly suffer with respect to noise on its negative supply. In order to appreciate the benefits of the cascoded amplifier, a review of the performance of the conventional circuit is in order.

The ac small-signal equivalent circuit is shown in Fig. 4. This has been analyzed many times previously [3], [4], and is well characterized by a dominant pole $\omega_{pd} \approx G_{01}G_{02}/g_{m2}C_C$ due to the Miller effect acting on C_C, enhancing its loading of the first stage by a factor of one plus the gain of the second stage. Here, $G_{01} = g_{02} + g_{04}$ represents the conductances of the first stage, $G_{02} = g_{06} + g_{07}$ represents the conductances of the second stage, and g_{m2} is the transconductance of M_6. In addition, there is a high frequency parasitic pole at $\omega_{pH} \approx g_{m2}/C_L$ from the effect of the ac "diode-connected" output transistor M_6 driving the load capacitance; there is also a zero due to the feed-forward path through the compensation network at $\omega_z \approx (g_{m2} - 1/R_Z)/C_C$, which reduces phase margin. The nulling resistor R_Z is inserted to cancel the zero, and so is normally made approximately equal to $1/g_{m2}$.

A small-signal model suitable for analyzing the PSRR to the positive rail (in this case) appears in Fig. 5; a recent paper [5] presents a similar model. Conductance G_{01} just equals g_{04} here; g_{02} connects to the source of the input pair which is an open-circuit for common-mode signals such as power supply noise and must be excluded. The other conductance G_{02} models the resistive V_{DD} coupling occurring through the p-channel device M_6 and therefore equals only g_{06}. Analysis of the model reveals that the PSRR as a function of the Laplace frequency variable s is

$$\text{PSRR}(s) \approx \frac{(s + \omega_{pd})}{(s + \omega_T)}$$

where $\omega_T \approx g_{m1}/C_C$, the unity-gain bandwidth of the amplifier, and ω_{pd} is the dominant pole defined above.

Unfortunately, the zero at the low frequency of the dominant pole prematurely degrades the PSRR. The explanation is that as frequency rises, the impedance of the compensation capacitor C_C becomes low and the gate and drain of M_6 begin to track one another. The transistor is current-source biased by M_7 and must maintain a relatively constant gate-source drive consistent with the bias current. This requirement forces the gate of M_6 to track V_{DD} fluctuations which are in turn transmitted by C_C to the drain, which is the output of the amplifier.

After this examination of the conventional op amp, it becomes evident that one approach to enhance ac PSRR is to find a means to decouple the compensation capacitor from the gate of the output driver (M_6). The cascode op amp, presented next, permits this and results in an appreciable PSRR improvement.

III. Internally Compensated Cascoded Op Amps

The circuit schematics of the cascoded, internally compensated op amps for virtual ground operation and high common-mode input range operation are shown in Figs. 2 and 3, respectively. They have the same small-signal equivalent circuit, and both offer excellent high-frequency PSRR. The equivalence can be appreciated by recognizing the similarity in the circuits from their n-channel cascodes (M_3 and M_4) and the p-channel current mirrors (M_5 and M_6), through to their output stages and compensation capacitor hookups. The only difference is in the polarity of their input stages, and the manner in which they connect to the cascode transistors.

The first circuit uses the direct connection of an n-channel source-coupled pair to the source of the cascode transistors. The other circuit, with the wide common-mode range, uses a current folding circuit technique, similar to that used in a Berkeley transconductance amplifier [6], to permit the direct connection of the drains of a p-channel source-coupled pair to the sources of the cascode devices.

This requires two additional transistors (M_{10} and M_{11}), operating as current sources, to bias the first stage. The current-source biased p-channel input stage and the n-channel current-stage devices introduce the same small-signal current variations through to the cascodes and the current mirror as does the n-channel input pair of the first circuit. Both circuits will force a small-signal current equaling the product of the input transconductance and half the differential input signal. Recognizing the similarity allows the conclusion that the two circuits will perform comparably with regard to small-signal performance. The first circuit, however, will be restricted in common-mode input range in the positive direction to voltages that do not cause an input device to be forced out of saturation by the source of a cascode transistor. With the other circuit, the comparison must be made with respect to negative common-mode input range, owing to the opposite polarity of the input pair. The circuit avoids the problem through the current folding, and will have wide range if the source, and hence, the gate bias of the cascode devices are low. This is easily achieved since the gate voltage of M_3 and M_4 can be quite low, restricted only by the need to maintain the n-channel current sources M_{10} and M_{11} in saturation. This can be done by borrowing the high swing cascode biasing technique [6] originally employed in a high-frequency amplifier.

A recent paper [7] presented an n-channel input circuit similar to the circuit of Fig. 3, and emphasized its wide common-mode input range. That circuit, however, suffers from a peculiar adversity due to its biasing, which can be discussed in the context of the p-channel input circuit of the present paper. If the gates of transistors M_{10} and M_{11} are driven by a fixed voltage, as in [7], then for large positive common-mode inputs, as exists with a voltage follower for example, the output will abruptly spike up to the positive supply voltage. The sources of the input transistors reduce the drain-source voltage M_7, for large positive common-mode inputs, and the bias current is reduced substantially. For large positive common-mode inputs, the input pair current is thus too small to be significant with respect to the fixed bias current of M_{10} and M_{11}, and the gate voltage of the output driver M_8 is therefore abruptly pulled down, causing the output to pull high.

Normally, when a common-mode input limit is exceeded, in a buffer for example, soft clipping of the output is the result. In the present case, however, rather than clipping, the output spikes to the positive rail when trying to follow a signal that exceeds its positive common-mode input range. This problem can easily be avoided by using the novel biasing technique for the n-channel current sources ($M_{12}-M_{13}$) shown in Fig. 3. A current mirroring approach is used here whereby the bias current through M_{10} and M_{11} tracks the current through the input source-coupled pair. For excessive positive common-mode inputs, the use of M_{13} with its gate driven by the plus input, will force the current of M_{12} to follow that of M_7. This imposes the same reduced drain-source voltage on M_{12} as is on M_7, and this current is mirrored to the n-channel transistors.

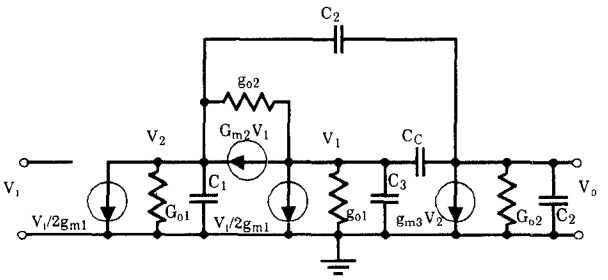

Fig. 6. An ac small-signal model for the cascode op amps of Figs. 2 and 3.

Difference-mode input components are normally held very small by feedback, and thus do not modify this behavior significantly. Through the use of this method there is no penalty when the common-mode input limit is exceeded other than soft clipping.

AC Small-Signal Model

In order to design these op amps it is very useful to work with an appropriate small-signal model that can be used to determine the open-loop frequency response. A model developed for this purpose which shows close agreement with both device level circuit simulations and actual measurements of a test circuit is shown in Fig. 6. The model is considerably more complicated than the one of Fig. 4; however, it has proved to be the simplest model, which adequately explains the operation of the circuit.

In this section, a brief explanation for the model is presented and can be followed in the context of either Fig. 2 or 3. The two current sources of value $V_i g_{m1}/2$ result from the action of the input source-coupled pair; the right-hand one corresponds to M_2 and connects to the compensation capacitor C_C and the source of the cascode transistor M_4; the left-hand device represents the effect of the small-signal current developed by M_1 after being reflected by the current mirror formed by M_5 and M_6. The voltages V_1 and V_2 in the model are the voltages on the two sides of the cascode transistor M_4, shown in Fig. 2 or Fig. 3. The conductance G_{01} is the small-signal conductance of M_6, whereas g_{01} is the small-signal conductance of M_2 for Fig. 2; g_{01} must also include the conductance of M_{10} for Fig. 3. The dependent current source $V_1 G_{m2}$ represents the transconductance of cascode device M_4, and g_{02} represents its associated small-signal conductance; its current is controlled by its source voltage V_1, according to the effective transconductance. Note that for a cascode device with a fixed gate bias, the effective transconductance G_m is the sum of the gate-source transconductance g_m and the substrate transconductance g_{mb}.

The driver of the second stage of the amplifier M_8 is represented by the current source of value $V_2 g_{m3}$ in shunt with a conductance G_{02} equaling the sum of the small-signal conductances of transistors M_8 and M_9. The voltage V_2 at the junction of the drains of M_6 and M_4 drives the gate of M_8 thereby controlling the output current source. The small-signal capacitances are included to effectively model the frequency response. The load capacitor C_L is connected

directly to the output, and the compensation capacitor C_C is connected from the output to the source of M_4. The three remaining capacitors represent parasitics: C_1 includes the gate-source capacitance of M_8 and junction capacitance; C_2 is the gate to drain capacitance of M_8, and is mainly the overlap capacitance since M_8 is normally saturated; and C_3 represents the source–gate capacitance of M_4 and its junction capacitance.

Having formed the model, a few comments and simplifications are in order. First, out of the input stage, only the action of transistors M_2, M_4, and M_6 is incorporated directly. These are the most important devices since they drive both the compensation capacitor and the gate of the second stage. The effect of the other side of the input stage is modeled by the left-most dependent current source. This implies that the current developed by transistor M_1 is mirrored with no bandwidth reduction by M_6; the current, however, will experience a frequency dependence due to the pole associated with the M_5/M_6 current mirror. For a voice-band amplifier if this pole is sufficiently fast, it can be neglected; if this is not the case, its effect can be incorporated in capacitor C_1. A simplification of the model is possible by the omission of conductances g_{01} and g_{02}; this reduces the complexity of the model to third order. Due to the cascoding of the input pair, the conductance seen looking into the V_2 node of the figures is the sum of G_{01} and the conductance looking into the drain of the cascode device; however, the latter is negligible due the impedance multiplication properties of a cascode circuit; the impedance is that of the lower device multiplied by the gain of the cascode transistor. Based on this, the dc gain of the circuit will be approximated, with very small error, by dropping the two conductances. The only other concern is the effect the conductances have on the output impedance at the V_1 node. Fortunately, the impedance is determined primarily by the effective G_m of the cascode device, i.e., $Z_{01} \approx 1/G_{m2}(1+g_{02}/G_{01})$, and so the conductances can be dropped with no appreciable error. Finally, C_3 may be neglected, since it is very small with respect to the Miller multiplied compensation capacitor.

The dominant pole of the amplifier is formed by the loading of C_C, increased by Miller effect, on the source of transistor M_4. The compensation capacitor C_C is multiplied by a factor of $1+V_0/V_1$, where $V_0/V_1 = G_{m2}g_{m3}/[(G_{01}+g_{02})G_{02}]$, the gain from the source of M_4 to the output. The time constant of the dominant pole is therefore

$$\tau_{pd} = Z_{01}\left[1+\frac{V_0}{V_1}\right]C_C = \frac{1}{G_{m2}}\left[1+\frac{g_{02}}{G_{01}}\right]\frac{G_{m2}g_{m3}}{(G_{01}+g_{02})G_{02}}C_C = \frac{g_{m3}C_C}{(G_{01}G_{02})}$$

and the frequency of the pole is $\omega_{pd} \approx G_{01}G_{02}/(g_{m3}C_C)$. This result shows that the dominant pole of the cascode op amp is located at the same frequency as a comparable noncascoded op amp; the reduced voltage swing at the left-hand side of C_C at the source of M_4 is exactly balanced by an increase in the Miller effect gain acting on C_C from that same node to the output. Omission of the conductances g_{01} and g_{02} does not change this fundamental conclusion. The dc gain of the amplifier can be shown to be

$$\left.\frac{V_0}{V_i}\right|_{DC} = \frac{g_{m1}g_{m3}}{\left[G_{01}+\dfrac{g_{01}(g_{02}+G_{01}/2)}{G_{m2}}\right]G_{02}} \approx \frac{g_{m1}g_{m3}}{G_{01}G_{02}}.$$

The cascoding of the input stage makes the effect of g_{01} and g_{02} negligible, and as a result, the gain of the first stage is larger than that of a noncascoded circuit.

Analysis of the ac small-signal model, after considerable algebra and the discarding of minor terms, results in the following polynomial transfer function:

$$\frac{V_0}{V_i} = \frac{-s^2\dfrac{g_{m1}}{2}C_C(C_1+2C_2)+s\dfrac{g_{m1}g_{m3}}{2}C_C+g_{m1}G_{m2}g_{m3}}{s^3C_LC_C(C_1+C_2)+s^2\{G_{m2}[C_L(C_1+C_2)+C_CC_1]+g_{m3}C_LC_2\}+sG_{m2}g_{m3}C_C+G_{m2}G_{01}G_{02}}.$$

The sign sequence of the numerator terms can only result from the product of two real zeros, one in the right half-plane and one in the left-half plane. A simplification of the equation can therefore be obtained, by factoring the numerator, and additionally, factoring out the dominant pole from the denominator. The result of this is

$$\frac{V_0}{V_i}(s) = \frac{-\dfrac{g_{m1}(C_1+2C_2)}{2C_L(C_1+C_2)}\left[s-\dfrac{g_{m3}}{(C_1+2C_2)}(1+\delta_2)\right]\left[s+2\dfrac{G_{m2}}{C_C}\dfrac{1}{(1+\delta_2)}\right]}{\left[s+\dfrac{G_{01}G_{02}}{g_{m3}C_C}\right]\left\{s^2+s\left[\dfrac{G_{m2}[C_L(C_1+C_2)+C_CC_1]+g_{m3}C_LC_2}{C_LC_C(C_1+C_2)}\right]+\dfrac{G_{m2}g_{m3}}{C_L(C_1+C_2)}\right\}}$$

where

$$\delta_2 = \frac{(1+\delta_1)^{1/2}-1}{2} \text{ and } \delta_1 = 8\frac{G_{m2}}{g_{m3}}\left(\frac{C_1}{C_C}+2C_2\right).$$

Design Techniques for Frequency Compensation

Despite the complexity of this expression, several useful design principles can now be extracted. The presence of the right-half plane zero $\omega_{zr} = [g_{m3}/(C_1+2C_2)](1+\delta_2)$ differs

from an equivalent left-half plane zero with respect to phase shift, and degrades phase margin by 90 degrees rather than increasing it. Fortunately, the frequency of this zero is substantially higher than the zero of a noncascoded op amp, and sufficient loop ability can be obtained despite its presence. The quadratic polynomial in the denominator $D_p(s)$ contributes a pair of high-frequency poles, which are best characterized by their natural frequency ω_{op} and quality factory Q_p. The equation for the pair of parasitic poles is

$$D_p(s) = s^2 + s\left[\frac{G_{m2}[C_L(C_1+C_2)+C_CC_1]+g_{m3}C_LC_2}{C_LC_C(C_1+C_2)}\right] + \frac{G_{m2}g_{m3}}{C_L(C_1+C_2)}.$$

The corresponding natural frequency and quality factor are

$$\omega_{op} = \left[\frac{G_{m2}g_{m3}}{C_L(C_1+C_2)}\right]^{1/2}$$

$$Q_p = \frac{[G_{m2}g_{m3}C_L(C_1+C_2)]^{1/2}C_C}{G_{m2}[C_L(C_1+C_2)+C_CC_1]+g_{m3}C_LC_2}.$$

In normal operation, output driver M_8 is saturated and the drain to gate capacitance C_2 is mainly overlap capacitance, in which case $C_2 \ll C_1$. With this assumption, the expressions for ω_{op} and Q_p can be simplified:

$$\omega_{op} \approx \left[\frac{G_{m2}g_{m3}}{C_LC_1}\right]^{1/2}$$

$$Q_p \approx \left[\frac{g_{m3}C_L}{G_{m2}C_1}\right]^{1/2}\frac{C_C}{C_L+C_C}; \qquad \text{for } C_2 \ll C_1.$$

In order to obtain a satisfactory degree of stability, peaking in the frequency response must be avoided. It is quite possible to obtain a design with seemingly adequate phase margin, which suffers from insufficient gain margin due to a peaking of the magnitude response beyond the unity-gain bandwidth, caused by a high Q in the poles of $D_p(s)$, as illustrated in Fig. 7. This can be avoided by keeping the parasitic pole Q low by making the transconductance of cascode transistors M_3 and M_4 large with respect to that of output driver M_8. In addition, a moderate value of C_C is required since, depending on the value of C_L, the sensitivity of Q_p to C_C

$$S_{C_C}^{Q_p} = \frac{G_{m2}C_L(C_1+C_2)+g_{m3}C_LC_2}{G_{m2}[C_L(C_1+C_2)+C_CC_1]+g_{m3}C_LC_2} \approx \frac{C_L}{C_L+C_C}; \qquad \text{for } C_2 \ll C_1$$

can approach unity, and gain peaking can occur. In such cases, with the value of the compensation capacitor reduced to avoid the peaking, the transconductance of the input transistors must correspondingly be increased to maintain the same unity-gain bandwidth. One other method

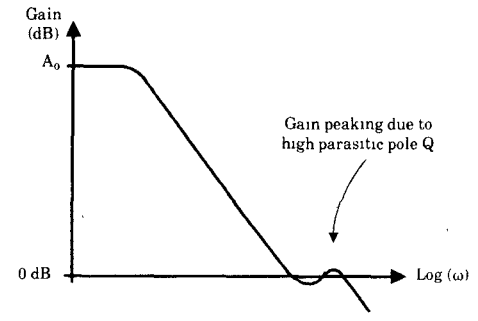

Fig. 7. Gain peaking of frequency response if Q of parasitic pole pair is too high.

remains for controlling the parasitic pole Q. This consists of using a relatively large value for C_1, which is principally the gate capacitance of the output driver. In practice, this can be achieved using a large area for the device, by giving it a relatively long length. The corresponding transconductance g_{m3} will be smaller than normal, but this moderates the Q as well and the net effect is therefore considerable.

Up to now, only methods of reducing the Q of the high-frequency parasitic pole pair have been considered. These methods will, of course, also adversely affect the parasitic zero locations. The overall transfer function, however, displays a greater sensitivity to the parasitic pole pair than it does to the real zeros, providing Q_p is high [8] and the design of cascoded op amps must therefore involve due consideration of pole Q factor. A workable design can be obtained if a cancellation of sorts can be achieved. If the parasitic pole pair has a Q close to one half, then there will actually be a double real pole at a frequency of ω_{op}. In this case, one of the poles will be close enough to approximately cancel the left-half plane zero located at $\omega_{z1} = 2(G_{m2}/C_C)(1+\delta_2)$. With this type of pole/zero cancellation, the op amp transfer function is approximately second order, consisting of a low-frequency dominant pole, a high-frequency parasitic pole and a right-half plane high frequency zero. The approximate transfer function assuming this type of cancellation is

$$\frac{V_o}{V_i}(s) \propto \frac{(s-\omega_{zl})}{(s+\omega_{pd})(s+\omega_{op})}.$$

A similar transfer function occurs in a noncascoded op amp; however, the right-half plane zero is at a low frequency, and must be cancelled through the use of a resistance in series with the compensation capacitor. In the present case, however, the zero is at high frequency and such measures are unnecessary.

AC Small-Signal Model for PSRR

The PSRR small-signal model derivation closely follows the model just discussed, and hence it is not neccessary to go into as much detail. The model appears in Fig. 8, and is similar to the model for the noncascoded op amp shown in Fig. 5, except it is in the context of the cascode model of Fig. 6. The conductance g_{01} is omitted here, since it connects to the source of the input pair, which is open

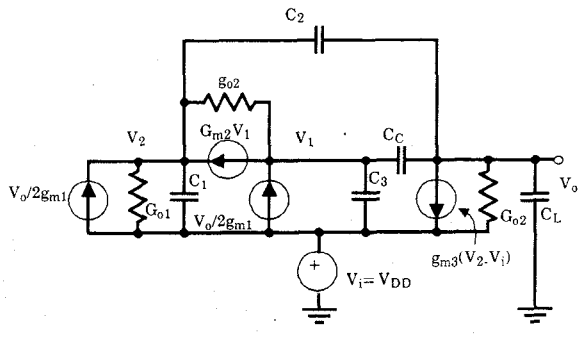

Fig. 8. A small-signal PSRR model for the cascode op amps of Figs. 2 and 3.

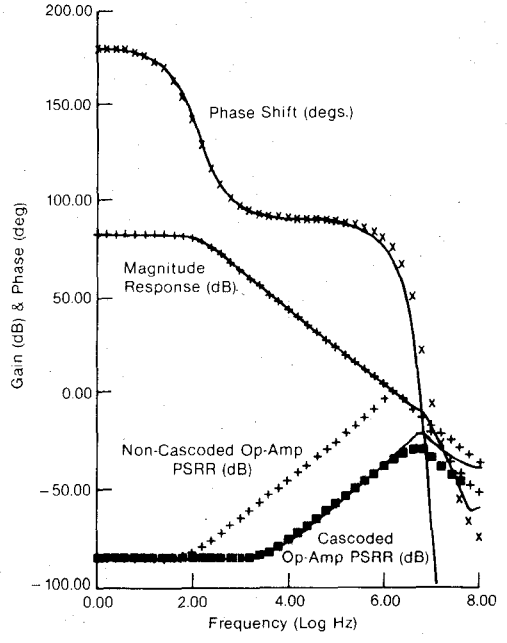

Fig. 9. Frequency response of the op amp model (points), and a complete SPICE circuit simulation (solid lines) of the cascode op amp of Fig. 2.

circuit for common-mode signals such as power supply noise. Conductance G_{02} now equals g_{08} since the resistive coupling at the output stage is only through M_8. As with the earlier PSRR model, the input signal V_i represents noise on the V_{DD} rail, and is therefore not an ac ground.

Analysis of this model reveals a significant increase in the frequency of the zero in the transfer function of the V_{DD} noise to the output. The transfer function can be reasonably approximated by

$$\mathrm{PSRR}(s) \approx \frac{C_2}{C_C(1+\delta_3)} \frac{\left[s + \dfrac{G_{01}G_{02}}{g_{m3}C_2}\right]}{\left[s + \omega_T \dfrac{1}{(1+\delta_3)}\right]}$$

where

$$\delta_3 = \frac{1}{2}\frac{g_{m1}}{G_{m2}} \text{ and } \omega_T = \frac{g_{m1}}{C_C} \text{ the unity-gain bandwidth.}$$

The expression for the zero is very similar to that for the noncascoded op amp. They differ only in the value of the

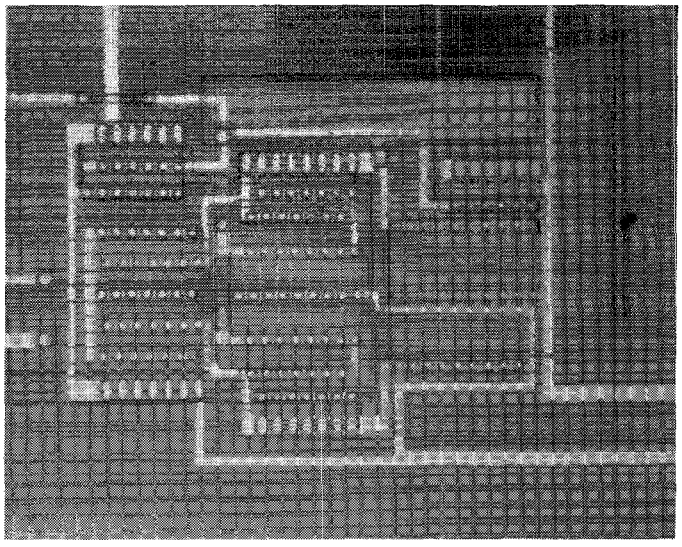

Fig. 10. A photomicrograph of the cascode op amp of Fig. 3.

capacitance: C_C for the previous op amp, and C_2 for the cascode op amp. From this analysis it is evident that the mechanism causing a zero is the same for either circuit, namely the amount of capacitance coupling the gate of M_8 to the output. The improvement in the zero frequency for the cascoded op amps is therefore the ratio of C_C to C_2, which is very high since C_C is the compensation capacitor whereas C_2 is only the drain to gate capacitance of a saturated transistor (M_8). The pole frequency is on the order of the unity gain bandwidth, $\omega_T = g_{m1}/C_C$, as in the previous case.

IV. Results

Comparison of Models with Full Circuit Simulation

In order to demonstrate the validity of the modeling and analysis of the cascode op amps, and the improved ac PSRR, a plot of frequency response is presented in Fig. 9. Here, a complete SPICE circuit simulation of the cascode circuit of Fig. 2 (solid lines) is compared with the ac small-signal models (points) for the open-loop frequency response and PSRR frequency response. The accuracy of the small-signal models are quite good and break down only at frequencies beyond the gain-bandwidth product of the amplifier. Also included in the figure is a PSRR frequency response curve for a noncascoded version of the same op amp. A major improvement in high frequency PSRR (> 30 dB) is evident for the cascoded op amps.

Test Results

Circuits for the cascoded op amps of Figs. 2 and 3 have been fabricated and tested. A photomicrograph of the wide common-mode input range op amp of Fig. 3 is shown in Fig. 10, for example. Its biasing network, consisting of transistors $M_{12}-M_{14}$, was not fabricated and so test results regarding its input common range are unavailable; however, simulations have validated its effectiveness in over-

TABLE I
TEST RESULTS FOR CASCODE OP AMP OF FIG. 2

V_{DD}=2.5 v. V_{SS}=-2.5 v.

Parameter	Conditions	Measured Values	Units
Input offset voltage		7.3	mV.
DC open loop gain		83.3	dB.
CMRR	@100 KHz.	44	dB.
PSRR (V_{DD})	@100 KHz.	55	dB.
PSRR (VSS)	@100 KHz.	67	dB.
Slew rate rising	C_L = 10 pF.	10	V/us.
Slew rate-falling	C_L = 10 pF.	3.3	V/us.
Input referred noise	@1 KHz.	95	nV./√Hz.
I_{DD}		124	uA.

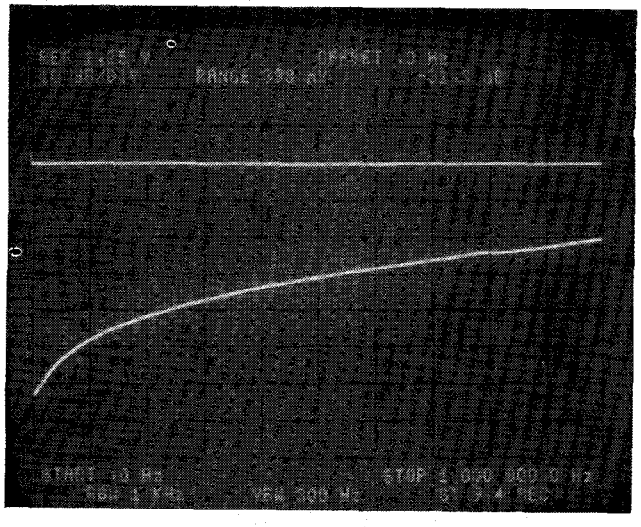

Fig. 11. V_{DD} PSRR for the cascode op amp of Fig. 3.

coming the output glitching problem. In all other respects similar test results were obtained for both amplifiers as expected and are outlined for the circuit of Fig. 2, in Table I. A photograph of the experimental V_{DD} PSRR for the circuit of Fig. 3 showing the excellent high-frequency rejection (> 49 dB at 100 kHz) appears in Fig. 11.

V. CONCLUSIONS

Two CMOS op amps with improved high-frequency PSRR have been reported; the first is for use in circuits with virtual ground operation such as switched-capacitor integrators. The second is a new circuit with wide common-mode input range and is therefore useful in buffer applications. The circuit solves an output spike phenomena which arose in a previously reported op amp. It is shown that both circuits are equally well described by the same small-signal model which is derived herein. Based on resulting considerations, design techniques for frequency compensation are presented. Test circuits for both op amps have been fabricated and corroborate the results of the small-signal model.

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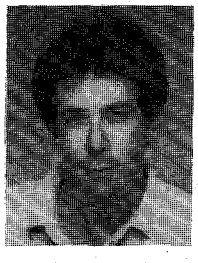

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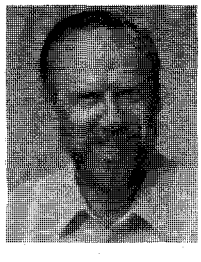

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