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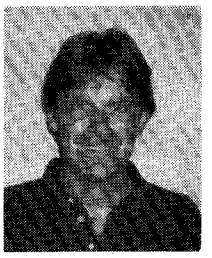
REFERENCES

[1] W. C. Black, Jr., D. J. Allstot, and R. A. Reed, "A high performance low power CMOS channel filter," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 921–929, Dec. 1980.
[2] D. Senderowicz, D. Hodges, and P. Gray, "High-performance NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 760–766, Dec. 1978.



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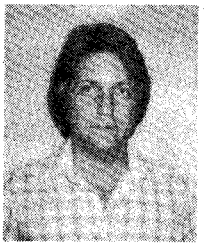

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An Improved Frequency Compensation Technique for CMOS Operational Amplifiers

BHUPENDRA K. AHUJA

Abstract—**The commonly used two-stage CMOS operational amplifier suffers from two basic performance limitations due to the *RC* compensation network around the second gain stage. First, this frequency compensation technique provides stable operation for limited range of capacitive loads, and second, the power supply rejection shows severe degradation above the open-loop pole frequency. The technique described here provides stable operation for a much larger range of capacitive loads, as well as much improved V_{BB} power supply rejection over very wide bandwidths for the same basic op amp circuit. This paper presents mathematical analysis of this new technique in terms of its frequency and noise characteristics followed by its implementation in all n-well CMOS process. Experimental results show 70 dB negative power supply rejection at 100 kHz and an input noise density of 58 nV/$\sqrt{\text{Hz}}$ at 1 kHz.**

I. INTRODUCTION

LINEAR CMOS techniques have achieved significant progress over the last five years to provide high-performance low-power analog building blocks like operational amplifiers (op amp), comparators, buffers, etc. These circuits have demonstrated comparable performance to their bipolar counterparts at much less silicon area and power dissipation, thus enabling single chip implementations of complex filtering functions, A/D and D/A conversions with quite stringent specification. Due to relatively simple circuit configurations and flexibility of design, CMOS technology has an edge over NMOS technology and is gaining rapid acceptance as the future technology for linear analog integrated circuits, especially in the telecommunication field [1], [2]. The most important building block in any analog IC is the op amp of which numerous implementations have been reported in both the technologies [3], [6].

The most commonly used op amp configuration in CMOS has two gain stages, the first one being the differential input stage with single-ended output, and the second one being either class *A* or class *AB* inverting output stage. Each stage typically is designed to have gain in the range of 40 to 100. Fig. 1(a) shows the circuit configuration while

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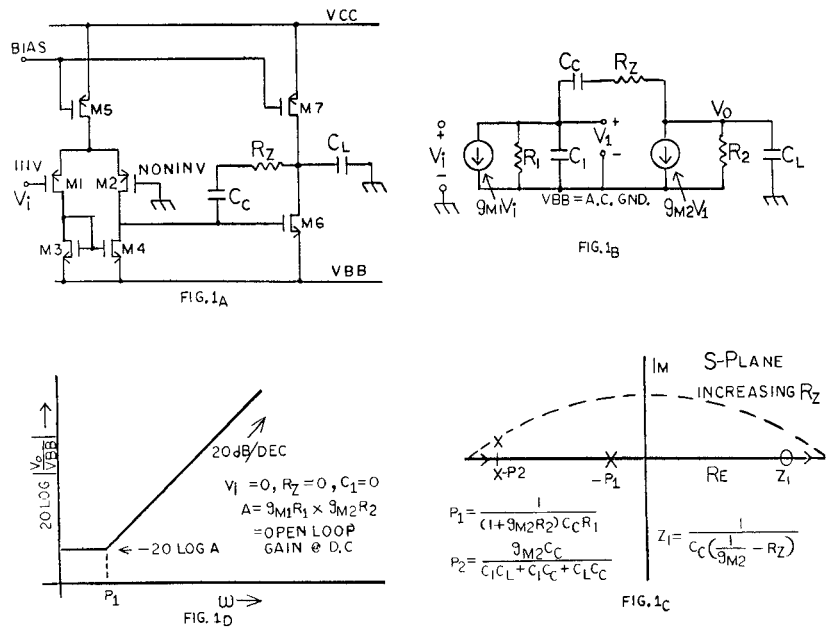

Fig. 1. (a) Commonly used two-stage operational amplifier. (b) Small signal equivalent model for the two-stage amplifier. (c) Pole-zero diagram of Fig. 1(b). (d) V_{BB} PSRR in unity gain configuration.

its first-order ac equivalent model is shown in Fig. 1(b). This configuration is most suitable for internal usage in the IC for driving capacitive loads only. Briefly, transistors $M1$ to $M5$ form the input differential stage and $M6$ and $M7$ form the output inverting gain stage. The series RC network across the second gain stage provides the frequency compensation for the op amp. This circuit, previously analyzed by many authors [5], [7], displays a dominant pole, two complex high frequency poles, and a zero which can be moved from the right half plane to the left half plane by increasing the compensating resistor value R_Z. This is pictorially shown in Fig. 1(c). Due to feedforward path with no inversion from the first stage output to the op amp output provided by the compensation capacitor at high frequencies, the op amp performance shows the following degradations:

1) The op amp stability is severely degraded for capacitive loads of the same order as compensation capacitor (C_L must be less than $g_{m2}C_c/g_{m1}$ to avoid second pole crossover of the unity gain frequency).

2) In case of p-channel MOS transistors for the input differential stage, the negative power supply displays a zero at the dominant pole frequency of the op amp in unity gain configuration. This results in serious performance degradation for sampled data systems which use high-frequency switching regulators to generate their power supplies. (In the case of n-channel MOS transistors for the input differential pair, it is the positive supply which shows similar degradation.) This is illustrated in Fig. 1(d).

The circuit technique described in this paper overcomes both of these limitations. This technique has been referenced earlier [7] as a private communication by Read and Weiser [8]. This paper provides analysis, implementation, and experimental results on the realization in an n-well CMOS process.

II. Improved Frequency Compensation Technique

The technique is based on removing the feed forward-path from the first stage output to the op amp output. The circuit shown in Fig. 1 has a current $C_c d(V_0 - V_1)/dt$ flowing into the first-stage output. If one can devise a circuit where only $C_c dV_0/dt$ current flows into the first-stage output, one would have eliminated the feedforward path while still producing a dominant pole due to the Miller effect. The only difference is that Miller capacitance is now A_2C_c rather than $(1 + A_2)C_c$ where A_2 is the second-stage voltage gain. Thus, the conceptual ac equivalent of such a circuit is shown in Fig. 2(a). Here the compensation capacitor is shown to be connected between the output node and a virtual ground (or ac ground), while the controlled current source having the same value as $C_c dV_0/dt$ charges the first-stage output. It can be shown that for such an arrangement, the open-loop gain of the op amp is given by

$$A = \frac{-A_1A_2}{1 + s(R_1C_1 + R_2C_L + R_2C_c + A_2R_1C_c) + s^2R_1R_2C_1(C_c + C_L)}$$

where $A_1 = g_{m1}R_1$ = dc gain of the first stage and

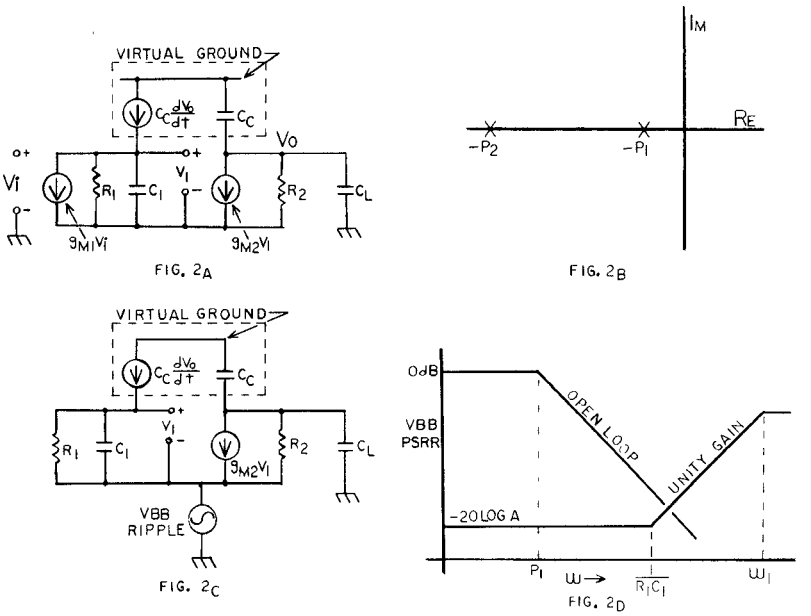

Fig. 2. (a) The new frequency compensation concept. (b) Resultant pole locations in s-plane. (c) Small signal model for V_{BB} PSRR analysis. (d) Expected V_{BB} PSRR frequency response of Fig. 1(a).

$$A_2 = g_{m2}R_2 = \text{dc gain of the second stage.} \tag{1}$$

Fig. 2(b) shows its pole-zero location. Notice that there is no finite zero in this circuit and that both the poles are real and are widely spaced.

$$P_1 \cong \frac{1}{(g_{m2}R_2)C_cR_1} \tag{2}$$

$$P_2 \cong \frac{g_{m2}C_c}{C_1(C_c+C_L)}. \tag{3}$$

Assuming the internal node capacitance C_1 being much smaller than the compensation capacitor C_c or the load capacitance C_L, the unity gain frequency W_1 is still given by g_{m1}/C_c. This results in

$$\frac{P_2}{W_1} = \frac{g_{m2}}{g_{m1}} \cdot \frac{C_c}{C_1} \cdot \frac{C_c}{(C_c+C_L)}. \tag{4}$$

Taking some typical design values of a two-stage amplifier as given by

$$g_{m2}/g_{m1} = 10,\ C_c = 5 \text{ pF},\ C_1 = 0.5 \text{ pF, and } P2/W_1 \geqslant 5,$$

the new compensation technique can drive up to 100 pF capacitive load as compared to 10 pF capability of the commonly used RC technique as shown in Fig. 1. Thus, the new technique offers an order of magnitude improvement in capacitive load capability for the same performance. The improvement factor is given by C_c/C_1, where C_1 can be reduced by careful layout and design of the first stage.

Another major performance improvement is found in the negative power supply rejection characteristics. Fig. 2(c) shows the model for computing the open-loop negative power supply rejection with grounded inputs. It can be shown that open-loop V_{BB} PSRR is given by

$$\frac{V_0}{V_{BB}} = \frac{1+sC_1R_1}{1+s\left[R_1C_1 + R_2(C_c+C_L) + A_2R_1C_c\right] + s^2R_1R_2C_1(C_c+C_L)}$$

$$\cong \frac{1+sC_1R_1}{(1+s/P_1)(1+s/P_2)} \tag{5}$$

which indicates that is has the same poles as the open-loop gain and a zero which is created by the parasitic capacitance at the first-stage output. Thus, in a unity gain configuration, the V_{BB} PSRR is given by

$$\frac{V_0}{V_{BB}} = \frac{1+sC_1R_1}{(1+s/P_1)(1+s/P_2)} \cdot \frac{1}{1+A_1A_2/(1+s/P_1)(1+s/P_2)}$$

$$\cong \frac{(1+sC_1R_1)}{A_1A_2(1+s/W_1)}. \tag{6}$$

This implies a flat response at $-20\log A_1A_2$, until the parasitic zero frequency of the first stage where it starts to degrade at 6 dB/octave rate and becomes flat again at unity gain frequency W_1. This is illustrated in Fig. 2(d).

III. A Circuit Implementation and Experimental Results

Although the above described scheme can be applied to any MOS amplifier design, it lends a relatively simple

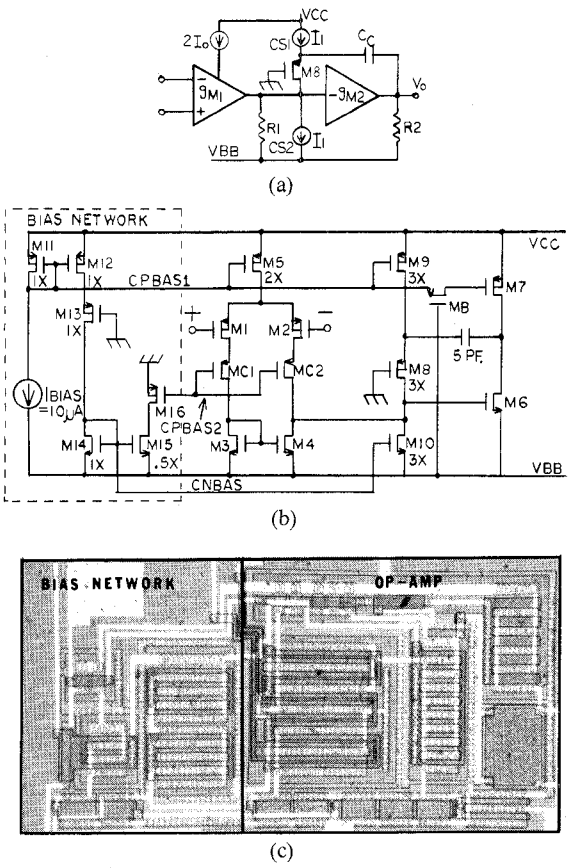

Fig. 3. (a) Implementation of the current transformer providing virtual ground. (b) Circuit schematic of the implemented amplifier. (c) Photomicrograph of the amplifier.

implementation in CMOS technology. Fig. 3(a) shows an implementation of the current transformer providing a virtual or ac ground to the compensation capacitor, while still able to dump $C_c dV_0/dt$ current into the second-stage input. The current source $CS1$ biases the source of $M8$ at a fixed dc potential above ground, thus providing the ac ground for the compensation capacitor. By matching the $CS2$ value to $CS1$, all displacement current $C_c dV_0/dt$ flows into or out of the first stage output.

Under large differential input conditions, the output can slew at a rate determined by the total input differential bias current $2I_0$, i.e.,

$$C_c \cdot \frac{dV_0}{dt} = \pm 2I_0. \tag{7}$$

In order to keep the current transformer biased during the slewing intervals, one must make I_1 greater than $2I_0$. Also, the size of M_8 and the value of I_1 should be large enough to keep V_{GS} of M_8 relatively constant under worst-case slewing conditions.

Fig. 3(b) shows a circuit schematic of the implemented amplifier. The input differential stage, formed by $M1$ to $M5$ transistors, uses cascode devices $MC1$ and $MC2$ to reduce supply capacitance from the negative power supply for switched-capacitor applications [5]. The current transformer is being realized by $M8$, $M9$, and $M10$. Due to its cascode configuration, this technique has been referred to as the "grounded gate cascode compensation" in [7]. The output stage is formed by $M6$ and $M7$. The transistor MB and the gate capacitance of the $M7$ transistor provide RC low-pass filtering of the high-frequency noise on the bias line $CPBAS1$. The associated bias circuit shown in the dotted box is shared among several such amplifiers, thus reducing power and area overhead cost due to this compensation technique. Fig. 3(c) shows the die photo of the amplifier. The amplifier has been designed in a 4 μm n-well CMOS process and occupies about a 165 mil^2 die area.

TABLE I
$V_{CC} = +5$ V, $V_{BB} = -5$ V, AND $T = 27°$C

Parameter	Measured Value
Open-Loop Gain	80 dB
Unity Gain Frequency	3.8 MHz
Phase Margin with $C_L = 15$ pF	70°
Input Common Mode Range	+4 to −2.5 V
CMRR at 1 kHz	−74 dB
Input noise density at	
1 kHz	58 nV/$\sqrt{\text{Hz}}$
100 kHz	8 nV/$\sqrt{\text{Hz}}$
C-msg Input Noise	−21 dBrnc
V_{CC} PSRR at	
1 kHz	−84.5 dB
10 kHZ	−84.5 dB
100 kHz	−73 dB
V_{BB} PSRR at	
1 kHz	−84 dB
10 kHz	−84 dB
100 kHz	−70 dB

The input referred noise of this amplifier is slightly worse than the one shown in Fig. 1(a) due to the noise contributions from transistors $M9$, $M10$, $M12$, and $M14$. However, these contributions can be reduced significantly by choosing large values of channel lengths of these devices with respect to the channel lengths of input transistors $M1$ and $M2$ [3], [7].

Some of the measured performance parameters are listed in Table I. The op amp exhibits open-loop gain of 80 dB, unity gain frequency of 3.8 MHz, and a phase margin of 70° with 15 pF load capacitance. The V_{CC} and V_{BB} PSRR at low frequencies are better than −80 dB due to the bias circuit design and the cascode transistors $MC1$ and $MC2$, respectively. The V_{BB} PSRR shows zero at about 60 kHz, which closely matches the simulated value of the parasitic zero frequency. The op amp displays an input referred noise density of 58 and 8 nV/$\sqrt{\text{Hz}}$ at 1 and 100 kHz frequencies, respectively.

Conclusions

An improved frequency compensation technique has been described with a brief review of the existing techniques. A CMOS implementation of the technique has also been presented with experimental results which show considerable high-frequency power supply rejection improvement over the existing techniques which would result in approximately −30 to −35 dB V_{BB} PSRR at 100 kHz.

Furthermore, the technique provides extended capacitive drive capability for the same size of the compensation capacitor.

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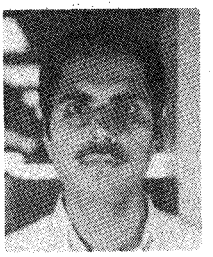
REFERENCES

[1] R. Gregorian and G. Amir, "A single chip speech synthesizer using a switched-capacitor multiplier," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 65–75, Feb. 1983.
[2] B. K. Ahuja *et al.*, "A single chip CMOS PCM codec with filters," in *ISSCC Dig. Tech. Papers*, pp. 242–243, Feb. 1981.
[3] P. R. Gray, "Basic MOS operational amplifier design—An overview," in *Analog MOS Integrated Circuits*. New York: IEEE Press, 1980, pp. 28–49.
[4] D. Senderowicz, D. A. Hodges, and P. R. Gray, "A high performance NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 760–768, Dec. 1978.
[5] W. C. Black *et al.*, "A high performance low power CMOS channel filter," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 929–938, Dec. 1980.
[6] V. R. Saari, "Low power high drive CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 121–127, Feb. 1983.
[7] P. R. Gray and R. G. Meyer, "MOS operational amplifier design—A tutorial overview," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 969–982, Dec. 1982.
[8] R. Read and J. Wieser, as referred in [7].



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