Multistage Amplifier Topologies with Nested G_m-C Compensation

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***Abstract*— This paper presents a multistage amplifier for low-voltage applications (<2 V). The amplifier consists of simple (noncascode) low gain stages and is stabilized using a nested transconductance-capacitance compensation (NGCC) scheme. The resulting topology is similar to the well known nested Miller compensation (NMC) multistage amplifier, except that the proposed topology contains extra G_m feedforward stages which are used to enhance the amplifier performance. The NGCC simplifies the transfer function of the proposed multistage amplifier which, in turn, simplifies its stability conditions. A comparison between the NGCC and NMC shows that the NGCC has wider bandwidth and is easier to stabilize. A four-stage NGCC amplifier has been fabricated using a 2-μm CMOS process and is tested using a $\pm$1.0 V power supply. A dc gain of 100 dB has been measured. A gain bandwidth product of 1 MHz with 58° of phase margin and power of 1.4 mW can be achieved. The op amp occupies an active area of 0.22 mm^2. Step response shows that the op amp is stable.**

***Index Terms*—Amplifiers, compensation, multistage amplifiers, operational amplifiers.**

I. Introduction

As the power supply voltage for integrated circuits continues to scale down, the analog design in mixed signal environments is becoming more difficult and challenging. The main reason is that the threshold voltage (V_T) is not expected to scale down proportionally to the supply voltage. The operational amplifier, which is a core building block for analog systems, is a perfect example to demonstrate how difficult it is to design in a low-voltage environment. The conventional vertical gain enhancement technique (cascoding) is no longer suitable for low-voltage applications. Instead, horizontal gain enhancement techniques (cascading) must be used. In designing a multistage op amp with multiple feedback loops, special precaution in the compensation must be taken to ensure stability [1]. Several op amps with multistage cascading have been designed, for instance, those designed for ISDN applications [1], [2]. Both papers do give some compensation guidelines to ensure the op amp stability. However, they do not give a strong theoretical analysis to support their proposed stability criteria. Both op amps are based on what is known as nested Miller compensation (NMC) technique. Eschauzier and Huijsing have analyzed the stability of the NMC topology [3]. The analysis is based on the theory of Miller splitting of two-stage amplifier and the treatment of the Miller capacitor as an ideal integrating capacitor. This approach provides the designer with some explanation of the effect of Miller splitting on the performance of multistage amplifiers. However, accuracy has been lost since they did not take into consideration the zeros generated from the two-stage Miller splitting. As will be shown in this paper, the zeros in the internal loop make the actual transfer function of the NMC op amp much more complicated. They cause some reduction in the gain bandwidth. The NMC-based op amps cannot, therefore, be considered an optimized structure. A new topology, the nested transconductance (G_m)-capacitance compensation (NGCC) topology, is proposed in this paper. This topology is based on the nesting of a basic module, which uses multipath Miller zero cancelation [3].

Since stability is one of the key concerns in designing multistage amplifiers, it is highly desirable to have some guidelines that can be used to achieve stable designs. These guidelines have to be in the form of simple stability conditions. In addition, the mapping of the specifications to the transistor level implementation must be manageable. Because of the complexity of the transfer function of the NMC-based multistage amplifiers, it is very difficult to derive stability conditions with reasonable complexity. This makes it quite difficult to come up with a systematic design procedure which would yield stable NMC amplifiers. While the performance of the proposed NGCC topology is comparable to other topologies, such as those reported in [4], its main strength is the simplicity of the design process required to achieve stable multistage amplifiers.

In this paper, the proposed NGCC topology will first be presented in Section II. The advantage of using G_m feedforward will be demonstrated in Section III. A detailed design procedure of the NGCC amplifier will be described in Section IV. Section V introduces the transistor-level realization of the multistage amplifier topology. The experimental results of an NGCC amplifier are included in Section VI.

II. The NGCC Topology

In this section, the concept of G_m feedforward and the NGCC topology will first be introduced. Then the simple general transfer function for NGCC amplifier will be derived and compared with that of the NMC amplifier.

A. Structure of the NGCC Amplifier

Previously reported amplifier topologies have used G_m feedforward technique. The amplifier topology in Fig. 1(a) is

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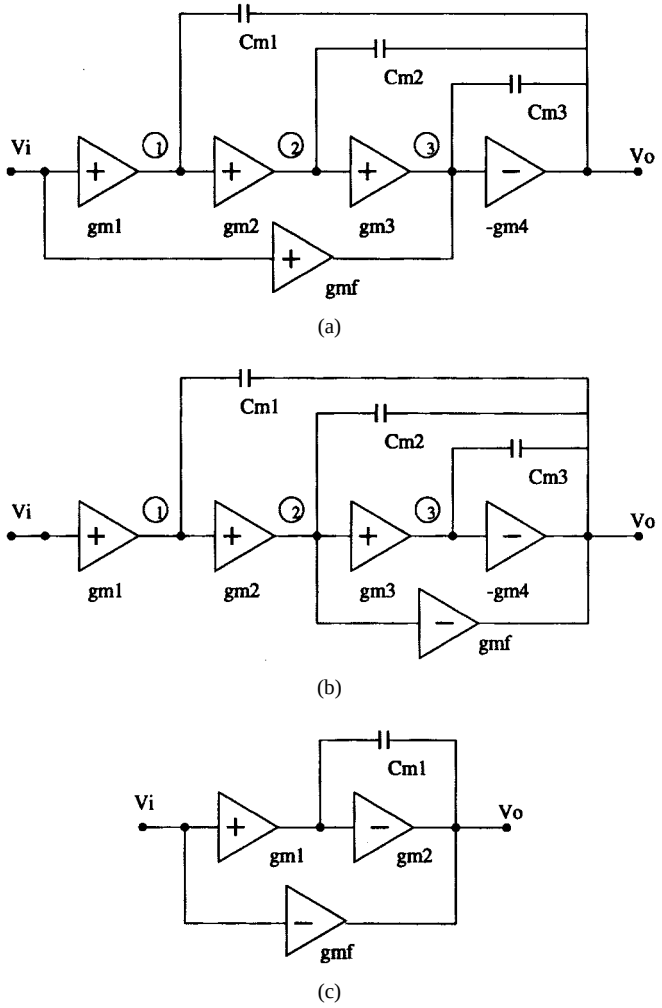


Fig. 1. (a) Multipath nested Miller compensation topology. (b) An abstract model for the amplifier proposed by Castello *et al.* (c) The amplifier with multipath Miller zero cancelation.

the multipath nested Miller compensation structure proposed by Eschauzier and Huijsing. The feedforward transconductance stage g_{mf} is used to maximize the amplifier bandwidth [5]. The signal is fedforward via (g_{mf}) from the input node to an internal node (node 3) while bypassing some intermediate nodes (1 and 2). Beside the feedforward from input node to internal node, a signal can be fedforward from internal nodes to the output node. One example is shown in Fig. 1(b), which is an abstract model for the amplifier proposed by Castello, *et al.* [1]. The use of feedforward stage in this amplifier is not for maximizing the bandwidth, instead it is used, along with g_{m3} and g_{m4} stages, to control the quiescent current of the class AB output buffer. The feedforward can also be made from the input node to output node, as shown in Fig. 1(c), where the g_{mf} stage is used to cancel out the right half plane (RHP) zero [6].

Fig. 1 shows that there exist so many ways for placing one or multiple feedforward stages. The scenario is similar to the placement of multiple compensation capacitors in a multistage cascaded amplifier. The question is, what is the best way to place G_m feedforward stages to maximize the amplifier bandwidth?

In this paper, we are proposing an NGCC topology. Fig. 2(a) depicts an n-stage NGCC amplifier topology. It consists of "n" nested levels of the basic module shown in Fig. 2(b). Note that the dc gain of the amplifier shown in Fig. 2(a) will be determined by the gain of the $n+1$ cascaded stages $(g_{m1}, g_{m2}, \cdots, g_{mn}, g_{mn+1})$. The feedforward transconductance g_{mfi} bypasses the stage from $i+1$ to n at high frequency when the gain of these stages drops. This will extend the bandwidth of the overall amplifier.

B. Small Signal Analysis of the NGCC Amplifier

Consider a three-stage NGCC amplifier. Assume that the capacitor C_L is connected at the output node and that the output conductance of the transconductance amplifiers g_{mi} and g_{mfi} is g_{oi}. It can be shown that the three-stage amplifier has transfer function shown in (1) at the bottom of the page. The actual transfer function contains some second order terms which have been ignored to simplify the transfer function without losing accuracy. It is observed from (1) that g_{mf1} and g_{mf2} will affect the zeros and the poles of the transfer function. By making $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$, (1) becomes (2), shown at the bottom of the page. It is interesting to observe that the RHP zeros of (1) have been cancelled. This is due to the multipath Miller zero cancelation phenomenon presented in [3]. More important is the simplification of the denominator of the transfer function.

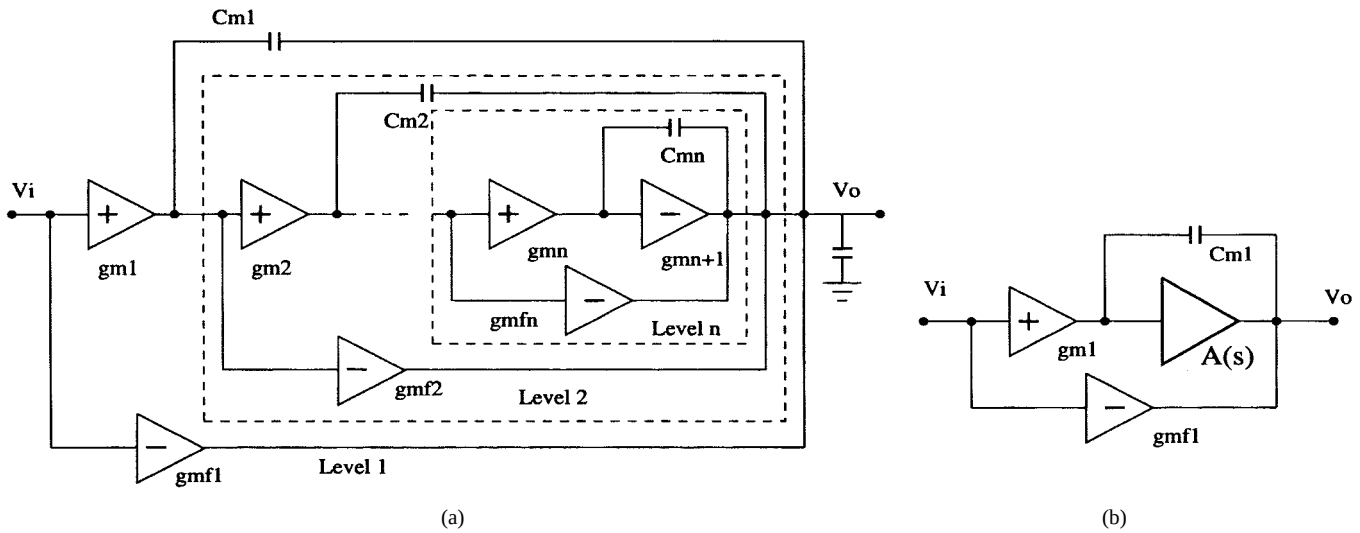
Based on the approximation procedure presented in Appendix A, (2) can be simplified to the form of (A.9). It is shown here for convenience

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-k_1 k_2 k_3}{\left(1 + \frac{k_1 k_2 k_3 s}{f_1}\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3}\right)} \tag{3}$$

where k_i and f_i $(i = 1, 2, 3)$ are defined in Appendix A. The regularity and modularity of the NGCC topology [see Fig. 2(a)] allows for writing the transfer function for a general

$$\frac{V_o(s)}{V_i(s)} = -\frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf2} - g_{m2})C_{m2} + (g_{mf1} - g_{m1})C_{m1}C_{m2}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2(g_{m3} + g_{mf2} - g_{m2})C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}} \tag{1}$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2g_{m3}C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}} \tag{2}$$



(a) (b)

Fig. 2. (a) Conceptual multistage amplifier topology with NGCC. (b) Basic module.

TABLE I
COMPARISON OF POLYNOMIAL COEFFICIENTS FOR FOUR-STAGE NMC AND NGCC AMPLIFIER

$P_h(s)$	a_1	a_2	a_3
NMC	$\frac{(g_{m4}C_{m2}-g_{m2}C_{m3})}{g_{m2}g_{m4}}$	$\frac{(g_{m4}-g_{m2}-g_{m3})C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$
NGCC	$\frac{C_{m2}}{g_{m2}}$	$\frac{C_{m2}C_{m3}}{g_{m2}g_{m3}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$
$Z(s)$	b_1	b_2	b_3
NMC	$\frac{C_{m3}}{g_{m4}}$	$\frac{C_{m2}C_{m3}}{g_{m3}g_{m4}}$	$\frac{C_{m1}C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$
NGCC	0	0	0

n-stage amplifier by inspection as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_o}{\left(1+\frac{A_o s}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\cdots+\frac{s^{n-1}}{\prod_{i=2}^{n} f_i}\right)} \quad (4)$$

where

$$A_o = \prod_{j=1}^{n} k_j.$$

If all the G_m feedforward stages are omitted, the NGCC topology reduces to an NMC topology [3]. Using a similar analysis to that used for the NGCC amplifier, the transfer function of a four-stage amplifier with NMC was derived and is given by

$$\frac{V_o(s)}{V_i(s)} = -A_o \frac{1-b_1 s-b_2 s^2-b_3 s^3}{(1+s/p_1)(1+a_1 s+a_2 s^2+a_3 s^3)} \quad (5)$$

where

$$A_o = k_1 k_2 k_3 k_4, \quad p_1 = \frac{f_1}{A_o} \quad \text{(i.e., } f_1 = \text{GB)}$$

and the b_i's and a_i's coefficients are shown in Table I, which compares the polynomial coefficients of four-stage amplifiers with NGCC (Fig. 3) and NMC. The dc gain (A_o) and the dominant pole (p_1) are similar for both amplifiers.

III. COMPARISON BETWEEN THE NGCC AND NMC AMPLIFIERS

Using multiple stages in an amplifier may lead to instability if certain conditions are not satisfied. It also results in bandwidth reduction. Both issues will be discussed next for the NGCC and NMC topologies.

A. Bandwidth Consideration

The bandwidth of a four-stage NGCC amplifier will be compared with that of an NMC amplifier of similar complexity. If the frequency is normalized with respect to the gain bandwidth (GB), the denominators of both amplifiers can be written as

for NGCC

$$D(s_n) = \left(1+\frac{A_o \text{GB} s_n}{f_1}\right) \times \left(1+a_1 \text{GB} s_n + a_2 \text{GB}^2 s_n^2 + a_3 \text{GB}^3 s_n^3\right) \quad (6.a)$$

for NMC

$$D'(s_n) = \left(1+\frac{A_o \text{GB}' s_n}{f_1'}\right) \times \left(1+a_1' \text{GB}' s_n + a_2' (\text{GB}')^2 s_n^2 + a_3' (\text{GB}')^3 s_n^3\right) \quad (6.b)$$

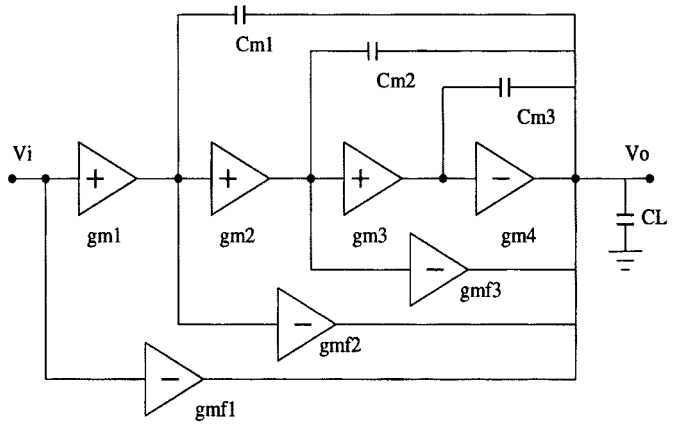


Fig. 3. A four-stage amplifier with NGCC.

where the primed symbols correspond to the NMC, and s_n is the normalized frequency (s/GB).

For both amplifiers to have the same normalized frequency response, the coefficients of both polynomials in (6.a) and (6.b) must be equal. Equating these coefficients and using the corresponding expressions from Table I, a relation between the cutoff frequency of the last stage (f_4) of the NGCC and that of the NMC (f_4') can be derived. Assuming that the compensation capacitors for both amplifiers are equal, it can be shown that

$$\frac{f_4}{\mathrm{GB}} = \frac{f_4'}{\mathrm{GB}'} - \frac{f_2' + f_3'}{\mathrm{GB}'}. \tag{7}$$

This implies that

$$\frac{f_4}{\mathrm{GB}} < \frac{f_4'}{\mathrm{GB}'}. \tag{8}$$

The inequality can be interpreted in two different ways. If the NGCC and the NMC are assumed to have the same gain bandwidth $(\mathrm{GB} = \mathrm{GB}')$, then $f_4 < f_4'$. This implies that the power of the last stage of the NGCC amplifier is less than that of the NMC amplifier. Since the last stage consumes more power than any other stage, as will be explained in Section IV, it can be concluded that for the same gain bandwidth, the NGCC will consume less power than the NMC. If, however, both amplifiers are compared for the same power (i.e., $f_4 = f_4'$), the NGCC will have a greater gain bandwidth product than the NMC.

B. Stability Analysis

The stability conditions of the NGCC amplifier were derived by applying the Routh stability criterion on the closed-loop transfer function of the unity gain follower. It can be shown that the NGCC amplifier has the following closed-loop transfer function:

$$H_{\mathrm{CL}}(s) = \frac{1}{1 + \frac{s}{f_1} + \frac{s^2}{f_1 f_2} + \frac{s^3}{f_1 f_2 f_3} + \frac{s^4}{f_1 f_2 f_3 f_4}}. \tag{9}$$

Applying the Routh stability criterion on the transfer function in (9), we get

$$f_4 > f_2 \tag{10.a}$$

$$f_4 > f_2 \frac{1}{(1 - f_1/f_3)}. \tag{10.b}$$

Since f_1/f_3 is smaller than unity, (10.b) becomes the necessary and sufficient condition. For the NMC amplifier, the stability conditions are

$$\left(\frac{1}{f_2} - \frac{1}{f_4}\right) \times \left(\frac{1}{f_2 f_3} - \frac{1}{f_2 f_4} - \frac{1}{f_3 f_4}\right) > \frac{1}{f_2 f_3 f_4} \tag{11.a}$$

$$\left(\left(\frac{1}{f_2} - \frac{1}{f_4}\right) \times \left(\frac{1}{f_2 f_3} - \frac{1}{f_2 f_4} - \frac{1}{f_3 f_4}\right) - \frac{1}{f_2 f_3 f_4}\right) > \left(\frac{1}{f_2 f_3} - \frac{1}{f_2 f_4} - \frac{1}{f_3 f_4}\right)^2 f_1. \tag{11.b}$$

Comparing the conditions in (10) and (11), it is obvious that the stability conditions of the NMC are very complex. It is, therefore, much easier to design an NGCC amplifier with the stability conditions being satisfied.

The effect of the G_m feedforward on the stability can also be verified by comparing the root loci of the NMC and NGCC topologies with equal gain bandwidth (GB). The loci of the NMC and the NGCC are shown in Fig. 4(a) and (b), respectively. The plots are obtained based on the assumption that $f_1 = 1$ MHz and $f_4 = 6$ MHz for both topologies. The "x" labeled loci correspond to $f_2 = 2$ MHz while the "o" labeled loci correspond to $f_2 = 3$ MHz. For both cases of f_2, f_3 is varied from 3 MHz to 6 MHz. It is observed from the figure that the NMC amplifier may have RHP poles. No RHP pole exists for the NGCC amplifier as shown in Fig. 4(b). Similar behavior for the root movement has been observed when f_1 and f_4 are changed while f_2 and f_3 are kept unchanged. In order to make the NMC topology stable, f_4 has to be at least 8 MHz. This suggests that power consumption of the NMC has to be greater than that of the NGCC which is in agreement with the conclusion of the previous subsection.

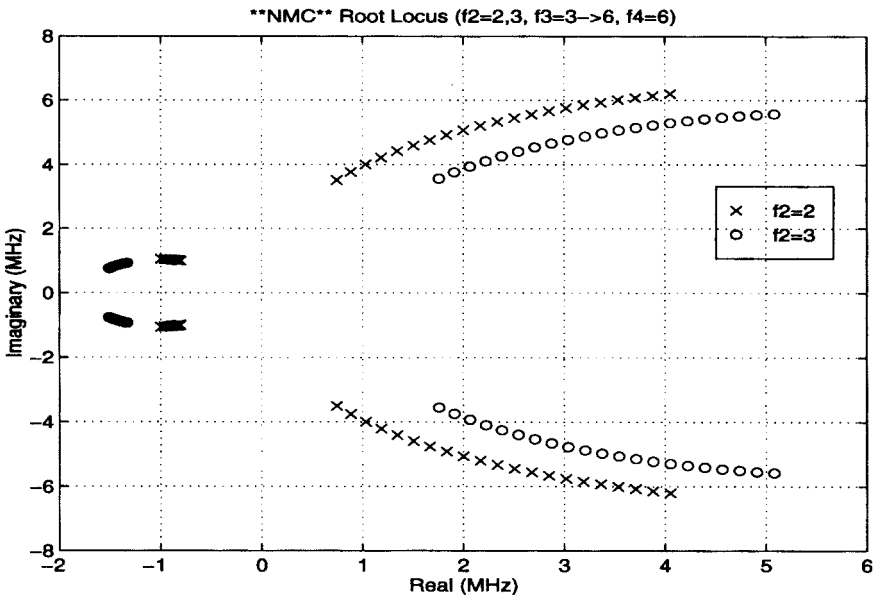
IV. Design

The design of a multistage amplifier is very challenging because of the large number of degrees of freedom available. This is due to the number of possible ways to locate the poles. It is, therefore, important to define the design strategy and design criteria carefully.

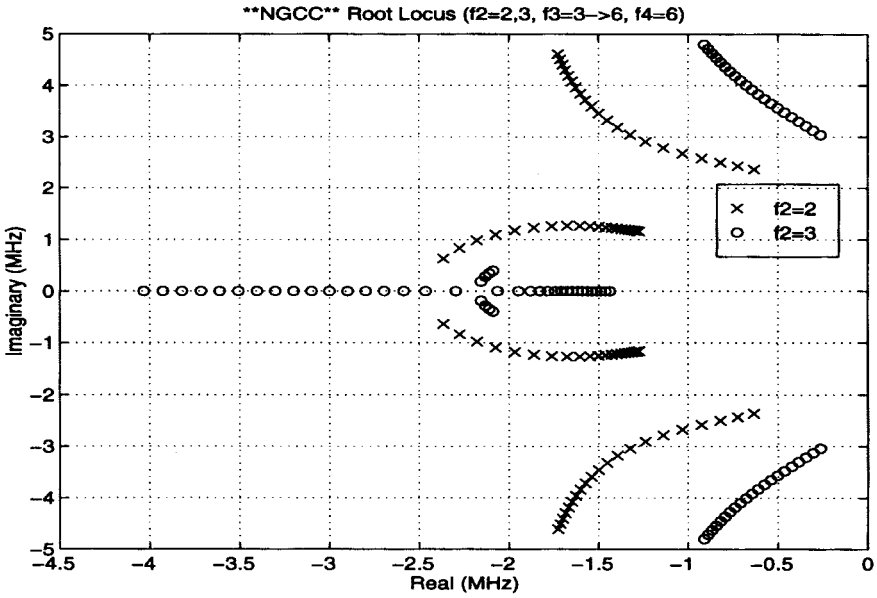
The gain-bandwidth product determines the location of the first pole. The phase margin (ϕ_m) is determined by the high-frequency poles. In a two-stage amplifier, the phase margin is closely related to the second pole (nondominant pole) and hence the design is quite simple. In a four-stage amplifier, the phase margin is determined by more than one pole (p_2, p_3, and p_4), which in turn are determined by the placement of f_2, f_3, and f_4. Using (4), and assuming that $f_1 = \mathrm{GB}$, and that f_3 and f_4 are both greater than f_2, it can be demonstrated that the phase margin (ϕ_m) is approximated by

$$\phi_m = 90^\circ - \tan^{-1}\left(\frac{\mathrm{GB}}{f_2} \times \frac{1 - \mathrm{GB}^2/f_3 f_4}{1 - \mathrm{GB}^2/f_2 f_3}\right) \approx 90^\circ - \tan^{-1}\left(\frac{\mathrm{GB}}{f_2}\right). \tag{12}$$

If $f_2 = 2\mathrm{GB}$, 60° of phase margin can be achieved as long as $f_3 > f_2$ and $f_4 > f_2$. This implies that there exists an infinite number of combinations for the locations of the poles p_3 and



(a)



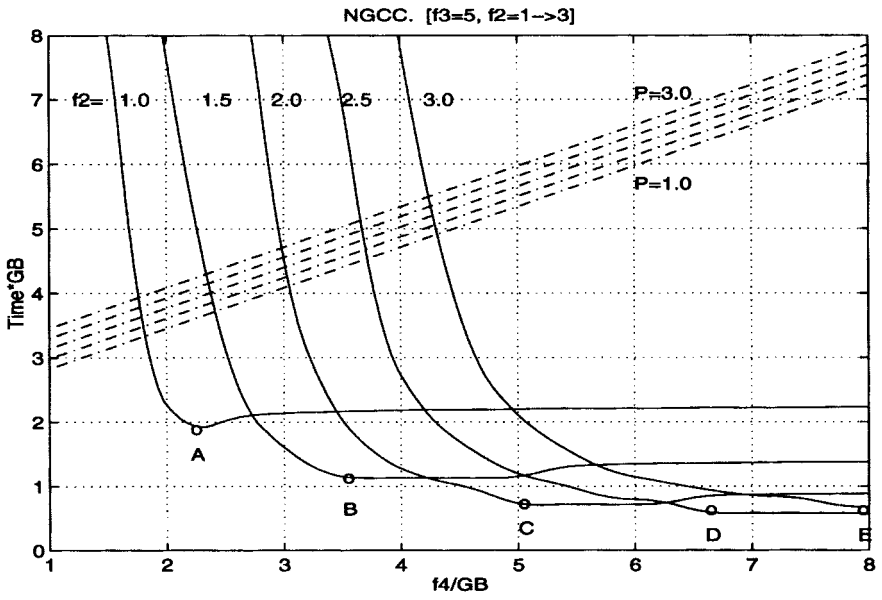
(b)

Fig. 4. The root loci of the (a) NMC amplifier and (b) NGCC amplifier.

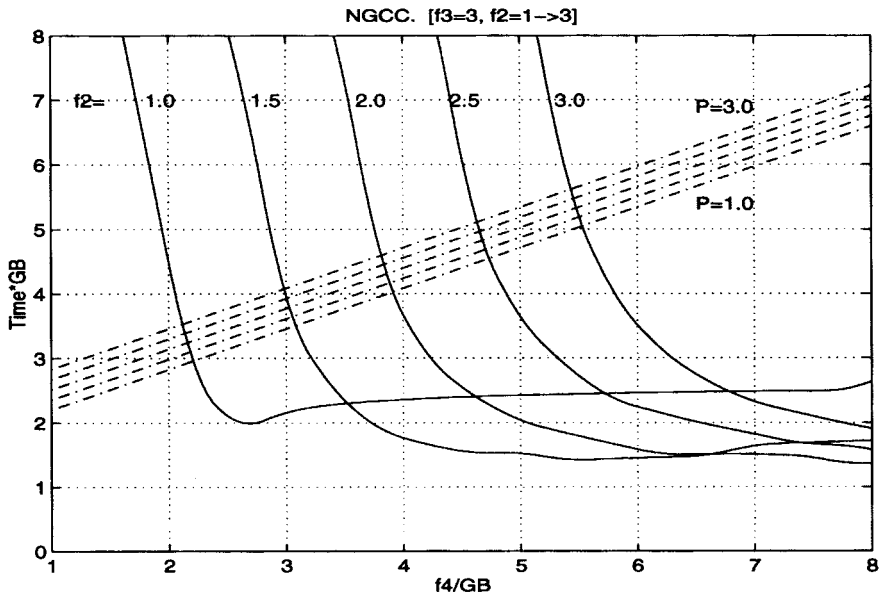
p_4 which would yield the same phase margin. However, it is not enough to base the design solely on the phase margin for a multistage amplifier. Hence, more design constraints are needed. Some of the most critical parameters that can be used in the design process are the settling time (T_s) and the power consumption (P).

To obtain high dc gain (>80 dB) from a multistage amplifier with simple (noncascode) gain stages, four stages will be typically required. Designing such an amplifier is difficult because of the relatively large number of variables (f_i, $i = 1, 2, \cdots, n$). To find the optimal set of cutoff frequencies which satisfy the requirements, we need to use a numerically based search in the design space. This is feasible at the macromodel level and does not need extensive computing. Note that (10) defines the design space where the amplifier is stable. This reduces the size of the space to be searched. In the case of the NMC, the stability conditions cannot be used to limit the design space due to their complexity.

The following example demonstrates the design procedure of a four-stage NGCC amplifier at the macromodel level. The design constraints are GB, T_s, and P. The GB determines f_1 [see (5)]. The rest of the parameters (f_2, f_3, and f_4) are to be determined based on T_s and P. For that purpose, a search in the design space, defined by (10), was conducted. Note that the cutoff frequencies were normalized with respect to GB. Fig. 5(a) shows the results for sweeping f_4/GB from one to eight for different values of f_2/GB $(1, 1.5, \cdots, 3)$ with f_3/GB fixed at five. Similar plots were generated for $f_3/\mathrm{GB} = 3$ and



(a)



(b)

Fig. 5. The normalized settling time (solid) and normalized power (dashed) versus f_4 when (a) $f_3 = 5$ and (b) $f_3 = 3$.

4. Fig. 5(b) shows the plot when $f_3/\mathrm{GB} = 3$. The plots show that the settling time drops sharply as f_4/GB increases and then levels out, and that the minimum settling time decreases as f_2/GB and f_3/GB increase simultaneously [as shown by the points A, B, C, D, and E in Fig. 5(a)]. Note that when f_4/GB is decreased to approach to the value of f_2/GB, the settling time increases exponentially. This indicates that the system will become unstable. This observation is in agreement with the stability criterion in (10.a). The comparison between (a) and (b) in Fig. 5 indicates that increasing f_3/GB will reduce the minimum settling time. It is important at this point to mention that T_s was estimated based on the closed-loop step response using MATLAB.

It is interesting to compare the change in the settling time versus that of the phase margin as a function of f_4/GB. Fig. 6 shows that the phase margin changes by 10% while the settling time changes by an order of magnitude for the same f_4/GB variation. This indicates that the phase margin cannot be used solely for design purposes.

The power consumption is a critical design parameter. Appendix B gives a derivation of the power expression used in this analysis. The normalized power values depicted in Fig. 5 were based on (B.8), where $\alpha_1 = \alpha_2 = \alpha_3 = 0.5$ and $\alpha_4 = 1$. Hence, the power is basically proportional to $0.5(\sum_1^3 f_i) + f_4$.[1] It is therefore expected that while the minimum T_s improves as f_2, f_3, and f_4 increase, the power increases as well. This tradeoff between power and settling time can be exploited to

[1]The contribution of the last stage to the total power consumption is more significant compared to other stages especially if α is small.

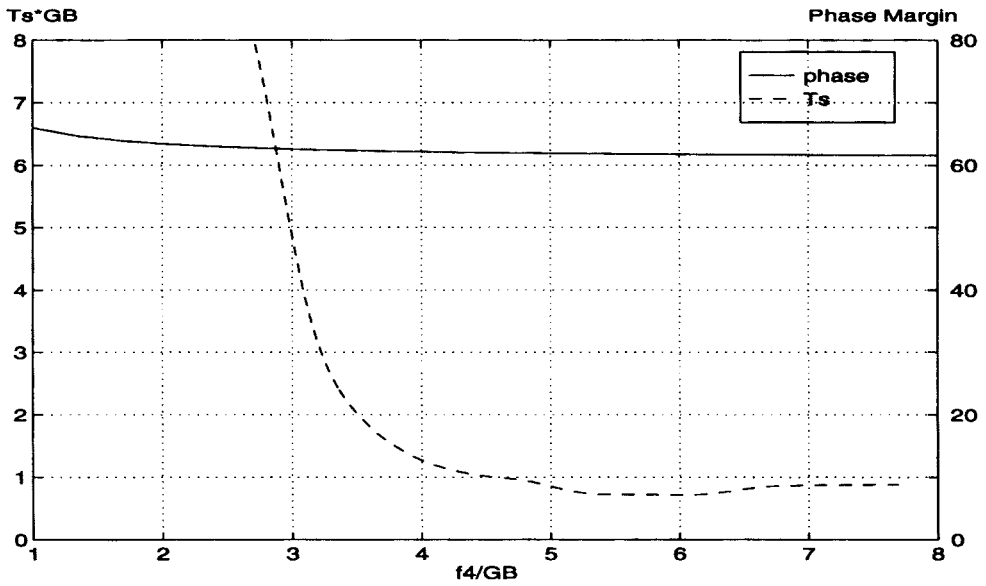


Fig. 6. The phase margin and normalized settling time (T_sGB) of an NGCC amplifier versus $f_4/$GB.

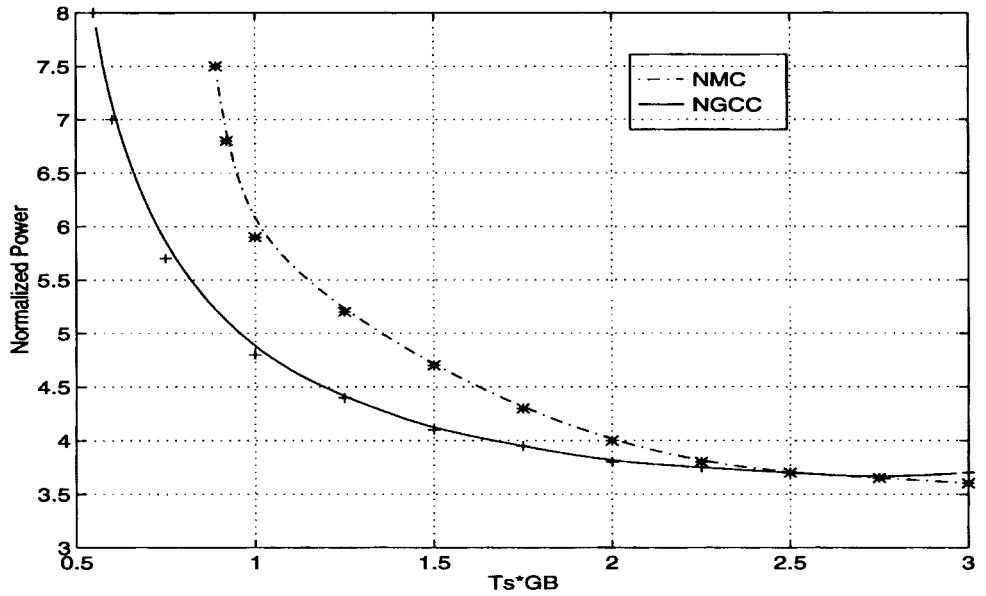


Fig. 7. The normalized power consumption of the NGCC and the NMC amplifiers as a function of the normalized settling time.

optimize the power for a given settling time. Through the search in the design space, it is possible to find the proper combination of f_1, f_2, f_3, and f_4 which would satisfy the settling time requirements with the least power consumption.

It must be noted that the power lines (in Fig. 5) depend on the selected α values. Reducing α will cause the power consumption to drop while T_s remains unchanged (T_s does not depend on α) and yields area savings. The value of α should, however, be kept large enough to ensure that the compensation capacitors are larger than the parasitic capacitance to reduce sensitivity to process variation. In our design analysis, the compensation capacitors are chosen to be half of the load capacitor, therefore $\alpha_1 = \alpha_2 = \alpha_3 = 0.5$.

The analysis described above was used to find the minimum power consumption of the NGCC amplifier for a given normalized settling time. The same procedure was applied to the NMC amplifier. Fig. 7 shows a comparison between the minimum normalized power for the NGCC and the NMC versus normalized settling time (T_sGB). The NGCC offers lower power consumption, in particular, for lower settling times.

V. Realization of Multistage Low-Voltage Amplifiers

Structurally, the only difference between NGCC and NMC is that the NGCC (Fig. 2) contains extra G_m feedforward stages. These extra G_m feedforward stages may be considered as an overhead in terms of area and power. In this section we address the implementation of the NGCC and demonstrate that this overhead is of no significance.

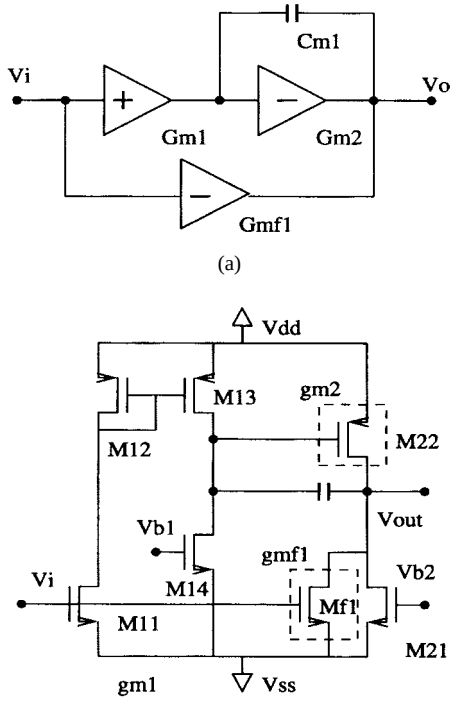


Fig. 8. (a) The basic module of the NGCC topology and (b) its transistor level realization.

A. Implementation of G_m Feedforward

Fig. 8(b) depicts the transistor level realization of the basic cell [see Fig. 8(a)] of an NGCC amplifier. The G_{m1} block is realized using the noninverting stage M_{11}–M_{14}. The transconductance of M_{11} must be equal to the desired transconductance of G_{m1}. The second stage G_{m2} is implemented using the inverting stage M_{21} and M_{22}. The transconductance of M_{22} is equal to that of G_{m2}. The simplest way to realize the feedforward stage G_{mf1} is to use a single MOS transistor (M_{f1}), which is driven by the input and connected to the output node. To ensure that $G_{m1} = G_{mf1}$, the transistor M_{f1} is sized the same as M_{11} and their layout should be closely matched. The operating current of M_{22} is partly delivered by M_{f1}. Since $g_{m22} > g_{mf1}$ (because G_{m2} is typically greater than G_{m1}), M_{22} may require more dc current than what M_{f1} can provide, it is therefore necessary to add M_{21} to provide the rest of the current. In short, the biasing transistor of the output stage has been broken into two parts, of which one is used to implement the feedforward stage. This implementation ensures that both silicon area and power consumption of the NGCC amplifier will not be greater than that of the NMC amplifier. In the case where $g_{mf1} > g_{m2}$, the transistor M_{21} must be removed and substituted by a P-MOS transistor in parallel with M_{22}.

The same approach can be extended to realize multistage amplifiers. Fig. 9 shows a four-stage op amp with G_m-feedforward, which is the realization of the four-stage NGCC amplifier in Fig. 3. A differential input stage and an extra G_m feedforward stage (g_{mf1}) have been added. The transistors M_3–M_5 in Fig. 9 realize the feedforward stage g_{mf1}. All gain stages, other than the differential stage, can operate with a supply voltage of $V_T + 2V_{\mathrm{DS_{sat}}}$ (~1.2 V for $V_T = 0.8$ V). The differential stage, which requires $V_T + 3V_{\mathrm{DS_{sat}}}$ (~1.4 V for $V_T = 0.8$ V), determines the power supply voltage. If low V_T devices are used for the input pair to increase the common-mode range, then the minimum possible power supply would be around 1.2 V.

B. Design Procedures for the NGCC Amplifier

Next we will illustrate the simplicity of mapping the design specifications down to the transistor level in the case of the NGCC multistage amplifier. To demonstrate this, a four-stage NGCC amplifier is used as an example. The following specification have been assumed: GB = 1 MHz, T_s less than 1 μs with minimum power consumption and a load capacitance of 10 pF.

The following steps summarize the proposed design procedures.

- The cutoff frequency of the first stage (f_1) is given by GB (=1 MHz).
- Suitable α values are chosen (e.g., $\alpha_1 = \alpha_2 = \alpha_3 = 0.5$). Note that α_4 is always unity.
- The cutoff frequency of the other stages is chosen based on the design space search. According to the search, point "C" in Fig. 5(a) ($f_2 = 2$ MHz, $f_3 = 5$ MHz, and $f_4 = 5$ MHz) happens to be the point of minimum power for the desired T_s.
- The transconductance of each stage (g_{mi}) is determined from the parameters f_i, α_i, and C_L [see (B.5)].
- The biasing current of each stage I_i is determined based on the desired power. Since the total power is given by

$$P = (V_{\mathrm{dd}} - V_{\mathrm{ss}})\left(\frac{\alpha_1 f_1}{f_4} + \frac{\alpha_2 f_2}{f_4} + \frac{\alpha_3 f_3}{f_4} + 1\right) I_4 \quad (13)$$

  the current I_i of the ith stage can be obtained from the following expression:

$$I_i = \frac{P\alpha_i f_i}{f_4(V_{\mathrm{dd}} - V_{\mathrm{ss}})\left(\frac{\alpha_1 f_1}{f_4} + \frac{\alpha_2 f_2}{f_4} + \frac{\alpha_3 f_3}{f_4} + 1\right)}. \quad (14)$$

  The desired value of the power P can either be part of the design specifications or chosen by the designer.
- Using the transconductance of the transistors in each stage and the biasing current, their aspect ratios can be determined.

Table II summaries the HSPICE simulated GB, phase margin (ϕ_m), settling time (T_s) which are compared to the desired values. Good agreement between the desired and the simulated performance is observed which implies that the mapping down to the transistor level can be easily achieved. To test the accuracy of the settling time predicted through the use of MATLAB, we have compared MATLAB results to those of HSPICE. Fig. 10 demonstrates the good agreement between the settling times estimated from the transistor level simulations (using HSPICE) and those obtained from the macromodel simulations (using MATLAB).

The four-stage NGCC op amp, was simulated in a unity gain follower configuration with small (100 mV) and large (800 mV) input steps. Fig. 11 depicts the HSPICE output

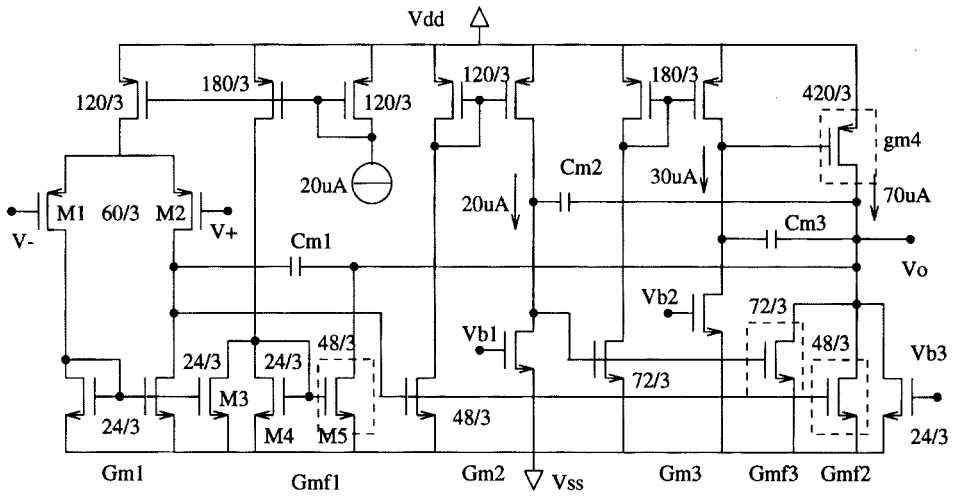


Fig. 9. The schematics of a four-stage NGCC operational amplifier.

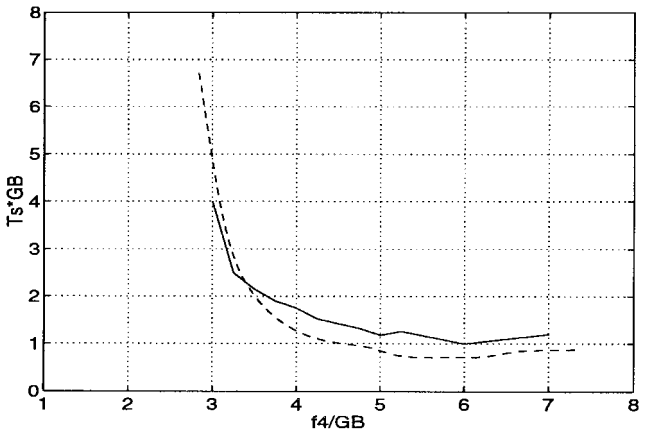


Fig. 10. Plots of settling time versus f_4 from transistor level simulation (solid) and micromodel simulation (dashed).

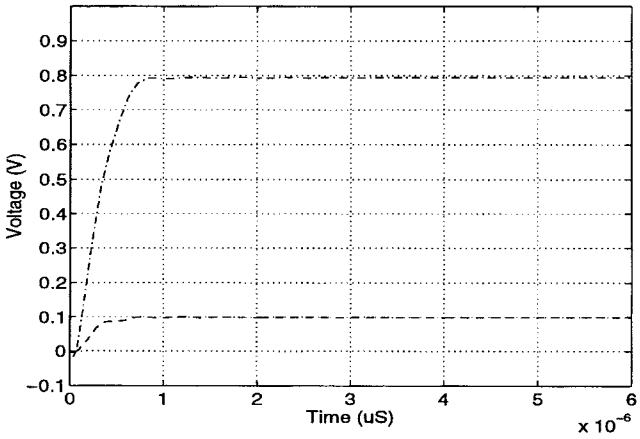


Fig. 11. HSPICE step response of the unity gain follower to the large and small signal input.

response for both the small and large input steps. The figure shows that the amplifier's output settles for both cases. The 0.2% settling times for the small and large signals were measured to be 0.72 μs and 0.92 μs, respectively.

TABLE II
COMPARISON OF OP AMP CHARACTERISTICS

Methods	GB(MHz)	$\phi_m(^\circ)$	$T_s(\mu s)$
Calculated	1.00	61.9	0.75
Simulated	1.06	63.1	0.72

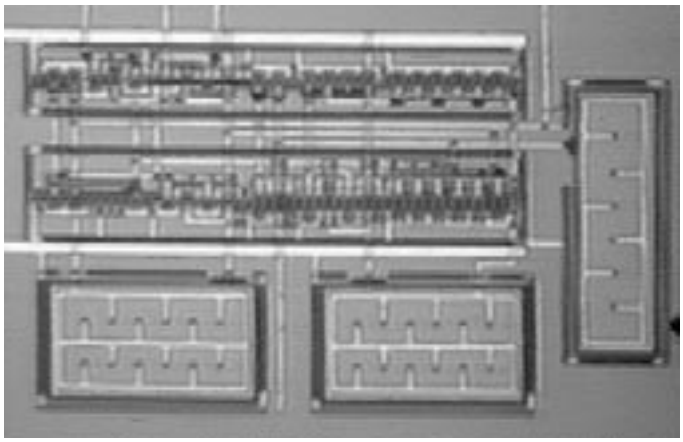


Fig. 12. The chip photomicrograph of the four-stage NGCC amplifier.

VI. EXPERIMENTAL RESULTS

A four-stage NGCC amplifier (Fig. 3) has been designed and fabricated using a 2.0-μm digital CMOS process through MOSIS. The chip micrograph is shown in Fig. 12. A $\pm$1.0 V supply voltage was used. The op amp under test was loaded with a 20-pF capacitor in parallel with a 10-kΩ resistor. Fig. 13 shows the measured frequency response of the op amp. The magnitude of the gain was measured using an HP 3588A spectrum analyzer. It is observed from the figure that the op amp has a unity gain bandwidth of 600 kHz with 60° of phase margin. The op amp consumes 0.68 mW of power. The gain bandwidth can be increased to 1 MHz with 1.4 mW of power consumption. Note that the op amp has a dc gain around 100 dB.

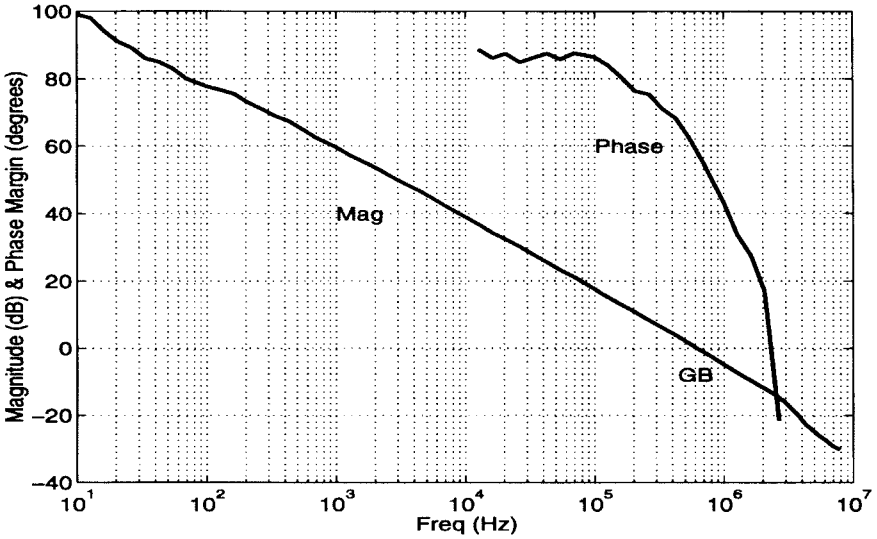


Fig. 13. Measured frequency response of the fabricated four-stage NGCC amplifier.

TABLE III
MEASURED PERFORMANCE OF THE FOUR-STAGE NGCC OP AMP

Power Consumption	$0.68mW$	$1.4mW$
DC Gain	$\approx 100dB$	$\approx 100dB$
Gain Bandwidth	$610kHz$	$1.0MHz$
Phase Margin	60^o	58^o
Input Offset	$5.2mV$	$5.2mV$
Slew Rate	$2.5V/\mu s$	$5.0V/\mu s$
Power Supply	$\pm 1.0V$	$\pm 1.0V$
Load Condition	$10k\Omega//20pF$	$10k\Omega//20pF$
Area	$0.22mm^2$	$0.22mm^2$

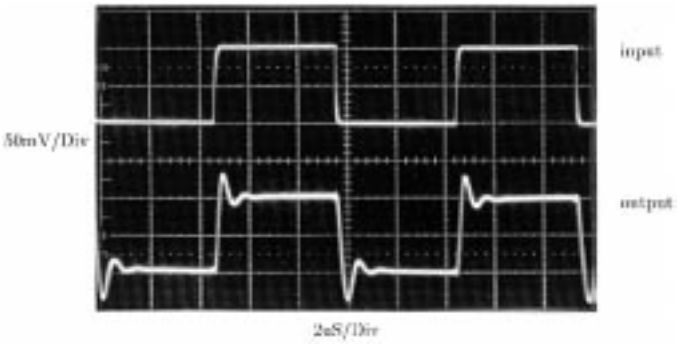


Fig. 14. Step response of four-stage NGCC amplifier configured as a unity gain follower.

The op amp has been configured as a unity gain follower, with the same loading conditions as mentioned above, for total harmonic distortion (THD) measurements and for testing the settling behavior. The op amp has a THD of -70 dB for a 1 kHz sinewave with 1.0 $V_{p\text{-}p}$ input. The measured step input response depicted in Fig. 14 shows the amplifier's settling behavior.

The common-mode input range of the op amp is 1 V. It can be increased if a process with smaller V_T or an input stage with floating gate input stage [11] is used. The amplifier occupies an active area of 0.22 mm^2. Table III gives a summary of the op amp performance.

VII. CONCLUSION

In this paper, a multistage amplifier NGCC topology has been presented. The topology is well suited for low voltage application. Compared with the well-known NMC amplifier topology, the NGCC amplifier shows better gain-bandwidth product. The NGCC topology is easier to stabilize. An implementation of the NGCC amplifier has been proposed. It uses a single transistor as its feedforward stage, thus consuming the same power as the NMC amplifier with little silicon area overhead. An NGCC op amp has been fabricated using 2.0-μm CMOS process. Experiments show that the NGCC amplifier can operate with ± 1.0 V power supply. A dc gain of 100 dB and a gain bandwidth of 1 MHz were measured. It consumes 1.4 mW of power and occupies an active area of 0.22 mm^2.

APPENDIX A
APPROXIMATION OF CHARACTERISTIC FUNCTION

Let $H(s)$ represent the transfer function of an N-stage amplifier

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{N(s)}{D(s)} \tag{A.1}$$

where

$$N(s) = \beta_0 + \beta_1 s + \beta_2 s^2 + \cdots + \beta_{n-1} s^{n-1} \tag{A.2}$$

$$D(s) = \alpha_0 + \alpha_1 s + \alpha_2 s^2 + \cdots + \alpha_n s^n. \tag{A.3}$$

$D(s)$ is the denominator of the transfer function of the amplifier, and can therefore be expressed in terms of its poles $(p_1, p_2, \cdots, p_n)$. Assume that p_1 is the dominant pole and all the others are the high-frequency poles. Hence, $D(s)$ can be written as

$$D(s) = k\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\cdots\left(1 + \frac{s}{p_n}\right)$$

or

$$D(s) = k\left(1 + \frac{s}{p_1}\right)\left(1 + a_1 s + a_2 s^2 + \cdots + a_{n-1} s^{n-1}\right) \tag{A.4}$$

where

$$a_1 = \sum_{i=2}^{n} \frac{1}{p_i} \quad a_2 = \sum_{i \neq j \neq 1} \frac{1}{p_i p_j} \quad \cdots \quad a_{n-1} = \prod_{i=2}^{n} \frac{1}{p_i}.$$

Since p_1 is the dominant pole, we have

$$p_1 < p_i \quad \text{for } 2 \leq i \leq n.$$

Equation (A.4) can be simplified as

$$\begin{aligned} D(s) &= k\left[1 + \left(a_1 + \frac{1}{p_1}\right)s + \left(a_2 + \frac{a_1}{p_1}\right)s^2 + \cdots \right. \\ &\qquad \left. + \left(a_n + \frac{a_{n-1}}{p_1}\right)s^n\right] \\ &\approx k\left[1 + \frac{1}{p_1}s + \frac{a_1}{p_1}s^2 + \cdots + \frac{a_{n-1}}{p_1}s^n\right]. \end{aligned} \tag{A.5}$$

By equating the coefficients of (A.5) and (A.3), the parameters k, p_1, and a_i in (A.5) can be expressed in terms of $\alpha_0, \alpha_1, \cdots,$ and α_n as follows:

$$k = \alpha_0, \quad p_1 = \frac{\alpha_0}{\alpha_1} \quad \text{and} \quad a_i = \frac{\alpha_{i+1}}{\alpha_1}. \tag{A.6}$$

Equation (A.4) can hence be rewritten as

$$\begin{aligned} D(s) &= \alpha_0\left(1 + \frac{s}{\alpha_0/\alpha_1}\right) \\ &\quad \times \left(1 + \frac{\alpha_2}{\alpha_1}s + \frac{\alpha_3}{\alpha_1}s^2 + \cdots + \frac{\alpha_n}{\alpha_1}s^{n-1}\right). \end{aligned} \tag{A.7}$$

Equation (A.7) shows that the denominator of the transfer function can be broken down into two polynomials; a first-order polynomial which corresponds to the dominant pole and a higher-order polynomial which corresponds to the high-frequency poles. The interesting feature of (A.7) is that the coefficients of high-order polynomial can be easily derived from the coefficients of the original $D(s)$ in (A.3).

The approximation approach discussed above can be applied to (2) to give

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_o}{(1 + s/p_1)(1 + a_1 s + a_2 s^2)} \tag{A.8}$$

where p_1, a_1, and a_2 can be obtained using (A6) and (2)

$$\begin{aligned} A_o &= \frac{g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3}} & p_1 &= \frac{g_{o1}g_{o2}g_{o3}}{g_{m2}g_{m3}C_{m1}} \\ a_1 &= \frac{C_{m2}}{g_{m2}} & a_2 &= \frac{C_{m2}C_L}{g_{m2}g_{m3}} \end{aligned}$$

where A_o is the amplifier dc gain and p_1 is the dominant low-frequency pole. The coefficients a_1 and a_2 will determine the other two poles of the three-stage amplifier, which are at high frequency. Now, two more parameters will be defined

$$k_i = \frac{g_{mi}}{g_{oi}} \quad \text{and} \quad f_i = \frac{g_{mi}}{C_{mi}}.$$

These two parameters represent the low-frequency gain and the cutoff frequency of the ith stage. Now, (A.8) can be written as

$$\frac{V_o(s)}{V_i(s)} = \frac{-k_1k_2k_3}{\left(1 + \frac{k_1k_2k_3 s}{f_1}\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3}\right)}. \tag{A.9}$$

APPENDIX B
POWER CONSUMPTION OF MULTISTAGE AMPLIFIER

The total power consumed by an n-stage amplifier is given by

$$P = (V_{\text{dd}} - V_{\text{ss}})\sum_{1}^{n} I_i \tag{B.1}$$

where I_i is the dc current of the ith stage. The above equation can be rewritten as

$$P = (V_{\text{dd}} - V_{\text{ss}})I_n \sum_{1}^{n} \frac{I_i}{I_n}. \tag{B.2}$$

Assuming that the I_i and $(W/L)_i$ are simultaneously scaled by the same factor, the ratio I_i/I_n becomes proportional to g_{mi}/g_{mn}. Hence (B.2) can be written as

$$P = (V_{\text{dd}} - V_{\text{ss}})I_n \sum_{1}^{n} \frac{g_{mi}}{g_{mn}}. \tag{B.3}$$

Let us now assume that

$$C_{mi} = \alpha_i C_L. \tag{B.4}$$

Then

$$g_{mi} = \alpha_i f_i C_L. \tag{B.5}$$

Substituting from (B.5) into (B.3) and knowing that $\alpha_n = 1$, the power expression can be rewritten as

$$P = (V_{\text{dd}} - V_{\text{ss}})I_n\left(1 + \sum_{1}^{n-1} \frac{\alpha_i f_i}{f_n}\right). \tag{B.6}$$

In the analysis described in Section IV, we use the normalized power consumption which is defined as

$$P_n = \left(f_n + \sum_{1}^{n-1} \alpha_i f_i\right). \tag{B.7}$$

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