A 1-V CMOS Pseudo-Differential Amplifier With Multiple Common-Mode Stabilization and Frequency Compensation Loops

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***Abstract*—This paper presents an operational amplifier for a 1-V supply voltage. It comprises three gain stages with ac-boosting and buffered Miller feedback compensation circuits. The implementation uses a standard 0.35-μm CMOS process ($V_{TN} = 0.6$ V and $V_{TP} = -0.72$ V). To accommodate maximum voltage headroom between power rails, a pseudo-differential structure is adopted in this amplifier. The large common-mode gain associated with the structure is suppressed by two common-mode stabilization loops. The amplifier driving 100-pF loads achieves a 4.3-MHz gain–bandwidth product. The settling time of a 1-V_{pp} input step signal is 1.1 μs. The amplifier consumes 249 μW and occupies 0.06-mm^2 silicon area.**

***Index Terms*—CMOS integrated circuits, frequency compensation, low voltage, operational amplifier.**

I. Introduction

AMPLIFIERS play an important role in most analog circuits because their behavior dominates the performance of the function blocks. For low-power application with a continuously decreasing supply, low-voltage, high-performance amplifier design becomes challenging. This study attempts to accomplish a 1-V operational amplifier without any special or low threshold voltage devices.

To get high dc gain under a low supply voltage, it is unfeasible to stack multiple devices between power rails. One solution is to cascade multiple gain stages. However, the scheme causes extra stability issues because additional low-frequency poles are introduced. The phase margin might be degraded significantly. Many researches worked on the construction of frequency compensation techniques [1]–[6]. These techniques can cancel the nondominant poles with zeros or shift them to higher frequencies to stabilize the multistage amplifiers. One example is the ac-boosting compensation (ACBC) [4], which provides a parallel gain path to bypass the band-limited intermediate stage. Moreover, to avoid the right-half-plane (RHP) zero generated with the Miller compensation-based structures [7], [8], a buffer stage in series with a compensation capacitor can be used to remove the zero by blocking the feedthrough path at high frequency.

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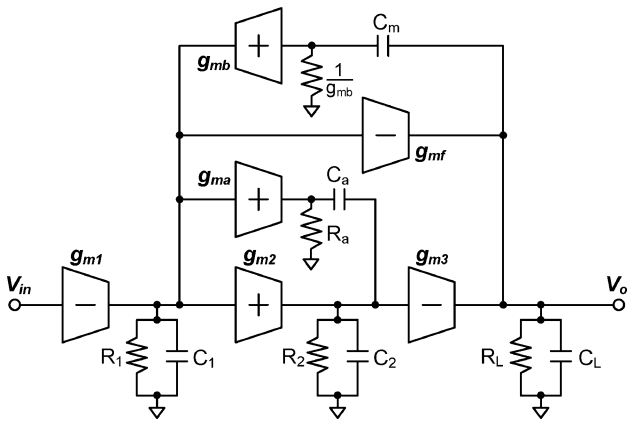

Fig. 1. Three-stage multiloop compensation scheme.

To survive the limited supply voltage, a pseudo-differential structure is adopted to save the voltage drop across the tail current source in a fully differential alternative. Meanwhile, the problems of the high sensitivity on common-mode voltage should be solved. In this study, we adopt a feedforward technique [9] along with the global feedback loop to stabilize the common-mode level. Its efficiency, especially under device mismatch, will be discussed in Section III.

This paper is organized as follows. Section II elucidates the multiloop compensation scheme. Sections III and IV present the circuit implementations and experimental results, respectively. Finally, Section V draws the conclusions.

II. Frequency Compensation Scheme

A. Multiloop Compensation Scheme

The topology of the proposed low-voltage amplifier is shown in Fig. 1. Transconductance stages $g_{m1} - g_{m3}$ comprise the three-stage amplifier. $R_{1,2}$ and $C_{1,2}$ represent the output resistance and the lumped parasitic capacitance of the first two stages. C_L and R_L are the output loading capacitor and resistor, respectively. The feedforward stage g_{mf}, along with the last gain stage g_{m3}, forms the push–pull output stage. A transconductance stage g_{ma} with the output resistance R_a is introduced to enhance high-frequency gain. C_m and C_a are the Miller compensation capacitor and the ac coupling capacitor, respectively. Transconductance g_{mb} is an isolation stage to block the feedthrough signal in the Miller compensation path.

To analyze the stability of the proposed multiloop amplifier, a small-signal transfer function is derived. Based on the practical considerations, the following assumptions are made:

$$\begin{aligned} R_1, R_2 &\gg R_a \\ g_{m1}R_1, g_{m2}R_2, g_{m3}R_L &\gg 1 \\ C_L &\gg C_m \\ C_a &\gg C_1, C_2. \end{aligned}$$

Neglecting the second order terms, the open-loop gain of the circuit in Fig. 1 can be expressed as

$$A(s) = \frac{A_{dc}\left(1+\frac{s}{\omega_5}\right)\left(1+\frac{s}{\omega_6}+\frac{s^2}{\omega_6\omega_7}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}+\frac{s^3}{\omega_1\omega_2\omega_3}+\frac{s^4}{\omega_1\omega_2\omega_3\omega_4}\right)} \quad (1)$$

where $A_{dc} = g_{m1}R_1g_{m2}R_2g_{m3}R_L$ is the dc voltage gain. The dominant pole is located at the first stage output with the equivalent capacitor equal to the Miller capacitor C_m amplified by the second and third stages as

$$\omega_{P1} \approx \frac{1}{R_1A_2A_3C_m} = \frac{1}{R_1g_{m2}R_2g_{m3}R_LC_m}. \quad (2)$$

The other poles and zeros in (1) can be expressed as follows:

$$\omega_1 = \frac{1}{(A_{2h}+k_t)}\frac{g_{m2}}{C_a} \quad (3)$$

$$\omega_2 = (A_{2h}+k_t)\frac{g_{m3}g_{mb}R_1}{C_L} \quad (4)$$

$$\omega_3 = \frac{1}{R_1C_1} \quad (5)$$

$$\omega_4 = \frac{1}{R_aC_2} \quad (6)$$

$$\omega_5 = \frac{g_{mb}}{C_m} \quad (7)$$

$$\omega_6 = \frac{1}{(A_{2h}+k_t)}\frac{g_{m2}}{C_a} \quad (8)$$

$$\omega_7 = (A_{2h}+k_t)\frac{1}{k_tR_aC_2} \quad (9)$$

$$A_{2h} = (g_{m2}+g_{ma})R_a \quad (10)$$

$$k_t = \frac{g_{mf}}{g_{m3}}. \quad (11)$$

The parameter A_{2h} can be regarded as the high-frequency gain of the second stage, which includes g_{m2} and the ac-boosting path g_{ma}. Parameter k_t is the transconductance ratio of the feedforward stage to the last gain stage. Since there is usually the same static current in the g_{m3} and g_{mf} stages, k_t is approximately one. Using these design equations, the gain–bandwidth product can be expressed as

$$\omega_0 = 2\pi\cdot\mathrm{GBW} = A_{dc}\cdot\omega_{P1} = \frac{g_{m1}}{C_m}. \quad (12)$$

B. Pole-Zero Allocation

To optimize the gain–bandwidth product and the phase margin, pole-zero locations should be properly arranged. Since A_{2h} is larger than unity, C_1 and C_2 are parasitic capacitances and thus very small; if the C_a is properly selected, an assumption can be made as follows:

$$\omega_1 \ll \omega_2 \ll \omega_3 \ll \omega_4. \quad (13)$$

The locations of the nondominant poles can be described by the following equations:

$$p_{nd1} = -\omega_1 = -\frac{1}{(A_{2h}+k_t)}\frac{g_{m2}}{C_a} \quad (14)$$

$$p_{nd2} = -\omega_2 = -(A_{2h}+k_t)\frac{g_{m3}g_{mb}R_1}{C_L} \quad (15)$$

$$p_{nd3} = -\omega_3 = -\frac{1}{R_1C_1} \quad (16)$$

$$p_{nd4} = -\omega_4 = -\frac{1}{R_aC_2}. \quad (17)$$

The high-frequency poles ω_3 and ω_4 are far away from the unity-gain frequency because C_1 and C_2 are small. With the similar assumptions, zeros in (1) can be derived as

$$z_{LHP1} = -\omega_5 = -g_{mb}/C_m \quad (18)$$

$$z_{LHP2} = -\omega_6 = -\frac{1}{(A_{2h}+k_t)}\frac{g_{m2}}{C_a} \quad (19)$$

$$z_{LHP3} = -\omega_7 = -(A_{2h}+k_t)\frac{1}{k_tR_aC_2}. \quad (20)$$

The first nondominant pole p_{nd1} and the LHP zero z_{LHP2} can be completely cancelled according to (14) and (19). Therefore, the first nondominant pole is then p_{nd2}. The z_{LHP3} is also far away from the unity-gain frequency and thus negligible. Based on these analysis, the overall phase margin can be determined as

$$\mathrm{PM} = 90^\circ - \tan^{-1}\frac{2\pi\mathrm{GBW}}{|p_{\mathrm{nd2}}} + \tan^{-1}\frac{2\pi\mathrm{GBW}}{|z_{\mathrm{LHP1}}|}. \quad (21)$$

III. Circuit Designs

A. Pseudo-Differential Input Stage With CMFF

Fully differential (FD) and pseudo-differential (PD) are two circuit topologies that can be used to achieve differential input stage. The FD amplifier consists of a differential pair with a tail current source, while the PD amplifier has two independent single-ended common source amplifiers. Compared with the FD structure, the PD structure has larger voltage headroom since there is no voltage drop across the tail transistor. This keeps a larger margin for process and temperature variations under low supply voltage. However, since its common-mode gain is the same as its differential gain, the PD amplifier is incapable of rejecting common-mode signal fluctuation. Therefore, a fast and powerful common-mode stabilization circuit is required in the PD amplifier.

Fig. 2 shows the proposed pseudodifferential input stage. It uses a common-mode feedforward circuit to setup the output common mode against the input common-mode variation. The circuit operations can be described as follows. First, the input voltage is decomposed of a common-mode term V_{ICM} and a differential term v_d. They can be expressed as $V_{ip} = V_{\mathrm{ICM}} + v_d/2$ and $V_{\mathrm{in}} = V_{\mathrm{ICM}} - v_d/2$. The input transistors $M_{11a,b}$, along

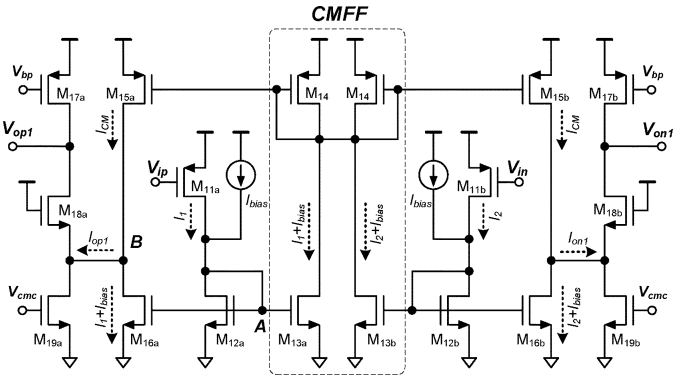

Fig. 2. Circuit diagram of the pseudo-differential input stage.

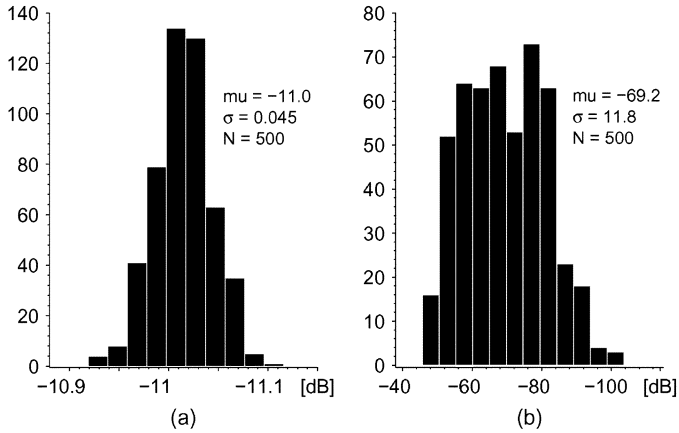

Fig. 3. Statistical distribution of the common-mode gain from 500 Monte Carlo simulations: (a)at node A, (b)at node B in Fig. 2.

with the current mirrors $M_{12a}-M_{13a}$ and $M_{12b}-M_{13b}$, convert the input differential voltage to the current signal. The differential currents are summed up at the diode-connected transistor M_{14} as

$$I_{\rm CM} = I_{M14} = I_{M15a,b} \tag{22}$$

$$= \frac{I_1 + I_2}{2} + I_{\rm bias} \tag{23}$$

$$= K_p\left(\frac{W}{L}\right)_{11}\left[V_{\rm ov}^2 + \left(\frac{v_d}{2}\right)^2\right] + I_{\rm bias} \tag{24}$$

where $V_{\rm ov} = V_{\rm DD} - V_{\rm ICM} - |V_{\rm TP}|$ is the overdrive voltage of the input transistors $M_{11a,b}$. $I_{\rm bias}$ is a small constant current to keep transistors $M_{12a,b}$ in the saturation region. After subtracting $I_{\rm CM}$ from the drain currents of M_{16a} and M_{16b}, the residue current is expressed as

$$I_{\rm op1} = I_{\rm CM} - (I_1 + I_{\rm bias}) = (I_2 - I_1)/2 \tag{25}$$

$$= K_p\left(\frac{W}{L}\right)_{11} \cdot V_{\rm ov} \cdot \frac{v_d}{2} \tag{26}$$

$$= g_{m11}\frac{v_d}{2} = -I_{on1}. \tag{27}$$

The differential output current then becomes

$$I_{\rm od} = I_{\rm op1} - I_{\rm on1} = I_2 - I_1 = g_{m11}v_d. \tag{28}$$

By using the feedforward technique, the differential output current of the PD amplifier becomes the function of the input transconductance and the voltage difference of two inputs and is similar to the FD amplifier. If no mismatch exists between two paths, the common-mode gain of the circuit is zero. However, a pseudo-differential structure always suffers from mismatch. It is more severe in a high-gain stage because the offset in the front stage may smear the input small signal and lead to a saturated output voltage in the following gain stages. The post-layout Monte Carlo simulation is adopted here to further confirm the influence of path mismatch. Fig. 3 depicts the common-mode gain distributions at node A and node B for 500 samples with local mismatches of the circuit parameters. The common-mode gain at node A is about -11 dB, while the common-mode gain at node B can decrease to a mean value of -69.2 dB. Although the distribution is sporadic, it can provide at least an order suppression with this technique.

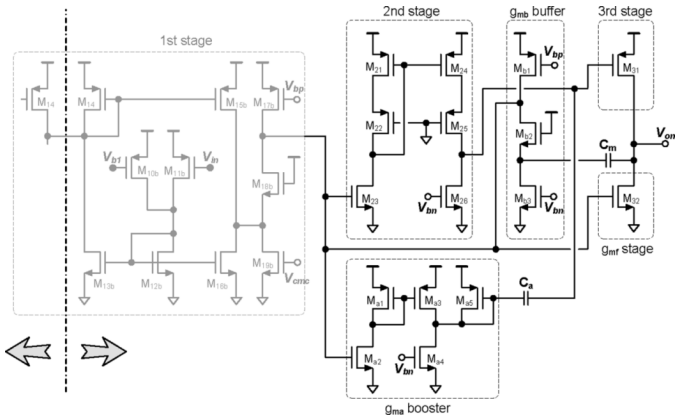

Fig. 4. The schematic of the second and the third gain stages. Only a half of differential circuit is depicted for clarity.

B. Intermediate and Output Stage With Frequency Compensation and CMFB

The schematics of the proposed second and third stages are depicted in Fig. 4. The second stage is composed of transistors $M_{21} - M_{26}$. Transistors $M_{a1} - M_{a5}$ and one capacitor C_a realize the gain-boost path g_{ma}. The output stage employs a push–pull structure to improve the slew rate. The Miller capacitor C_m along with the buffer stage g_{mb} forms the frequency compensation loop, which splits the poles at the input and output stages for closed-loop stability. The buffer can prevent the generation of the RHP zero and the phase response can therefore be improved.

A common-mode feedback (CMFB) circuit is mandatory to set up the common-mode voltage of the two output nodes for a differential amplifier. To attain maximum output swing, the output voltage should be half of the power supply, where 0.5 V is set in this case. Unfortunately, this voltage level is too small to turn on neither p- nor n-type transistors of the adopted technology. To solve this problem, a current-compared CMFB circuit in Fig. 5 is used [10]. The common-mode current is extracted by the resistors $2R$. The detected common-mode signal is then compared with a reference signal generated by $V_{\rm ocm}$ over R to produce the feedback voltage $V_{\rm cmc}$, which results in a voltage change at the gates of $M_{19a,b}$ in Fig. 2. The dc gain of

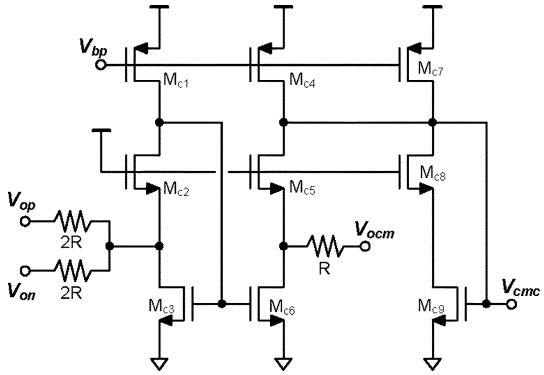

Fig. 5. Current-compared CMFB circuit.

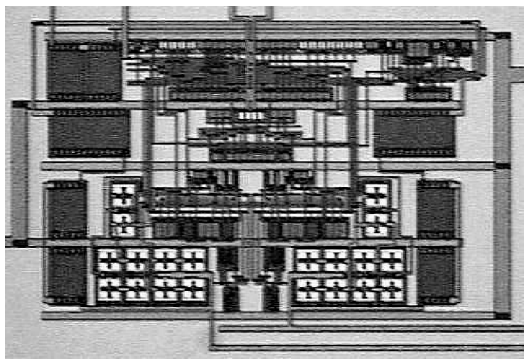

Fig. 6. Die photograph of the proposed operational amplifier.

TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED AMPLIFIER

$g_{m1} = 29\mu$S	$g_{m2} = 150\mu$S	$g_{m3} = 450\mu$S
$g_{ma} = 500\mu$S	$g_{mb} = 150\mu$S	$g_{mf} = 450\mu$S
$C_m = 1$pF	$C_a = 0.55$pF	off-chip $C_L = 100$pF

the common-mode feedback path is determined by the current sensing resistor and the transconductance of M_{c7}.

IV. EXPERIMENTAL RESULTS

A three-stage operational amplifier with multiple frequency compensation and common-mode stabilization loops is designed for a single 1-V supply operation. This amplifier was fabricated in a 0.35-μm standard CMOS technology with threshold voltages of nMOS and pMOS equal to 0.6 and -0.72 V, respectively. Fig. 6 shows the photograph of the integrated amplifier. The circuit parameters and other component values are listed in Table I.

The open-loop gain and phase response of the proposed amplifier are plotted in Fig. 7. The simulated dc gain is around 80 dB with a unity-gain frequency of 5.4 MHz and 71° phase margin driving 100-pF loadings. The measured unity-gain frequency is 4.3 MHz and the phase margin is 68°. The measured common-mode rejection ratio (CMRR) at 100 kHz is larger than 45 dB.

For the p-type input stage, 0.1-V bias is selected because the bias level has to be lower than $V_{\rm DD} - V_{\rm GS,11}$. Fig. 8 is the low-voltage bias scheme adopted in this design [10]. Two

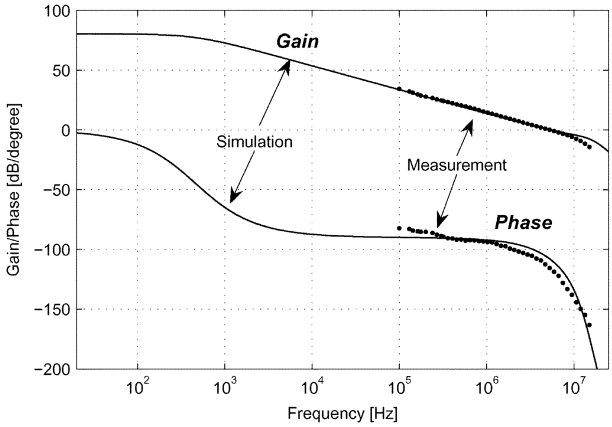

Fig. 7. Gain and phase responses of the open-loop measurements.

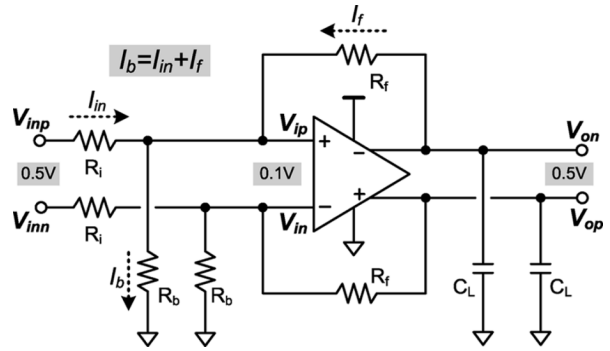

Fig. 8. Closed-loop connection for low-input voltage biasing.

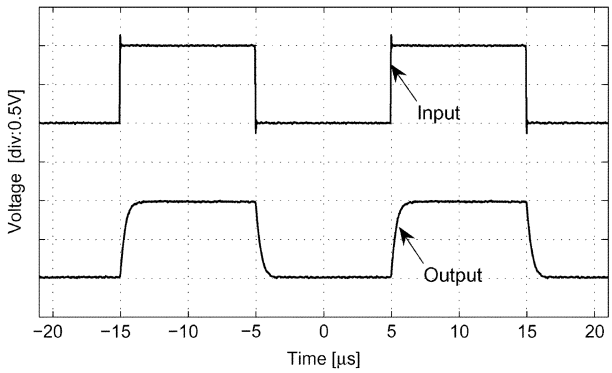

Fig. 9. Measured unity-gain step response.

TABLE II
PERFORMANCE SUMMARY

A_{dc}	80.2dB*	GBW	4.3MHz
$SR_{+/-}$	1.20/1.22V/μs	Phase Margin	68°
V_{dd}	1V	$TS_{+/-}$(to 0.1%)	1.17/1.13μs
I_{dd}	249μA	Power	249μW
THD	-60.7dB#	Active Area	0.06mm^2

* derived from post-layout simulation.
# 1-V_{pp}, 200-kHz sine wave.

bias resistors R_b are connected between the input nodes to the ground to provide the dc paths required by R_i and R_f.

Fig. 9 depicts the measured step response in unity-gain configuration. The response to a 1-$V_{\rm pp}$ 50-kHz square wave

TABLE III
COMPARISON WITH OTHER LOW-VOLTAGE AMPLIFIERS

Design Feature	Blalock'98 [11]	Carrillo'00 [12]	Chatterjee'05 [13]	Bez-Villegas'06 [14]	This Work
Technology	2μm CMOS	1.2μm CMOS	0.18μm CMOS	0.5μm CMOS	0.35μm CMOS
Supply Voltage (V)	1	1	0.5	1	1
Differential Output	NO	NO	YES	NO	YES
Current (mA)	0.287	0.208	0.150	0.095	0.249
DC Gain (dB)	49	70.5	62	60	80
Unity Gain Bandwidth	1.3MHz @22pF	2.1MHz @15pF	10MHz @20pF	4.1MHz @15pF	4.3MHz @100pF
Slew Rate (V/μs)	0.7/1.6	0.9/1.7	2.0	0.8/0.86	1.2/1.22
FOM_S (GBW$\times C_L$/Power)	100	151	2667	647	1730
FOM_L ($\text{SR}_{avg}\times C_L$/Power)	88.2	93.8	533	131.1	485.9

demonstrates a slew rate of 1.2 V/μs and a settling time of 1.13 μs with 0.1% error tolerance. Total power dissipation is 249 μW under a single 1-V supply. Table II summarizes the performance. Table III presents the parameters among several state-of-the-art low-voltage amplifiers. This study exhibits competitive figure of merits in both small-signal and large-signal performances.

V. CONCLUSION

This paper presents the design techniques for a multistage differential amplifier with a supply voltage of 1-V in a 0.35-μm standard CMOS technology. The pseudo-differential topology with the common-mode feedforward bias extends the voltage swing of the input stage. The amplifier using the parallel gain booster, buffered Miller feedback, and feedforward frequency compensations exhibits high speed, high linearity, and fast settling with a small increase in circuit complexity and power consumption.

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