A 1.2V Fully Differential Amplifier with Buffered Reverse Nested Miller and Feedforward Compensations

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***Abstract*— This paper presents a low voltage CMOS fully differential operational amplifier. It comprises three gain stages with two compensation schemes, buffered reverse nested Miller compensation (B-RNMC) and feedforward transconductance compensation (FFTC). In B-RNMC, a transconductance stage is inserted in the feedback path to eliminate the right half plane (RHP) zero which may degrade phase margin. In FFTC, a feedforward transconductance helps to enhance output large signal response.**

Using standard 0.35-μm CMOS technology, measurement results demonstrate that DC gain greater than 90dB, gain-bandwidth product of 8.9MHz, and phase margin of 86° is achieved with 100pF output loads. The settling time for a 1.2V_{pp} step is 2.4μs. All the circuits dissipate 342μW under a single 1.2V power supply.

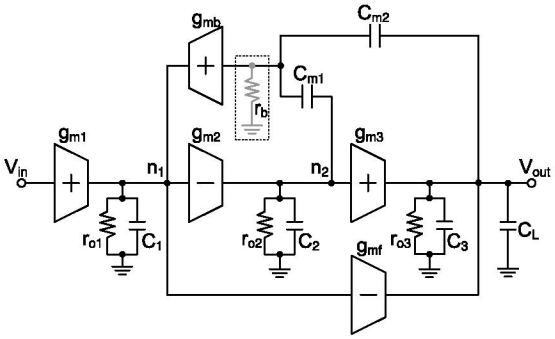

Fig. 1. Block diagram of the amplifier with B-RNMC and FFTC.

I. Introduction

An amplifier with large gain, high dynamic range, and wide bandwidth is indispensable in most analog circuits. As the technology scales down to deep submicron, supply voltage decreases with the same extent for reliability issue. Under low supply voltage, traditional approach of cascoding gain stage is not feasible. Therefore, more circuit designers are aware of the multi-stage amplifier design. Stability, however, becomes an important issue as a multi-stage amplifier induces more low frequency poles than a two-stage alternative does. Hence a multi-stage amplifier must be properly compensated to cancel or shift the nondominant poles and zeros to high frequency. Nested Miller compensation (NMC) is a well-known compensation technique for the multi-stage amplifier. It uses multiple feedback loops to assign each pole/zero location. Though NMC scheme provides good stability, it suffers from severe bandwidth reduction and large power dissipation, as mentioned in [1].

To overcome the limitations of NMC, especially when driving heavy capacitive loads, the reversed nested Miller compensation (RNMC) is proposed [2]. Compared to NMC, RNMC exhibits broader bandwidth as the inner compensation loop is not connected to the large capacitors at output. However, it still suffers from right half plane (RHP) zero that degrades the phase margin. To remove the RHP zero, several methods have been proposed [3] [4]. In this paper, the buffered reversed nested Miller compensation is used to extend the amplifier bandwidth. A buffer composed of a transconductance stage is connected in series with compensation capacitors. In addition, a parallel feedforward transconductance widely used in either zero location movement or slew rate enhancement is applied in this design to improve small and large signal performance.

This paper is organized as follows. The operating principle and the small-signal analysis of the proposed amplifier are discussed in Section II. Section III and Section IV show the detailed circuit implementation and measurement results, respectively. Finally a conclusion is given in Section V.

II. Circuit Architecture

The block diagram of the proposed topology is shown in Fig. 1. A conventional three stage amplifier consists of three transconductance stages g_{m1}-g_{m3}. Parameters r_{oi} and C_i (i=1-3) represent the output resistance and the lumped parasitic capacitance of ith stage. The feedforward stage, g_{mf}, along with g_{m3} forms the output push pull stage to improve the slew rate. A buffer stage g_{mb} is inserted between the common end of two Miller capacitors C_{m1} and C_{m2} and the output of the g_{m1} stage. It helps to break the feedthrough path from input to output. Thus the RHP zero is eliminated.

A. Transfer function

Before deriving the small-signal transfer function of the proposed amplifier, some assumptions are made for simplicity:

$$g_{m1}r_{o1}, g_{m2}r_{o2}, g_{m3}r_{o3} \gg 1$$
$$C_L, C_{m1}, C_{m2} \gg C_{1-3}.$$

The input impedance of the buffer stage is modeled as r_b, which can be presumed:

$$r_b = \frac{1}{g_{mb}}. \tag{1}$$

Neglecting second order terms, the open loop gain of the circuit shown in Fig. 1 is given by the following equation:

$$A(s) = -\frac{A_{dc}(1+\frac{s}{\omega_3}+\frac{s^2}{\omega_4})}{(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})} \tag{2}$$

where

$$A_{dc} = g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3} \tag{3}$$

$$\omega_1 = \frac{g_{m2}g_{m3}C_{m2}}{C_{m1}(g_{mf}C_{m2}+g_{m2}(C_{m2}+C_L))} \tag{4}$$

$$\omega_2 = \frac{g_{mb}r_{o1}(g_{mf}C_{m2}+g_{m2}(C_{m2}+C_L))}{C_{m2}C_L} \tag{5}$$

$$\omega_3 = \frac{g_{m2}g_{m3}g_{mb}}{g_{mf}g_{mb}C_{m1}+g_{m2}g_{m3}(C_{m1}+C_{m2})} \tag{6}$$

$$\omega_4 = \frac{g_{m2}g_{m3}g_{mb}}{(g_{m2}+g_{mf})C_{m1}C_{m2}}. \tag{7}$$

Due to Miller effect, C_{m2} is amplified by the last two gain stage. So the dominant pole is located at

$$\omega_{P1} \approx \frac{1}{r_{o1}A_2A_3C_{m2}} = \frac{1}{r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m2}}. \tag{8}$$

The gain-bandwidth product can be expressed as

$$\omega_0 = 2\pi \cdot GBW = A_{dc}\cdot\omega_{P1} = \frac{g_{m1}}{C_{m2}}. \tag{9}$$

Because the coefficients of s and s^2 in the numerator are both positive, two zeros are located at left half plane (LHP). Furthermore, the transconductance of last two stages, g_{m2} and g_{m3}, can be reduced since g_{mb} provides additional gain in feedback loops. Therefore, smaller power consumption is expectable.

Generally r_b is small. If the feedforward stage transconductance g_{mf} is neglected, the transfer function (2) can be simplified as

$$A(s) = -\frac{A_{dc}}{(1+\frac{s}{\omega_{P1}})[1+\frac{C_{m1}(C_{m2}+C_L)}{g_{m3}C_{m2}}s]}. \tag{10}$$

The phase margin is

$$PM \approx \tan^{-1}(\frac{g_{m3}}{g_{m1}}\frac{C_{m2}^2}{C_{m1}(C_{m2}+C_L)}). \tag{11}$$

Once C_{m2} is decided by the required unity gain bandwidth, and g_{m1}, g_{m3} and C_L are already known, the phase margin can be solely determined by selecting C_{m1} adequately [3].

B. System estimator

To estimate the system parameters efficiently, a tool based on Matlab is developed. The kernel of this tool is a symbolic analyzer [5]. According to Kirchhoff's voltage and current laws, the matrix between each node voltage and branch current is firstly constructed. Then the output to input symbolic transfer function can be solved with the assistance of Matlab routines. The symbolic analysis is much more precise than simplified equations from hand calculation. The main problem of the symbolic analysis is the computation complexity. For example, the transfer function of the proposed amplifier contains three poles and two zeros. Each coefficient contains a complicated combination of different component values. For ease of usage, we developed a user-friendly interface, as shown in Fig. 2. Designers can enter each parameter of the amplifier, then the frequency response, settling behavior, pole/zero locations and root locus come out in the main window. In addition, the performance difference can be easily observed by altering the parameters. With the aid of this tool, designers can estimate the system performance quickly and precisely.

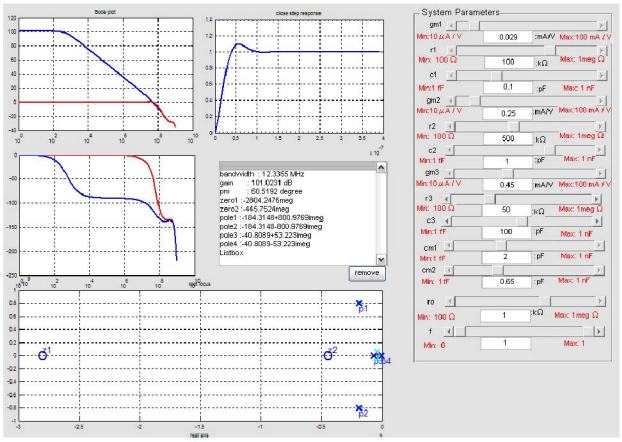

Fig. 2. System estimation platform.

III. Circuit Implementation

The schematic of the three stage fully differential amplifier is shown in Fig. 3. First stage composed of M_{11}-M_{16} is a classical folded cascode OTA, which has a wide input common mode range and large output impedance. A simple common source amplifier, M_{21} and M_{22}, is adopted as the second stage. To attain fast time domain response, a push pull output stage is accomplished by M_{31}-M_{34} to enhance slewing in both charging and sinking directions. The buffer stage g_{mb} comprising M_{c2} blocks the high frequency signal path from drain of M_{16} to output node through C_{m2}.

For a fully differential amplifier, a common mode feedback (CMFB) circuit is necessary to set up the common mode voltage of the two output nodes. To attain maximum output swing, the output voltage should be at the half of supply voltage, that is 0.6V in this work. Unfortunately, this voltage level is too small to turn on neither P nor N-type transistor of the technology we used. A current compared CMFB circuit, as depicted in Fig. 4, is used to solve this problem [6]. This topology transfers the output voltages to a common mode current by $2R$ resistors. The current is then compared with a reference current generated by V_{ocm} to produce the CMFB voltage V_{cmc}. V_{cmc} is connected to the gate of M_{14} to form

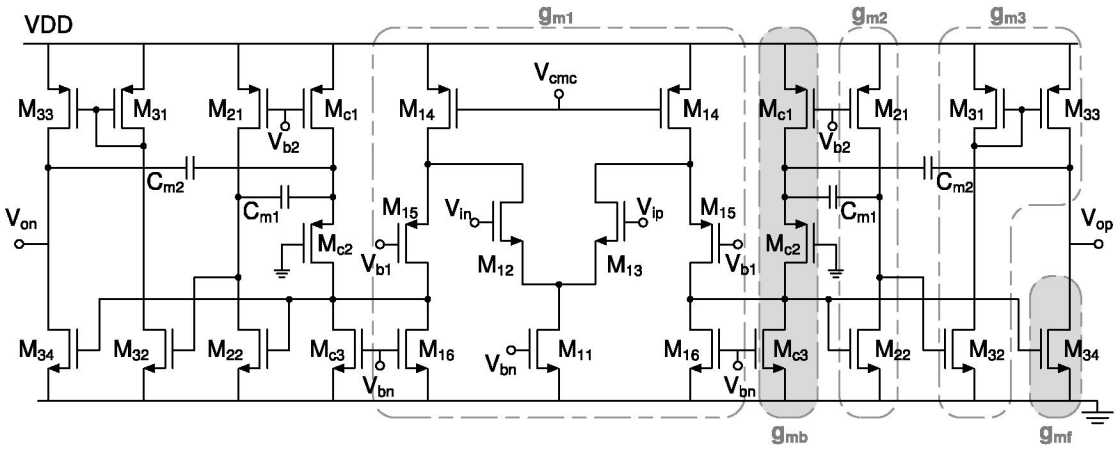

Fig. 3. Schematic of the proposed fully differential amplifier.

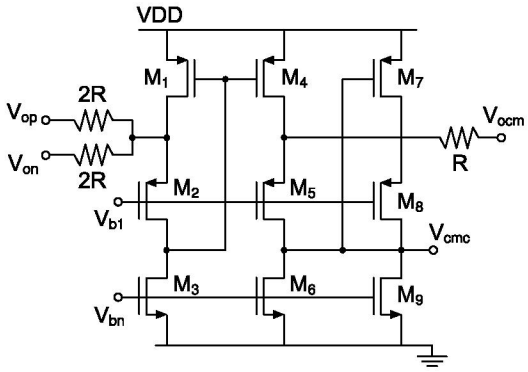

Fig. 4. Current compared CMFB circuit.

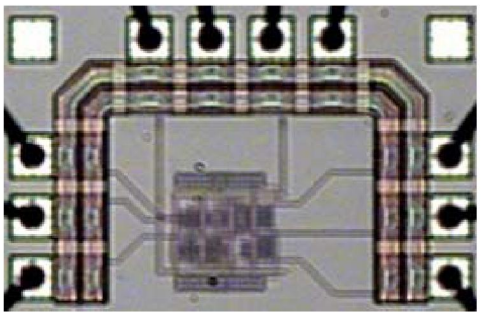

Fig. 5. Microphotograph of the test chip.

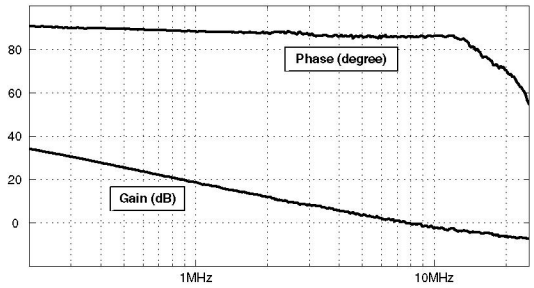

Fig. 6. Measured open loop ac response.

the feedback loop. The gain of this CMFB loop is decided by the current sensing resistor and the transconductance of M_7, which is $A_{CMFB} = (g_{m7} \cdot R)^{-1}$.

IV. Measurement Results

Fig. 5 shows the chip microphotograph. It uses 0.35-μm double poly four metal CMOS technology. Under a 1.2V supply and 100pF output capacitance loads, the open loop frequency response is shown in Fig. 6. The unity gain frequency is 8.9MHz and phase margin is 86°.

To maximize the signal swing, the input dc voltage is normally set at $V_{DD}/2$. However, this voltage level is not large enough to turn on any transistor in our case. As illustrated in Fig. 7, the low voltage bias scheme for close loop measurement is adopted to solve this problem [6]. Since input common mode voltage has to be greater than $V_{TN} + V_{DSsat,12} + V_{DSsat,11}$, operating points of V_{ip} and V_{in} are chosen as 0.75V. Two bias resistors R_b are connected to provide dc setup current required by R_i and R_f.

The measured transient response is shown in Fig. 8. Slew rate under a 1.2V step signal is 5.5V/μs and the settling time to 1% is 2.4μs. For a 100kHz 1V_{pp} input signal, HD_3 of this test chip is below -70dB. Total power dissipation is 342μW under a single 1.2V power supply. Table I summarizes the measurement results.

TABLE I
Measurement Results

C_L	100pF	A_{dc}	>90dB
GBW	8.9MHz	Phase Margin	86°
V_{dd}	1.2V	I_{dd}	0.285mA
Power	0.342mW	THD	<-70dB
Slew Rate	5.5V/μS	Settling Time	2.4μS

The summary of the performance of different amplifiers in the literature is given in Table II. The comparison between

TABLE II

PERFORMANCE COMPARISON OF DIFFERENT COMPENSATION TOPOLOGY

		C_L (pF)	Vdd (V)	Idd (mA)	Power (mW)	GBW (MHz)	SR (V/μs)	FOM_S ($\frac{GBW \cdot C_L}{Power}$)	FOM_L ($\frac{SR \cdot C_L}{Power}$)
NMC	[1]	100	8.0	9.5	76	60	20	79	26
RNMCR	[4]	15	3.0	0.467	1.4	19.46	11.1	209	119
GFPC	[7]	300	3.0	0.817	2.45	10.4	3.5	1273	469
AFFC	[8]	120	2.0	0.20	0.40	4.5	1.49	1350	447
DLPC	[9]	120	1.5	0.22	0.33	7.0	3.3	2545	1200
ACBC	[10]	500	2.0	0.162	0.324	1.90	1.0	2932	1543
TCFC	[11]	150	1.5	0.03	0.045	2.85	1.03	9500	3450
This Work		100	1.2	0.130*	0.156*	8.9	5.5	5705	3526

* equivalent case as all the amplifiers are with single ended output.

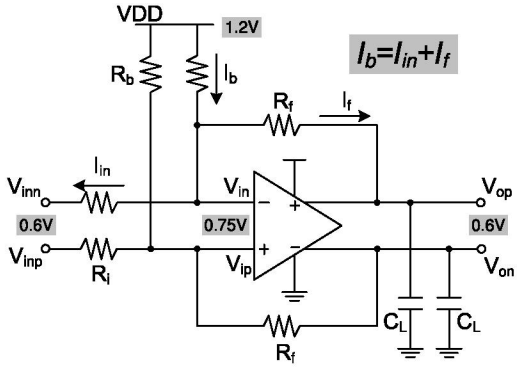

Fig. 7. Close loop bias scheme.

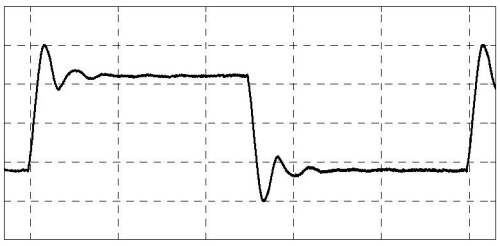

Fig. 8. Measured pulse response for large input signal.(Xdiv:2μS. Ydiv:0.5V)

different compensation topologies is based on two figures of merits, FOM_S and FOM_L [11]. To make fair comparisons, current and power consumption of our work are reconfigured as the single-ended case. Our work exhibits competitive performance in both small-signal bandwidth and large-signal slew rate.

V. CONCLUSION

In this paper, a parallel of buffered reverse nested Miller and feedforward transconductance compensations is introduced. Based on this topology, a 1.2V CMOS fully differential amplifier, including a current compared common mode feedback circuit, has been successfully verified with silicon. Apart from that, a symbolic estimator with a user-friendly interface is developed to precisely analyze high order system. This work exhibits remarkable performance either in small signal bandwidth or large signal behavior compared with other compensation topologies.

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