Transconductance With Capacitances Feedback Compensation for Multistage Amplifiers

Xiaohong Peng and Willy Sansen, *Fellow, IEEE*

***Abstract*—A new performance-boosting frequency compensation technique is presented, named Transconductance with Capacitances Feedback Compensation (TCFC). A transconductance stage and two capacitors introduce negative feedback to a three-stage amplifier, which significantly improves the performance such as gain-bandwidth product, slew rate, stability and sensitivity.**

An optimized TCFC amplifier has been implemented, and fabricated in a 0.35-μm CMOS process. The TCFC amplifier driving a 150-pF load capacitor achieved 2.9-MHz gain-bandwidth product dissipating only 45-μW power with a 1.5 V supply, which shows a significant improvement in MHz $\cdot$ pF/mA performance.

***Index Terms*—Amplifier, compensation, low power, multistage.**

I. Introduction

As the supply voltage continues to scale down, multistage amplifiers are becoming more and more essential. The methodologies to design multistage amplifiers are much in demand. Due to the complexity of a multistage amplifier, the stabilization is difficult to achieve. A special frequency compensation measure must be taken to ensure stability. For this purpose, some frequency-compensation topologies such as Nested Miller Compensation (NMC) [1] have been used to implement multistage amplifiers. In these amplifiers, although the stability problem has been basically solved, the enormous power dissipation and bandwidth reduction remain a serious problem. In order to minimize the power-consuming effect of the Miller capacitances on multistage amplifiers, a new topology, Transconductance with Capacitances Feedback Compensation (TCFC) is presented in this paper. As demonstrated later, a transconductance stage and two capacitors are added to introduce negative feedback to a three-stage amplifier achieving stability, such that the power dissipation is considerably reduced while the frequency characteristics and transient response are improved significantly.

II. Review of Nested Miller Compensation

In the three-stage NMC topology, there are two Miller capacitors C_{m1} and C_{m2} connected from the output to the output of each stage, respectively, forming two negative feedback loops. They stabilize the amplifier but seriously reduce the high-frequency gain. As a result, extra power is needed to compensate this gain reduction. Moreover, the Miller capacitor C_{m2} that shorts the last stage gives the additional disadvantages that the phase shift reaches 180° as frequency increases, leading to a positive-feedback loop involving C_{m1}, g_{m2}, and C_{m2}, which is a serious source of instability. Therefore, the transconductance g_{m3} must be large enough to counter this shorting effect. To ensure stability, the last-stage transconductance g_{m3} required in a three-stage NMC amplifier is given by

$$g_{m3} \geq 4\,(2\pi\,\mathrm{GBW})C_L. \tag{1}$$

Apparently, in a NMC amplifier, the required transconductance for the last stage alone is four times the transconductance for a single-stage amplifier. It is thus not suited for low-power applications. Obviously, this power-consuming effect is mainly caused by the inner Miller capacitor C_{m2}. The first Miller capacitor C_{m1} causes the slope to be -20 dB per decade in frequency, as in any amplifier. Hence, it is the second Miller capacitor C_{m2} which causes an unnecessary reduction in high-frequency gain such that a large transconductance g_{m3} is needed for the last stage.

In some topologies such as NGRNMC [2], a nulling resistor is added to ease the high-frequency-gain reduction and the shorting effect on the last stage caused by the inner Miller capacitor. However, the performance improvement is not sufficient since the nulling resistance has to be kept small enough to keep the Miller capacitance to be effective for pole splitting.

Based on these considerations, it becomes clear that taking away the inner Miller capacitor C_{m2} could be a possible way to achieving better performance. However in this case the first nondominant pole would be determined by parasitic capacitances, resulting in layout-sensitive circuits. Moreover, a safe gain margin would not be ensured due to the effects of the zeros caused by the parasitic capacitances. Besides, since the second-stage dc gain A_{v2} appears in the expression of the first nondominant pole as a multiplier to other parameters, the sensitivity must be high.

For sake of comparison, the case that the inner Miller capacitor is excluded from the three-stage NMC topology is discussed first and presented in the next section.

III. Unique Miller Compensation

The case that the inner Miller capacitor is excluded from the three-stage NMC topology is referred to as Unique Miller Compensation (UMC), which is shown in Fig. 1.

In Fig. 1, g_{m1-3} and R_{1-3} represent the transconductance and output resistance of each stage, respectively. C_{1-3} symbolize the lumped parasitic capacitance of each stage. C_{m1} is the unique Miller capacitor, accomplishing the frequency compensation. C_L is the load capacitor.

Manuscript received November 1, 2004; revised January 27, 2005.

The authors are with the ESAT-MICAS, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium (e-mail: willy.sansen@esat.kuleuven.ac.be).

Digital Object Identifier 10.1109/JSSC.2005.847216

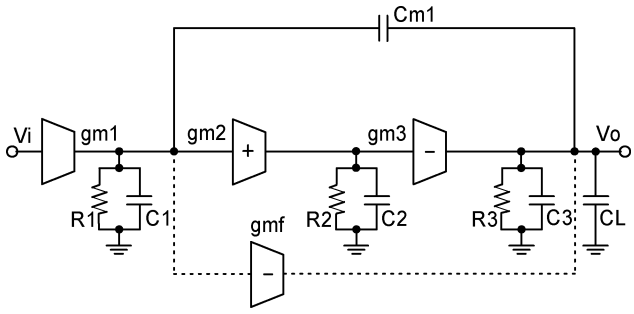


Fig. 1. Unique Miller compensation (UMC) topology.

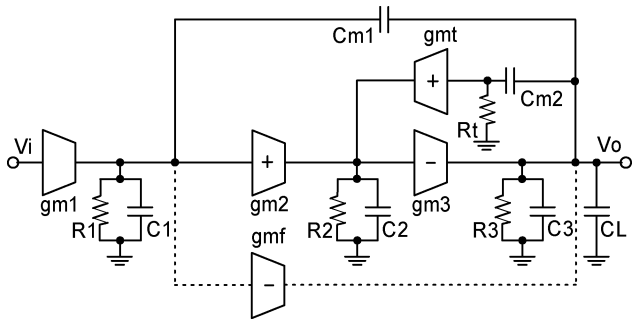


Fig. 2. TCFC topology.

The small-signal transfer function of the open-loop gain of the UMC amplifier is given by

$$A_v(s) = \frac{A_{dc}\left(1+\frac{s}{\omega_3}+\frac{s^2}{\omega_3\omega_4}\right)}{\left(1+\frac{s}{|p_{-3\mathrm{dB}}|}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}\right)}. \tag{2}$$

where A_{dc} and $p_{-3\mathrm{dB}}$ are the dc gain and the dominant pole, respectively, which are given as

$$A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \tag{3}$$

$$p_{-3\mathrm{dB}} = -\frac{1}{g_{m2}g_{m3}R_1R_2R_3C_{m1}}. \tag{4}$$

Another important frequency factor ω_0, which represents the gain-bandwidth product (GBW), is given by

$$\omega_0 = 2\pi\,\mathrm{GBW} = A_{dc}|p_{-3\mathrm{dB}}| = \frac{g_{m1}}{C_m}. \tag{5}$$

ω_{1-2} and ω_{2-3} are the frequency factors in the denominator and the numerator of (2) respectively. They are given by

$$\omega_1 = A_{v2}\frac{g_{m3}}{C_L} \tag{6}$$

$$\omega_2 = \frac{1}{R_2C_2} \tag{7}$$

$$\omega_3 = -A_{v2}\frac{g_{m3}}{C_m} \tag{8}$$

$$\omega_4 = \frac{1}{R_2C_2}. \tag{9}$$

in which A_{v2} $(= g_{m2}R_2)$ is the gain of the second stage.

Although C_2 is a lumped parasitic capacitance, the frequency factor ω_2 cannot be kept high since the second-stage output resistance R_2 is large with regard to the other small equivalent resistance $1/g_m$. Consequently, this results in a complex-pole arrangement for the nondominant poles. In this case, both the frequency factors ω_1 and ω_2 determine the location of the first nondominant pole. Therefore, in the unity-feedback configuration, to ensure a third-order Butterworth frequency response with the damping ratio $\zeta = (1/2Q) = 0.707$, the stability conditions are given by

$$\omega_0 = 2\pi\mathrm{GBW} = \frac{1}{2}\omega_1 = \frac{1}{2}A_{v2}\frac{g_{m3}}{C_L} = \frac{1}{4}\omega_2 = \frac{1}{4}\frac{1}{R_2C_2}. \tag{10}$$

Clearly, the stability conditions given in (10) are hard to maintain, since both A_{v2} and R_2 cannot be accurately specified. They are greatly dependent on the operating points of the relevant transistors. Moreover, the lumped parasitic capacitance C_2, which is also imprecise, can inevitably lead to vulnerable layout-dependent circuits. In conclusion, with the three imprecise values: A_{v2}, R_2, and C_2, the stability condition (10) cannot be reliably ensured in practical implementations.

Even if the feed-forward stage g_{mf}, as shown by dotted lines in Fig. 1, is taken into account, the effects of the imprecise parameters are still in existence. As such the problem remains unsolved.

Therefore, other topologies have to be devised. The NMC has accomplished this by employing another Miller capacitor C_{m2}. However, due to the loading and shorting impact of the inner Miller capacitor, the high-frequency gain and the gain-bandwidth product are badly reduced. Although the use of the nulling resistor can ease this impact, the performance improvement is still limited since the nulling resistance cannot be too large to keep the Miller capacitance effective.

In order to further supplement the techniques on implementing low-power multistage amplifiers and further overcome the disadvantages of the sensitivity and the stability uncertainty as well as the operation unreliability due to the imprecise parameters in designing multistage amplifiers, the new topology, TCFC, is proposed and described in the next section

IV. Transconductance With Capacitances Feedback Compensation

A. Topology

The three-stage TCFC topology, using transconductance with capacitance feedback as a compensation technique, is shown in Fig. 2.

The transconductance stages g_{m1}, g_{m2} and g_{m3} compose the conventional three-stage amplifier. The output resistance and the lumped parasitic capacitance of each stage are represented by R_{1-3} and C_{1-3}, respectively. C_L is a load capacitor.

C_{m1} is the Miller capacitor forming the outer feedback loop. Capacitance C_{m2} along with the transconductance stage g_{mt} makes up the internal feedback loop. As C_{m2} is separated from the internal node by the transconductance stage g_{mt}, the high-frequency shorting effect on the last stage is avoided. Therefore, positive-feedback phenomena cannot be present and the stability can be well ensured even with a small transconductance in the last stage. Moreover, since only parasitic capacitances are connected to the internal node, the second-stage high-frequency gain reduction is minimized. Furthermore, the param-

eters of the feedback loop involving g_{mt} and C_{m2} can be adequately adapted, as a consequence, a suitable gain reduction above the unity-gain frequency is generated, achieving a sufficient gain margin. In this way, the effects of the parasitic device parameters are eliminated due to the negative feedback, minimizing the sensitivity and dependability to device parameters and layout variability.

To improve the large-signal performance such as slew rate, a feed-forward stage g_{mf}, with which the last stage constitutes a push-pull output stage, is easily included in the TCFC topology as shown by the dotted lines in Fig. 2.

B. Transfer Function

The small-signal transfer function of the open-loop gain of the TCFC amplifier shown in Fig. 2 can be obtained by means of analyzing its equivalent small-signal circuit.

For simplification, we assume that the dc gain and the output resistance of each stage are large enough, all the compensating capacitances are much larger than the relevant parasitic capacitances and far smaller than the load capacitance, as given by

$$g_{m1}R_1,\ g_{m2}R_2,\ g_{m3}R_3 \gg 1 \tag{11}$$

$$C_{m1} \gg C_1,\ C_{m2} \gg C_2 \tag{12}$$

$$C_{m1},\ C_{m2} \ll C_L. \tag{13}$$

Also, for simplicity, the following relation is presumed:

$$R_t = \frac{1}{g_{mt}}. \tag{14}$$

Thus, the small-signal transfer function of the open-loop gain of the TCFC amplifier can then be expressed by a fourth-order expression which is given by

$$A_v(s) = \frac{A_{dc}\left(1+\frac{s}{\omega_4}+\frac{s^2}{\omega_4\omega_5}+\frac{s^3}{\omega_4\omega_5\omega_6}\right)}{\left(1+\frac{s}{|p_{-3\mathrm{dB}}|}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}+\frac{s^3}{\omega_1\omega_2\omega_3}\right)}. \tag{15}$$

In (15), all the symbols are defined by (16)–(24) and explained afterwards.

$$A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \tag{16}$$

$$p_{-3\mathrm{dB}} = -\frac{1}{C_{m1}g_{m2}g_{m3}R_1R_2R_3} \tag{17}$$

$$\omega_1 = \frac{1}{1+k_t}\frac{g_{m2}}{C_{m2}} \tag{18}$$

$$\omega_2 = (1+k_t)\frac{C_{m2}}{C_2}\frac{g_{m3}}{C_L} \tag{19}$$

$$\omega_3 = \frac{1}{k_t}\frac{g_{m2}}{C_{m2}} \tag{20}$$

$$\omega_4 = \frac{1}{k_t}\frac{g_{m2}}{C_{m2}} \tag{21}$$

$$\omega_5 = -k_t\frac{C_{m2}}{C_2}\frac{g_{m3}}{g_{m1}}\omega_0 \tag{22}$$

$$\omega_6 = \frac{1}{k_t}\frac{g_{m2}}{C_{m2}} \tag{23}$$

$$k_t = \frac{g_{m2}}{g_{mt}}. \tag{24}$$

A_{dc} is the low-frequency gain. $p_{-3\mathrm{dB}}$ is the dominant pole. ω_{1-3} and ω_{4-6} represent frequency factors in the denominator and numerator of (15), respectively. Finally, k_t is a transconductance ratio of the second stage g_{m2} to the feedback stage g_{mt}. In this design, its value is 2.

In (22), ω_0 is another important frequency factor, which represents the gain-bandwidth product and is given by

$$\omega_0 = 2\pi\,\mathrm{GBW} = A_{dc}|p_{-3\mathrm{dB}}| = \frac{g_{m1}}{C_m}. \tag{25}$$

C. Stability and Gain-Bandwidth Product

The stability is studied on the closed-loop transfer function in the unity-gain feedback configuration, which can be given by (26) after neglecting the zeros. In fact, there is one effective left half plane (LHP) zero since C_m is much smaller than C_L. Moreover, as the order of the numerator of $A_{\mathrm{cl}}(s)$ is less than that of the denominator, the stability depends on the denominator [10].

$$A_{\mathrm{cl}}(s) = \frac{1}{1+\frac{s}{\omega_0}+\frac{s^2}{\omega_0\omega_1}+\frac{s^3}{\omega_0\omega_1\omega_2}+\frac{s^4}{\omega_0\omega_1\omega_2\omega_3}}. \tag{26}$$

By applying Routh stability criterion, the stability conditions can be obtained as

$$\omega_3 = \frac{1}{k_t}\frac{g_{m2}}{C_{m2}} > \omega_1 = \frac{1}{1+k_t}\frac{g_{m2}}{C_{m2}} \tag{27}$$

$$\omega_0 = 2\pi\,\mathrm{GBW} < \frac{C_{m2}}{C_2}\frac{g_{m3}}{C_L}. \tag{28}$$

Obviously, the condition (27) is always satisfied when $k_t > 0$. Remember that k_t is the transconductance ratio of g_{m2} to g_{mt}, which is always a positive value. Therefore, the other condition (28) becomes the key limitation of the gain-bandwidth product. According to (28), for a specific transconductance g_{m3} driving a given load capacitance C_L, the achievable gain-bandwidth product GBW depends on the ratio C_{m2}/C_2. Obviously, this ratio can be made large, since C_2 is a lumped parasitic capacitance which is rather small compared with the compensation capacitance C_{m2}. Hence, this proves theoretically that the gain-bandwidth product of the TCFC amplifier can be extended significantly with respect to that of the NMC amplifier.

D. Design Constraints

The design constraints are usually dependent on the pole-zero locations of the open-loop small-signal transfer function. In order to optimize the gain-bandwidth product as well as the phase margin, it is important to arrange properly the pole-zero locations.

Since the ratio C_{m2}/C_2 can be made large, it can be supposed that ω_2 is sufficiently higher than ω_1, as given by

$$\omega_1 = \frac{1}{1+k_t}\frac{g_{m2}}{C_{m2}} \ll \omega_2 = (1+k_t)\frac{C_{m2}}{C_2}\frac{g_{m3}}{C_L}. \tag{29}$$

Thus, the first nondominant pole is determined by ω_1, which is given by

$$p_{nd1} = -\omega_1 = -\frac{1}{1+k_t}\frac{g_{m2}}{C_{m2}}. \tag{30}$$

The first nondominant pole given in (30) is obviously independent of imprecise parasitic capacitances. Moreover, since the other nondominant poles are far higher than the first nondominant pole, their effects on phase margin are insignificant. In a similar way, the zeros can be determined as well. Since the ratio C_{m2}/C_2 is large and g_{m3} is usually larger than g_{m1}, the frequency factor ω_5 is much larger than ω_0 or $2\pi\mathrm{GBW}$. The following condition can thus be well satisfied:

$$\omega_4 = \frac{1}{k_t}\,\frac{g_{m2}}{C_{m2}} \ll |\omega_5| = k_t\,\frac{C_{m2}}{C_2}\,\frac{g_{m3}}{g_{m1}}\,\omega_0. \tag{31}$$

Due to the very large frequency factor ω_5, two zeros only show up at very high frequencies. As a consequence, only one LHP zero is left, which is given by

$$z_{\mathrm{LHP1}} \approx -\omega_4 = -\frac{1}{k_t}\,\frac{g_{m2}}{C_{m2}} = \frac{1+k_t}{k_t}\,p_{nd1}. \tag{32}$$

According to (32), the LHP zero z_{LHP1} which improves the phase margin, is obviously located higher than the first nondominant pole. This leads to the desired open-loop frequency response and does not deteriorate the gain margin.

Based on these considerations, the overall phase margin can be given by

$$\mathrm{PM} \approx 90^\circ - \arctan\frac{2\pi\,\mathrm{GBW}}{|p_{nd1}|} + \arctan\frac{2\pi\,\mathrm{GBW}}{|z_{\mathrm{LHP1}}|}. \tag{33}$$

A similar compensation scheme has been used before on two-stage amplifiers [13]. It does not provide the same precise positioning of the LHP zero, however.

E. Finite Output Resistance

In practice, the output resistances of each stage are not infinitely high. In the TCFC amplifier, the finite output resistance R_2 may affect the high-frequency behavior. The influence of this finite output resistance R_2 is considered next.

First, the frequency factors ω_{1-3} that determine the nondominant poles are examined, which are given by

$$\omega_1 \approx \frac{1}{1+k_t+\frac{1}{A_{v2}}\,\frac{C_L}{C_{m2}}}\,\frac{g_{m2}}{C_{m2}} \tag{34}$$

$$\omega_2 \approx \frac{1+k_t+\frac{1}{A_{v2}}\,\frac{C_L}{C_{m2}}}{1+\frac{k_t}{A_{v2}}\,\frac{C_{m2}}{C_2}}\,\frac{C_{m2}}{C_2}\,\frac{g_{m3}}{C_L} \tag{35}$$

$$\omega_3 \approx \frac{1}{k_t}\,\frac{g_{m2}}{C_{m2}} + \frac{1}{R_2C_2}. \tag{36}$$

Herein, A_{v2} is the second-stage low frequency gain, which is given by

$$A_{v2} = g_{m2}R_2. \tag{37}$$

Comparing these frequency factors ω_{1-3} with those given in (18) – (20), it is seen that ω_3 tends to shift upwards while ω_1 which determines the first nondominant pole goes downwards. The frequency factor ω_2 may also move downwards but not as far as ω_1 does. This means that the nondominant poles are separated even further compared to the case of the infinite second-stage output resistance R_2 discussed before. Consequently, the stability condition $\omega_3 > \omega_1$ is satisfied more sufficiently. Moreover, the assumption $\omega_2 \gg \omega_1$, which is supposed to minimize the sensitivity, can still be well ensured.

In a similar way, the frequency factors ω_{4-6} which determine the zeros are examined and given by

$$\omega_4 \approx \frac{1}{k_t-\frac{1}{A_{v2}}\,\frac{C_{m1}}{C_{m2}}}\,\frac{g_{m2}}{C_{m2}} \tag{38}$$

$$\omega_5 \approx \frac{\frac{1}{A_{v2}}\,\frac{C_{m1}}{C_{m2}}-k_t}{1+\frac{k_t}{A_{v2}}\,\frac{C_{m2}}{C_2}}\,\frac{C_{m2}}{C_2}\,\frac{g_{m3}}{g_{m1}}\,2\pi\mathrm{GBW} \tag{39}$$

$$\omega_6 \approx \frac{1+\frac{k_t}{A_{v2}}\,\frac{C_{m2}}{C_2}}{k_t}\,\frac{g_{m2}}{C_{m2}}. \tag{40}$$

Apparently, the frequency factor ω_4 is larger than ω_1. The first LHP zero z_{LHP1} is thus located higher than the first nondominant pole p_{nd1}. This is desired and is the same case as discussed in the case of infinite second-stage output resistance R_2.

It can also be proven that the other zeros are still located high enough to be neglected, since $|\omega_5|$ is much larger than $2\pi\mathrm{GBW}$. Moreover, the geometric average of the frequency factor ω_5 and ω_6 is in fact little changed, which is given by

$$\begin{aligned}\sqrt{|\,\omega_5\,\omega_6|} &\approx \sqrt{\frac{k_t-\frac{1}{A_{v2}}\,\frac{C_{m1}}{C_{m2}}}{k_t}\,\frac{g_{m2}}{C_2}\,\frac{g_{m3}}{g_{m1}}\,2\pi\mathrm{GBW}}\\ &\approx \sqrt{\frac{g_{m2}}{C_2}\,\frac{g_{m3}}{g_{m1}}\,2\pi\mathrm{GBW}}.\end{aligned} \tag{41}$$

The geometric average of the frequency factor ω_5 and ω_6 is definitely far above the unity-gain frequency, since $g_{m3} > g_{m1}$ and $g_{m2}/C_2 \gg 2\pi\mathrm{GBW}$ can be readily satisfied.

Thus, it has been shown that the stability can still be well ensured in the case of a finite output resistance R_2 of the second stage of the TCFC amplifier.

F. Slew Rate

Like most multistage amplifiers, the overall slew rate of the TCFC amplifier is limited by the slowest stage in the amplifier.

For the second stage of the TCFC amplifier, the capacitance load is the lumped parasitic capacitance C_2, which is much smaller than the compensating capacitances C_{m1} and the load capacitance C_L. Therefore, the overall slew rate is determined by the first stage which needs to drive the capacitance C_{m1} or the last stage which has to drive the capacitances C_L, C_{m1} and C_{m2}.

Since the load capacitance is much larger than the other capacitances, the overall slew rate of the TCFC amplifier can be simplified as in

$$\mathrm{SR} = \min\left(\frac{I_1}{C_{m1}}, \frac{I_3}{C_L}\right) \tag{42}$$

where I_1 and I_3 represent the currents in the first stage and the last stage, respectively.

Because the load capacitance C_L is much larger than the outer Miller capacitance C_{m1}, the second term in (42) tends to be the main limitation of the overall slew rate especially for low-power applications. Nonetheless, this limitation can be overcome by addition of a feed-forward stage g_{mf} as shown in Fig. 2. In

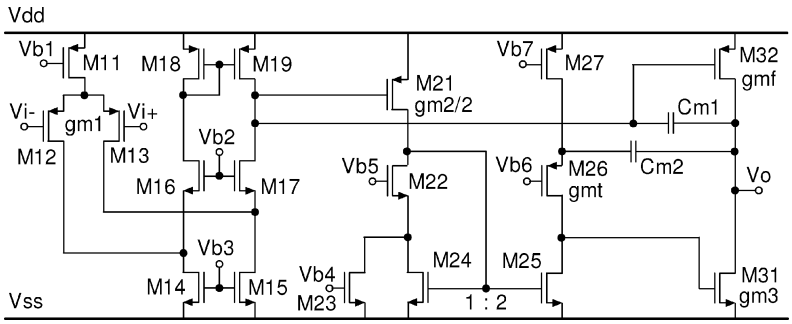


Fig. 3. Schematic of the TCFC amplifier.

TABLE I
PARAMETERS OF THE TCFC AMPLIFIER

g_{m1} = 24 μS	g_{m2} = 128 μS	g_{m3} = 128μS
	g_{mt} = 64 μS	g_{mf} = 128 μS
C_{m1} = 1.1 pF	C_{m2} = 0.92 pF	off-chip C_L = 150 pF

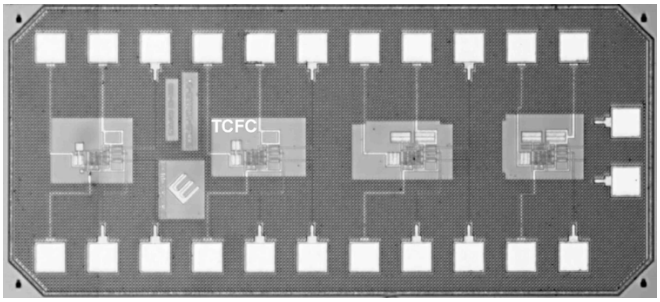


Fig. 4. Microphotograph of the implemented TCFC amplifier.

this case, the last stage forms a push-pull output stage which slews fast in both directions. Therefore, the first stage driving the Miller capacitance becomes the dominant limitation of the overall slew rate (SR), which can also be given and further derived as

$$\mathrm{SR} = \frac{I_1}{C_m} \propto \frac{g_{m1}}{C_m}(V_{GS1} - V_{T1}) = 2\pi\,\mathrm{GBW}(V_{GS1} - V_{T1}). \tag{43}$$

It can be seen that the overall slew rate is proportional to the gain-bandwidth product. As GBW is being improved, simultaneously the overall slew rate is being extended accordingly. It can thereby be concluded that for the TCFC amplifier with the feed-forward stage g_{mf}, increasing the gain-bandwidth product leads to a corresponding improvement of the slew rate.

V. IMPLEMENTATION

The schematic of the implemented three-stage TCFC amplifier is shown in Fig. 3.

The first stage is a classical folded cascode OTA. It consists of transistors M11–M19, which ensure that the common mode input range can reach the lower rail voltage V_{SS}. The differential pair M11 and M12 generates the transconductance g_{m1}.

The transistor M21 provides half the second-stage transconductance g_{m2}, which is doubled by the transistor M25 via the current mirror composed by M24 and M25.

TABLE II
MEASURED RESULTS OF THE TCFC AMPLIFIER

C_L	150pF	A_{dc}	>100dB
GBW	2.85MHz	Phase Margin	58.6°
Power	0.045mW	Gain Margin	22dB
V_{dd}	1.5V	I_{dd}	0.03mA
SR $_{+/-}$	0.96/1.11 V/μS	TS $_{+/-}$ (to 1%)	2.8/1.7 μS

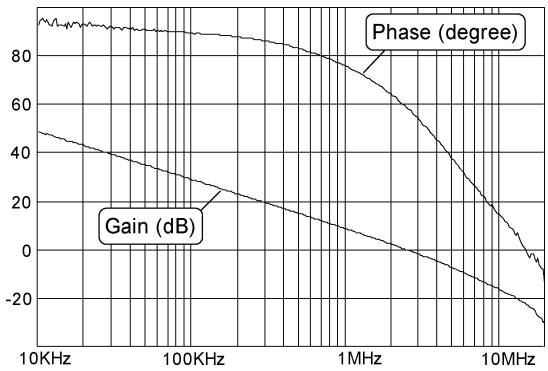


Fig. 5. Measured open-loop gain-frequency responses.

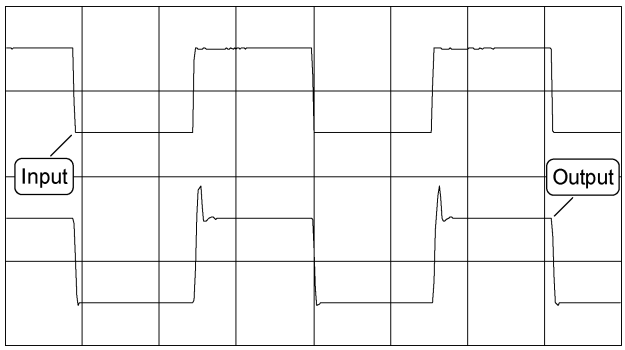


Fig. 6. Measured transient response (Xdiv: 10 μS, Ydiv: 0.5 V).

The feedback transconductance g_{mt} is generated by the transistor M26, which also acts as a cascoding stage in the second stage. Obviously, with this configuration, the benefits are that the output resistance of the second stage shunted by r_{o25} is increased and the overall dc gain is boosted while no extra power is needed for implementing the feedback transconductance g_{mt}.

TABLE III
PERFORMANCE COMPARISON OF DIFFERENT AMPLIFIERS

		A_{dc} dB	C_L pF	V_{dd} V	I_{dd} mA	Power mW	GBW MHz	SR $V/\mu S$	FOM_S $\frac{MHz\cdot pF}{mW}$	FOM_L $\frac{V/\mu S\cdot pF}{mW}$	$IFOM_S$ $\frac{MHz\cdot pF}{mA}$	$IFOM_L$ $\frac{V/\mu S\cdot pF}{mA}$
NMC	[3]	100	100	8.0	9.50	76	60	20	79	26	632	211
MNMC	[3]	100	100	8.0	9.50	76	100	35	132	46	1053	368
NGCC	[4]	100	20	2.0	0.34	0.68	0.61	2.5	18	74	36	148
NCFF	[5]	90	12	2.5	5.6	14	250	-	214	-	535	-
NMCFNR	[6]	>100	100	2.0	0.20	0.406	1.8	0.79	443	195	886	390
ETC	[7]	102	40	3.0	2.30	6.90	47	69	272	400	817	1200
DFCFC	[8]	>100	100	2.0	0.21	0.42	2.6	1.32	619	314	1238	629
PFC	[9]	>100	130	1.5	0.19	0.275	2.7	1.0	1276	473	1915	709
AFFC	[10]	>100	120	2.0	0.20	0.40	4.5	1.49	1350	447	2700	894
DLPC	[11]	>100	120	1.5	0.22	0.33	7.0	3.3	2545	1200	3818	1800
$ACBC_F$	[12]	>100	500	2.0	0.162	0.324	1.90	1.0	2932	1543	5864	3086
TCFC	this work	>100	150	1.5	0.03	0.045	2.85	1.035	9500	3450	14250	5175

In order to minimize the lumped parasitic capacitance C_2, the last-stage transconductance g_{m3} is realized with a nMOS transistor M31, while the transistor M32 acts as the feed-forward transconductance stage g_{mf}.

C_{m1} is the Miller capacitor establishing the outer feedback loop. C_{m2} is the other feedback capacitor which along with the feedback transconductance g_{mt} accomplishing the internal feedback loop. C_L is an off-chip load capacitor.

The circuit parameters of the implemented TCFC amplifier are given in Table I.

The TCFC amplifier was fabricated in a 0.35-μm CMOS process. A microphotograph of the implemented amplifiers is shown in Fig. 4. The active area for a TCFC amplifier is smaller than 0.02 mm^2.

VI. EXPERIMENTAL RESULTS

A. Measured Results

The implemented TCFC amplifier was measured for both dc and ac specifications. The measured results, which are obtained using an HP3577A network analyzer and a Tektronix TDS680B oscilloscope, are summarized in Table II. The frequency characteristic and the transient response are shown in Figs. 5 and 6, respectively. It can be seen that a sufficient gain margin 22 dB is obtained due to the use of the specific compensation strategy.

B. Performance Comparison

To quantitatively evaluate different amplifiers, usually two formulas are used as given by

$$\mathrm{FOM_S} = \frac{\mathrm{GBW}\cdot C_L}{\mathrm{power}} \tag{44}$$

$$\mathrm{FOM}_L = \frac{\mathrm{SR}\cdot C_L}{\mathrm{power}}. \tag{45}$$

However, as both the GBW and SR depend on the currents flown in the relevant transistors rather than the power itself, It is more reasonable to use two other formulas defined by

$$\mathrm{IFOM_S} = \frac{\mathrm{GBW}\cdot C_L}{\mathrm{I_{dd}}} \tag{46}$$

$$\mathrm{IFOM}_L = \frac{\mathrm{SR}\cdot C_L}{\mathrm{I_{dd}}}. \tag{47}$$

The comparison results of applying these formulas on the different amplifiers are given in Table III. Obviously, the TCFC amplifier shows the most outstanding performance.

VII. CONCLUSION

A new frequency compensation topology, Transconductance with Capacitances Feedback Compensation topology for multistage amplifiers, has been presented and proven to be well suited for low-voltage low-power applications. It has been shown that by adequate application of negative feedback, the stability can be well ensured while the high-frequency behavior is not degraded. As demonstrated, the remarkable improvements for both small- and large-signal performance have been accomplished in an optimized low-power three-stage TCFC amplifier powered by low-voltage supplies.

REFERENCES

[1] J. H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output stages," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1144–1150, Dec. 1985.

[2] X. Peng and W. Sansen, "Nested feed-forward gm-stage and nulling resistor plus nested-Miller compensation for multistage amplifiers," in *Proc. IEEE Custom Integrated Circuits Conf.*, Orlando, FL, May 2002, pp. 329–332.

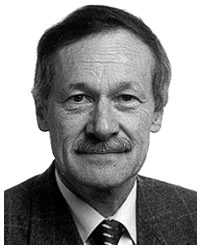
[3] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.

[4] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[5] B. K. Thandri and J. Silva-Martínez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.
[6] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low-power CMOS design," *IEEE Trans. Circuits Syst. II: Analog Digital. Signal Process.*, vol. 48, no. 4, pp. 388–394, Apr. 2001.
[7] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 339–347, Mar. 1999.
[8] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.
[9] J. Ramos, X. Peng, M. Steyaert, and W. Sansen, "Three stage amplifier frequency compensation," in *Proc. Eur. Solid-State Circuits Conf.*, Lisbon, Portugal, Sep. 2003, pp. 365–368.
[10] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.
[11] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extention amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.
[12] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2074–2079, Nov. 2004.
[13] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.

Xiaohong Peng was born in Henan, China, in 1962. He received the B.S. degree in electronics from the Xidian University (originally North-west Institute of Telecommunication Engineering), China, in 1982. The subject of his thesis was the generation of radar noise. In 1985, he received the M.S. degree in electronics from the Beijing University of Aeronautics and Astronautics, China. The subject of his M.S. thesis was microprocessor in-circuit emulation. In November 2004 he received the Ph.D. degree on the design of multistage amplifiers, from the Katholieke Universiteit Leuven, Belgium.

He is a Research Assistant at the ESAT-MICAS, Katholieke Universiteit Leuven.



Willy Sansen (S'66–M'72–SM'86–F'95) has received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven in 1967 and the Ph.D. degree in electronics from the University of California at Berkeley in 1972.

In 1972, he was appointed by the National Fund of Scientific Research (Belgium) at the ESAT Laboratory of the K.U.Leuven, where he has been a Full Professor since 1980. During 1984–1990, he was the head of the Electrical Engineering Department. Since 1984, he has headed the ESAT-MICAS Laboratory on analog design, which counts about 60 members and which is mainly active in research projects with industry. He is a member of several boards of directors. In 1978, he was a Visiting Professor at Stanford University, in 1981 at the EPFL Lausanne, in 1985 at the University of Pennsylvania, Philadelphia, in 1994 at the T.H. Ulm, and in 2004 at Infineon, Villach. He has been involved in design automation and in numerous analog integrated circuit designs for telecommunications, consumer electronics, medical applications and sensors. He has been supervisor of over 50 Ph.D. theses in these fields. He has authored and coauthored 12 books and more than 550 papers in international journals and conference proceedings.

Prof. Sansen is a member of several editorial and program committees of journals and conferences. He is cofounder and organizer of the workshops on Advances in Analog Circuit Design in Europe. He is a member of the executive and program committees of the IEEE ISSCC conference, and was program chair of the ISSCC 2002 conference.