AC Boosting Compensation Scheme for Low-Power Multistage Amplifiers

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***Abstract*—A new power-efficient frequency compensation scheme is proposed, called the AC Boosting Compensation (ACBC) scheme. An ac path is added to the internal stage of the conventional multistage amplifier, which improves significantly the performance such as the gain-bandwidth product and the slew rate without increasing the total power consumption. Analysis shows that the stability can be perfectly ensured.**

Two three-stage amplifiers have been implemented with and without a feed-forward stage, and fabricated in a 0.35-μm CMOS process. The ACBC amplifiers driving a 500-pF capacitance achieved 1.9-MHz gain-bandwidth product (GBW) dissipating only 0.3-mW power with a 2-V supply. An amplifier based on conventional nested Miller compensation (NMC) could only achieve 0.11-MHz GBW with the same load and power conditions, which shows an improvement of a factor of 17 in GBW.

***Index Terms*—AC boosting, amplifier, amplifiers, compensation, low power, multistage.**

I. Introduction

AN AMPLIFIER is needed in almost all electronic systems. Its theories and design methodologies have been well developed. However, they have to keep up with the fast advances in present-day technologies. As the channel lengths and supply voltages are further scaling down, single-stage amplifiers based on cascoding transistors are no longer possible. Instead, multistage amplifiers have come into use for low supply voltages. They will prevail especially when high dc gain is compulsory for high-precision purposes. Nonetheless, there are various difficulties in implementing a multistage amplifier. Doubtless the stability is among the most important design constraints. The high-resistance nodes between the stages generate poles and zeros with the parasitic capacitances, which can interfere with the required frequency responses. Hence, a multistage amplifier must be properly compensated in frequency; the redundant poles and zeros are either cancelled or shifted to higher positions than the unity-gain frequency.

For this purpose, the frequency compensation topology nested Miller compensation (NMC) [1] has been used. It employs Miller capacitors to split the poles so that the nondominant poles can be located higher than unity-gain frequency. Although such NMC amplifiers provide good stability, they lead to enormous power consumption and reduced gain-bandwidth product. Several transformed structures based on the NMC topology have been reported subsequently, such as MNMC [2] and NGCC [3]. They improve the performance by means of addition of feed-forward paths. However, the improvements are not significant.

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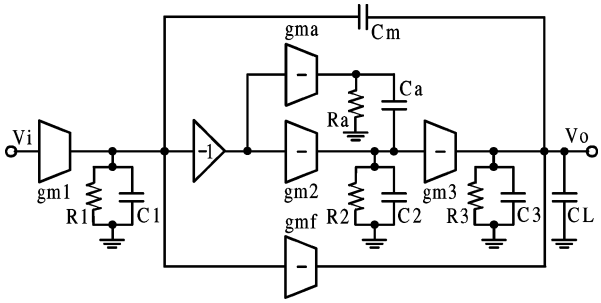

Fig. 1. Three-stage ac boosting compensation topology.

Some other reported frequency compensation methods using passive components such as nulling resistors [5], [11], [12] are also based on the NMC topology. As the nulling resistances cannot be too large to keep the Miller capacitances effective, the performance improvements are still insignificant. Besides, the nonprecise resistance, which is liable to vary, is an obvious disadvantage for reliable fabrication.

In order to further supplement the techniques in implementing multistage amplifiers, an AC Boosting Compensation (ACBC) scheme for low-power multistage amplifiers with even better performance is proposed in this paper. In this new frequency compensation topology ACBC, an ac amplifier is added in parallel with the internal stage to compensate the high-frequency gain reduction, which is normally one of the main factors limiting the overall performance of the multistage amplifiers.

The principle and the analysis of the three-stage ACBC amplifiers are presented in Section II. The discussions on stabilities and design constraints are also included. In Section III, the implementations of the circuits are described. The experimental results and performance comparison are given in Section IV. The final conclusion is drawn in Section V.

II. AC Boosting Compensation

A. AC Boosting Amplifier

The topology of the three-stage ACBC amplifier is shown in Fig. 1. Each of the amplifying stages is realized with a transconductance stage, as is usual in CMOS technologies. The transconductance stages g_{m1}, g_{m2}, and g_{m3} make up the conventional three-stage amplifier, while the g_{ma} stage acts as the ac-boosting path of the second stage. R_a is the output resistance of this g_{ma} stage. C_a is the ac coupling capacitor and C_m is the Miller capacitor. The output resistance and the lumped parasitic capacitance of each stage are noted by R_{1-3} and C_{1-3}, respectively. C_L is the load capacitance.

An inverter is required for the Miller capacitor C_m to realize a negative feedback loop. The distinction with other amplifiers is that this inverter is explicitly separated to allow the easy realization of both ac and dc paths of the second stage. As a result, both g_{m2} and g_{ma} stages can be realized with single transistors.

The major distinction of the ACBC topology from the other ones is that an ac amplifier is added in parallel with the second stage. This makes that the second stage consists of two signal paths. The first one g_{m2} is a dc path mainly for a high dc gain, and the other one g_{ma} is an ac path for boosting the high-frequency gain, which is usually quite small in conventional three-stage amplifiers. Boosting the high-frequency gain means that the nondominant poles are shifted to higher frequencies. Consequently the gain-bandwidth product or the unity-gain frequency can be set at a higher frequency.

Suppose that $A_2(f)$ represents the overall gain of the second stage (both paths), by neglecting the effects of the parasitic capacitances, the ultimate high-frequency gain of the second stage can be defined by (1):

$$A_{2h} = \lim_{f\to\infty} |A_2(f)|. \tag{1}$$

It will be proven later that in the ACBC amplifiers, the first nondominant pole can be moved by a factor of A_{2h} toward higher frequencies with a specific transconductance of the last stage driving a given load capacitance. Consequently, the gain-bandwidth product can be extended accordingly.

In order to improve the slew rate as well, a feed-forward stage g_{mf} can be included in the ACBC amplifier as shown in Fig. 1.

B. Transfer Function

The open-loop small-signal transfer function can be obtained by means of analyzing the equivalent small-signal circuit of the ACBC amplifier as shown in Fig. 1.

In order to simplify the expressions, the following assumptions are reasonably made:

$$R_2 \gg R_a \tag{2}$$

$$g_{m1}R_1,\ g_{m2}R_2,\ g_{m3}R_3 \gg 1 \tag{3}$$

$$C_a \gg C_2,\ C_L \gg C_3,\ C_L \gg C_m \gg C_1. \tag{4}$$

Thus, the simplified small-signal transfer function can be expressed by

$$A_{\mathrm{v}}(s) = \frac{A_{dc}\left(1+\frac{s}{\omega_4}+\frac{s^2}{\omega_4\omega_5}+\frac{s^3}{\omega_4\omega_5\omega_6}\right)}{\left(1+\frac{s}{|p_{-3\ \mathrm{dB}}|}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}+\frac{s^3}{\omega_1\omega_2\omega_3}\right)}. \tag{5}$$

All of the symbols in (5) are defined in (6)–(14) and explained subsequently:

$$A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \tag{6}$$

$$p_{-3\ \mathrm{dB}} = -\frac{1}{C_{m1}g_{m2}g_{m3}R_1R_2R_3} \tag{7}$$

$$\omega_1 = \frac{1}{\left(A_{2h}+\frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a} \tag{8}$$

$$\omega_2 = \left(A_{2h}+\frac{g_{mf}}{g_{m3}}\right)\frac{g_{m3}}{C_L} \tag{9}$$

$$\omega_3 = \frac{1}{R_aC_2} \tag{10}$$

$$\omega_4 = \frac{1}{\left(A_{2h}+\frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a} \tag{11}$$

$$\omega_5 = -\left(A_{2h}+\frac{g_{mf}}{g_{m3}}\right)\frac{g_{m3}}{C_m} \tag{12}$$

$$\omega_6 = \frac{1}{R_aC_2} \tag{13}$$

$$A_{2h} = (g_{m2}+g_{ma})R_a. \tag{14}$$

A_{dc} is the low-frequency gain. $p_{-3\ \mathrm{dB}}$ is the dominant pole. ω_{1-3} and ω_{4-6} represent frequency factors in the denominator and numerator of (5), respectively. The second-stage high-frequency gain A_{2h} in (14) is derived according to (1) after neglecting the parasitic capacitance C_2.

The gain-bandwidth product GBW is another important frequency factor, which is given by (15):

$$\omega_0 = \mathrm{GBW} = A_{dc}|p_{-3\ \mathrm{dB}}| = \frac{g_{m1}}{C_m}. \tag{15}$$

C. Stability and Gain-Bandwidth Product

The stability of an amplifier is generally investigated on its closed-loop transfer function in the unity-gain feedback configuration, which can be given as in (16) by assuming that the effects of the zeros are negligible. Actually, there is only one effective left half plane (LHP) zero, since C_2 and C_m are considerably smaller than C_a and C_L, respectively. Moreover, as the order of the numerator of $A_{\mathrm{cl}}(s)$ is less than that of the denominator, the stability of the ACBC amplifier depends on the denominator [9], [13] of the expression

$$A_{\mathrm{cl}}(s) = \frac{1}{1+\frac{s}{\omega_0}+\frac{s^2}{\omega_0\omega_1}+\frac{s^3}{\omega_0\omega_1\omega_2}+\frac{s^4}{\omega_0\omega_1\omega_2\omega_3}}. \tag{16}$$

Thus, by applying the Routh stability criterion [3], [13] on (16) and substituting the frequency factors ω_{1-3} with the expressions defined in (8)–(10), the stability condition of the ACBC amplifier can be obtained as

$$\mathrm{GBW} = \omega_0 < \left(A_{2h}+\frac{g_{mf}}{g_{m3}}-g_{m2}R_a\frac{C_2}{C_a}\right)\frac{g_{m3}}{C_L}. \tag{17}$$

According to (17), for a given load capacitance C_L, the GBW can be boosted if either g_{m3} or the value between the parentheses is increased. Since increasing g_{m3} results in larger power dissipation, the latter option should be preferred. According to assumption (4), and since the value of C_a can always be set large enough, the third term in the parentheses of (17) is negligible. Moreover, because of the same currents in both transistors of the feed-forward stage and the last stage, the transconductance g_{mf} is normally quite comparable to g_{m3}. Therefore, it is only the A_{2h} that can be the dominant term in boosting the GBW. In fact, A_{2h} can be much larger than one and it is not necessary to increase current to achieve a large A_{2h}.

From the above analysis, it is clear that the GBW of the ACBC amplifier can be extended by a factor of A_{2h} with a specific output transconductance stage driving a given load capacitor. The feed-forward stage g_{mf} contributes little in boosting GBW.

D. Design Constraints

The design of an amplifier is usually an operation of arranging the positions of the poles and zeros so that the GBW is optimized with an adequate phase margin.

Since C_2 is a lumped parasitic capacitance and C_a can be freely selected, it is practical to take the assumption

$$\omega_1 \ll \omega_2 \ll \omega_3. \tag{18}$$

If (18) is satisfied, the locations of the nondominant poles can be simply separated as in (19)–(21):

$$p_{nd1} = -\omega_1 = -\frac{1}{\left(A_{2h} + \frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a} \tag{19}$$

$$p_{nd2} = -\omega_2 = -\left(A_{2h} + \frac{g_{mf}}{g_{m3}}\right)\frac{g_{m3}}{C_L} \tag{20}$$

$$p_{nd3} = -\omega_3 = -\frac{1}{R_a C_2}. \tag{21}$$

The task left now is to obtain the zeros. Since C_m is far smaller than C_L, the conditions (22) and (23) can be deduced from (18) as follows:

$$\omega_4 = \omega_1 \ll \omega_2 \ll |\omega_5| \tag{22}$$

$$\omega_4 = \omega_1 \ll \omega_2 \ll \omega_6. \tag{23}$$

Apparently, as two zeros occur at very high frequencies even much higher than the second nondominant pole p_{nd2}, their effects can be neglected. Hence, there is only one effective LHP zero, which is given by

$$z_{\mathrm{LHP1}} = -\omega_4 = -\frac{1}{\left(A_{2h} + \frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a}. \tag{24}$$

Comparing z_{LHP1} to p_{nd1}, it is clear that they are always equal to each other, which yields complete cancellation of this pole–zero pair. Consequently the effect of this pole–zero pair on the transient responses can also be neglected although the position of this pair is lower than the unity-gain frequency.

After the first nondominant pole p_{nd1} is eliminated by the LHP zero z_{LHP1}, the pole p_{nd2} takes over as the first nondominant pole to determine the GBW and phase margin. In fact, the other nondominant pole p_{nd3} is parasitic capacitance related and is easily positioned at high frequency, minimizing circuit's sensitivity to nonprecise parasitic parameters.

In that case, the phase margin PM can be approximately expressed by

$$\mathrm{PM} \approx 90^\circ - \arctan\left(\frac{\mathrm{GBW}}{|p_{nd2}|}\right). \tag{25}$$

According to (25), p_{nd2} should be placed at two times the GBW to obtain a phase margin about 60°. Thus, the constraint on the Miller capacitance can be obtained:

$$C_m = \frac{2g_{m1}}{|p_{nd2}|} = \frac{2g_{m1}}{A_{2h}g_{m3} + g_{mf}}C_L. \tag{26}$$

It is worth noting that the assumption $R_2 \gg R_a$ given in (2) is mainly for simplification. In the case of smaller R_2, the overall equivalent resistance that affects A_{2h} becomes $R_a//R_2$. Considering this effect, the pole–zero positions can still be determined.

E. Slew Rate

The slew rate is another major performance parameter of an amplifier. It limits not only the settling time of the transient response but also the output signal range at high frequencies. Therefore, when designing amplifiers, it is important to extend the slew rate as much as the gain-bandwidth product.

For the internal stage of the ACBC amplifier, the capacitance load is the lumped parasitic capacitance C_2, which is much smaller than the other nonparasitic capacitances such as C_m and C_L. Besides, as both the ac stage and second stage work in parallel, the capacitor C_a does not have to be charged or discharged at the large signal transitions. Simulations show that the overall slew rate stays unchanged when C_a varies. Therefore, the overall slew rate is determined by other stages. Moreover, since the feed-forward stage g_{mf} and the last stage g_{m3} form a push-pull output stage, which slews fast in both directions, such that the first stage driving the Miller capacitance turns out to be the dominant limitation of the overall slew rate (SR), which can be given and further derived as

$$\mathrm{SR} = \frac{I_1}{C_m} \propto \frac{g_{m1}}{C_m}(V_{GS1} - V_{T1}) = \mathrm{GBW}(V_{GS1} - V_{T1}). \tag{27}$$

Obviously, from (27), it can be seen that the slew rate is proportional to the GBW. As the GBW is improved by means of increasing the second-stage high-frequency gain A_{2h}, simultaneously, the slew rate is extended accordingly.

III. Implementation

The schematic of the implemented ACBC amplifier is shown in Fig. 2. The first stage consists of the transistors M10–M18, which guarantee that the common mode input range, can reach the lower rail voltage V_{SS}. The differential pair of M11 and M12 generates transconductance g_{m1}. The transistors Mi and Mi0 constitute an inverter. The transistor M2 and M20 act as the second stage, whereas Ma, Ma0, and Ma1 realize the ac-boosting stage; M2 and Ma generate g_{m2} and g_{ma}, respectively.

For the ac-boosting stage, the gain can be precisely determined by the ratio of sizes of Ma and Ma1. Moreover, as it does not have to directly drive other gates, the $(V_{GS} - V_T)$ of Ma1 can be set larger to achieve a required voltage gain. Furthermore, It is known that the pole–zero pair are always cancelled by each other and the impact of the second nondominant pole variation is small because it occurs at higher frequencies. As a result, the performance mainly depends on the second-stage

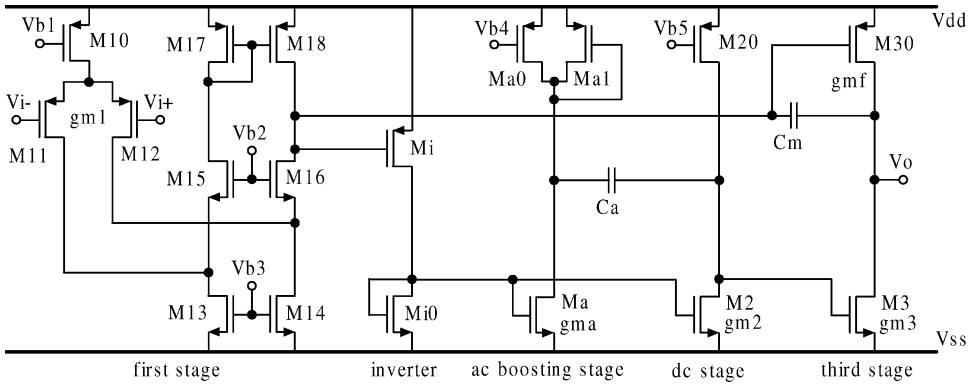

Fig. 2. Schematic of the ac boosting amplifier.

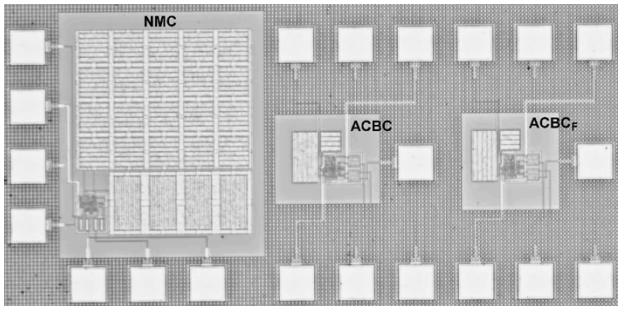

Fig. 3. Micrograph of the implemented amplifiers.

high-frequency gain A_{2h} rather than R_a itself. Since A_{2h} is a trasconductance ratio of the relevant transistors, it can readily be kept tracking. The value of A_{2h} is set at about 10, which is large enough to achieve a better performance than most of the reported amplifiers. In fact, A_{2h} could even be set as high as the second-stage dc gain.

In order to minimize the lumped parasitic capacitance C_2, the last stage g_{m3} is realized with a NMOS transistor M3, whereas transistor M30 acts as the feed-forward stage g_{mf}.

The load capacitance C_L is taken to be 500 pF and the unity-gain frequency is set at about 2 MHz. The Miller capacitance C_m is 10 pF, which is much larger than the lumped parasitic capacitance C_1 which includes the input capacitance of M30. The value of C_a is not important, as long as the poles are separated enough. A relatively small capacitance 3 pF is adopted. The transconductance g_{m1} is decided by the GBW and the Miller capacitance, while g_{m2} and g_{ma} are minimized for the stability. All the transconductances for the implemented amplifiers are given by $g_{m1} = 115\ \mu$S, $g_{m2} = g_{ma} = 60\ \mu$S, and $g_{m3} = g_{mf} = 1.2$ mS.

It should be emphasized that the relatively large transconductance adopted for g_{m3} is mainly for maintaining the same power dissipation as for an NMC amplifier, which is also implemented for sake of comparison. In fact, for stability, the g_{m3} can have small values. Besides, by increasing A_{2h}, the required g_{m3} can even be smaller.

The ACBC amplifier is also feasible for relatively small load capacitances operating at larger unity-gain frequencies. Simulations show that the ACBC amplifier can provide a 20-MHz unity-gain frequency with a phase margin larger than 50°, employing a 50-pF load and 1-pF Miller capacitance.

TABLE I
MEASURED RESULTS OF IMPLEMENTED AMPLIFIERS

	NMC	ACBC	ACBC$_F$
C_L (pF)	500		
A_{dc} (dB)	>100		
GBW (MHz)	0.109	1.89	1.90
PM	51°	53°	52°
SR $_{+/-}$ (V/μS)	0.07/0.09	0.2/1.2	0.8/1.2
TS $_{+/-}$ (μS)	18/14	6.9/1.2	1.9/1.2
V_{dd} (V)	2		
I_{dd} (mA)	0.167	0.158	0.162
Power (mW)	0.334	0.316	0.324
Area (mm^2)	0.26	0.02	0.02

Both ac-boosting amplifiers with and without the feed-forward stage g_{mf} were implemented and fabricated in a 0.35-μm CMOS process. A micrograph of the implemented amplifiers is shown in Fig. 3. In the micrograph, the $\mathrm{ACBC_F}$ and ACBC indicate both the ac-boosting amplifiers with and without the feed-forward stage. The area for one ac-boosting amplifier is about 0.02 mm^2. As seen in the micrograph, an NMC amplifier with a much larger area (0.26 mm^2) was also implemented and fabricated for comparison.

IV. EXPERIMENTAL RESULTS

A. Measured Results

All the implemented amplifiers are measured for both dc and ac specifications. The measured results, which are obtained using an HP3577A network analyzer and a Tektronix TDS680B oscilloscope, are summarized in Table I. The frequency characteristics and the transient responses are shown in Fig. 4 and Fig. 5, respectively. Evidently, the performance results of the ac boosting amplifiers are outstanding compared with their NMC counterpart. For the same load capacitance and similar power consumption, the GBW is about 17 times higher.

B. Performance Comparison

It is difficult to make accurate evaluations on different amplifiers that are implemented in different technologies with

TABLE II
PERFORMANCE COMPARISON OF DIFFERENT AMPLIFIERS

		A_{dc} dB	C_L pF	V_{dd} V	I_{dd} mA	Power mW	GBW MHz	SR $V/\mu S$	FOM_S $\frac{MHz \cdot pF}{mW}$	FOM_L $\frac{V/\mu S \cdot pF}{mW}$	$IFOM_S$ $\frac{MHz \cdot pF}{mA}$	$IFOM_L$ $\frac{V/\mu S \cdot pF}{mA}$
NMC	[2]	100	100	8.0	9.50	76	60	20	79	26	632	211
MNMC	[2]	100	100	8.0	9.50	76	100	35	132	46	1053	368
NGCC	[3]	100	20	2.0	0.34	0.68	0.61	2.5	18	74	36	148
NCFF	[4]	90	12	2.5	5.6	14	250	-	214	-	535	-
NMCFNR	[5]	>100	100	2.0	0.20	0.406	1.8	0.79	443	195	886	390
EFC	[6]	102	40	3.0	2.30	6.90	47	69	272	400	817	1200
DFCFC	[7]	>100	100	2.0	0.21	0.42	2.6	1.32	619	314	1238	629
PFC	[8]	>100	130	1.5	0.19	0.275	2.7	1.0	1276	473	1915	709
AFFC	[9]	>100	120	2.0	0.20	0.40	4.5	1.49	1350	447	2700	894
DLPC	[10]	>100	120	1.5	0.22	0.33	7.0	3.3	2545	1200	3818	1800
ACBC	this work	>100	500	2.0	0.158	0.316	1.89	0.7	2991	1108	5981	2215
$ACBC_F$	this work	>100	500	2.0	0.162	0.324	1.90	1.0	2932	1543	5864	3086

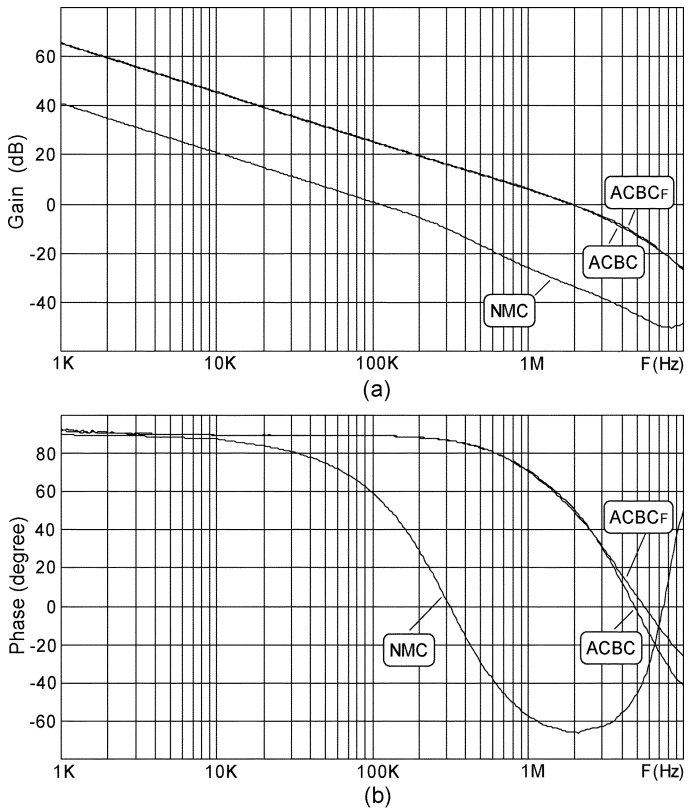

Fig. 4. Measured open-loop frequency responses: (a) gain and (b) phase.

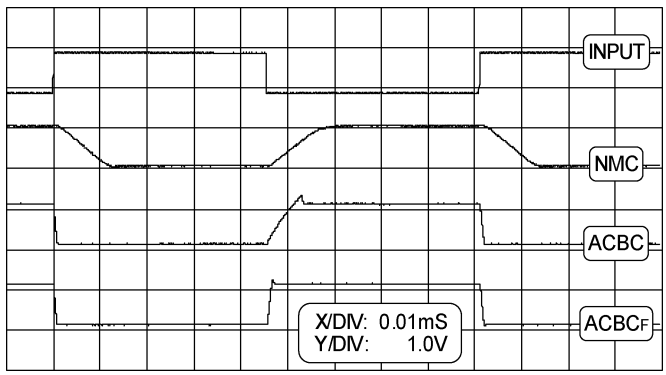

Fig. 5. Measured unity-gain transient responses.

different operating points. There is a trend, however, to use $\mathrm{FOM_S} = \mathrm{GBWC_L/power}$ and $\mathrm{FOM_L} = \mathrm{SRC_L/power}$ to evaluate different amplifiers. Nonetheless, as both the GBW and the SR are directly related to the currents in the relevant transistors, the evaluation is relatively rough, especially when the supply voltages are different. As the supply voltage is further scaling down, the newly implemented amplifiers are always better. Not to exploit this advantage, it is also possible to take the total quiescent current of an amplifier rather than the power itself, forming two new formulas, given by $\mathrm{IFOM_S} = \mathrm{GBWC_L/I_{dd}}$ and $\mathrm{IFOM_L} = \mathrm{SRC_L/I_{dd}}$.

By using these formulas, the comparative results are listed in Table II. Obviously, the ac-boosting amplifiers have significantly outperformed all the other amplifiers. In fact, the performance can be even better provided that the second-stage high-frequency gain is set at higher values.

V. CONCLUSION

This brief has shown that a new ac-boosting compensation scheme which provides lower power consumption is well suited for low-voltage applications. Although an additional ac stage exists, the performance has been enhanced considerably. It also shows that both the gain-bandwidth product and the slew rate can be remarkably improved simultaneously.

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