Advances in Active-Feedback Frequency Compensation With Power Optimization and Transient Improvement

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Abstract—This paper presents a low-power stability strategy to significantly reduce the power consumption of a three-stage amplifier using active-feedback frequency compensation (AFFC). The bandwidth of the amplifier can also be enhanced. Simulation results verify that the power dissipation of the AFFC amplifier is reduced by 43% and the bandwidth is improved by 32.5% by using the proposed stability strategy. In addition, a dynamic feedforward stage (DFS), which can be embedded into the AFFC amplifier to improve the transient responses without consuming extra power, is proposed. Implemented in a 0.6-μm CMOS process, experimental results show that both AFFC amplifiers with and without DFS achieve almost the same small-signal performances while the amplifier with DFS improves both the negative slew rate and negative 1% settling time by two times.

Index Terms—Active feedback, amplifiers, dynamic feedforward stage (DFS), frequency compensation, low-power stability strategy, multistage amplifiers.

I. INTRODUCTION

NOWADAYS, multistage amplifiers are growing in demand as they can provide high gain and large output swing in low-voltage conditions. However, multistage amplifiers suffer from stability problems due to the presence of multi-poles. Different frequency-compensation topologies have been reported to solve the stability problems by sacrificing the bandwidth of the amplifier [1]–[7]. Recently, active-feedback frequency compensation (AFFC) topology, which achieves the widest bandwidth compared to other reported compensation topologies [8], has been developed in a three-stage amplifier. The stability of the AFFC amplifier is achieved by following the Butterworth frequency response to arrange the location of poles. However, this results in nonpower-optimized dimension conditions [8]. This paper develops a new low-power stability strategy to systematically optimize the power consumption of the AFFC amplifier while further enhancing the amplifier bandwidth.

In addition, a dynamic feedforward stage (DFS) for AFFC amplifiers to improve their original transient responses and simplify the biasing scheme is proposed. As verified by experimental results, the DFS improves the slew rate and settling time

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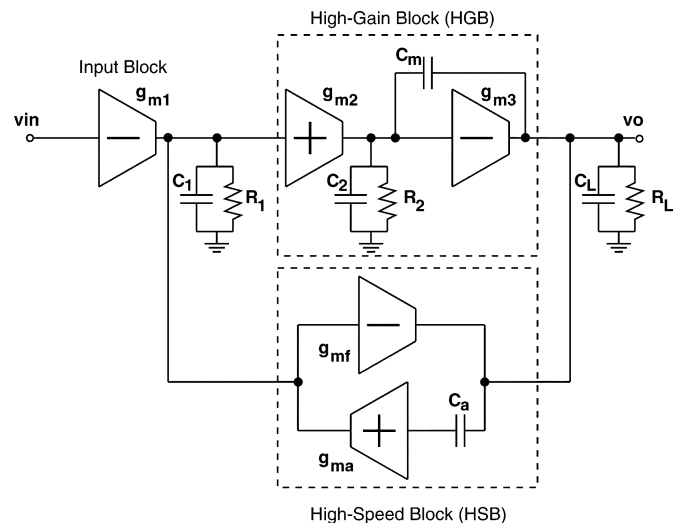
Fig. 1. Structure of a three-stage generic AFFC amplifier.

of the AFFC amplifier without consuming additional dc power and degrading original frequency responses.

In Section II, some design concerns of the generic AFFC amplifier are described. The proposed low-power stability strategy is then discussed and verified in Section III. The functions of the DFS in the AFFC amplifier are presented in Section IV. Finally, experimental results and conclusions are given in Sections V and VI, respectively.

II. AFFC

The structure of a three-stage generic AFFC amplifier, which consists of an input block, a high-gain block (HGB) and a high-speed block (HSB) [8] is shown in Fig. 1. In Fig. 1, $g_{m(1,2,3)}$, $R_{1,2}$ and $C_{1,2}$ are the transconductances, equivalent parasitic resistances, and lumped parasitic capacitances of gain stages, respectively, while C_L and R_L are the output loading capacitor and loading resistor of the amplifier. In the HGB, two gain stages with $g_{m(2,3)}$ and a compensation capacitor, C_m, form a two-stage Miller amplifier [9] to boost the dc gain of the three-stage amplifier. The HSB has a feedforward stage (FFS) and a feedback stage (FBS) with transconductances, g_{mf} and g_{ma}, respectively, and a dominant compensation capacitor, C_a, is connected in series with the FBS to realize an active-capacitive-feedback network. By using the assumptions: (1) C_L, C_a,

TABLE I
SUMMARY OF AFFC AMPLIFIER WITH DIFFERENT STABILITY STRATEGIES

Stability Strategy	Dimension Conditions	GBW	PM	Q-value of $p_{2,3}$
Butterworth Response	$g_{mf} > g_{m2}$ $g_{ma} = 4 \cdot g_{m1}$ $C_a = \sqrt{\dfrac{2 \cdot g_{m1} C_1 C_L}{g_{mf} - g_{m2}}} = C_{(Butterworth)}$ $C_m \le C_a$	$\sqrt{\dfrac{g_{m1}(g_{mf} - g_{m2})}{2 \cdot C_1 C_L}}$ $= GBW_{(Butterworth)}$	74°	$1/\sqrt{2}$
Low Power (Case 1)	$g_{mf} > g_{m2}$ $g_{ma} = 2 \cdot g_{m1}$ $C_a = \sqrt{\dfrac{1.16 \cdot g_{m1} C_1 C_L}{g_{mf} - g_{m2}}} = 0.76 \cdot C_{(Butterworth)}$ $C_m \le C_a$	$\sqrt{\dfrac{g_{m1}(g_{mf} - g_{m2})}{1.16 \cdot C_1 C_L}}$ $= 1.31 \cdot GBW_{(Butterworth)}$	60°	0.761
Low Power (Case 2)	$g_{mf} > g_{m2}$ $g_{ma} = 2 \cdot g_{m1}$ $C_a = \sqrt{\dfrac{0.83 \cdot g_{m1} C_1 C_L}{g_{mf} - g_{m2}}} = 0.65 \cdot C_{(Butterworth)}$ $C_m \le C_a$	$\sqrt{\dfrac{1.2 \cdot g_{m1}(g_{mf} - g_{m2})}{C_1 C_L}}$ $= 1.55 \cdot GBW_{(Butterworth)}$	45°	0.417

and $C_m \gg C_1, C_2$, and (2) $g_{m(1,2,3)} R_{(1,2,L)}$ and $g_{ma} R_1 \gg 1$, the transfer function of the AFFC amplifier is given by

$$A_{v(\text{AFFC})}$$
$$= \frac{A_{\text{dc}}\left(1 + s\frac{C_a}{g_{ma}}\right)}{\left(1 + \frac{s}{p_{-3\text{ dB}}}\right)\left(1 + s\frac{C_1 C_L}{C_a(g_{mf} - g_{m2})} + s^2\frac{C_1 C_L}{g_{ma}(g_{mf} - g_{m2})}\right)} \quad (1)$$

where $A_{\text{dc}} = g_{m1} g_{m2} g_{m3} R_1 R_2 R_L$ is the dc voltage gain, $p_{-3\text{ dB}} = 1/(C_a g_{m2} g_{m3} R_1 R_2 R_L)$ is the dominant pole, $\text{GBW} = A_{\text{dc}} \cdot p_{-3\text{ dB}} = g_{m1}/C_a$ is the gain-bandwidth (GBW) product, and a left-half-plane (LHP) zero, $z_{\text{LHP}} = g_{ma}/C_a$, is created in the AFFC amplifier.

Similar to most reported three-stage amplifiers, the AFFC amplifier follows the Butterworth frequency response for both stabilization and bandwidth maximization [1], [2], [4]–[6]. The Butterworth frequency response arranges the two nondominant poles of a three-stage amplifier to form a pair of complex poles with its Q-value equal to $1/\sqrt{2}$. When the AFFC amplifier is in unity-gain feedback configuration with its poles having a third-order Butterworth response [8], the dimension conditions are given by

$$C_{a(\text{Butterworth})} = \sqrt{\frac{2g_{m1} C_1 C_L}{g_{mf} - g_{m2}}} \quad (2)$$

$$g_{ma(\text{Butterworth})} = 4 \cdot g_{m1}. \quad (3)$$

The value of C_m can be set to equal C_a in the design phase for simplicity. As g_{m1} is generally large to minimize the noise and input offset voltage in practical circuit implementations, a large current consumption is thus needed to bias the FBS in order to satisfy the condition stated in (3). Although the power consumption can be decreased through implementing g_{m1} by PMOS transistors and realizing g_{ma} by a NMOS transistor [8], the power consumption of the AFFC amplifier can be further optimized if the required value of g_{ma} is reduced.

Due to the presence of one dominant pole, a pair of complex poles and one LHP zero in the AFFC amplifier, its phase margin is given by

$$\text{PM} = 180° - \arctan\left(\frac{\text{GBW}}{p_{-3\text{ dB}}}\right)$$
$$- \arctan\left(\frac{\left(\frac{\text{GBW}}{|p_{-3\text{ dB}}|}\right)}{Q\left(1 - \left(\frac{\text{GBW}}{|p_{2,3}|}\right)^2\right)}\right) + \arctan\left(\frac{\text{GBW}}{z_{\text{LHP}}}\right) \quad (4)$$

where $|p_{2,3}| = \sqrt{g_{ma}(g_{mf} - g_{m2})/C_1 C_L}$ and $Q = \sqrt{C_a^2(g_{mf} - g_{m2})/C_1 C_L g_{ma}}$. In particular, by substituting the dimension conditions of (2) and (3) into (4), the phase margin based on Butterworth response is then given by

$$\text{PM}_{(\text{Butterworth})} \approx 60° + \arctan\left(\frac{g_{m1}}{g_{ma}}\right) = 74°. \quad (5)$$

From (5), the presence of the LHP zero contributes an extra 14° phase margin to the AFFC amplifier. Generally, the phase margin of 60° is sufficient to ensure the stability of an amplifier [2]; therefore, the phase margin of the AFFC amplifier is more than necessary in most applications.

In the AFFC amplifier, the value of g_{m2} is set to much smaller than g_{mf} to reduce the required value of C_a from (2) such that the bandwidth can be maximized. Small g_{m2} can also lower the static power consumption. However, the small biasing current in the noninverting second stage with static biasing scheme slows down the rate of charging or discharging the compensation capacitor C_m and hence limits the slew rate of the amplifier.

III. PROPOSED LOW-POWER STABILITY STRATEGY

In order to reduce power consumption, the stability strategy used in the two-stage amplifier [10] is modified and extended to design the three-stage AFFC amplifier for power optimization. There are two criteria in the proposed stability strategy. The first stability criterion is given as

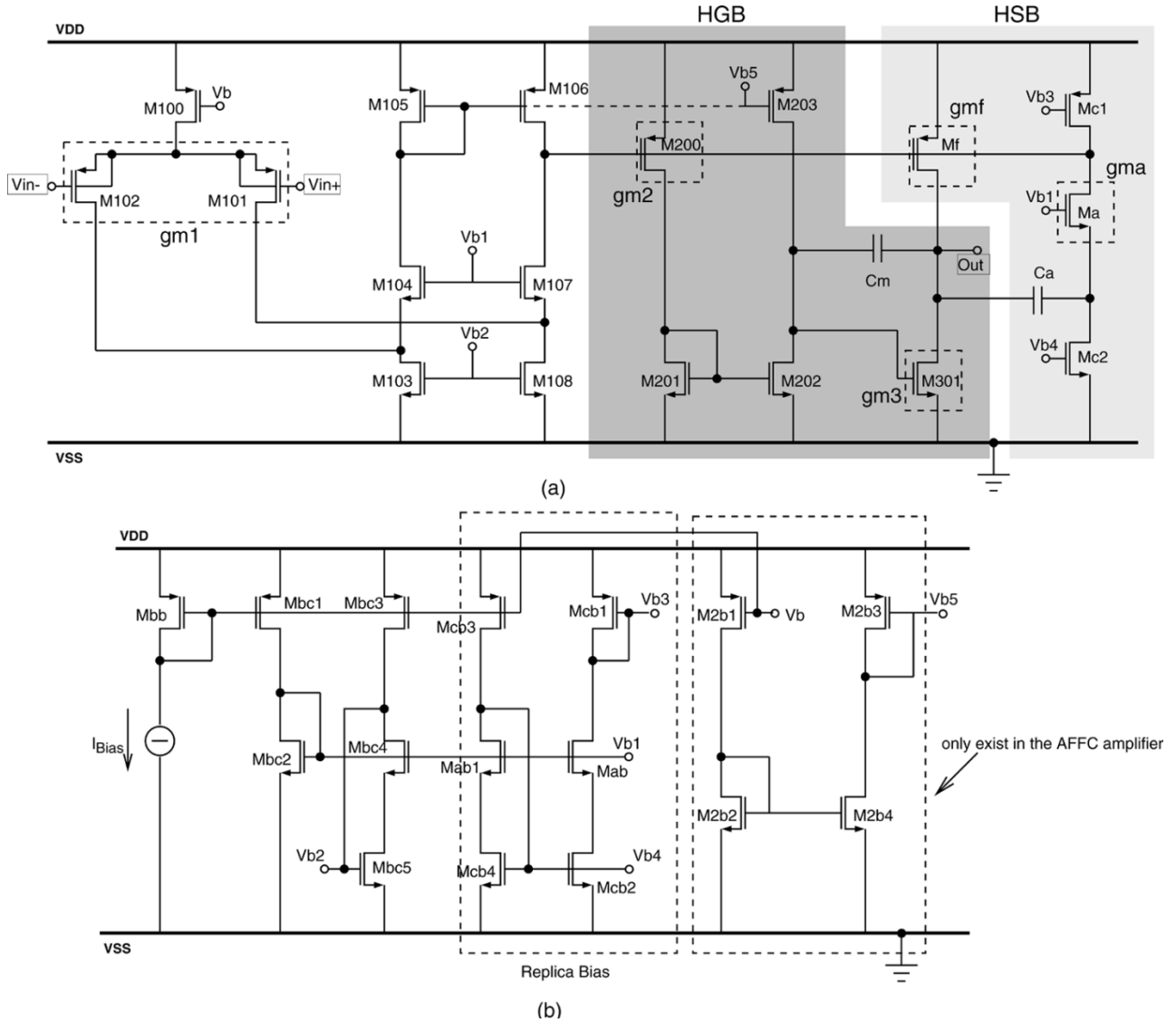$$\text{Re}\,(p_{2,3}) \ge \text{GBW} \quad (6)$$

Fig. 2.   (a) Circuit diagram and (b) biasing circuit of the AFFC amplifier (gate of M203 is connected to Vb5 by solid line) and the AFFC-DFS amplifier (gate of M203 is connected to gate of M106 by dash line).

where

$$p_{2,3} = \frac{g_{ma}}{2C_a} \pm j\frac{g_{ma}}{2C_a}\sqrt{\frac{4C_a^2(g_{mf} - g_{m2})}{C_1 C_L g_{ma}} - 1}.$$

The criterion in (6) is to ensure the dominant-pole behavior of the amplifier as only the dominant pole, $p_{-3\,\mathrm{dB}}$, is allowed to exist in the passband of the amplifier. By applying $GBW = g_{m1}/C_a$ into (6), a low-power dimension condition of g_{ma} results

$$g_{ma(\mathrm{low-power})} \geq 2 \cdot g_{m1}. \tag{7}$$

By comparing (3) and (7), the dimension condition of g_{ma} can be reduced as much as two times for power optimization with the first low-power criterion.

However, the first stability criterion cannot control the Q-value of the nondominant poles of the AFFC amplifier. For example, if the dimension conditions of $g_{ma(\mathrm{low-power})} = 2g_{m1}$ and $C_{a(\mathrm{Butterworth})}$ are used to

compensate the amplifier, the Q-value of the nondominant poles is then increased to 1. A magnitude peak occurs at the location of the nondominant poles and degrades the settling behavior of the amplifier. Since the criterion in (7) defines the value of g_{ma}, and then fixes the position of the nondominant poles, the Q-value can thus be decreased by reducing the phase margin of the amplifier according to (4). In addition, due to the presence of LHP zero, the phase margin of the AFFC amplifier is 74°. It has the capability to trade off a lower phase margin for a lower Q-value. The second stability criterion is thus given as

$$\mathrm{PM}_{(\mathrm{low-power})} = 60°. \tag{8}$$

Equation (8) leads to a new dimension condition of C_a. By using $g_{ma(\mathrm{low-power})} = 2g_{m1}$ and substituting (4) into (8), the following equation is obtained:

$$\arctan\left(\frac{\left(\frac{\mathrm{GBW}}{|p_{2,3}|}\right)}{Q\left(1 - \left(\frac{\mathrm{GBW}}{|p_{2,3}|}\right)^2\right)}\right) = 56.6°. \tag{9}$$

By solving (9), the dimension condition of $C_{a(\text{low}-\text{power})}$ is given as

$$C_{a(\text{low}-\text{power})} = \sqrt{\frac{1.16 g_{m1} C_1 C_L}{g_{mf} - g_{m2}}}. \qquad (10)$$

Compared with the size of $C_{a(\text{Butterworth})}$, $C_{a(\text{low}-\text{power})}$ is reduced by 24%, which implies that the GBW of the AFFC amplifier can be further enhanced by using the proposed low-power stability strategy. By using both $g_{ma(\text{low}-\text{power})}$ and $C_{a(\text{low}-\text{power})}$, the Q-value of the nondominant poles is 0.761, which has only increased by 7.6% as compared to that in Butterworth response. Therefore, no significant magnitude peaking occurs at the locations of nondominant poles and good settling behavior of the amplifier can still be attained. It should be noted that the second stability criterion stated in (8) is application dependent, which implies that the value of C_a can be determined with enhanced flexibility by specifying different phase margins. Table I summarizes both the dimension conditions and amplifier performances of a three-stage AFFC amplifier using either Butterworth frequency response or the proposed low-power stability strategy. In addition, the proposed low-power stability criteria stated in (6) and (8) only scale the values of g_{ma} and C_a by a constant number. The proposed low-power stability criteria thus do not alter the sensitivity of GBW and Q-value of the nondominant poles, as compared to Butterworth frequency response.

In order to justify the effectiveness of the proposed low-power stability strategy, a three-stage AFFC amplifier is designed to drive a 100-pF // 25-kΩ load. The circuit diagram and biasing circuit of the AFFC amplifier are shown in Fig. 2(a) and (b), in which the gate of transistor M203 is biased by a static current source at Vb5. The compensation capacitors, $C_{a(\text{low}-\text{power})}$ and $C_{m(\text{low}-\text{power})}$, are designed to be 5.4 and 4 pF, respectively. Similarly, a three-stage AFFC amplifier using Butterworth frequency response is also implemented for comparison purpose. A simulation using a BSim3v3 model of a 0.6-μm CMOS process from Austria Mikro Systeme International AG (AMS) was carried out. Fig. 3(a) and (b) shows the frequency responses of AFFC amplifiers using both stability strategies by the magnitude-phase plot and pole-zero plot, respectively. The detailed simulation results are summarized in Table II. Compared to the amplifier with Butterworth frequency response, the power-optimized AFFC amplifier reduces the power consumption by 43%, reduces the value of C_a by 24%, and improves the GBW by 32.5% with 10° decrease in the phase margin. The simulation results are similar to the theoretical analysis.

IV. Proposed AFFC With DFS

Based on the generic implementation of the AFFC amplifier in Fig. 2(a), the slew rate is not limited by the push–pull output stage. Instead, the slew rate is limited by the small amount of the static current in the noninverting second stage to charge C_m. As a result, both the negative slew rate and negative settling time are degraded in the AFFC amplifier. This problem can be mitigated by using a push–pull second stage that can increase the amount of dynamic current to charge C_m in the transient state, while the small bias current is still used in the quiescent state to provide a small value of g_{m2} for bandwidth optimization. A DFS is thus
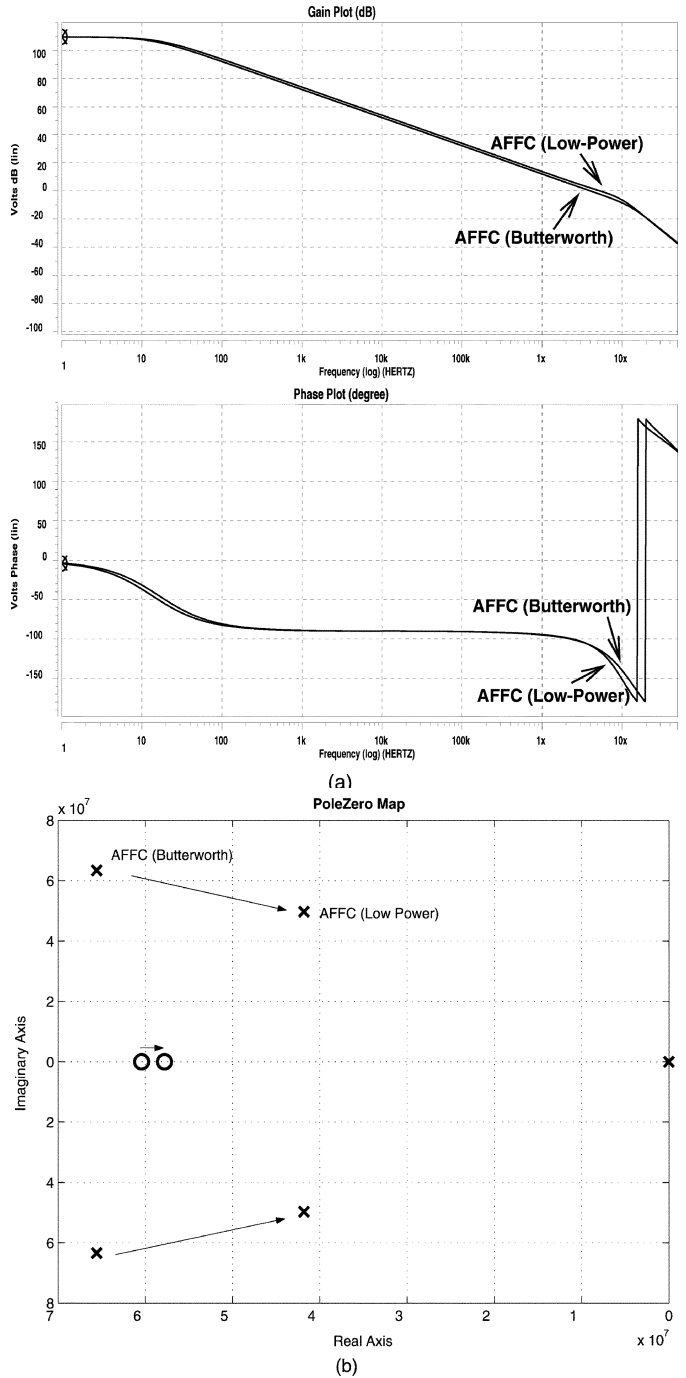

Fig. 3. Simulated (a) magnitude-phase plot and (b) pole-zero plot of the AFFC amplifiers using the Butterworth response and low-power stability strategy.

proposed as an addition to the generic AFFC structure in order to achieve the push–pull effect, which improves the transient responses. The proposed DFS is connected from the input of the amplifier to the output of the second gain stage as shown in Fig. 4(a) such that the DFS does not affect its original value of g_{m2}.

Although the structure of the proposed DFS in the AFFC amplifier is the same as that of the feedforward stage in the multipath nested Miller compensated (MNMC) amplifier [2], their functions are totally different. In the MNMC, the feedforward stage affects the frequency responses of the amplifier. The feedforward stage generates a low-frequency LHP zero to cancel the

TABLE II
SIMULATION RESULTS OF THREE-STAGE AFFC AMPLIFIERS

	AFFC (Butterworth)	AFFC (Low-Power)
Loading	25 kΩ // 100 pF	
Supply Voltage	1.5 V	
DC Gain	110 dB	110 dB
GBW	4 MHz	5.3 MHz
PM	73°	63°
Power Consumption	466 μW	265 μW
C_a	7 pF	5.4 pF
C_m	4 pF	4 pF

Fig. 5.   Chip micrograph of three-stage AFFC and AFFC-DFS amplifiers.
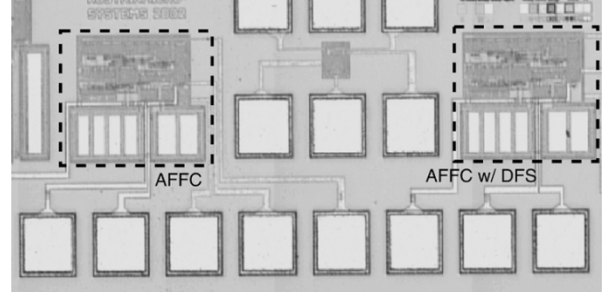

Fig. 4.   (a) Structure and (b) equivalent small-signal circuit of the proposed three-stage AFFC-DFS amplifier.
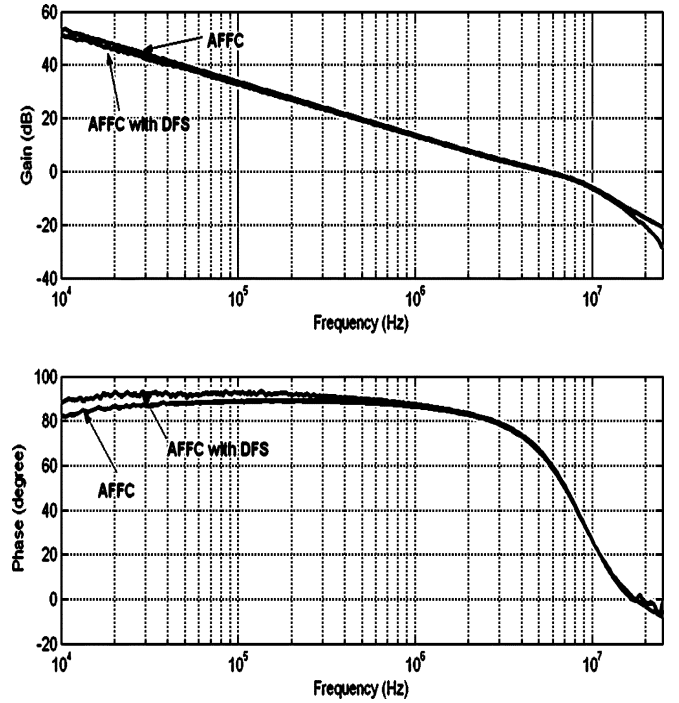
Fig. 6.   Measured ac responses of the AFFC and AFFC-DFS amplifiers driving a 100-pF // 25-kΩ load.

second nondominant pole, resulting in bandwidth extension [2]. On the other hand, the proposed DFS does not affect the frequency responses of the AFFC amplifier. In order to analyze the effect of the DFS on the frequency response of the generic AFFC structure, the transfer function of the AFFC-DFS structure using its equivalent small-signal diagram as shown in Fig. 4(b), is derived as

$$A_{v(\text{AFFFC-DFS})}$$

$$\approx \frac{\left(1+s\frac{C_a}{g_{ma}}\right)\left(1-s\frac{g_{mf2}C_1}{g_{m1}(g_{mf}-g_{m2})}\right)}{\frac{s}{\text{GBW}}\left(1+s\frac{C_1 C_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_1 C_L}{g_{ma}(g_{mf}-g_{m2})}\right)}$$

$$\approx \frac{\left(1+s\frac{C_a}{g_{ma}}\right)}{\frac{s}{\text{GBW}}\left(1+s\frac{C_1 C_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_1 C_L}{g_{ma}(g_{mf}-g_{m2})}\right)}$$

$$= A_{v(\text{AFFC})} \qquad\qquad (11)$$

where g_{mf2} is the transconductance of the DFS. From (11), the DFS only contributes a high-frequency right-half-plane (RHP) zero to the amplifier. Since the RHP zero only depends on the parasitic capacitor C_1 and its location is located at a much higher frequency than the GBW of the amplifier, the effect of the RHP zero can be neglected. Hence, both the AFFC-DFS and generic AFFC structures have the same transfer function. This verifies that the addition of the DFS in the AFFC amplifier only improves the transient responses without affecting the ac responses. Therefore, the AFFC-DFS amplifier can also use the same low-power stability strategy to achieve the same ac responses as the generic AFFC counterpart.

To implement the DFS, Fig. 2(a) demonstrates a possible circuit implementation, in which the DFS is realized by a transistor M203 which has a gate terminal connected to the gates of transistors M105 and M106 by a dash line. The quiescent current through the DFS can be properly controlled by simply scaling the device ratios between transistors M105 and M203. In the transient state, the push–pull effect is achieved by transistors
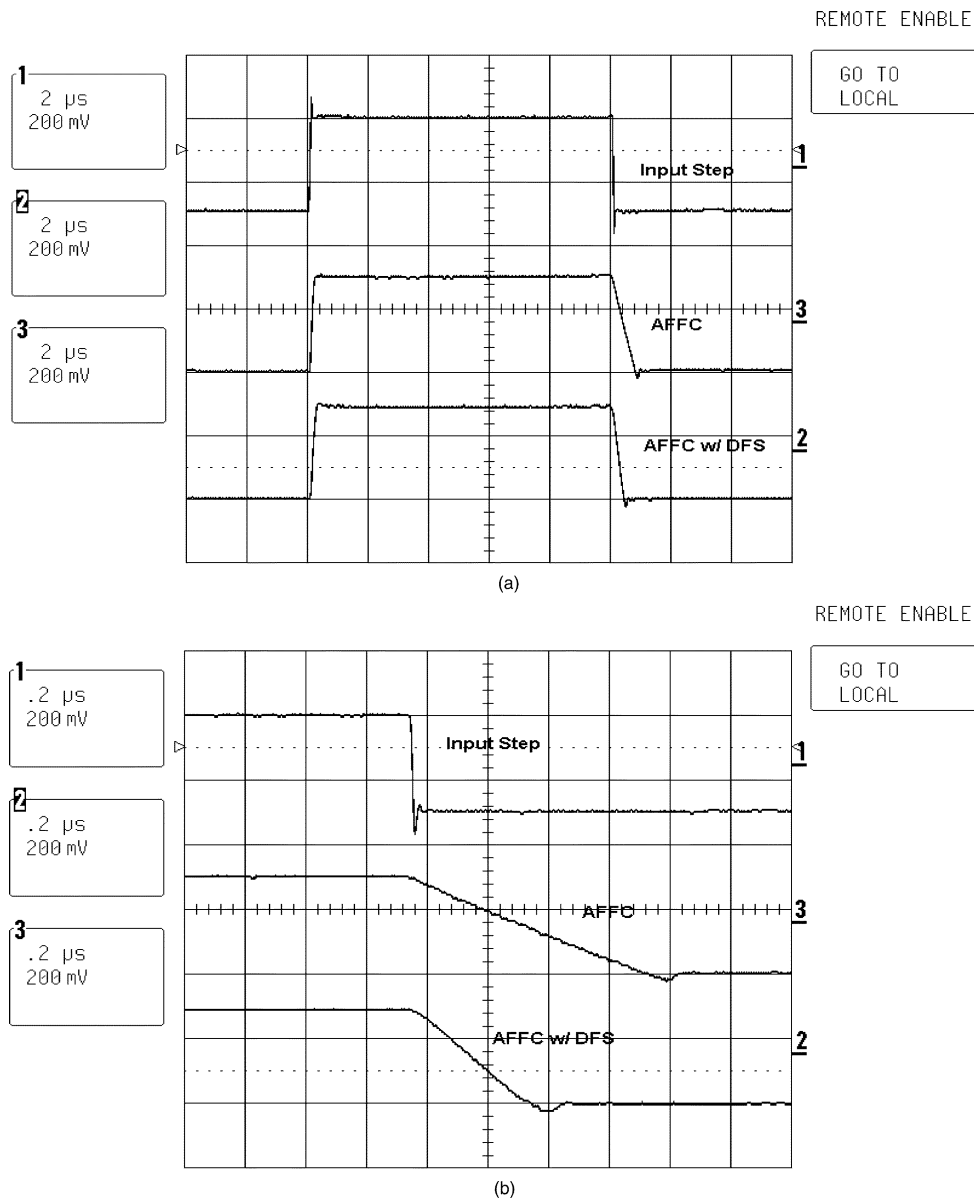
Fig. 7. (a) Measured transient responses of the AFFC and AFFC-DFS amplifiers. (b) Close view of the AFFC and AFFC-DFS amplifiers driving a 100-pF // 25-kΩ load.

TABLE III
MEASURED RESULTS OF AFFC AND AFFC-DFS AMPLIFIERS

	AFFC	AFFC with DFS
Loading	25 kΩ // 100 pF	
DC Gain	> 100 dB	> 100 dB
GBW	5.5 MHz	5.5 MHz
PM	61°	61°
SR$^+$/SR$^-$ (V/μs)	2/0.42	2/0.82
T$_s^+$/T$_s^-$ (μs) (to 1%)	0.23/0.83	0.23/0.48
Power Consumption @Vdd	252 μW @1.5 V	250 μW @1.5 V
C$_a$	5.4 pF	5.4 pF
C$_m$	4 pF	4 pF
Area	0.05 mm^2	0.05 mm^2

M203 and M202 to charge and discharge C_m during the negative slewing and positive slewing periods, respectively. Compared to the circuit of the generic AFFC amplifier as shown in Fig. 2(a) and (b), where the gate of M203 is biased by a voltage generated by the current source at node Vb5, the DFS does not require any extra current source for static biasing. The amplifier with DFS is thus simpler and more power efficient. Moreover, the addition of DFS increases the amount of current through M203 dynamically to charge C_m during the negative slewing period. Therefore, the negative slew rate, the negative settling

time and the overall transient responses of the AFFC amplifier are improved.

V. EXPERIMENTAL RESULTS

To demonstrate the functionality of DFS in the AFFC amplifier, both AFFC and AFFC-DFS amplifiers using low-power stability strategy have been fabricated using AMS 0.6-μm CMOS process. The chip micrograph is shown in Fig. 5. The frequency responses of both amplifiers have been measured with an input common-mode voltage of 0.3 V, while the slew rate and 1% settling time have been tested when the amplifiers are in unity-gain noninverting configuration with a 0.3-V step input. The measured frequency responses and the transient responses of both amplifiers are shown in Figs. 6 and 7, respectively. The detailed performances are summarized in Table III. Both AFFC and AFFC-DFS amplifiers achieve the same GBW and phase margin while dissipating almost the same power at 1.5-V supply. Therefore, the DFS does not affect the frequency responses of the AFFC amplifier. On the other hand, the DFS improves the amplifier transient responses. This is shown in Fig. 7, where the AFFC amplifier with the DFS doubles the negative slew rate and almost halves the negative 1% settling time as compared to the amplifier without the DFS.

VI. CONCLUSION

A low-power stability strategy, which gives new dimension conditions to three-stage amplifiers using AFFC, resulting in both power optimization and bandwidth enhancement, is introduced. In addition, a DFS is proposed to realize a push–pull second stage to improve the transient responses of the generic AFFC amplifier without affecting its original power consumption and frequency responses. The DFS also simplifies the generic AFFC structure by reducing its biasing points. Both simulation and experimental results are presented to verify the theoretical analysis.

REFERENCES

[1] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A-MHz 100-dB operational amplifier with multipath nested miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1709–1717, Dec. 1992.

[2] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Boston, MA: Kluwer, 1995.

[3] E. M. Cherry, "Comment on a 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 31, pp. 753–754, May 1996.

[4] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2000–2011, Dec. 1997.

[5] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 221–230, Feb. 2000.

[6] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 1041–1056, Sept. 2001.

[7] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 339–347, Mar. 1999.

[8] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, pp. 511–520, Mar. 2003.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[10] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," *IEEE Trans. Circuits Systs. I*, vol. 44, pp. 257–262, Mar. 1997.
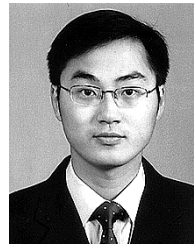
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