Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers

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***Abstract*—An active-feedback frequency-compensation (AFFC) technique for low-power operational amplifiers is presented in this paper. With an active-feedback mechanism, a high-speed block separates the low-frequency high-gain path and high-frequency signal path such that high gain and wide bandwidth can be achieved simultaneously in the AFFC amplifier. The gain stage in the active-feedback network also reduces the size of the compensation capacitors such that the overall chip area of the amplifier becomes smaller and the slew rate is improved. Furthermore, the presence of a left-half-plane zero in the proposed AFFC topology improves the stability and settling behavior of the amplifier.**

Three-stage amplifiers based on AFFC and nested-Miller compensation (NMC) techniques have been implemented by a commercial 0.8-μm CMOS process. When driving a 120-pF capacitive load, the AFFC amplifier achieves over 100-dB dc gain, 4.5-MHz gain-bandwidth product (GBW) , 65° phase margin, and 1.5-V/μs average slew rate, while only dissipating 400-μW power at a 2-V supply. Compared to a three-stage NMC amplifier, the proposed AFFC amplifier provides improvement in both the GBW and slew rate by 11 times and reduces the chip area by 2.3 times without significant increase in the power consumption.

***Index Terms*—Active feedback, active-capacitive-feedback network, amplifiers, frequency compensation, multistage amplifiers.**

I. Introduction

With the advanced technology scaling in CMOS processes, supply voltages of digital circuits are required to be reduced to 0.9 V by the year 2008, according to the Semiconductor Industry Association's roadmap [1]. The continuous decrease in the supply voltage, however, poses challenges and difficulties to the design of analog circuits in mixed-signal systems as the threshold voltage of the transistors does not scale down proportionally to the supply voltage. The operational amplifier, which acts as a fundamental block in most analog systems, is required to achieve high gain and large bandwidth simultaneously in low-voltage condition. To achieve high gain, a conventional cascode amplifier, which increases the gain by stacking up transistors, is not suitable in low-voltage design as the cascode structure results in small voltage swings. Instead, a multistage amplifier is widely used to boost the gain by increasing the number of gain stages horizontally. However, all multistage amplifiers suffer from the closed-loop stability problem due to the presence of multiple poles. A frequency-compensation technique is, therefore, needed to ensure the stability of the multistage amplifier.

Different frequency-compensation topologies for multistage amplifiers have been reported [2]–[10]. Nested-Miller compensation (NMC) [2]–[5] is a well-known pole-splitting technique for compensating multistage amplifiers. However, as mentioned by Eschauzier *et al.* [3], [4], NMC suffers from bandwidth reduction when the number of gain stages increases. In particular, the bandwidth of a three-stage NMC amplifier is reduced to one quarter of that of a single-stage amplifier. Therefore, based on NMC, multipath nested Miller compensation (MNMC) [3] has been developed. This technique uses a feedforward stage to create a left-half-plane (LHP) zero to cancel the second nondominant pole and results in the bandwidth extension by pole-zero cancellation in the passband of the amplifier. Another problem of the NMC structure is the presence of a right-half-plane (RHP) zero, which requires a large output transconductance to ensure stability and, thus, makes the amplifier unsuitable for low-power design [6], [7]. As a result, nested G_m-C compensation (NGCC) [6] and NMC with feedforward transconductance stage and nulling resistor (NMCFNR) [7] have been reported to improve the stability by removing the RHP zero of the NMC amplifier and allowing the amplifier to achieve low-power design. Compared to NMC, the bandwidth enhancement provided by MNMC, NGCC, or NMCFNR is not significant especially when driving large capacitive loads. In order to significantly increase the bandwidth of the multistage amplifier, other nonstandard NMC topologies such as embedded tracking compensation (ETC) [8] and damping-factor-control frequency compensation (DFCFC) [9], [10] have been developed to remove the capacitive nesting structure; therefore, the output capacitive load due to Miller capacitors is reduced. The ETC amplifier extends the bandwidth by using the pole-zero cancellation approach while the DFCFC amplifier improves the bandwidth by the pole-splitting method and uses a damping-factor-control block to ensure stability when the inner Miller capacitor is removed. However, as all published compensation topologies use passive-capacitive-feedback networks, the bandwidth of the amplifier is still limited for high-speed applications in low-power condition.

In order to further improve the bandwidth of the amplifier in low-power design, a novel active-feedback frequency-compensation (AFFC) technique [11] is presented in this paper. In contrast to using passive-capacitive-feedback networks, AFFC proposes to use an active-capacitive-feedback network, in which an active positive gain stage is added in series with the dominant compensation capacitor so that the required compensation capacitor in AFFC is smaller than that in all reported passive com-

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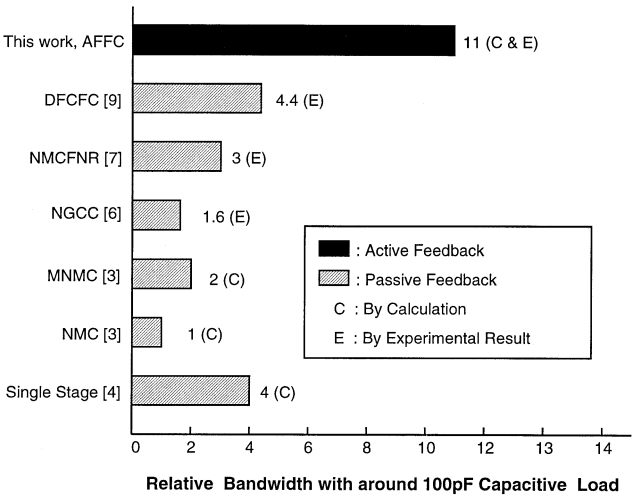


Fig. 1. Comparison of bandwidth on different frequency-compensation topologies (take NMC as the reference).

pensation topologies. As a result, the physical dimension of the proposed amplifier is greatly reduced and both the bandwidth and transient responses are improved. In addition, a high-speed block directs the high-frequency signal to bypass the slow-response intermediate high-gain stages; therefore, the bandwidth of the AFFC amplifier can be further enhanced. The comparison on the bandwidth of three-stage amplifiers using different pole-splitting compensation topologies driving a capacitive load of around 100 pF, as shown in Fig. 1, indicates that a three-stage AFFC amplifier achieves the largest reported bandwidth. Moreover, the active-capacitive-feedback network generates an LHP zero to improve the phase margin and, thus, the stability of the amplifier.

Furthermore, when considering the dc gain, 100-dB gain is generally sufficient for most applications and can be provided by three-stage amplifiers. Any extra gain stage simply increases the power consumption and complicates the frequency-compensation structures [3], [7]–[10]. Therefore, this paper will mainly focus on discussing AFFC for three-stage amplifiers as the performance of the three-stage amplifier is optimum for the trade-offs between the dc gain ($\sim$ 100 dB), bandwidth, and power consumption in practical circuit implementations.

This paper is organized as follows. The operational principle and different issues of a three-stage AFFC amplifier are discussed in Section II. Comparisons between AFFC and NMC amplifiers are also given. In Sections III and IV, circuit implementations and experimental results are presented to verify the functionality and improvement of the proposed AFFC amplifier. Finally, conclusions are given in Section V.

II. Active-Feedback Frequency Compensation

In this section, the transfer function and stability issue of the AFFC amplifier are analyzed. Different design issues such as dimension conditions, gain-bandwidth product (GBW), transient responses, and low-power design considerations are also discussed.

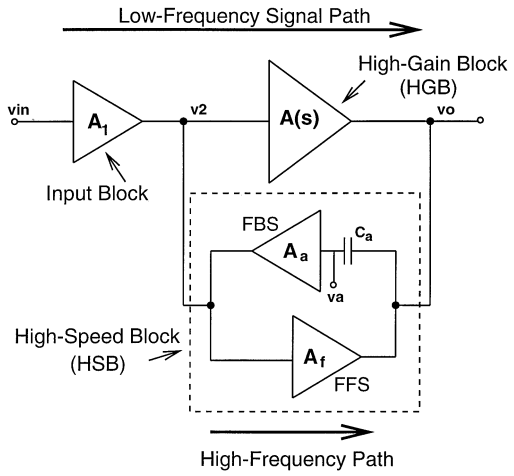


Fig. 2. Basic structure of an AFFC amplifier.

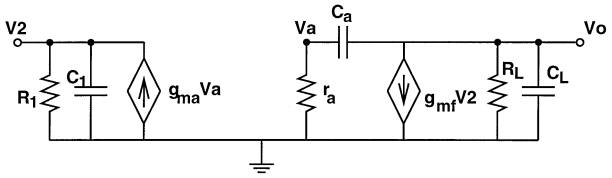


Fig. 3. Equivalent small-signal circuit of the HSB in the AFFC amplifier.

A. Principle of Operation

The basic structure of an AFFC amplifier, shown in Fig. 2, consists of three main blocks: input block, high-gain block (HGB), and high-speed block (HSB). The input block with the gain of A_1 is realized by a differential pair. The HGB denoted as $A(s)$ consists of two gain stages cascaded together to boost up the dc gain of a three-stage amplifier. The HSB consists of a feedforward stage (FFS) with the gain of A_f and a feedback stage (FBS) with the gain of A_a connected in series with a compensation capacitor C_a, realizing the active-capacitive-feedback network. The function of the HSB is to control the high-frequency operation of the amplifier, which implies that it determines the location and Q value of the nondominant complex poles and, thus, the bandwidth of the amplifier. Fig. 3 shows the equivalent small-signal circuit of the HSB in the AFFC amplifier, in which the input resistance of the FBS is r_a, and the equivalent resistance and capacitance at node V2 due to the input block and the HSB are R_1 and C_1, respectively. The transconductances of the FBS and FFS are represented by g_{ma} and g_{mf}, respectively. At high frequencies, any output signal change will be sensed through the input resistance of the FBS such that the signal at Va is almost the same as the signal at Vo and is given as

$$\frac{\text{Va}}{\text{Vo}} = \frac{r_a}{r_a + \frac{1}{sC_a}} \approx 1 \quad \text{(at high frequencies)}. \tag{1}$$

The signal at Va will then be directed to the output of the input block and amplified by the positive gain of the FBS. The amplified feedback signal at the output of the input block will then be feedforwarded to the output again, through the FFS, in order to

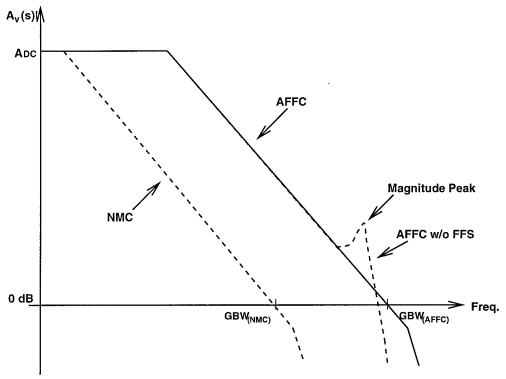


Fig. 4. Bode plot of NMC and AFFC amplifiers.

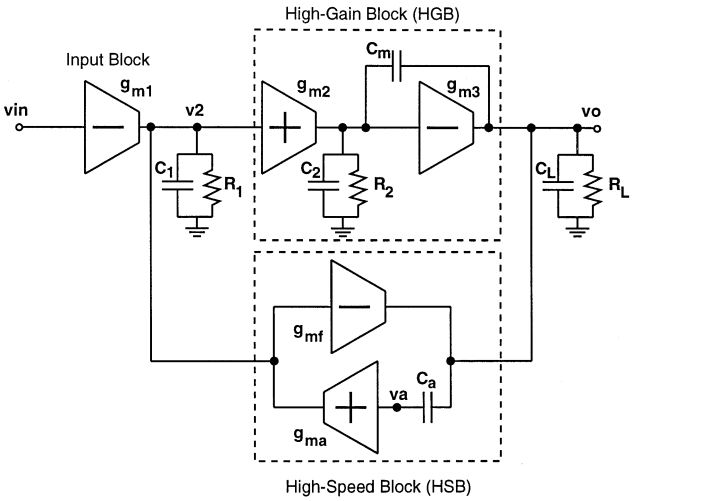
reduce the original output signal change. As the negative feedback loop is established in the HSB, the stability of the high-frequency signal can be achieved. In addition, since the slow-response gain stages in the HGB are bypassed during the whole negative feedback action at high frequencies, the structure of the HGB does not affect the speed of the amplifier. A smaller C_a can also be used due to the positive gain of the FBS. As a result, a significant bandwidth enhancement of the AFFC amplifier is achieved.

Previously, the structure of the FBS with the compensation capacitor is only used in the frequency compensation of two-stage amplifiers as it is efficient for the gain-bandwidth [12], [13] and power-supply rejection ratio performance [14], [15]. The input resistance of the FBS and the compensation capacitor can also introduce an LHP zero to increase the phase margin of the amplifier. However, this structure cannot be directly applied to a three-stage amplifier with an inverting output stage as the Q value of the nondominant complex poles cannot be controlled, and the three-stage amplifier will then become unstable as illustrated in Fig. 4. As a result, the FFS structure of the HSB is very critical as it can guarantee the stability of the amplifier by properly controlling the Q value of the nondominant complex poles. In addition, the structure of the active-capacitive-feedback network in the HSB not only removes the RHP zero by blocking the feedforward signal current, but also creates an LHP zero to boost the phase margin; therefore, it improves the stability and settling behavior of the amplifier.

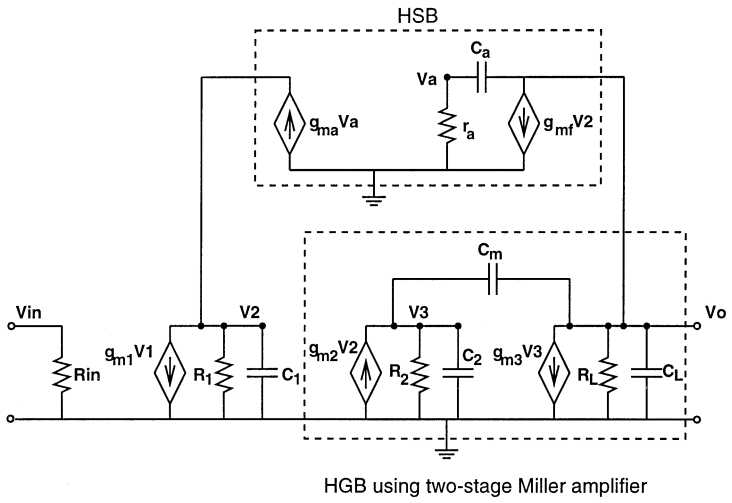
B. Transfer Function

The detailed structure and its equivalent small-signal circuit of the three-stage AFFC amplifier are shown in Fig. 5, in which the high-gain block (HGB) is implemented by a two-stage Miller amplifier [16]. In the figure, g_{mi}, R_i, and C_i are defined as the transconductance, output resistance, and lumped output parasitic capacitance of the ith gain stage, respectively. In particular, R_L is the loading resistance, C_L is the loading capacitance, and C_m is the compensation capacitor in the HGB.

To analyze the stability of the AFFC amplifier, the small-signal transfer function of the amplifier should be derived. The following assumptions are made to simplify the transfer function without losing accuracy in order to provide a clearer insight to the proposed structure.



(a)



(b)

Fig. 5. (a) Structure and (b) equivalent small-signal circuit of the proposed three-stage AFFC amplifier.

1) The input resistance of the FBS is equal to the reciprocal of its transconductance (i.e., $r_a = 1/g_{ma}$).
2) The loading and compensation capacitors are much greater than the lumped output parasitic capacitance of each stage (i.e., C_L, C_a and $C_m \gg C_1$, C_2).
3) The gains of all stages are much greater than one (i.e., $g_{m(1,2,3)}R_{(1,2,L)}$ and $g_{ma}R_1 \gg 1$).
4) For simplicity, both compensation capacitors are set to equal to each other (i.e., $C_a = C_m$).

Based on the above assumptions, the transfer function of the proposed AFFC amplifier is given as

$$A_{v(\mathrm{AFFC})} = \frac{A_{dc}\left(1+s\frac{C_a}{g_{ma}}\right)}{\left(1+\frac{s}{p_{-3\mathrm{dB}}}\right)\left(1+s\frac{C_1C_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_1C_L}{g_{ma}(g_{mf}-g_{m2})}\right)} \approx \frac{\left(1+s\frac{C_a}{g_{ma}}\right)}{\frac{s}{\mathrm{GBW}}\left(1+s\frac{C_1C_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_1C_L}{g_{ma}(g_{mf}-g_{m2})}\right)} \quad (2)$$

where $A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_L$ is the dc voltage gain, $p_{-3\text{dB}} = 1/(C_a g_{m2}g_{m3}R_1R_2R_L)$ is the dominant pole, and GBW $= g_{m1}/C_a$ is the gain-bandwidth product of the amplifier. In fact, the transfer function still holds true even if $C_a \neq C_m$, and normally one can optimize the size of compensation capacitors by setting $C_a > C_m$. From (2), an LHP zero, z_{LHP}, is created to boost the phase margin of the amplifier, which is given by $z_{\text{LHP}} = g_{ma}/C_a$. In addition, the location of nondominant poles $|p_{2,3}|$ and their corresponding Q value are, respectively, calculated as

$$|p_{2,3}| = \sqrt{\frac{g_{ma}(g_{mf} - g_{m2})}{C_1C_L}} \tag{3}$$

$$Q = \sqrt{\frac{C_a^2(g_{mf} - g_{m2})}{C_1C_Lg_{ma}}}. \tag{4}$$

Equations (3) and (4) indicate that both the location and Q value of the nondominant complex poles depend on the HSB as they are mainly controlled by g_{ma}, g_{mf}, and C_a. Therefore, the HSB controls the bandwidth of the AFFC amplifier.

C. Stability Analysis

The stability condition of the AFFC amplifier can be determined by first neglecting the effect of the LHP zero in (2) and then considering the closed-loop transfer function $A_{cl}(s)$ of the amplifier connected as in unity-gain feedback configuration. The closed-loop transfer function can, thus, be derived as

$$A_{cl}(s) = \frac{1}{1 + s\frac{C_a}{g_{m1}} + s^2\frac{C_1C_L}{g_{m1}(g_{mf}-g_{m2})} + s^3\frac{C_1C_aC_L}{g_{m1}g_{ma}(g_{mf}-g_{m2})}}. \tag{5}$$

As the order of the numerator in (5) is less than that of the denominator, the stability of the AFFC amplifier depends on the denominator of $A_{cl}(s)$. By applying the Routh stability criterion to the denominator of (5) [6], the AFFC amplifier is stable if and only if

$$g_{mf} > g_{m2}. \tag{6}$$

D. Dimension Conditions, GBW, and Phase Margin

The stability of the AFFC amplifier can also be achieved by considering the denominator of the closed-loop transfer function in (5) having a third-order Butterworth polynomial $B(s)$ with a cutoff frequency of ω_o, which is given by [3], [4]

$$B(s) = 1 + 2\left(\frac{s}{\omega_o}\right) + 2\left(\frac{s}{\omega_o}\right)^2 + \left(\frac{s}{\omega_o}\right)^3. \tag{7}$$

If (7) is satisfied, the Q value of the nondominant poles is $1/\sqrt{2}$. By comparing the coefficients of the denominators of (5) with those of (7), we obtain

$$\frac{2}{\omega_o} = \frac{C_a}{g_{m1}} \tag{8}$$

$$2\left(\frac{1}{\omega_o}\right)^2 = \frac{C_1C_L}{g_{m1}(g_{mf} - g_{m2})} \tag{9}$$

$$\left(\frac{1}{\omega_o}\right)^3 = \frac{C_1C_aC_L}{g_{m1}g_{ma}(g_{mf} - g_{m2})}. \tag{10}$$

For a fixed g_{mf}, the dimension conditions of g_{ma} and C_a are found by using (8)–(10) and eliminating ω_o. They are given as

$$g_{ma} = 4g_{m1} \tag{11}$$

$$\begin{aligned} C_{a(\text{AFFC})} &= C_{m(\text{AFFC})} \\ &= \sqrt{\frac{2g_{m1}C_1C_L}{g_{mf} - g_{m2}}} \\ &= \frac{4}{N}\left(\frac{g_{m1}}{g_{m3}}\right)C_L \\ &= \frac{1}{N}C_{m1(\text{NMC})} \end{aligned} \tag{12}$$

where

$$N = \sqrt{8\left(\frac{C_L}{C_1}\right)\left[\frac{g_{m1}(g_{mf} - g_{m2})}{g_{m3}^2}\right]}. \tag{13}$$

From (12) and (13), the dimension condition of the compensation capacitor in the AFFC amplifier is less sensitive to the global variations of circuit parameters as it only depends on the ratios of transconductances and capacitances. Compared with the compensation capacitor, $C_{m1(\text{NMC})}$, in the NMC amplifier [9], the size of C_a is much smaller in the AFFC amplifier as $N \gg 1$. As N increases with C_L, as shown in (13), a larger reduction in the size of the compensation capacitor results in large capacitive load applications. In multistage amplifiers, most of the chip area will be occupied by the compensation capacitors, especially when driving large capacitive loads. Therefore, the area of the AFFC amplifier is significantly smaller than that of the NMC counterpart. Also, the transconductance of the FFS can be chosen to be equal to that of the output stage of the amplifier in order to implement a push-pull output stage for improving the slewing performance of the amplifier (i.e., $g_{mf} = g_{m3}$).

By applying (12) and (13) into (2), the GBW of the AFFC amplifier is calculated as

$$\begin{aligned} \text{GBW}_{(\text{AFFC})} &= \frac{g_{m1}}{C_a} \\ &= \sqrt{\frac{g_{m1}\,(g_{mf} - g_{m2})}{2C_1C_L}} \\ &= N\frac{g_{m3}}{4C_L} \\ &= N \cdot \text{GBW}_{(\text{NMC})} \end{aligned} \tag{14}$$

where $\text{GBW}_{(\text{NMC})} = g_{m3}/(4C_L)$ [9]. From (14), the GBW of the AFFC amplifier depends on the difference between g_{mf} and g_{m2}, so g_{mf} should be much larger than g_{m2} in order to optimize the GBW. In addition, the GBW of the AFFC amplifier is enhanced by N times as compared with that of the NMC counterpart. As discussed previously, N increases with the loading capacitor; therefore, bandwidth improvement of the AFFC amplifier increases when driving large capacitive loads.

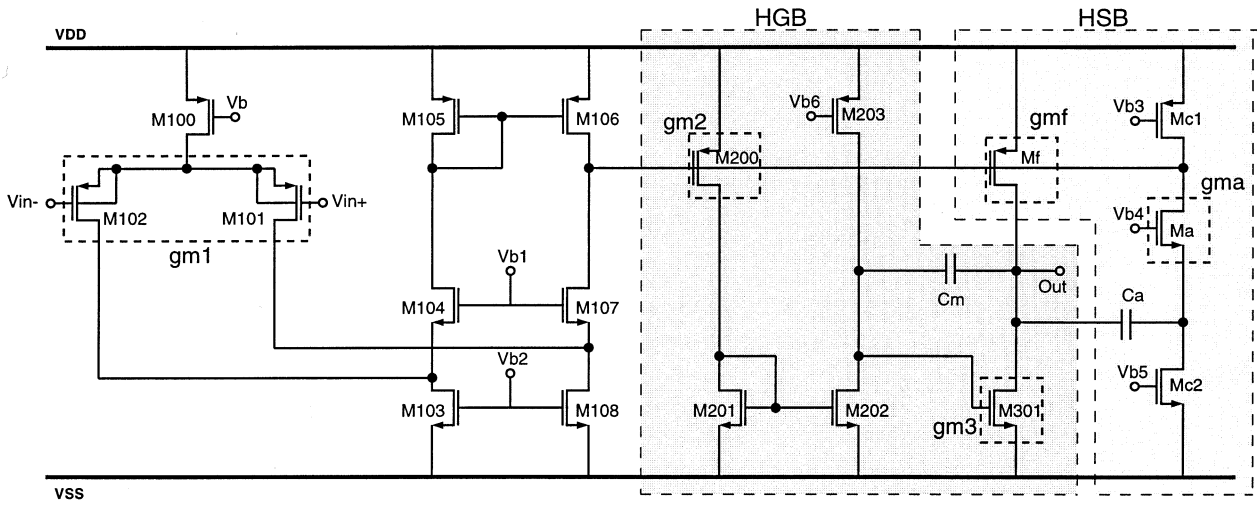


Fig. 6. Circuit diagram of a three-stage AFFC amplifier.

By taking both the LHP zero and the dimension conditions shown in (11)–(13) into consideration, the phase margin (PM) of the AFFC amplifier is given by

$$\begin{aligned}\mathrm{PM}_{(\mathrm{AFFC})} &= 180^\circ - \arctan\left[\frac{\mathrm{GBW}_{(\mathrm{AFFC})}}{p_{-3\mathrm{d}B}}\right] \\ &\quad - \arctan\left[\frac{\left(\frac{\mathrm{GBW}_{(\mathrm{AFFC})}}{|p_{2,3}|}\right)}{Q\left[1-\left(\frac{\mathrm{GBW}_{(\mathrm{AFFC})}}{|p_{2,3}|}\right)^2\right]}\right] \\ &\quad + \arctan\left[\frac{\mathrm{GBW}_{(\mathrm{AFFC})}}{z_{\mathrm{LHP}}}\right] \\ &\approx 60^\circ + \arctan\left[\frac{g_{m1}}{g_{ma}}\right] \\ &= 74^\circ. \end{aligned} \tag{15}$$

The phase margin of the NMC amplifier is 60° with Butterworth response [3], [4]. From (15), the stability of the AFFC amplifier is, thus, improved when compared with the NMC amplifier as it has extra 14° phase margin. The extra phase margin is due to the presence of the LHP zero, which contributes a positive phase shift to the AFFC amplifier.

E. Transient Responses

The settling time of an amplifier can be divided into a quasi-linear region and a slewing region [17]–[19]. In order to optimize the settling behavior of the amplifier in the quasi-linear region, the phase margin needs to be maximized and the absence of pole-zero doublet in the passband of the amplifier is required. In the proposed AFFC amplifier with third-order Butterworth frequency response, the theoretical phase margin is much larger than 60° due to the presence of an LHP zero. In addition, pole-zero doublet does not exist in the passband of the AFFC amplifier. Therefore, the output voltage of the AFFC amplifier can settle within a short duration in the quasi-linear region.

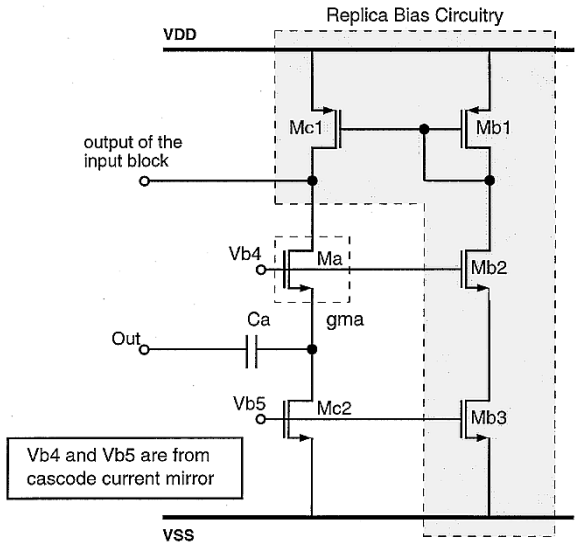


Fig. 7. Replica bias circuit for the FBS.

With the push-pull output stage in the AFFC amplifier, the slew rate is only limited by the amount of the biasing current and the size of compensation capacitors. The slew rate (SR) of the AFFC amplifier is, thus, given by

$$\mathrm{SR} = \min\left(\frac{I_a}{C_a}, \frac{I_2}{C_m}\right) \tag{16}$$

where I_a and I_2 are the amount of biasing current charging or discharging compensation capacitors in the HSB and the HGB, respectively. To increase the slew rate, it is generally not efficient to increase the biasing current in low-power design. Instead, the only method is to reduce the size of compensation capacitors. Based on the dimension condition stated in (12), the size of compensation capacitors in the AFFC amplifier is reduced by N times compared to that in the NMC amplifier and the slew rate of the AFFC amplifier can then be improved by N times with the same power consumption. Furthermore, as N increases with the value of the loading capacitor, the slew rate

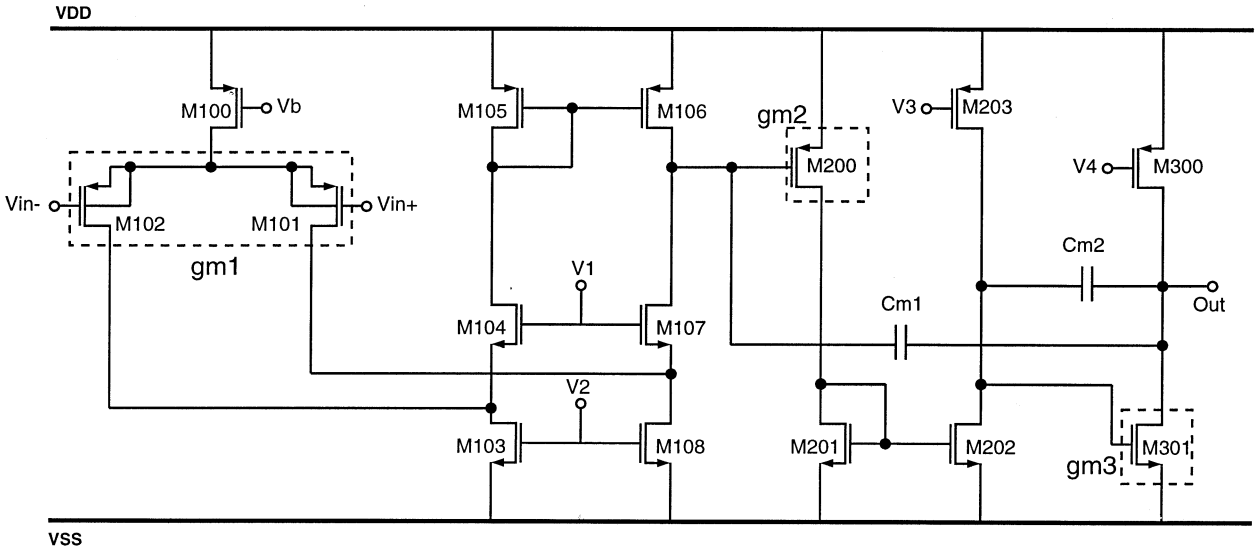


Fig. 8. Circuit diagram of a three-stage NMC amplifier.

enhancement of the AFFC amplifier is even better when driving large capacitive loads.

F. Low-Power Design Considerations

In the proposed AFFC amplifier, the second stage is a noninverting gain stage, which typically consumes more power than an inverting gain stage to achieve the same magnitude of transconductance. However, only a small second-stage transconductance g_{m2} is required in the AFFC amplifier as the second gain stage is mainly for dc gain boosting. In fact, a smaller g_{m2} can even provide a better GBW as shown in (14). Therefore, the power consumption of the AFFC amplifier can be reduced since a small static current is needed to bias the second gain stage.

Good stability of the NMC amplifier is required to satisfy the dimension condition of $g_{m3} \gg g_{m1}$ and g_{m2} due to the presence of an RHP zero [7]. As g_{m1} is generally quite large, either to reduce the offset voltage of the amplifier by using larger transistor size of the input differential pair [16] or to improve the slew rate of the amplifier with larger biasing current, the dimension condition is difficult to achieve in low-power design. In contrast, the absence of the RHP zero in the AFFC amplifier can preserve the stability of the amplifier when g_{m3} and g_{mf} are in the same order of magnitude as g_{m1}. The AFFC amplifier is, thus, suitable for low-power design.

Based on the dimension condition stated in (11), the required transconductance of the FBS should be four times larger than that of the input stage. It seems that a large current is needed to bias the FBS in order to achieve the required transconductance. However, the input stage of the amplifier with transconductance g_{m1} is generally implemented by pMOS transistors in low-voltage design to eliminate the body effect of transistors in a n-well process when the bulk and source terminals are connected together. The static power dissipation can be optimized when an nMOS transistor is used to implement the FBS as the effective mobility of an nMOS transistor is typically two to three times larger than that of a pMOS transistor [16]. As a result, the amount of current required to achieve a particular g_{ma} can be minimized.

TABLE I
SUMMARY OF DEVICE SIZE

	Transistors	Size
HGB	M200, M203	8 μm / 1.6 μm
	M201, M202	3.6 μm / 1.6 μm
	M301	100 μm / 1.6 μm
HSB	Mc1	128 μm / 2 μm
	Ma, Mc2	100 μm / 2 μm
	Mf	220 μm / 1.6 μm

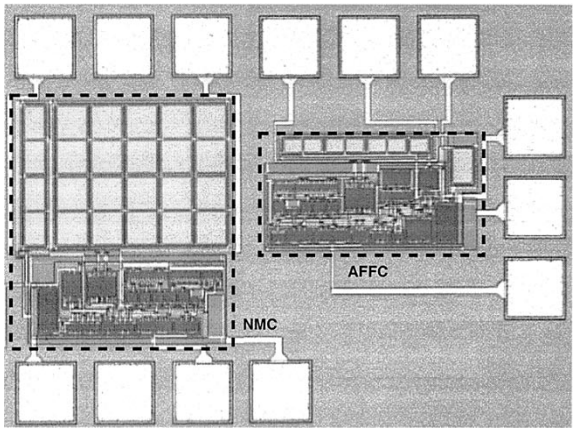


Fig. 9. Chip micrograph of three-stage AFFC and NMC amplifiers.

III. CIRCUIT IMPLEMENTATIONS OF AMPLIFIERS

The circuit implementation of a three-stage AFFC amplifier is shown in Fig. 6. In the AFFC amplifier, the first gain stage

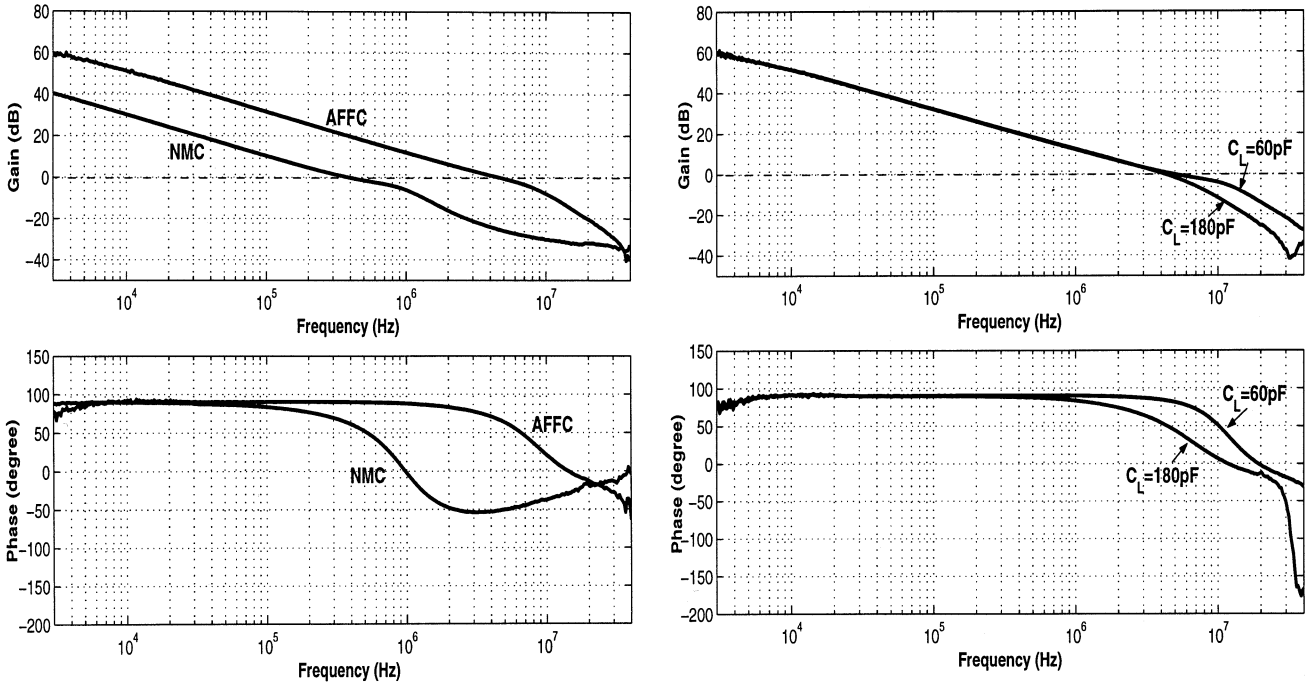


Fig. 10. Measured ac responses of (a) the AFFC and NMC amplifiers driving a 120-pF 25-kΩ load, and (b) the AFFC amplifier driving different capacitive loads.

is realized by transistors M101–M108 with a pMOS input differential pair. The second noninverting gain stage and the third stage are implemented by transistors M200–M203 and M301, respectively, to build the HGB. In the HSB, the FBS is implemented by a common-gate amplifier with an nMOS transistor Ma while the transistor Mf realizes the FFS. The operation of the common-gate amplifier requires proper biasing of two transistors Mc1 and Mc2. In order to minimize the systematic offset of the AFFC amplifier, replica biasing scheme [13], as shown in Fig. 7, is adopted to bias transistors Mc1, Ma, and Mc2 by using transistors Mb1–Mb3, respectively. In fact, Mb1–Mb3 are scaled-down copies of Mc1, Ma, and Mc2, respectively, to minimize the current consumption and to ensure that the biasing current in Mc1 equals to that in Mc2. To optimize the size of the compensation capacitors, C_a and C_m are fine tuned based on the tradeoffs between the bandwidth and phase margin. For a 120-pF capacitive load, the optimized values of compensation capacitors C_a and C_m are 7 and 3 pF, respectively, and the corresponding device size of each transistor in the HGB and HSB is summarized in Table I.

For comparison with the proposed AFFC topology, a three-stage NMC amplifier is also implemented, which is designed based on the Butterworth response stability criteria, as shown in Fig. 8 for reference purposes. In our design, the outer and inner compensation capacitors are designed to be 88 and 11 pF, respectively, in order to achieve stability.

IV. Experimental Results and Discussions

To verify the functionality of the proposed AFFC amplifier and compare its performance with that of the NMC amplifier, both 2-V three-stage AFFC and NMC amplifiers have been fabricated in a commercial 0.8-μm CMOS process with $V_{tn} = 0.85$ V and $V_{tp} = -0.78$ V. The micrograph is shown in Fig. 9.

Both amplifiers have been tested with a 120-pF capacitive load including the probe capacitance. The frequency responses of the amplifiers have been measured with an input common-mode voltage of 0.3 V, while the slew rate and settling time have been tested when the amplifiers are in unity-gain noninverting configuration with a 0.5-V step input. The measured frequency and the transient responses of both NMC and AFFC amplifiers are shown in Figs. 10(a) and 11(a), respectively. From Fig. 10(a), the AFFC amplifier achieves a GBW of 4.5 MHz with 65° phase margin. A smaller phase margin than that in (15) results from the tradeoff with the wider bandwidth. From Fig. 11(a), the average slew rate and average 1% settling time of the AFFC amplifier are 1.49 V/μs and 0.64 μs, respectively, with no transient overshoot. In addition, the proposed AFFC amplifier is tested with different capacitive loads. Figs. 10(b), 11(b), and 11(c) show the frequency and transient responses of the AFFC amplifier when the loading capacitance has ±50% variation from its optimized value of 120 pF. Based on the measurement results, the AFFC amplifier is verified to be stable when driving both 60-pF and 180-pF loads. The detailed performances of amplifiers are summarized in Table II.

Compared to the performances of NMC amplifiers when driving a 120-pF load, the AFFC amplifier improves the GBW by 11.3 times, the average slew rate by 10.6 times, and the average 1% settling time by 7.6 times, with only 5.3% increase in power consumption. In addition, as the AFFC amplifier requires smaller compensation capacitors when driving large capacitive loads, the chip area of the AFFC amplifier is reduced by 2.3 times compared with the NMC counterpart.

To provide a clearer picture of the improvement by AFFC, a comparison of some published compensation topologies is shown in Table III. Two figures of merit FOM_S and FOM_L are

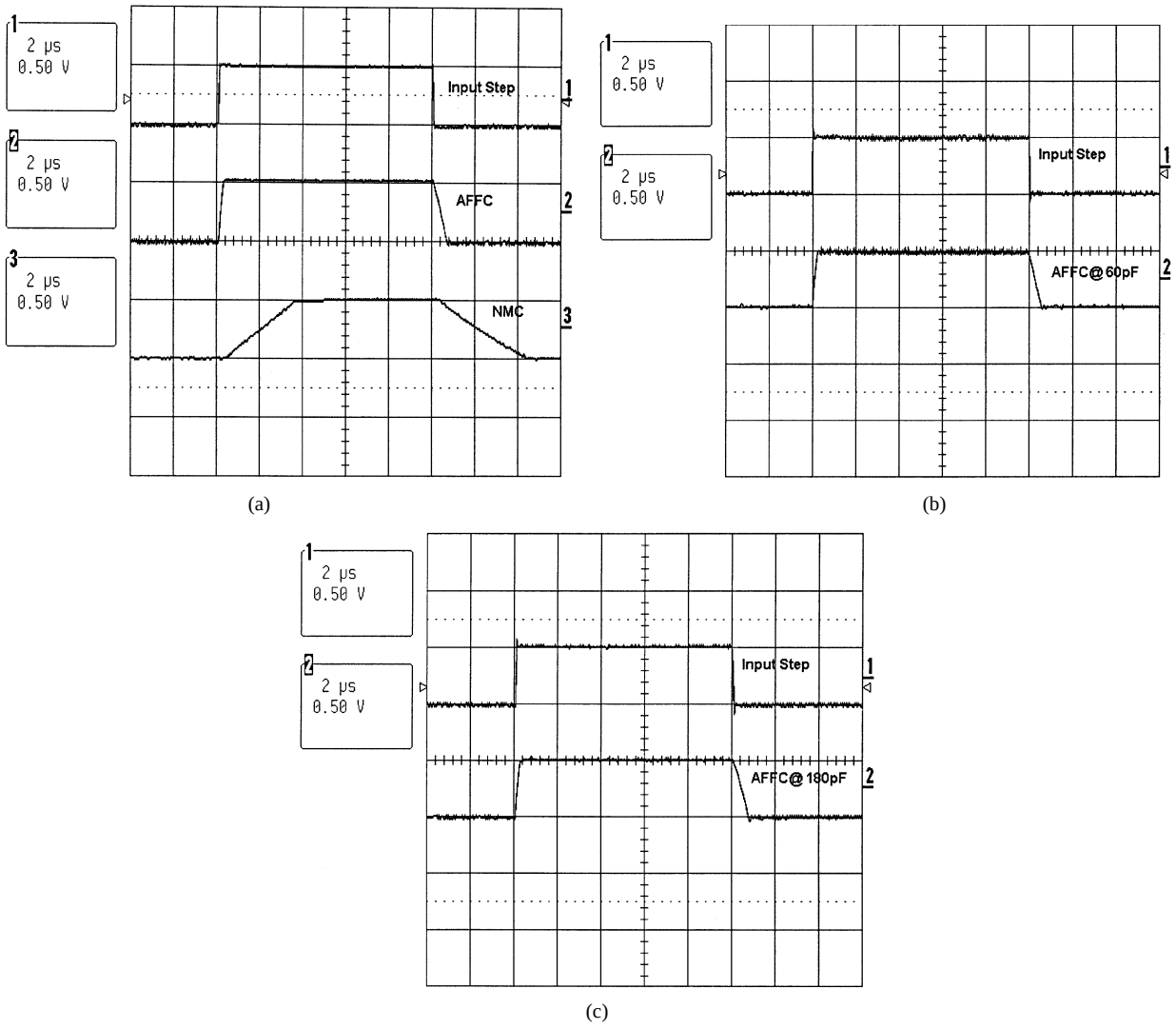


Fig. 11. Measured transient responses of (a) the AFFC and NMC amplifiers driving a 120-pF 25-kΩ load, and the AFFC amplifier driving (b) a 60-pF 25-kΩ load and (c) a 180-pF 25-kΩ load.

TABLE II
MEASURED RESULTS OF NMC AND AFFC AMPLIFIERS

	NMC	AFFC		
Loading	120 pF // 25 kΩ	60 pF // 25 kΩ	120 pF // 25 kΩ	180 pF // 25 kΩ
DC Gain (dB)	> 100			
GBW (MHz)	0.4	4.7	4.5	4.2
PM	61^o	83^o	65^o	52^o
SR^+/SR^- (V/μs)	0.15/0.13	2.36/0.85	2.20/0.78	2.15/0.72
T_s^+/T_s^- (μs) (to 1%)	4.9/4.7	0.35/0.78	0.42/0.85	0.44/0.90
Power Consumption (mW)@Vdd	0.38 @ 2 V	0.4 @ 2 V		
$C_{m1(NMC)}/C_{a(AFFC)}$	88 pF	7 pF		
$C_{m2(NMC)}/C_{m(AFFC)}$	11 pF	3 pF		
Area	0.14 mm^2	0.06 mm^2		

TABLE III
COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

	NMC [3]	MNMC [3]	NGCC [6]	NMCFNR [7]	ETC [8]	DFCFC [9]	This work AFFC
C_L (pF)	100	100	20	100	40	100	120
DC Gain (dB)	100	100	100	> 100	102	> 100	> 100
GBW (MHz)	60	100	0.61	1.8	47	2.6	4.5
SR† (V/μs)	20	35	2.5	0.79	69	1.32	1.49
Power (mW@Vdd)	76@8	76@8	0.68@2	0.406@2	6.9@3	0.42@2	0.4@2
FOM_S ($\frac{\text{MHz·pF}}{\text{mW}}$)	79	132	18	443	272	619	1350
FOM_L ($\frac{\text{V}/\mu\text{s·pF}}{\text{mW}}$)	26	46	74	195	400	314	447
Technology	3 GHz f_t BJT	3 GHz f_t BJT	2 μm CMOS	0.8 μm CMOS	0.6 μm CMOS	0.8 μm CMOS	0.8 μm CMOS

†Average value is used

used to characterize small-signal (GBW) and large-signal (slew rate) performances of the amplifier and are given by [8], [9]

$$\text{FOM}_S = \frac{\text{GBW} \cdot C_L}{\text{power}} \tag{17}$$

$$\text{FOM}_L = \frac{\text{SR} \cdot C_L}{\text{power}}. \tag{18}$$

A larger FOM implies a better frequency-compensation topology. From Table III, the proposed AFFC topology achieves the largest FOM_S and FOM_L compared with other reported compensation topologies.

V. CONCLUSION

An active-feedback frequency-compensation (AFFC) technique for three-stage amplifiers is introduced. With the active-capacitive-feedback network, the low-frequency and high-frequency signal paths are separated by an HGB and an HSB, respectively. The HGB provides a high dc gain while the HSB significantly enhances the bandwidth of the amplifier as the slow-response intermediate high-gain stages are bypassed by the HSB at high frequencies. Thus, the AFFC amplifier can achieve high gain and wide bandwidth simultaneously. The chip area of the AFFC amplifier is also reduced as smaller compensation capacitors are required. Moreover, both the stability and transient responses are improved due to the presence of an LHP zero in the amplifier. The dimension conditions are also suitable for low-power design. Based on AFFC, a three-stage amplifier has been designed, implemented and verified. Comparisons of experimental results with other published passive-feedback topologies are presented. The proposed AFFC amplifier has better small-signal and large-signal performances than other reported compensation topologies.

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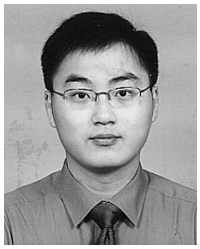
REFERENCES

[1] *Int. Technol. Roadmap for Semiconductors*, Semiconductor Industry Association, San Jose, CA, 2001.
[2] J. H. Huijsing, "Multistage amplifier with capacitive nesting for frequency compensation," U.S. Patent 602 234, Apr. 19, 1984.
[3] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1709–1717, Dec. 1992.
[4] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Boston, MA: Kluwer, 1995.
[5] E. M. Cherry, "Comment on 'A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure'," *IEEE J. Solid-State Circuits*, vol. 31, pp. 753–754, May 1996.
[6] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested Gm-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2000–2011, Dec. 1997.
[7] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low-power CMOS design," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 388–394, Apr. 2001.
[8] H.-T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 339–347, Mar. 1999.
[9] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 221–230, Feb. 2000.
[10] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 1041–1056, Sept. 2001.
[11] H. Lee and P. K. T. Mok, "Active-feedback frequency compensation for low-power multistage amplifiers," in *Proc. IEEE Custom Integrated Circuits Conf.*, Orlando, FL, May 2002, pp. 325–328.

[12] R. Castello, "CMOS buffer amplifier," in *Analog Circuit Design*, J. Huijsing, R. van der Plassche, and W. Sansen, Eds. Boston, MA: Kluwer, 1993, pp. 113–138.
[13] R. Reay and G. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE J. Solid-State Circuits*, vol. 30, pp. 591–594, May 1995.
[14] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 629–633, Dec. 1983.
[15] M. Steyaert and W. Sansen, "Power-supply rejection ratio in operational transconductance amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1077–1084, Sept. 1990.
[16] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: Wiley, 1984.
[17] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347–352, Dec. 1974.
[18] C. T. Chang, "Analysis of the settling behavior of an operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 74–80, Feb. 1982.
[19] H. C. Yang and D. J. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 326–334, Mar. 1990.



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